THE DATASHEET OF

Z86C3312PECR2035

zilog®

A Littelfuse Company

Z86C33/C43

CMOS Z8® MCU CONSUMER CONTROLLER PROCESSOR

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C33	4	237	12, 16
Z86C43	4	236	12, 16

Note: *General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (C43)
  28-Pin DIP, 28-Pin SOIC, 28-Pin PLCC (C33)
- 3.0- to 5.5-Volt Operating Range
- Clock Free Watch-Dog Timer (WDT) Reset
- –40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (C43)
  24 Input/Output Lines (C33)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C33/C43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® MCU single-chip family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C33/C43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers.

For applications demanding powerful I/O capabilities, the Z86C33 provides 24 pins, and the Z86C43 provides 32 pins dedicated to input and output. These lines are configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C33/C43 offers two on-chip counter/timers with a large number of user-selectable modes.

With ROM/ROMless selectivity, the Z86C43 provides both external memory and pre-programmed ROM, which enables this Z8® MCU to be used in high-volume applications, or where code flexibility is required.

GENERAL DESCRIPTION (Continued)

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

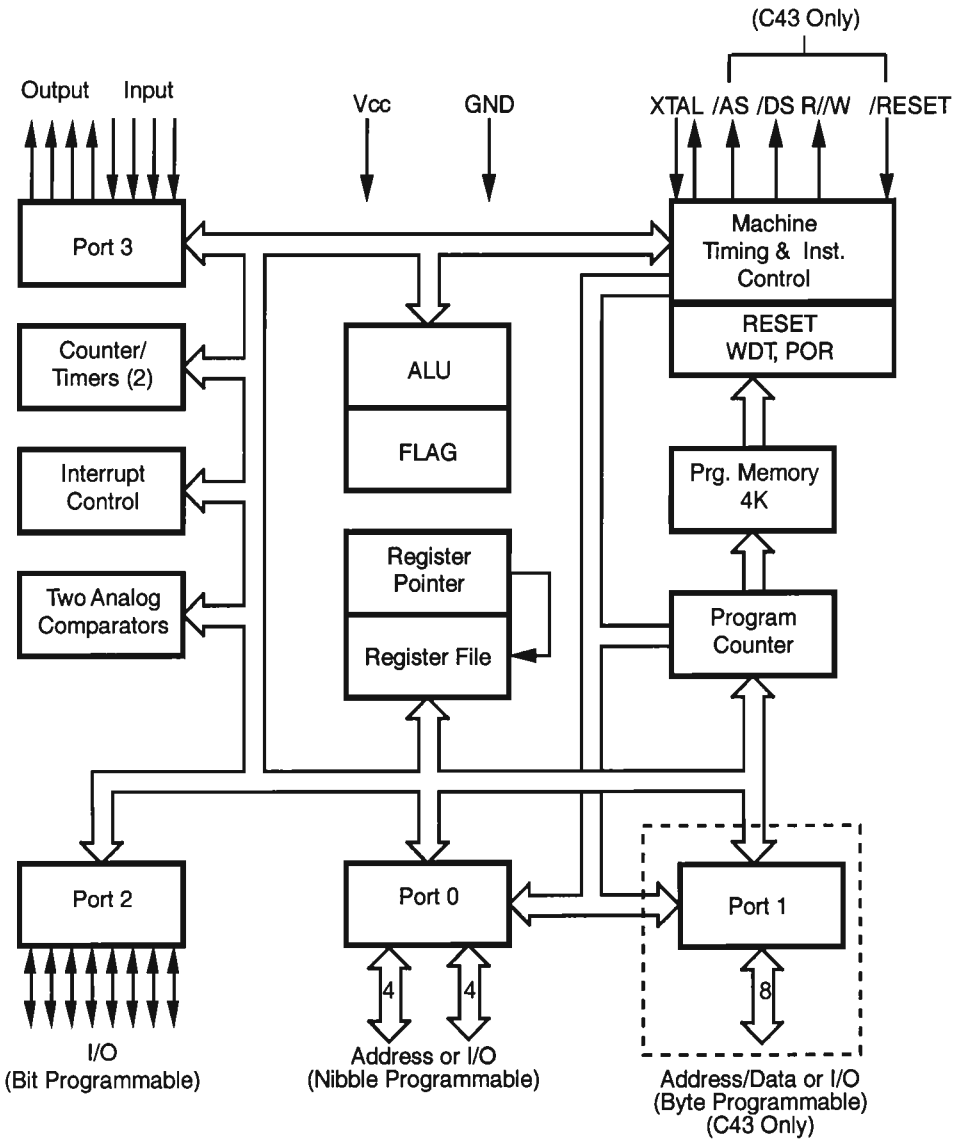


Figure 1. Functional Block Diagram

PIN DESCRIPTION

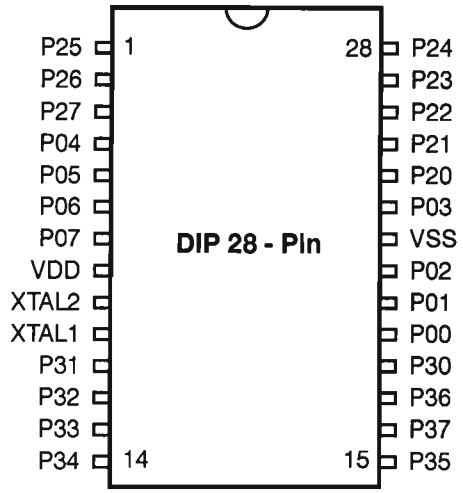


Figure 2. 28-Pin DIP/SOIC Pin Configuration

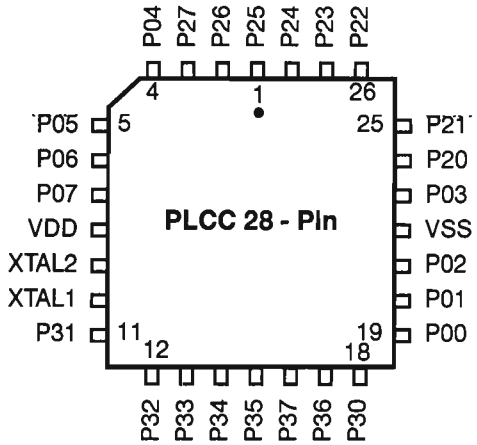


Figure 3. 28-Pin PLCC Pin Configuration

Table 1. 28-Pin DIP/SOIC/PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-33	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

PIN DESCRIPTION (Continued)

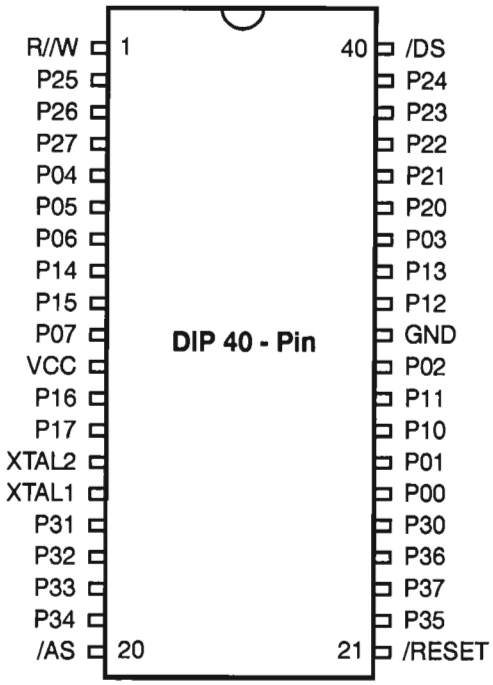


Figure 4. 40-Pin DIP Assignments

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
1	R//W	Read/Write	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output
8-9	P14-15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V_{CC}	Power Supply	
12-13	P16-17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output
15	XTAL1	Crystal, Oscillator Clock	Input
16-18	P31-33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-01	Port 0, Pin 0,1	In/Output
28-29	P10-11	Port 1, Pin 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-13	Port 1, Pin 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

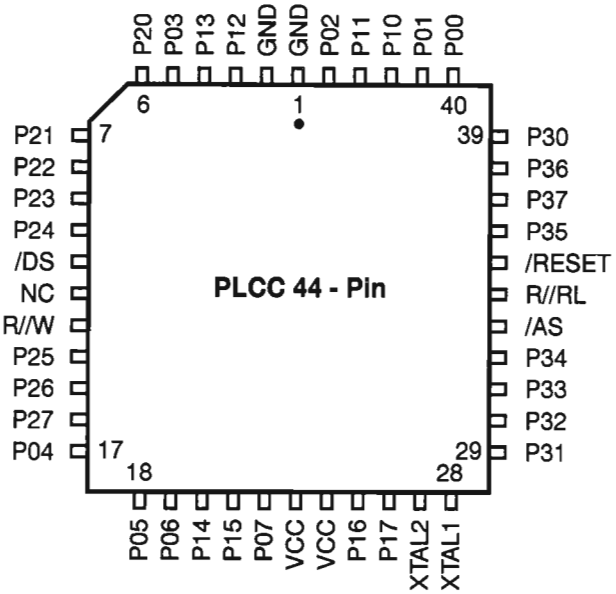


Figure 5. 44-Pin PLCC Pin Assignments

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	N/C	Not Connected	
13	R//W	Read/Write	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output
20-21	P14-15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23,24	V_{CC}	Power Supply	
25-26	P16-17	Port 1, Pins 6,7	In/Output

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
27	XTAL2	Crystal, Oscillator Clock	Output
28	XTAL1	Crystal, Oscillator Clock	Input
29-31	P31-33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless Control	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-01	Port 0, Pins 0,1	In/Output
42-43	P10-11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN DESCRIPTION (Continued)

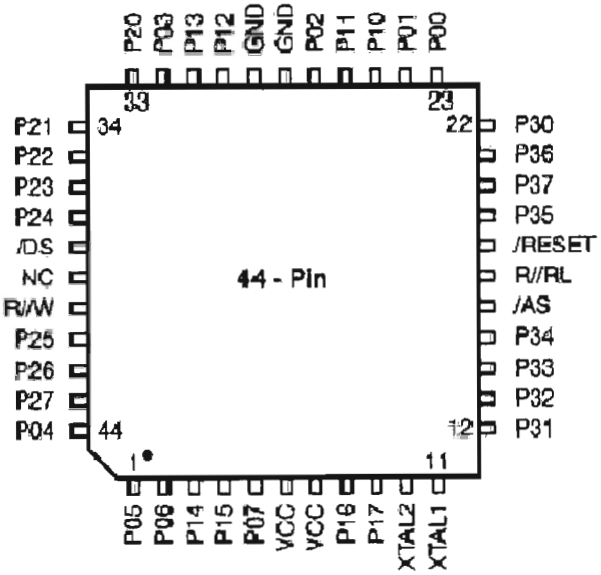


Figure 6. 44-Pin LQFP Pin Assignments

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output
3-4	P14-15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	V_{CC}	Power Supply	
8-9	P16-17	Port 1 Pins 6,7	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output
11	XTAL1	Crystal, Oscillator Clock	Input
12-14	P31-33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless Control	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output

Table 4. 44-Pin LQFP Pin Identification

Pin #	Symbol	Function	Direction
21	P36	Port 3, Pin 6	Output
22	P30	Port 3, Pin 0	Input
23-24	P00-01	Port 0, Pins 0,1	In/Output
25-26	P10-11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	N/C	Not Connected	
40	R//W	Read/Write	Output
41-43	P25-27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA
3. This excludes XTAL pins.
4. Device pin is not atan output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7.)

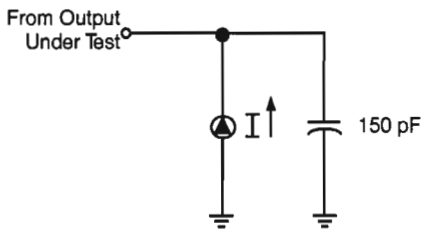


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.4	V	I_{OL} = +12 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.8	V		13
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.6	V		13
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		13
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.6	V		13
V_{OLR}	Reset Output Low Voltage	3.0V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
		5.5V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	13
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	2	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
IIR	Reset Input Current	3.0V	-20	-130	-18	-130	-60	µA		
		5.5V	-20	-180	-18	-180	-85	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	4
		5.5V		25		25	20	mA	@ 16 MHz	4
		3.0V		15		15	5	mA	@ 12 MHz	4
		5.5V		20		20	15	mA	@ 12 MHz	4

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		5.5V		10		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,11, 14
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10

Sym	Parameter	V_{CC} Note [3]	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [1] @ 25°C	Units	Conditions	Notes
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	0.7	10	3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	1.4	15	1.4	20	5	µA	$0V < V_{IN} < V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.0V	-0.6	-5	-0.6	-7	-3	µA	$0V < V_{IN} < V_{CC}$	9
		5.5V	-1.0	-8	-1.0	-10	-6	µA	$0V < V_{IN} < V_{CC}$	9
V_{LV}	V_{CC} Low Voltage Protection Voltage				2.0	3.3	2.8	V	4 MHz max Int. CLK Freq.	7,15
			2.2	3.1			2.8		6 MHz max Int. CLK Freq.	7,14
V_{OH}	Output High Voltage (Low EMI Mode)	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -0.5 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -0.5 mA	
V_{OL}	Output Low Voltage (Low EMI Mode)	3.0V		0.6		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0 mA	

Notes:

1. Typicals are at V_{CC} = 5.0V and 3.3V.
2. GND = 0V.
3. The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC}=3.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC}-5.0V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 10 pF.
6. Same as note [4] except inputs at V_{CC}.
7. The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
8. Standard Mode (not Low EMI).
9. Auto Latch (Mask Option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Z86C43 only.
14. 0°C to 70°C (standard temperature).
15. –40°C to 150°C (extended temperature).

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (C43 Only)

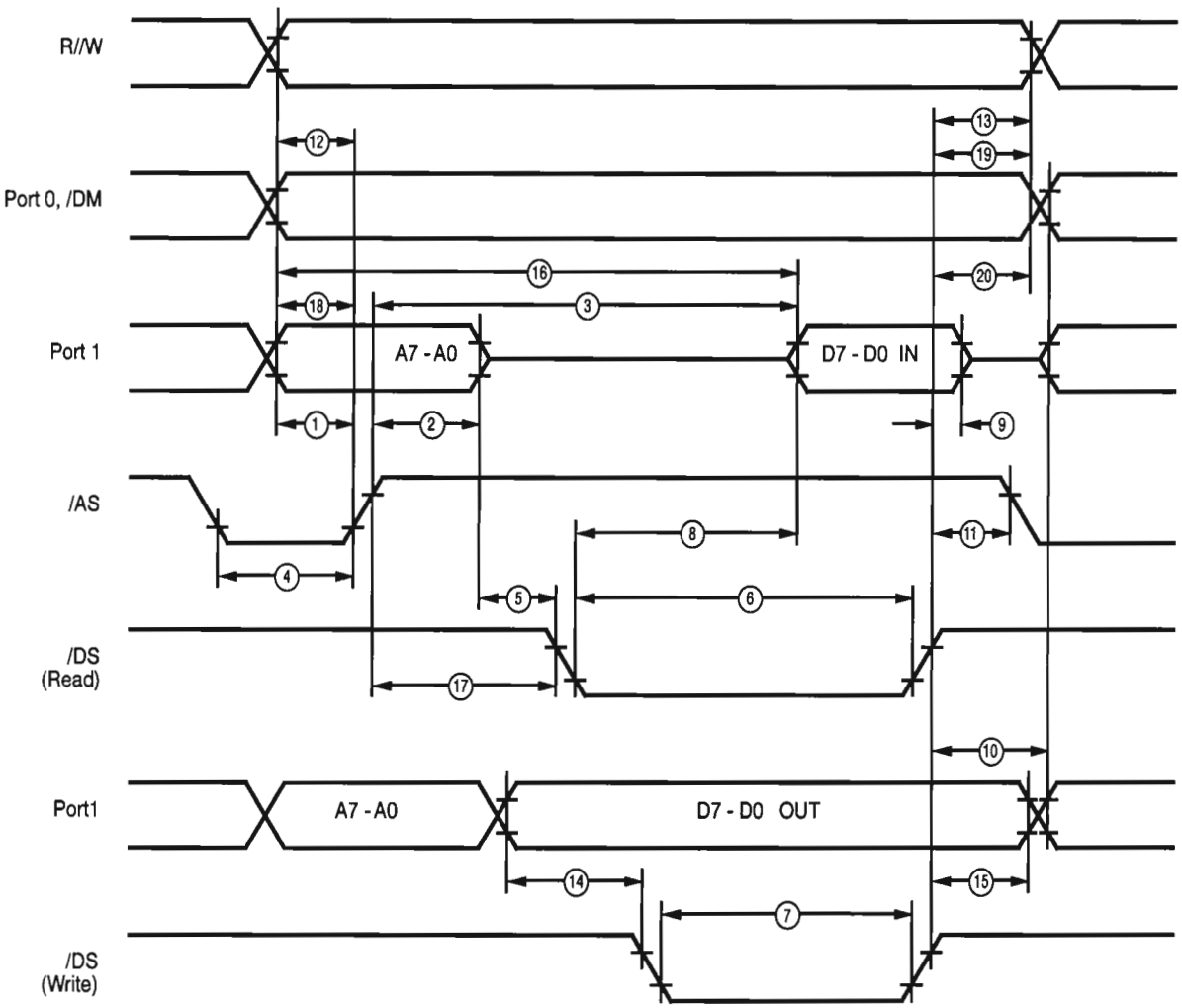


Figure 8. External I/O or Memory Read and Write Timing Table (Z86C43 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (C43 Only) (SCLK/TCLK = XTAL/2)

			Note	T_A=–0°C to 70°C				T_A = –40°C to +105°C					
			[3]	12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25		ns	2
			5.5	35		25		35		25			2
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	1,2
			5.5		250		180		250		180	ns	2
4	TwAS	/AS Low Width	3.0	55		40		55		40		ns	2
			5.5	55		40		55		40		ns	2
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135		ns	1,2
			5.5	200		135		200		135		ns	1,2
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80		ns	1,2
			5.5	110		80		110		80		ns	1,2
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	1,2
			5.5		150		75		150		75	ns	1,2
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.0	0		0		0		0		ns	2
			5.5	0		0		0		0		ns	2
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50		ns	2
			5.5	55		50		55		50		ns	2
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35		ns	2
			5.5	45		35		45		55		ns	2
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	3.0	45		25		45		25		ns	2
			5.5	45		25		45		25		ns	2
13	TdDS(R/W)	/DS Rise to R//W Not Valid	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25		ns	2
			5.5	55		25		55		25		ns	2
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	1,2
			5.5		310		230		310		230	ns	1,2
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45		ns	2
			5.5	65		45		65		45		ns	2
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30		ns	2
			5.5	35		30		35		30		ns	2

AC CHARACTERISTICS (Continued)

No	Symbol	Parameter	Note [3] V_{CC}	T_A=–0°C to 70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A = –40°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
19	TdDs(DM)	/DS Rise to DM	3.0	45		35		45		35		ns	2
		Valid Delay	5.5	45		35		45		35		ns	2
20	ThDS(AS)	/DS Valid to Address	3.0	45		35		45		35		ns	2
		Valid Home Time	5.5	45		35		45		35		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

Additional Timing Diagram

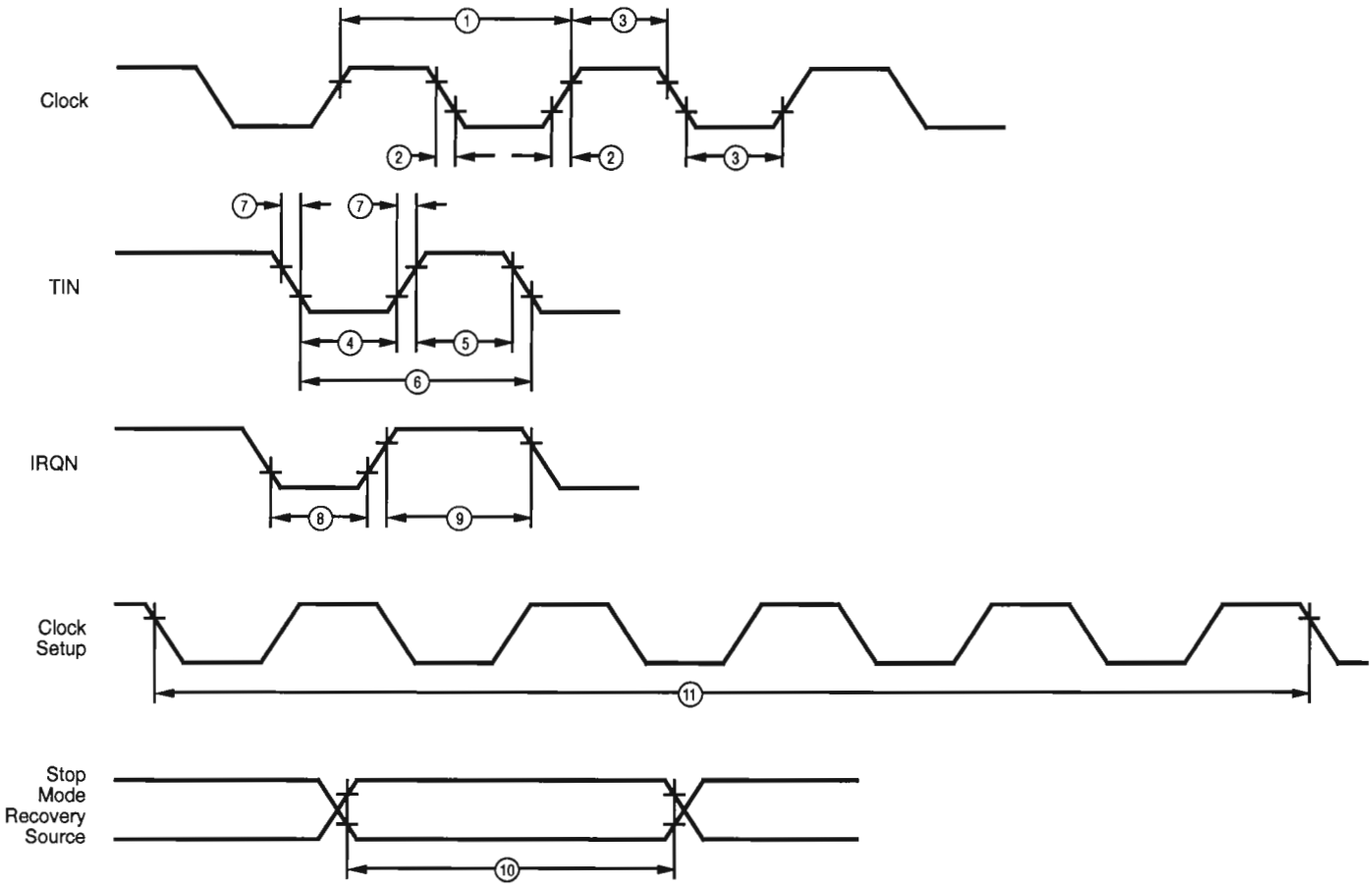


Figure 9. Additional Timing

AC CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3] V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A =–4 0°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1,7
			3.0V	250	DC	250	DC	250	DC	250	DC	ns	1,8
			5.5V	250	DC	250	DC	250	DC	250	DC	ns	1,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
			3.0V	125		125		125		125		ns	1,8
			5.5V	125		125		125		125		ns	1,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		4
			5.5V		5TpC		5TpC		5TpC		5TpC		4
													D1, D0 [Note]
12	Twdt	Watch-Dog Timer Delay Time before time-out	3.0V	7		7		7		7		ms	0, 0 [5]
			5.5V	3.5		3.5		3.5		3.5		ms	0, 0 [5]
			3.0V	14		14		14		14		ms	0, 1 [5]
			5.5V	7		7		7		7		ms	0, 1 [5]
			3.0V	28		28		28		28		ms	1, 0 [5]
			5.5V	14		14		14		14		ms	1, 0 [5]
			3.0V	112		112		112		112		ms	1, 1 [5]
			5.5V	56		56		56		56		ms	1, 1 [5]

No	Symbol	Parameter	Note [3] V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	T_A =–4 0°C to +105°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
13	TPOR	Power-On Reset Delay	3.0V	3	24	3	24	3	25	3	25	ms	
			5.5V	1.5	13	1.5	13	1	14	1	14	ms	

Notes: :

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. Standard Oscillator mode, Pcon RegD7=1.
8. Maximum frequency for external XTAL Clock is 4MHz when using low EMI oscillator mode, Pcon Reg D7=0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 8 MHz Min	Max	T_A = 40°C to +105°C 8 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
			3.0V	125	DC	125	DC	ns	1,7
			5.5V	125	DC	125	DC	ns	1,7
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7
			5.5V		25		25	ns	1,7
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
			3.0V	62		62		ns	1,7
			5.5V	62		62		ns	1,7
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7
			5.5V	70		70		ns	1,7
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			1,7
			5.5V	3TpC		3TpC			1,7
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7
			5.5V	4TpC		4TpC			1,7
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7
			5.5V		100		100	ns	1,7
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,2,7
			5.5V	70		70		ns	1,2,7
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			1,3,7
			5.5V	3TpC		3TpC			1,3,7
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			1,2,7
			5.5V	3TpC		2TpC			1,2,7
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4
			5.5V	12		12		ns	4
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		4,9
			5.5V		5TpC		5TpC		4,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0.
8. Maximum frequency for external XTAL clock is 4 MHz when using low EMI Oscillator mode Pcon Reg.D7=0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Diagrams

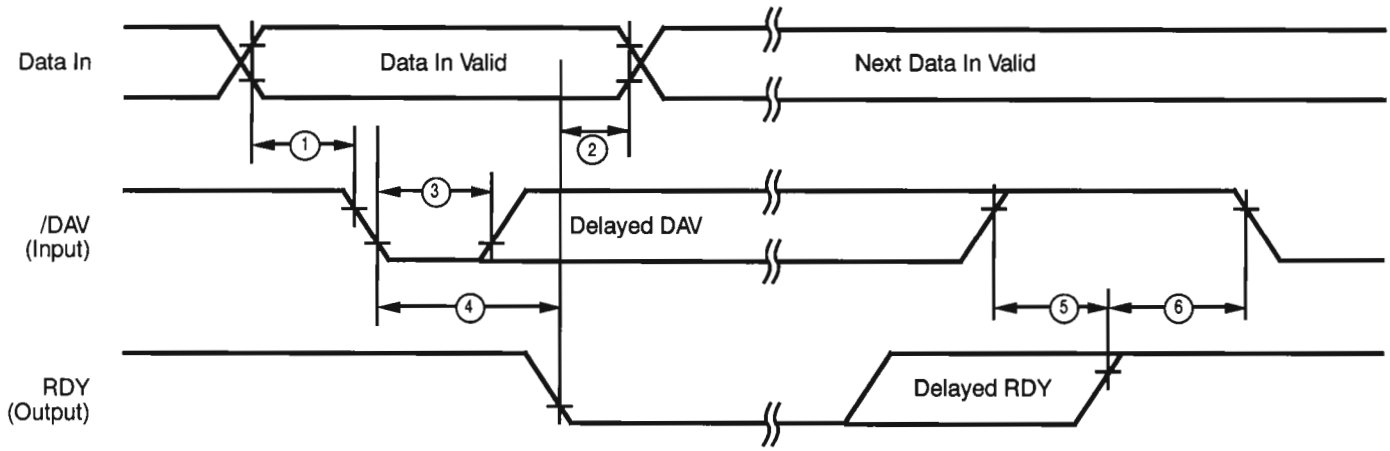


Figure 10. Input Handshake Timing

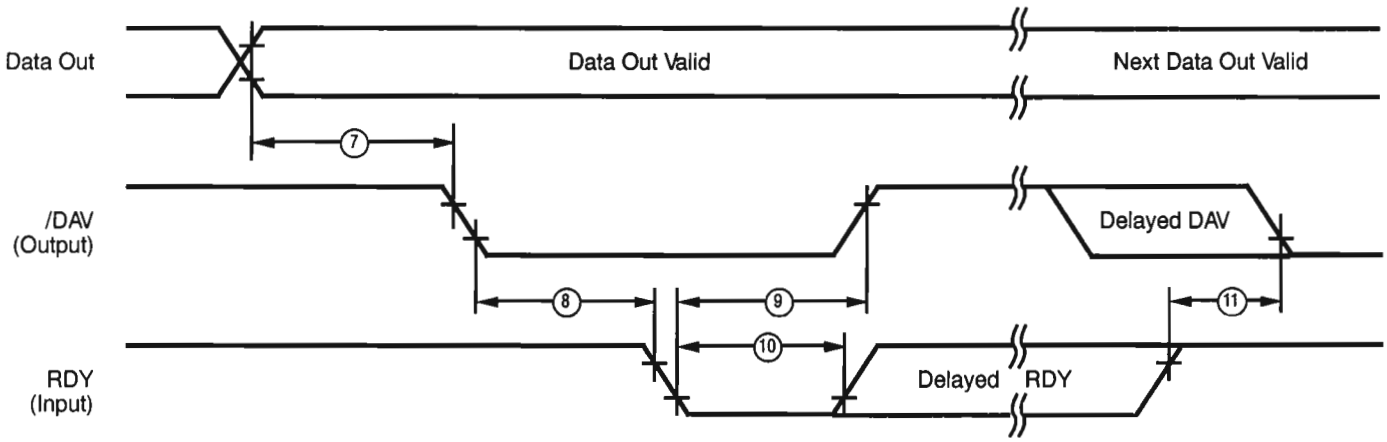


Figure 11. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

				T_A= 0°C to +70°C				T_A = –40°C to +105°C				
			V_{CC}	12 MHz		16 MHz		12 MHz		16 MHz		Direction
No	Symbol	Parameter	Note [1]	Min	Max	Min	Max	Min	Max	Min	Max	Data
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
2	ThDI(RDY)	Data In Hold Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
3	TwDAV	Data Available Width	3.0V	155		155		155		155		IN
			5.5V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		0		0		0		0	IN
			5.5V		0		0		0		0	IN
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	3.0V		120		120		120		120	IN
			5.5V		80		80		80		80	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		42		31		OUT
			5.5V	42		31		42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		0		0		OUT
			5.5V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160		160		160	OUT
			5.5V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		110		110		OUT
			5.5V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110		110		110	OUT
			5.5V		80		80		80		80	OUT

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

ROM Mask options available:

1. Enable ROM Protect
2. Enable RAM Protect
3. RC or Crystal Clock Source
4. WDT automatically enabled after reset.
5. Enable autolatches

PIN FUNCTIONS

/ROMless (input, active Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a Z86C90 ROMless Z8. (Note that, when left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version) Not available on Z86C33.

Note: When using in ROM Mode in High EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid. Not available on Z86C33.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write. Not available on Z86C33.

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W (output, write Low). Read/Write, the R//W signal is Low when the Z86C33/43 is writing to the external program or data memory. Not available on Z86C33.

Port 0 (P00-P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03-P00 input/output and P07-P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W (Figure 12).

PIN FUNCTIONS (Continued)

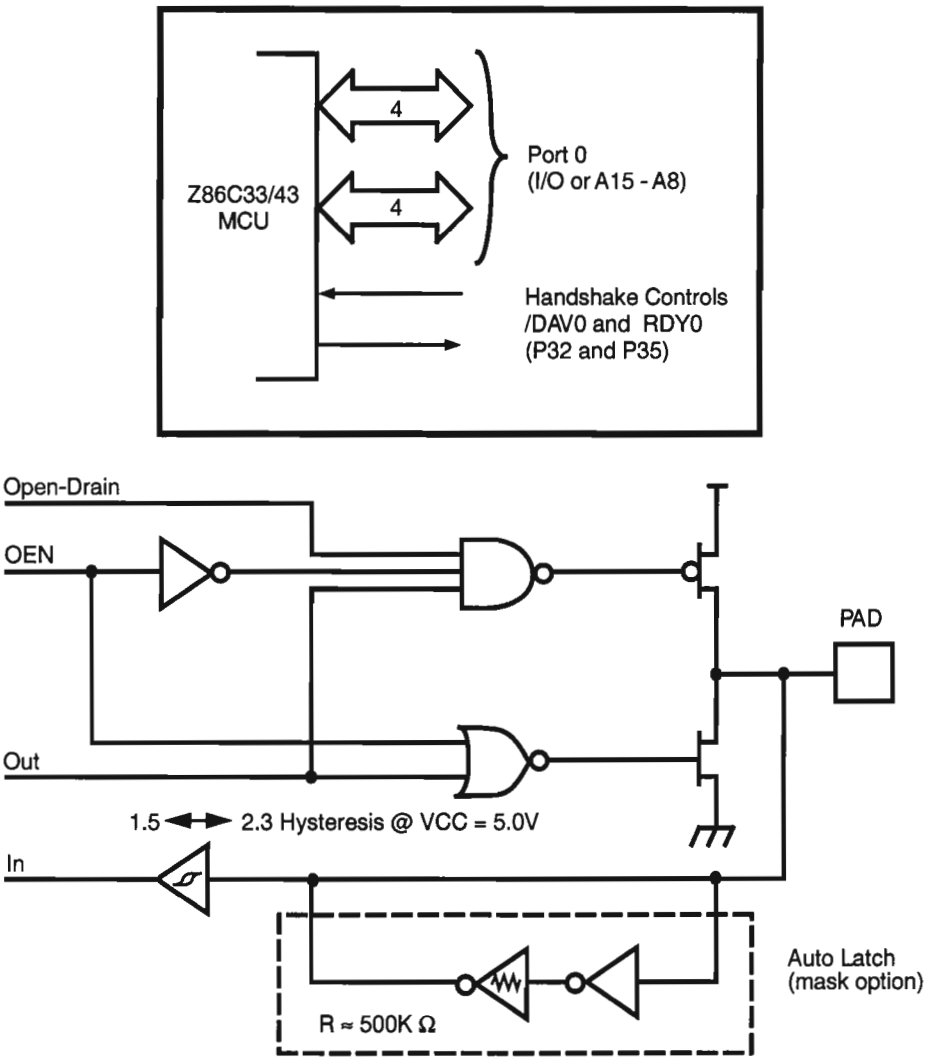


Figure 12. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port (Figure 13), with multiplexed Address (A7-A0) and Data (D7-D0) ports. For the Z86C33/43 ROM device, these eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Note: Port 1 is not available on Z86C33 and P01M Register for Z86C33 must have Bit D4,D3 set as 00.

Note: Low EMI mode is not supported on the emulator for Port1. Pcon reg. D4 must be 1.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 4095 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86C33/43 to share common resources in multiprocessor and DMA applications.

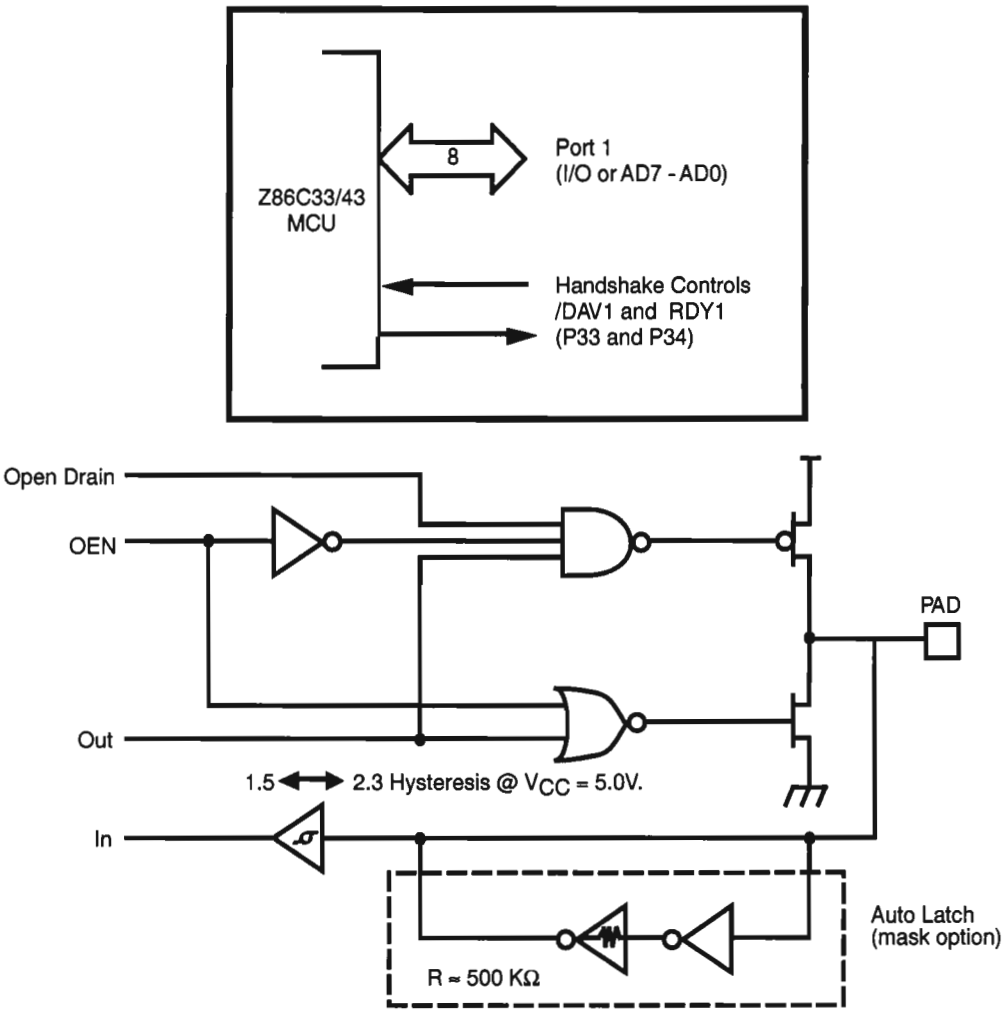


Figure 13. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 14).

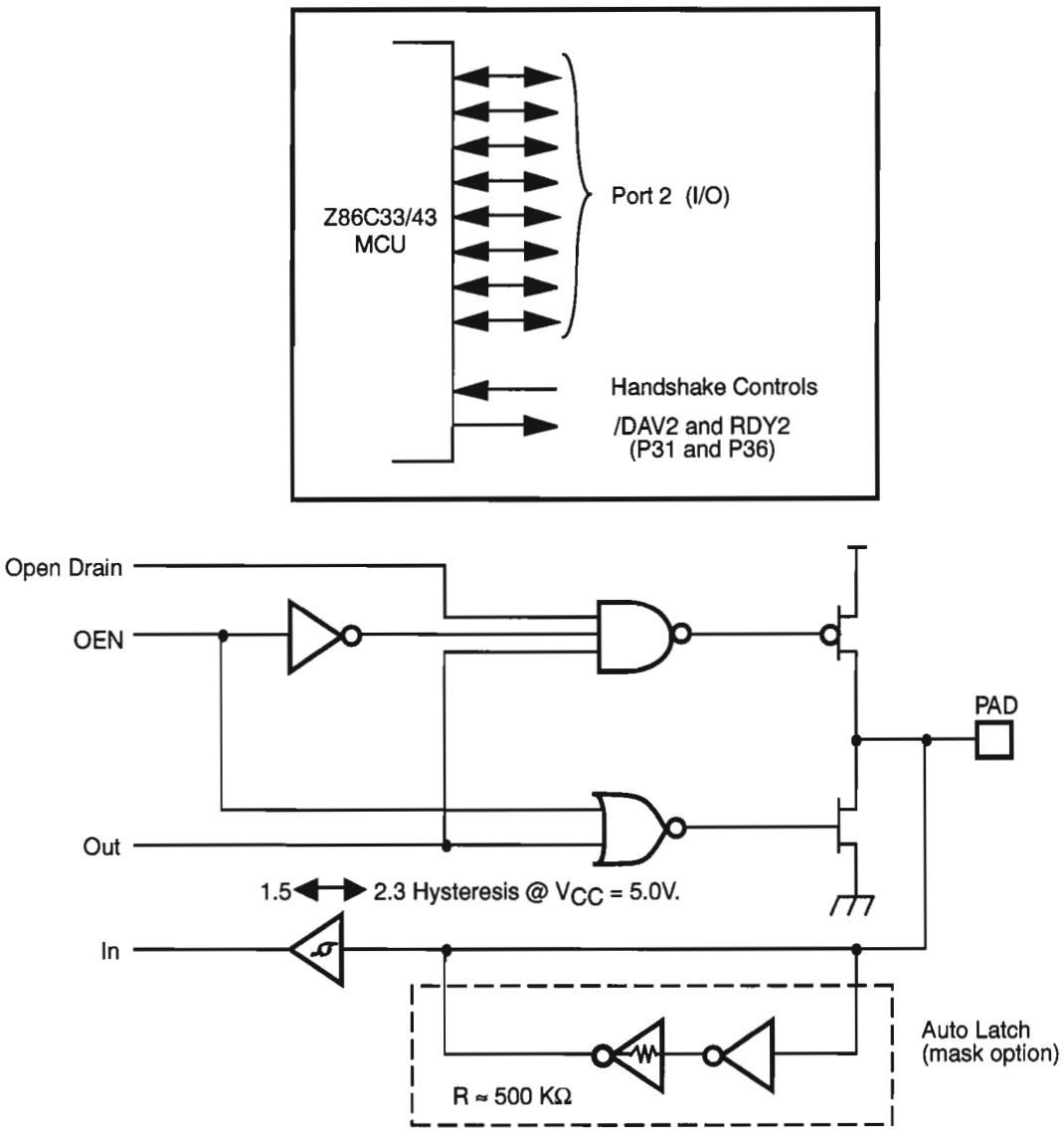


Figure 14. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible, four fixed inputs (P33-P30) and four fixed outputs (P34-P37), and is configured under software control for Input/Output, Counter/Timers, interrupt, port handshake, and Data Memory functions. Port 3, pin 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, P36, P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 0 and pin 3 are falling edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (TIN) and P36 (TOUT). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (TIN and TOUT); Data Memory Select (/DM, see Table 5, Figure 43).

P34 output can be software-programmed to function as a Data Memory Select (DM). The Port 3 mode register (P3M) bit D3, D4 selects this function. When accessing external Data Memory, the P34 goes active Low; when accessing external program memory, the P34 goes High.

Table 5. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P1 HS	P2 HS	Ext
P30	IN			IRQ3				
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT		AN1-OUT			R/D		/DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT		AN2-OUT					

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto Latch instruction puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Deletion of all Port Auto Latches is available as a ROM Mask option. The Auto Latch Delete option is selected by the customer when the ROM code is submitted.

Comparator Inputs. Port 3, Pins P31 and P32 each have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. P34 and P37 outputs the comparator outputs by software-programming the PCON Reg. bit D0 to 1.

Note: Must add a two NOP delay after selecting the P3M bit D1 to 1 before the comparitor output is valid. IRQ0, IRQ1, and IRQ2 should be cleared in IRQ register when the comparitor is enabled or disabled to avoid spurious noise creating a false interrupt.

PIN FUNCTIONS (Continued)

/RESET (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. RESET does depend on oscillator operating to achieve full reset conditions except a permanently enabled WDT reset.** Pull-up is provided internally.

Note: /RESET pin is not available on Z86C33.

After the POR time, /RESET is a Schmitt-triggered input. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000C (HEX), after the RST is released. For Power-On Reset, the reset output time is TPOR ms.

Once program execution begins, /AS and /DS toggles only for external memory accesses. The Z86C33/43 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a Stop-Mode Recovery operation or from a WDT reset out of STOP Mode.

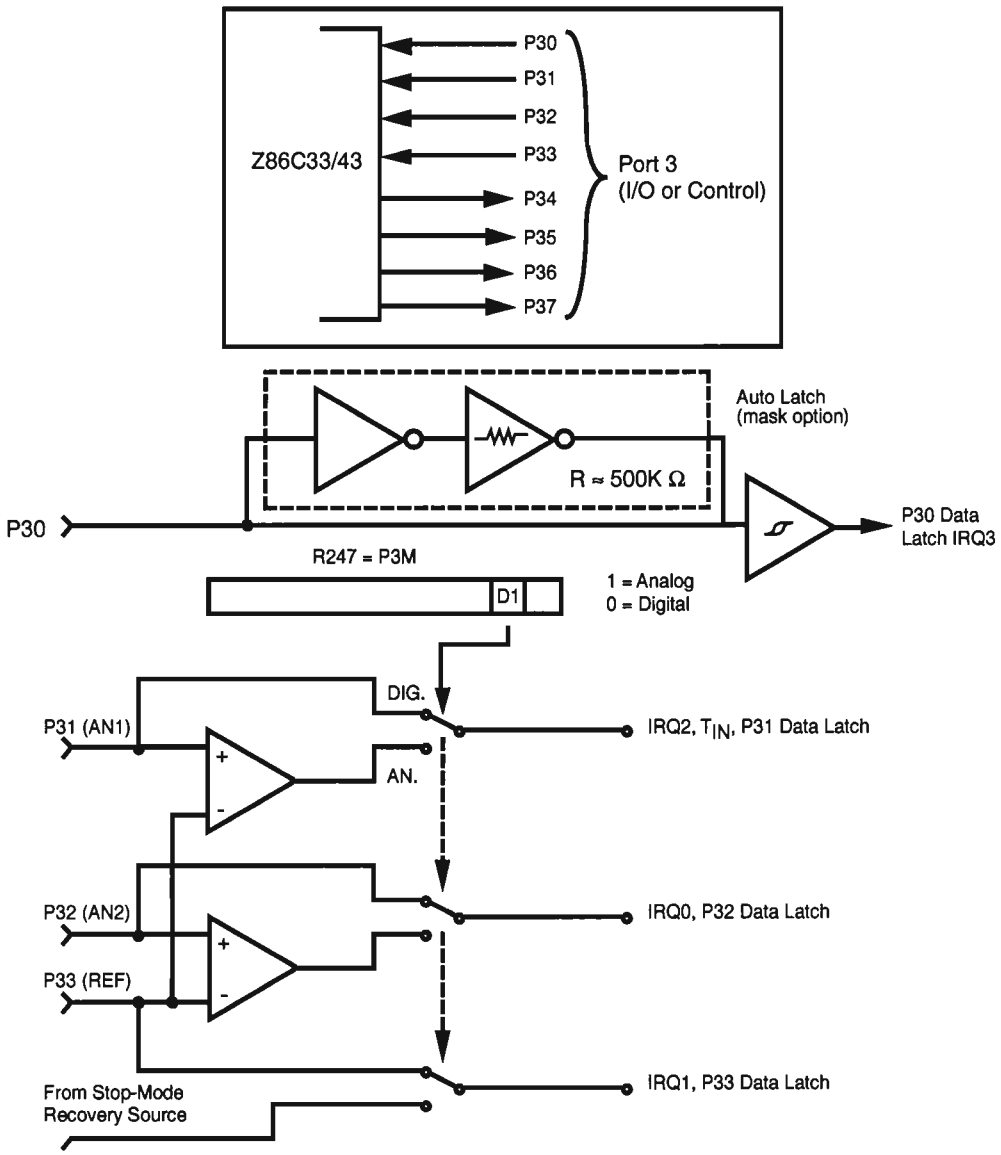


Figure 15. Port 3 Configuration

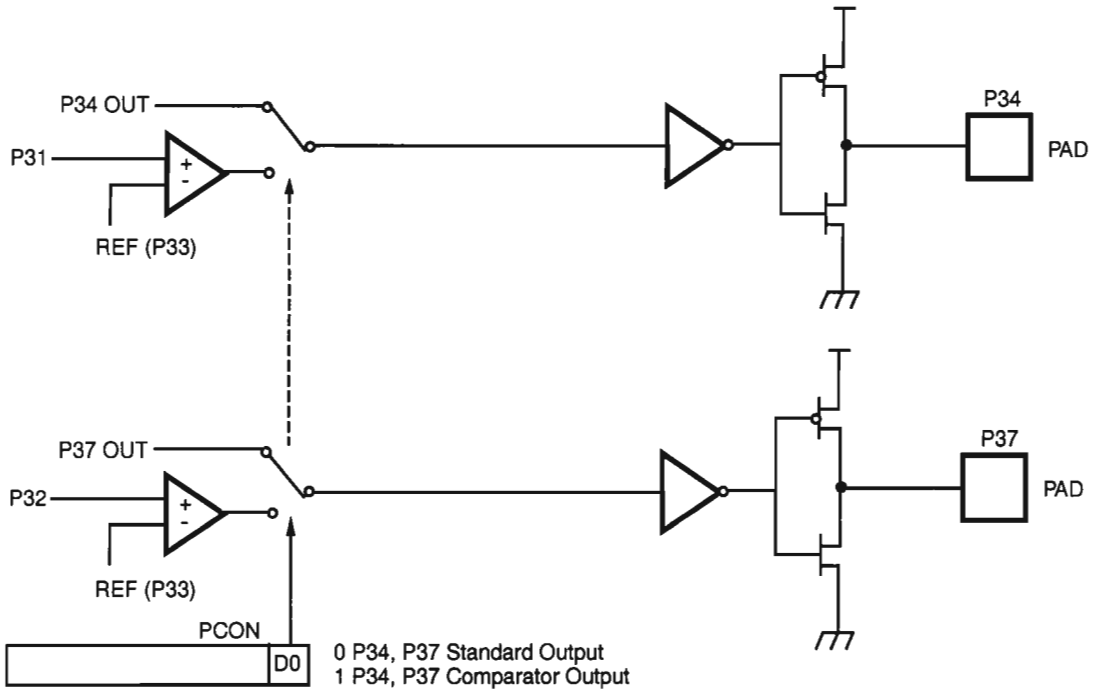


Figure 16. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86C33/43 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Auto Power-On Reset circuitry is built into the Z86C33/43, eliminating the need for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the Reset pin, so a pull-up resistor is not required; however, in high EMI (noisy) environment, it is recommended that a small value pull-up resistor be used.

Note: /RESET pin is not available on Z86C33.

Program Memory. The Z86C33/43 addresses up to 4 KB of internal program memory and 60 KB of external memory (Figure 18). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address 4095 consists of on-chip mask-programmed ROM. At addresses 4096 and greater, the Z86C33/43 executes external program memory fetches through Port 0 and Port 1 in Address/Data mode.

The 4 KB program memory is mask programmable. **A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to Program Memory in external program mode. ROM look-up tables can be used with this feature.**

The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

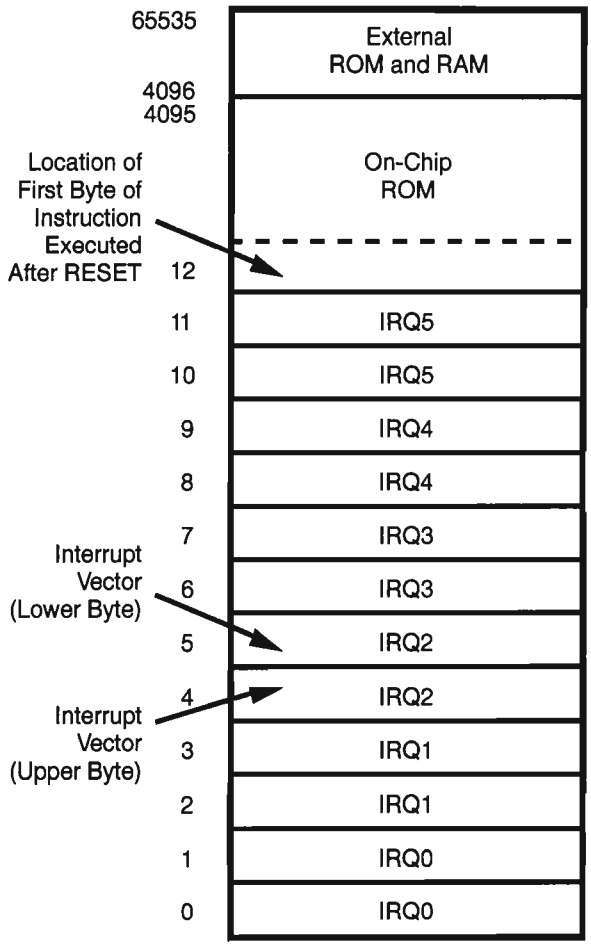


Figure 17. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Data Memory (/DM). The Z86C33/43 ROM version can address up to 60 KB of external data memory beginning at location 4096. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 19). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode. Available only on Z86C43.

Expanded Register File (ERF). The Z86C33/43 register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group (Figure 18). These register groups are known as the Expanded Register File (ERF). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 18). Three system configuration registers reside in the Expanded Register File at Bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented, and is open for future expansion.

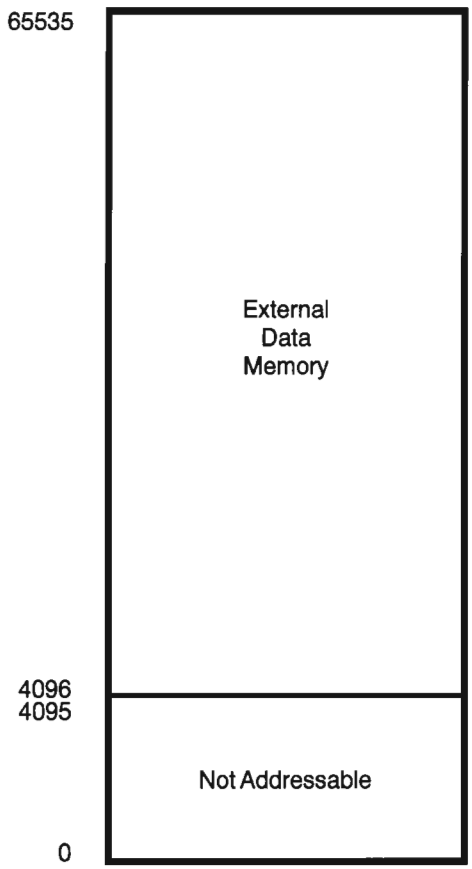


Figure 18. Data Memory Map

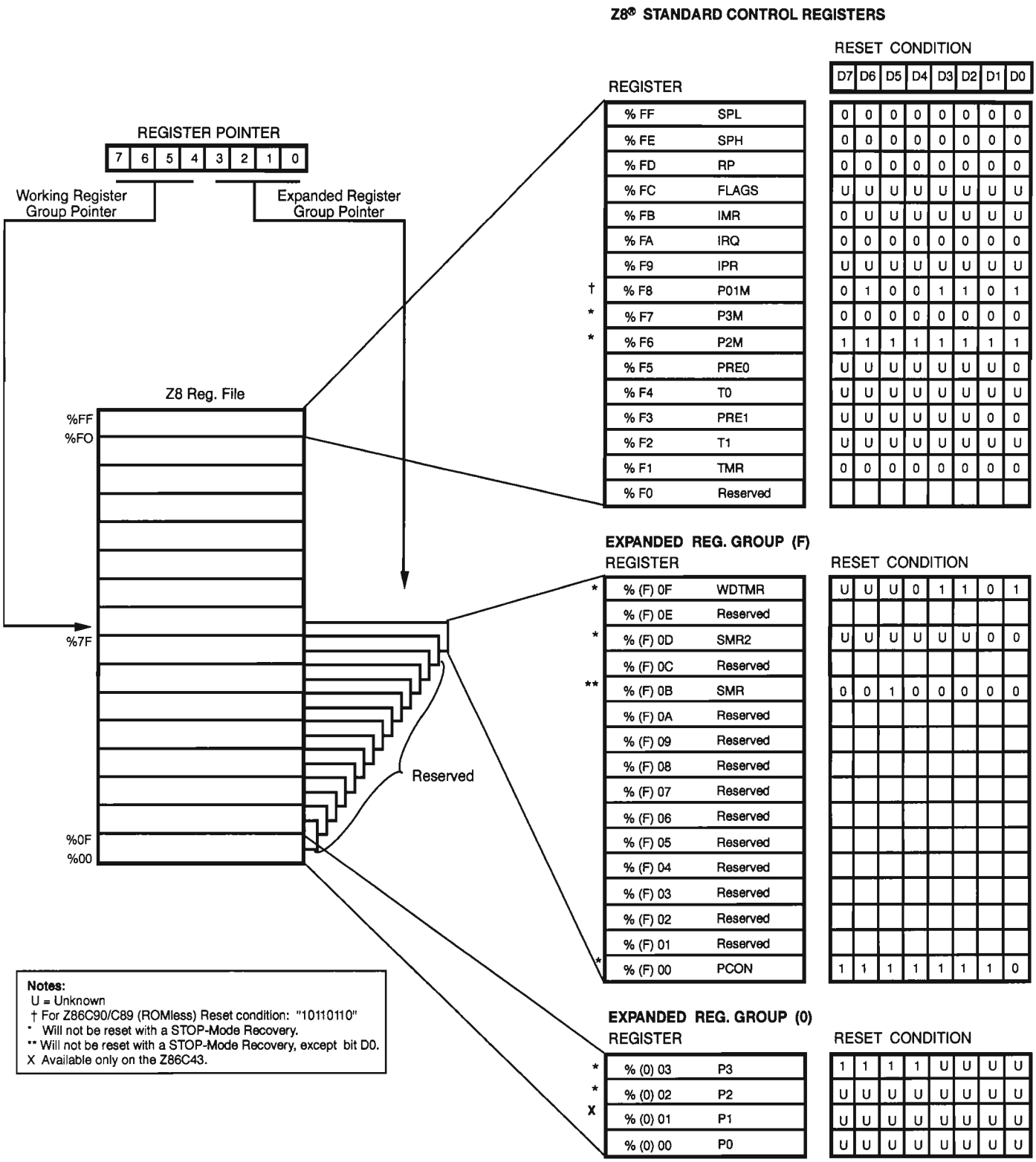


Figure 19. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Register File. The register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), plus three system configuration registers in the expanded register group. The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 22). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

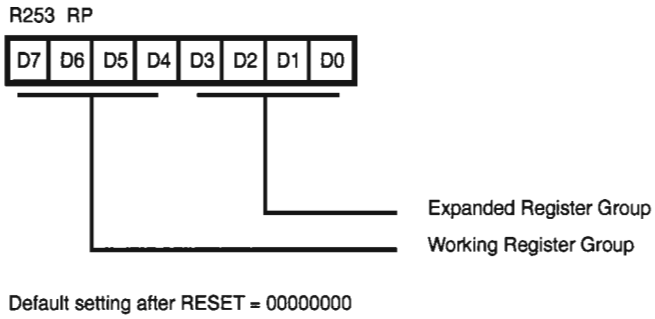


Figure 20. Register Pointer Register

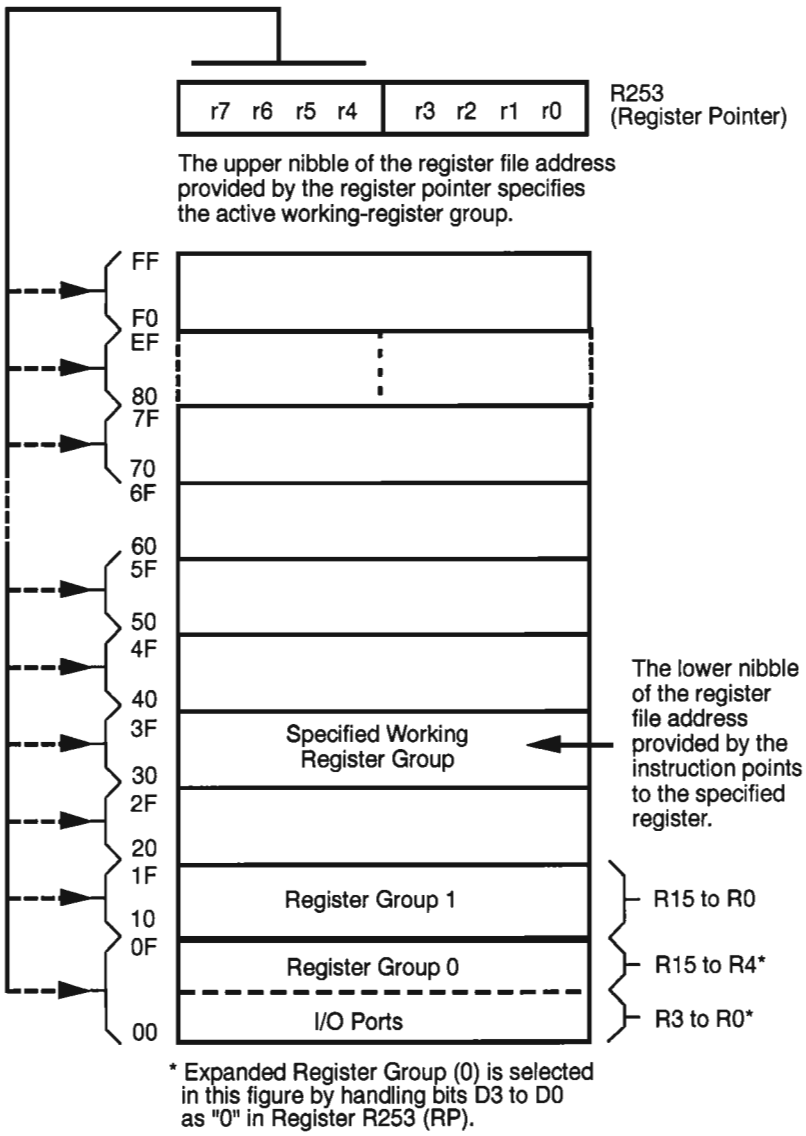


Figure 21. Register Pointer

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the IMR register, bit D6. A 1 in D6 enables RAM Protect.

Stack. The Z86C33/43 external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH is used as a general-purpose register when using internal stack only. The Z86C33 uses the 8-bit stack pointer (R255) for internal stack only.

Note: R254 and R255 are set to 00Hex after any reset or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 23).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. TIN Mode is enabled by setting R243 PRE1 Bit D1 to 0.

FUNCTIONAL DESCRIPTION (Continued)

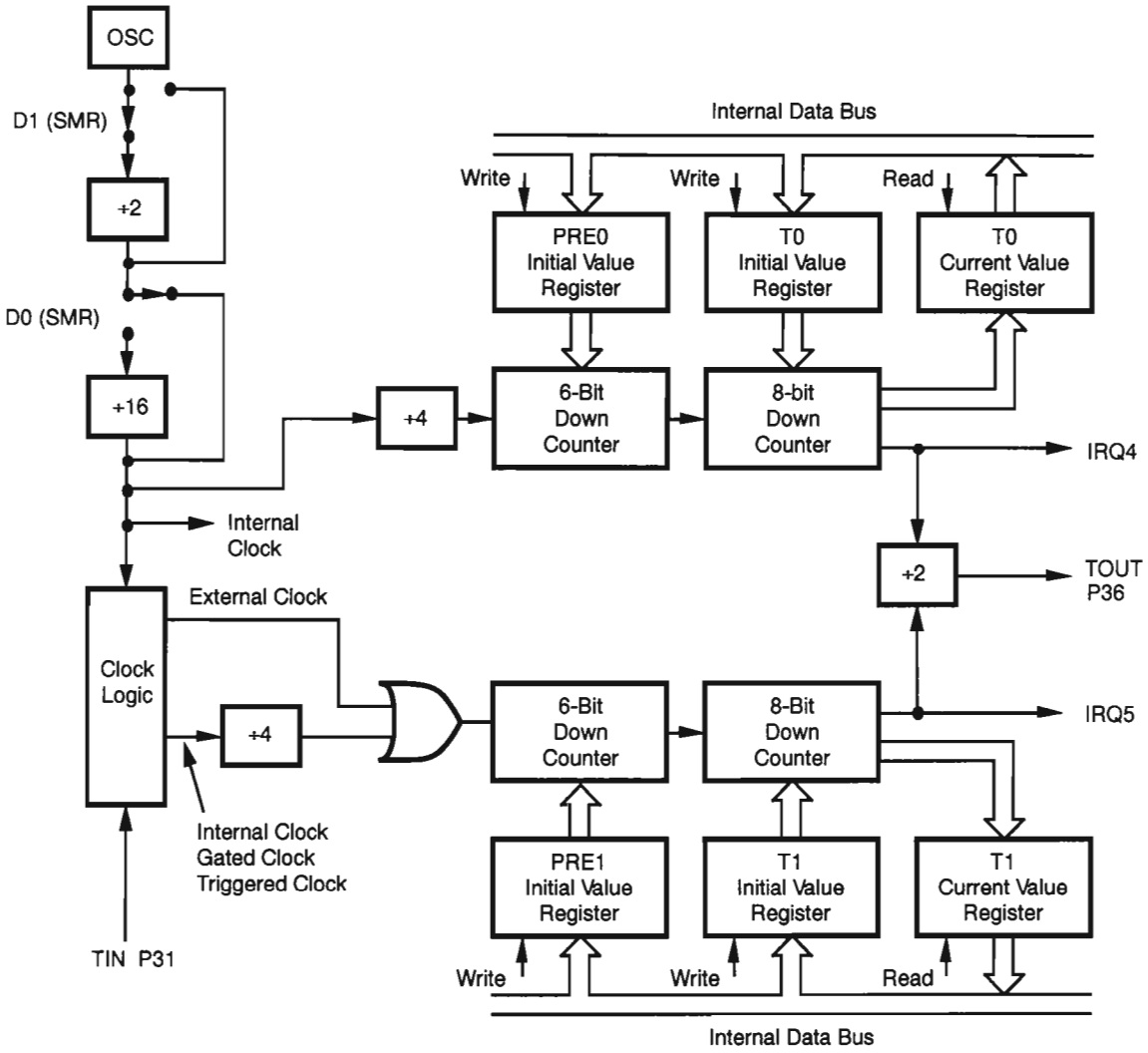


Figure 22. Counter/Timer Block Diagram

Interrupts. The Z86C33/43 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 23) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 6). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

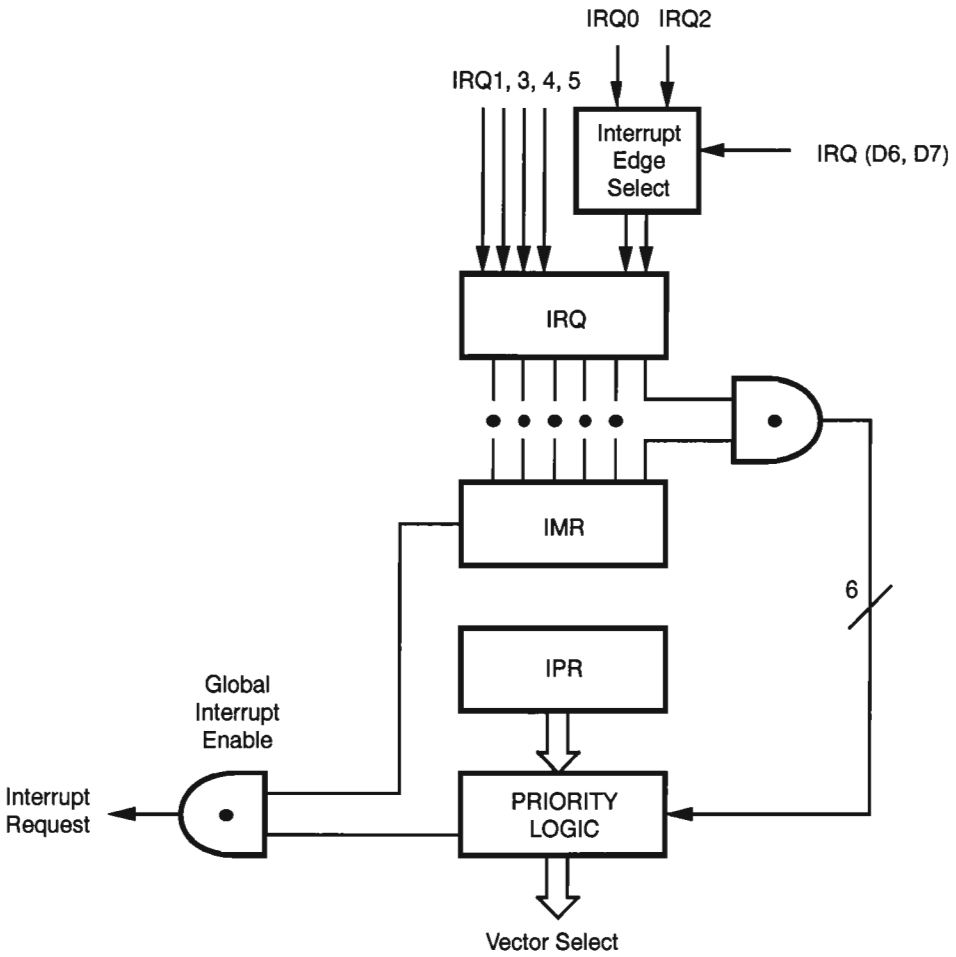


Figure 23. Interrupt Block Diagram

Table 6. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, TIN	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z86C33/43 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin. When in analog mode, the IRQ1 is generated by the Stop-Mode Recovery source selected by SMR Reg. bits D4,D3,D2, or SMR2 D1or D0.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 7.

Table 7. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**P31**	**P32**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86C33/43 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when counting from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator. The RC oscillator option is mask-programmable on the Z86C33/43 and is selected by the customer at the time when the ROM code is submitted. (Note that the RC option is available up to 8 MHz.) The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 24).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).

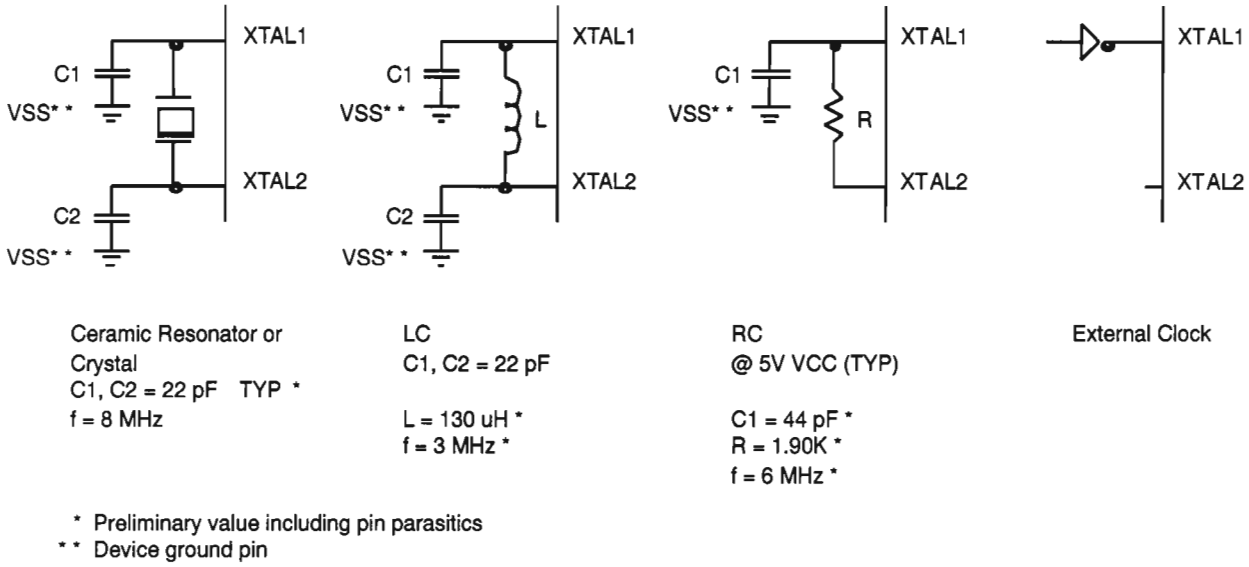


Figure 24. Oscillator Configuration

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR=1).
3. WDT time-out.

The POR time is a specified as TPOR. Bit 5 of the STOP-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be enabled and executed to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                  or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. It also reduces the standby current to 10 µA or less. The STOP Mode is terminated by a reset only, either by WDT time-out, POR, SMR recovery, or external reset. This causes the processor to restart the application program at address 000C (HEX).A WDT time out in STOP Mode will affect all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If permanent WDT is selected, the WDT will run in all modes and can not be stopped or disabled if on board RC oscillator is selected to drive the WDT.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 25).

FUNCTIONAL DESCRIPTION (Continued)

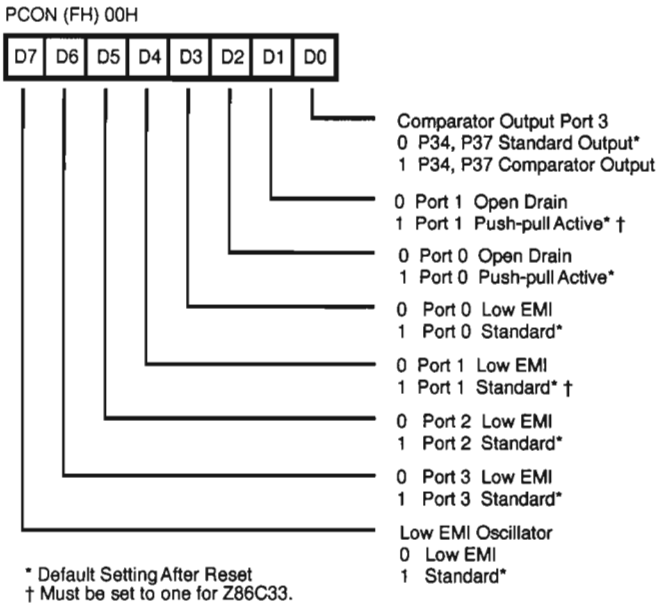


Figure 25. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1. Must set D1=1 for Z86C33.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1. Must be set D4=1 for Z86C33.

Note: For emulator, this bit must be set to 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

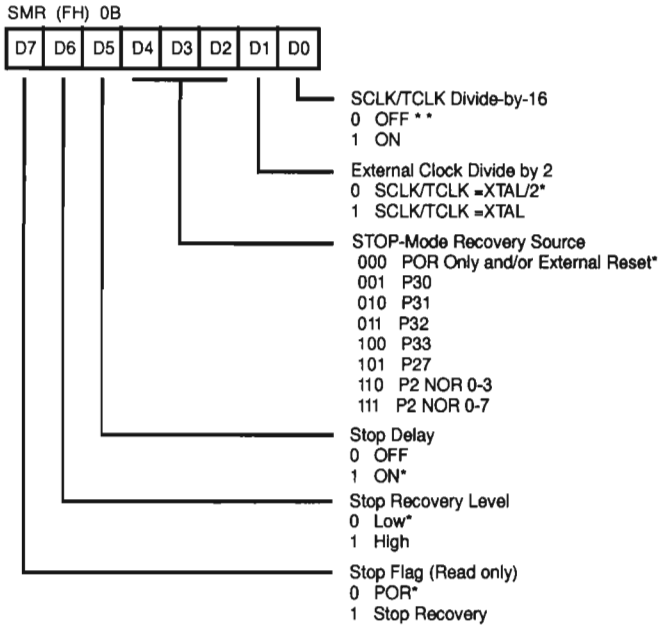
Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator, /DS, /AS and R//W with standard drive, while a 0 configures the oscillator, /DS, /AS and R/W with low noise drive. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1. **Note:** Maximum external clock frequency of 4 MHz when running in the low EMI oscillator mode.

Low EMI Emission. The Z86C33/43 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator
- Internal SCLK/TCLK= XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

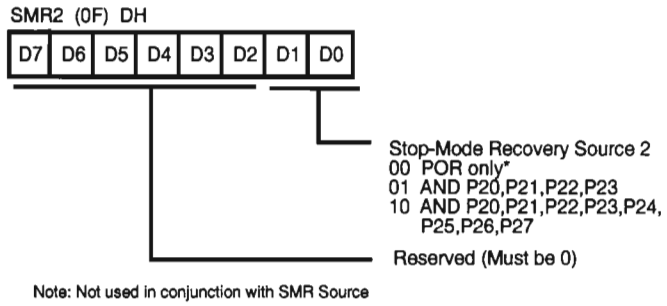
Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 26 and 27). All bits are Write Only, except bit 7 which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

FUNCTIONAL DESCRIPTION (Continued)



Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 26. Stop-Mode Recovery Register (Write Only Except Bit D&, Which Is Read Only)



Note: Not used in conjunction with SMR Source

Figure 27. Stop-Mode Recovery Register 2 (0F) DH: Write Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 4 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 28 and Table 8). When the STOP-Mode Recovery Sources are selected in this register then SMR2 register bits D0, D1 must be set to zero.

Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.

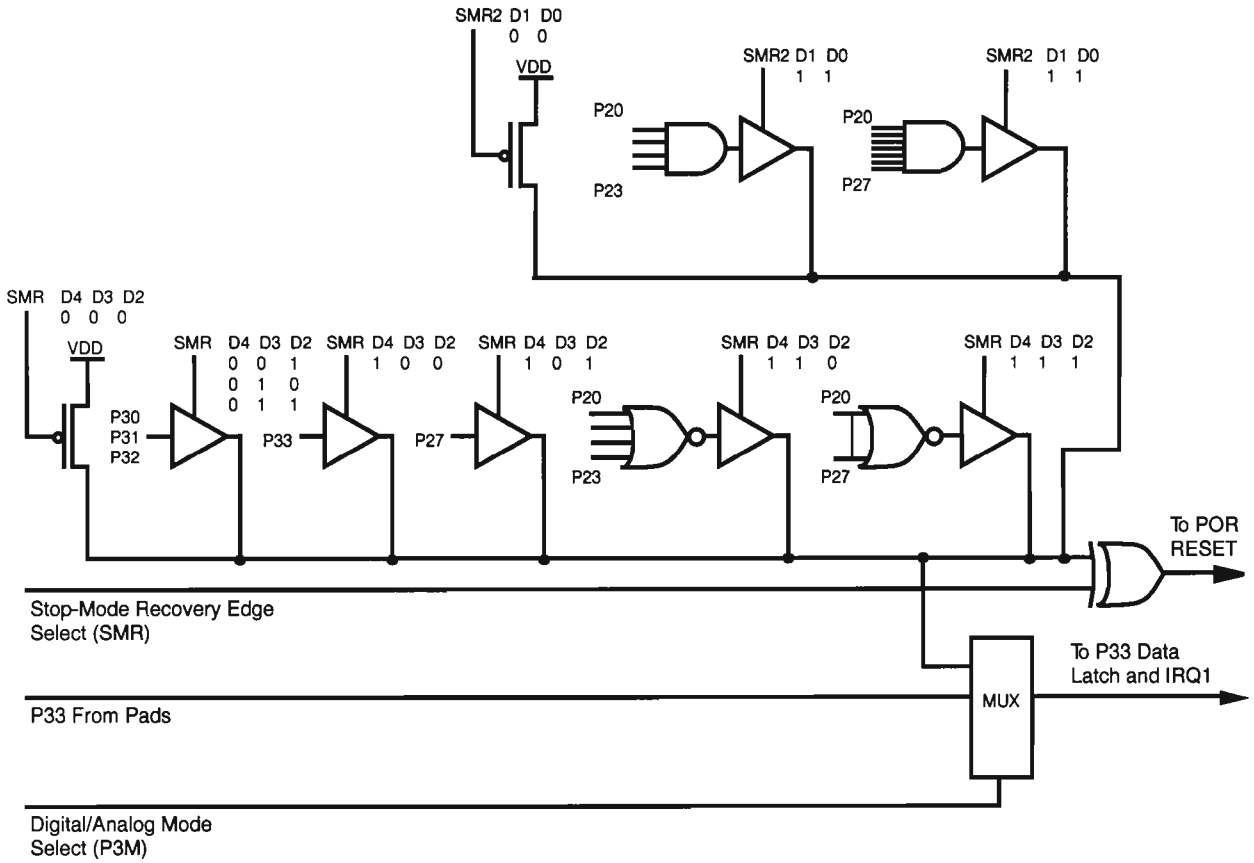


Figure 28. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

Table 8. Stop-Mode Recovery Source

SMR:432 D4	D3	D2	Operation Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the TPOR /RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C33/43 from STOP Mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 27). This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source. Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR2 circuitry.

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

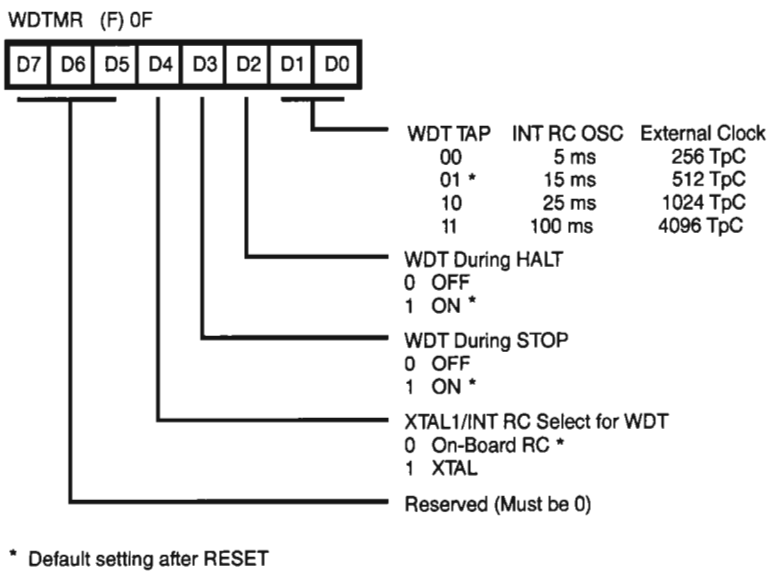
Table 9. Stop-Mode Recovery Source

SMR:10 D1	D0	Operation Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 29).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in STOP-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter will still be enabled even though the SMR stop delay is disabled.



* Default setting after RESET

Figure 29. Watch-Dog Timer Mode Register (Write Only)

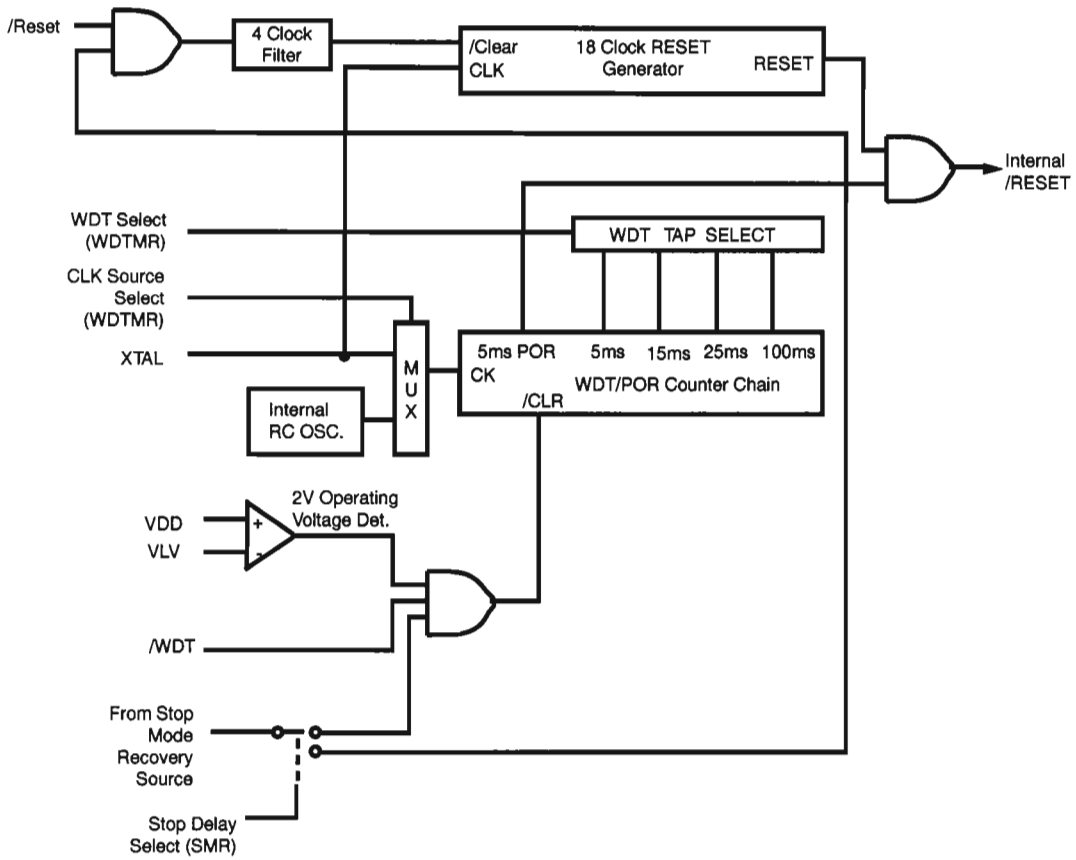


Figure 30. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

WDT Time Select. (D0,D1). Selects the WDT time period and is configured as shown in Table 10.

Table 10. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Notes:
SCLK = system bus clock cycle
The default on reset is 15 ms.
Values given are for V_{CC} = 5.0V.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Note: If permanent WDT is selected, the WDT will run in all modes and can not be stopped or disabled if the on board RC oscillator is selected as the clock source for WDT.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the Internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, watch dog reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 30).

Note: The WDT can be permanently enabled (automatically enabled after reset) through a mask programming option. The option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP Modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage (Low Voltage Protection). The minimum operating voltage is varying with the temperature and operating frequency, while the Low Voltage Protection (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3V and above 1.4V under the following conditions.

Maximum (V_{LV}) Conditions:

Case 1: TA = –40°C, +105°C, Internal Clock Frequency equal or less than 4 MHz

Case 2: TA = –40°C, +85°C, Internal Clock Frequency equal or less than 6 MHz

Note: The internal clock frequency relationship to the XTAL clock is dependent on SMR Bit 0 1 setting.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, above. The device is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 32).

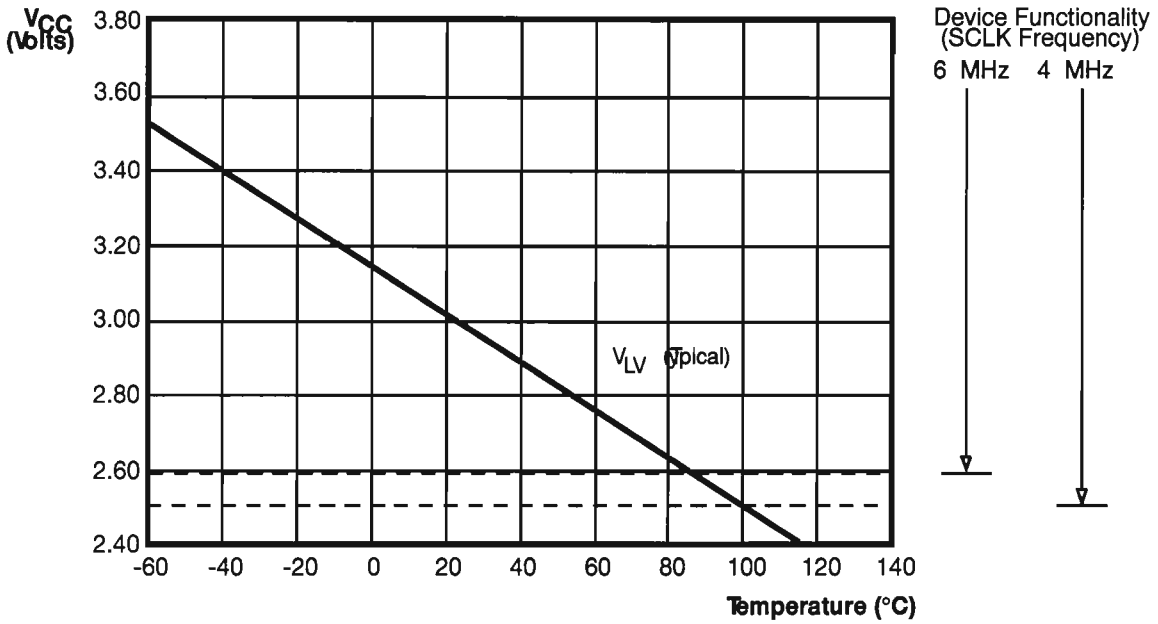
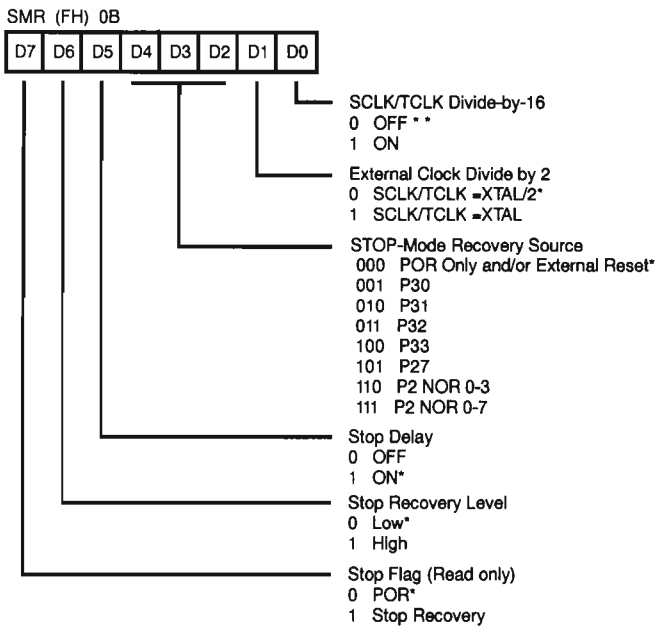


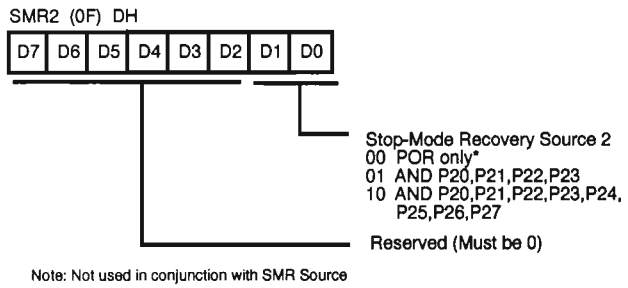
Figure 31. Typical Z86C33/43 Low Voltage Protection vs Temperature

EXPANDED REGISTER FILE CONTROL REGISTERS



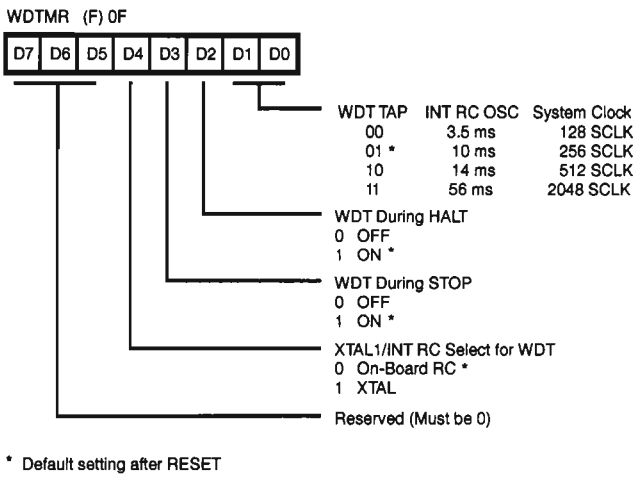
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 32. Stop-Mode Recovery Register (Write Only Except Bit D7, Which Is Read Only)



Note: Not used in conjunction with SMR Source

Figure 33. Stop-Mode Recovery Register2



* Default setting after RESET

Figure 34. Watch-Dog Timer Mode Register (Write Only)

Z8 CONTROL REGISTERS

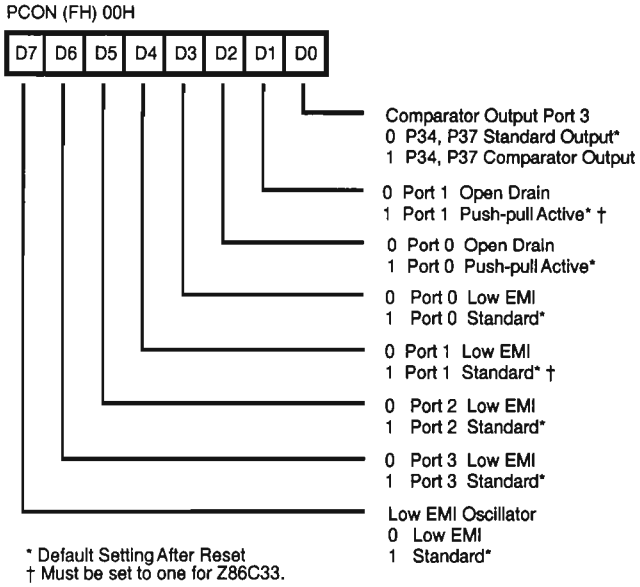


Figure 35. Port Configuration Register (PCON) (Write Only)

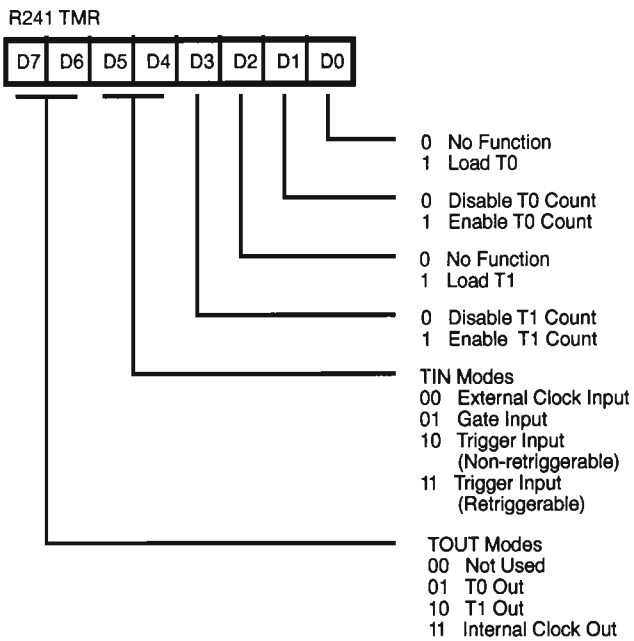


Figure 36. Timer Mode Register ($F1_H$: Read/Write)

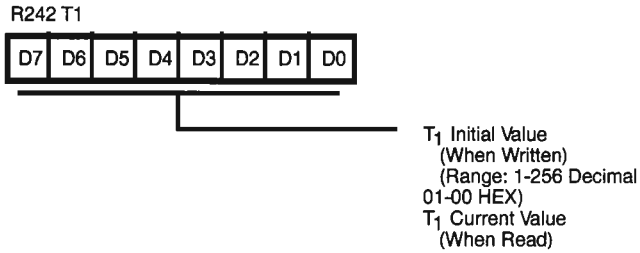


Figure 37. Counter/Timer 1 Register ($F2_H$: Read/Write)

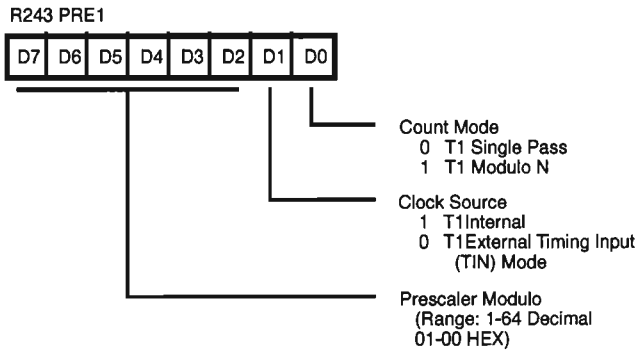


Figure 38. Prescaler 1 Register ($F3_H$: Write Only)

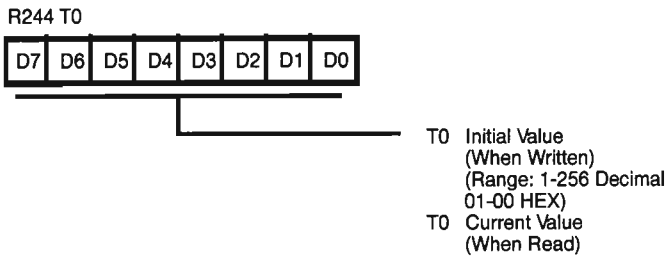


Figure 39. Counter/Timer 0 Register ($F4_H$: Read/Write)

Z8 CONTROL REGISTERS (Continued)

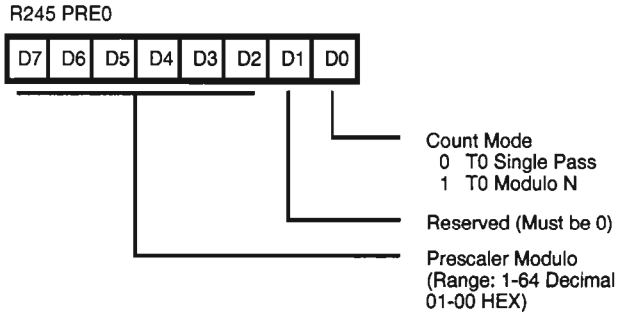


Figure 40. Prescaler 0 Register ($F5_H$: Write Only)

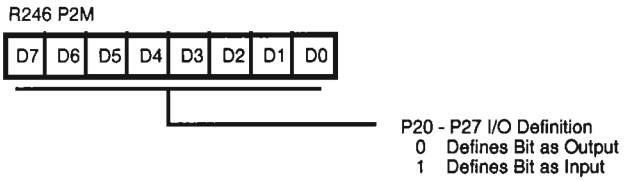


Figure 41. Port 2 Mode Register ($F6_H$: Write Only)

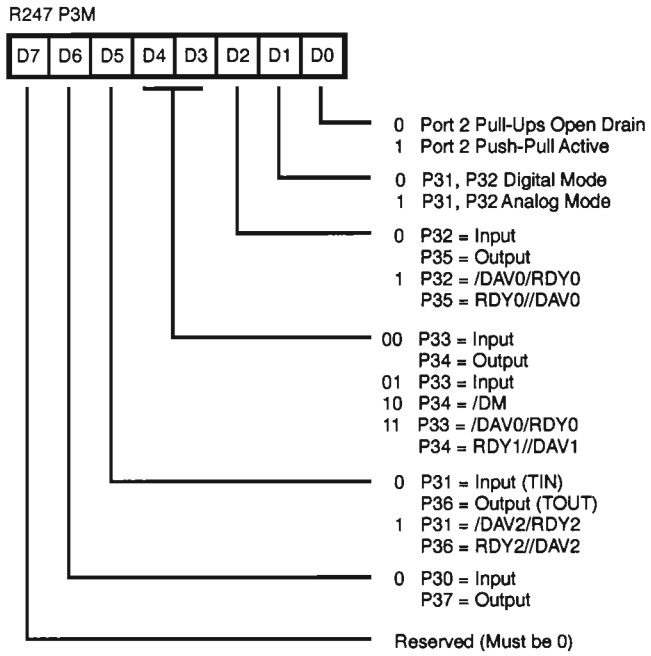


Figure 42. Port 3 Mode Register ($F7_H$: Write Only)

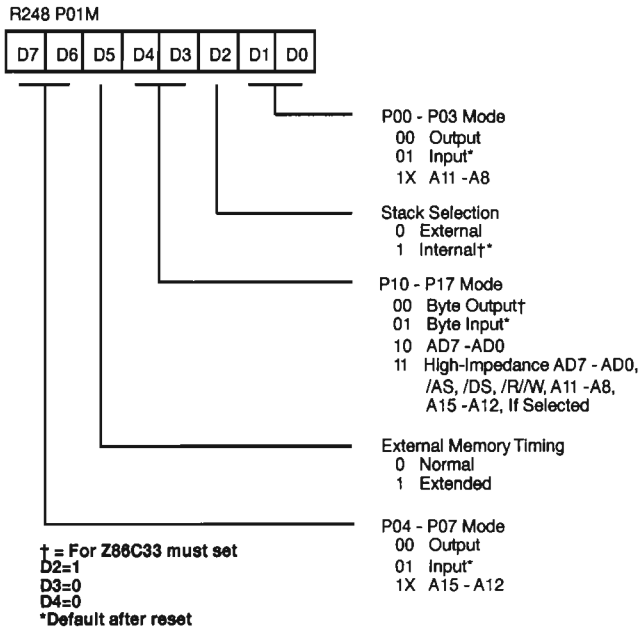


Figure 43. Port 0 and 1 Mode Register ($F8_H$: Write Only)

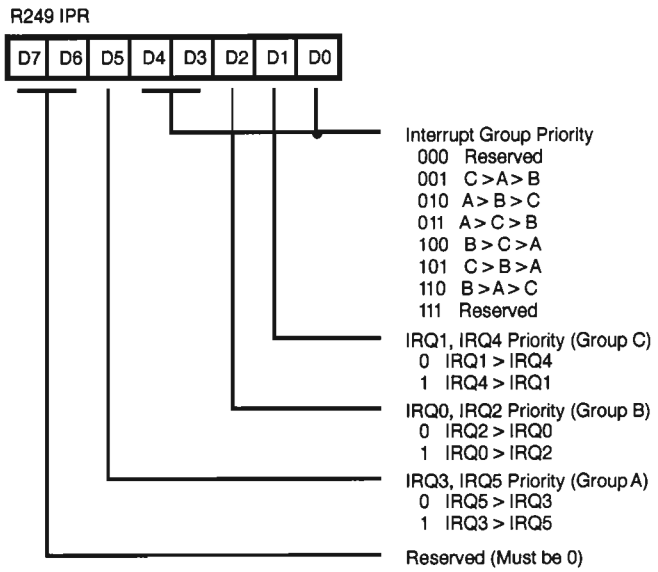


Figure 44. Interrupt Priority Register ($F9_H$: Write Only)

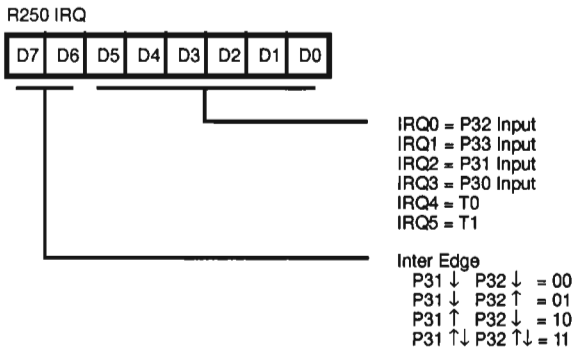


Figure 45. Interrupt Request Register (FA_H: Read/Write)

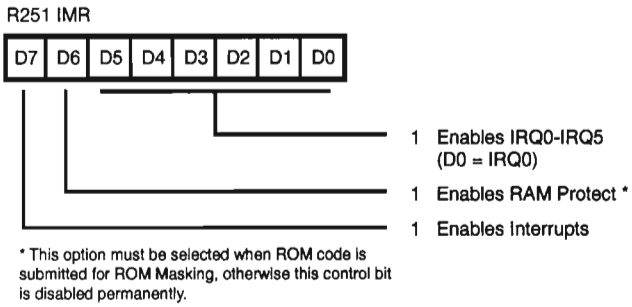


Figure 46. Interrupt Mask Register (FB_H: Read/Write)

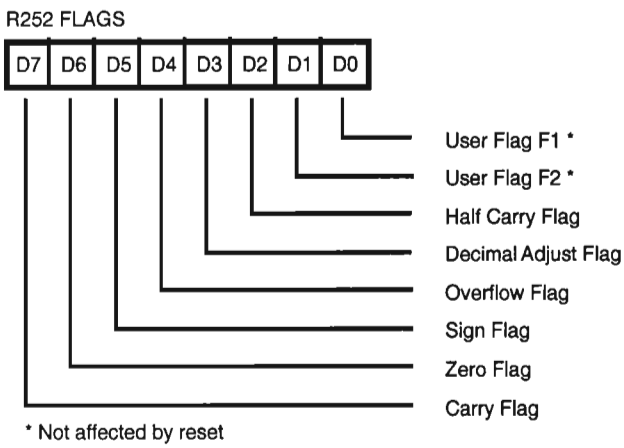


Figure 47. Flag Register (FC_H: Read/Write)

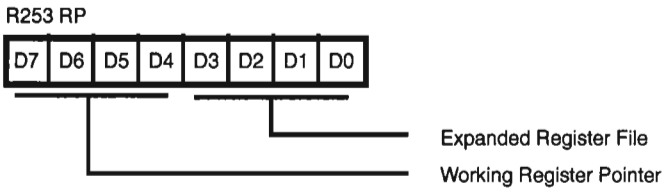


Figure 48. Register Pointer (FD_H: Read/Write)

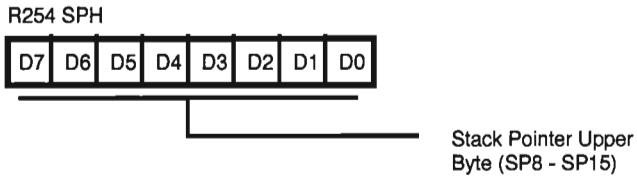


Figure 49. Stack Pointer High (FE_H: Read/Write)

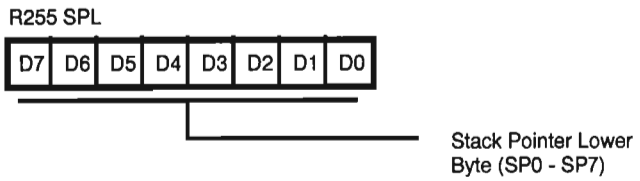
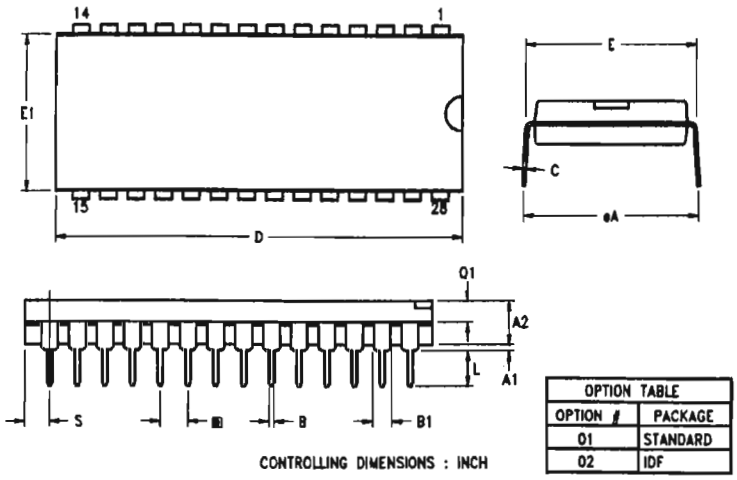


Figure 50. Stack Pointer Low (FF_H: Read/Write)

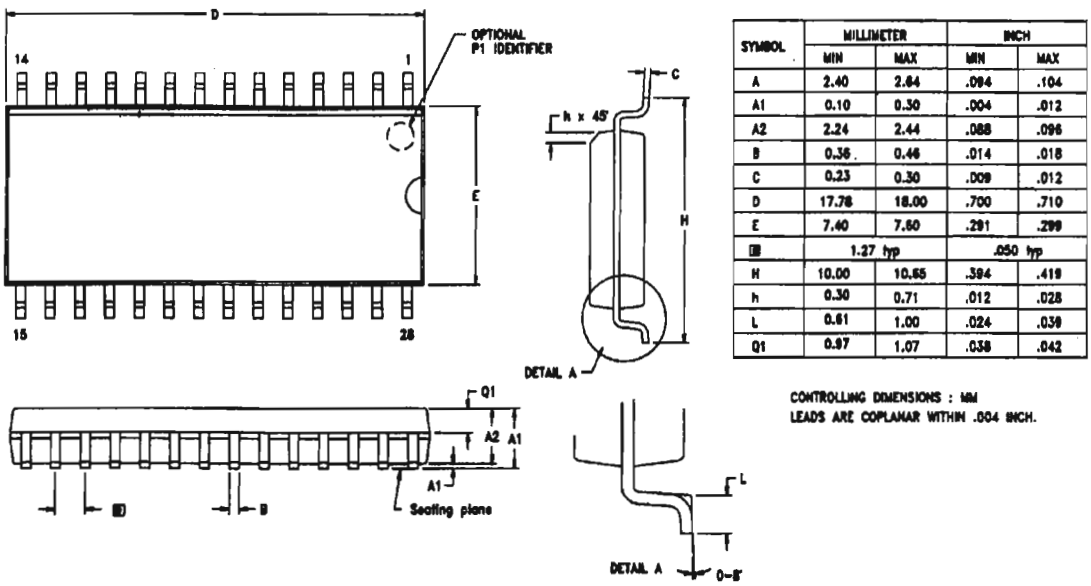
PACKAGE INFORMATION



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

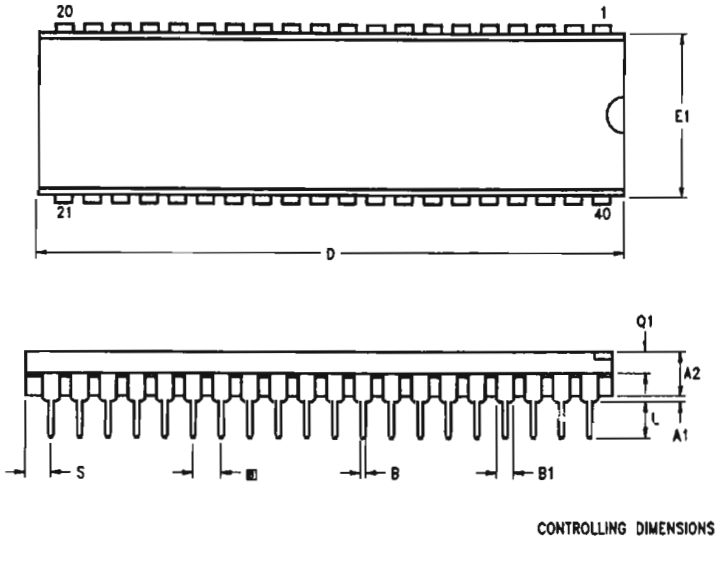
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 51. 28-Pin DIP Package Diagram



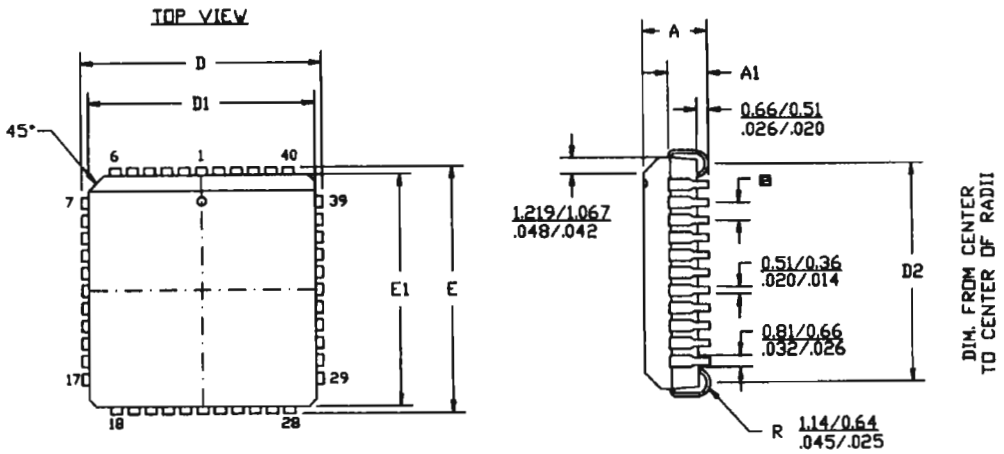
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

Figure 52. 28-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

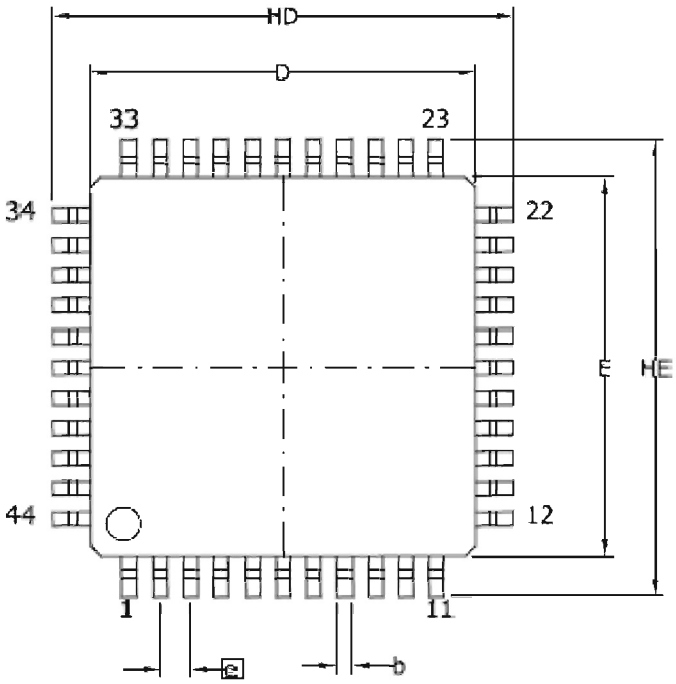
Figure 53. 40-Pin DIP Package Diagram

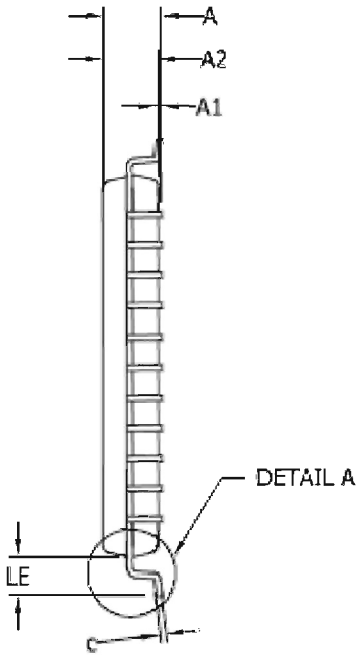


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

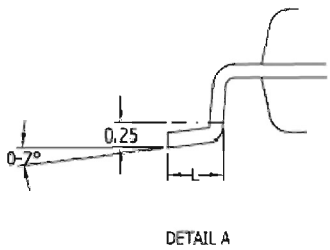
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 54. 44-Pin PLCC Package Diagram





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	



DETAIL A

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm / 0.004"

Figure 55. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z86C33

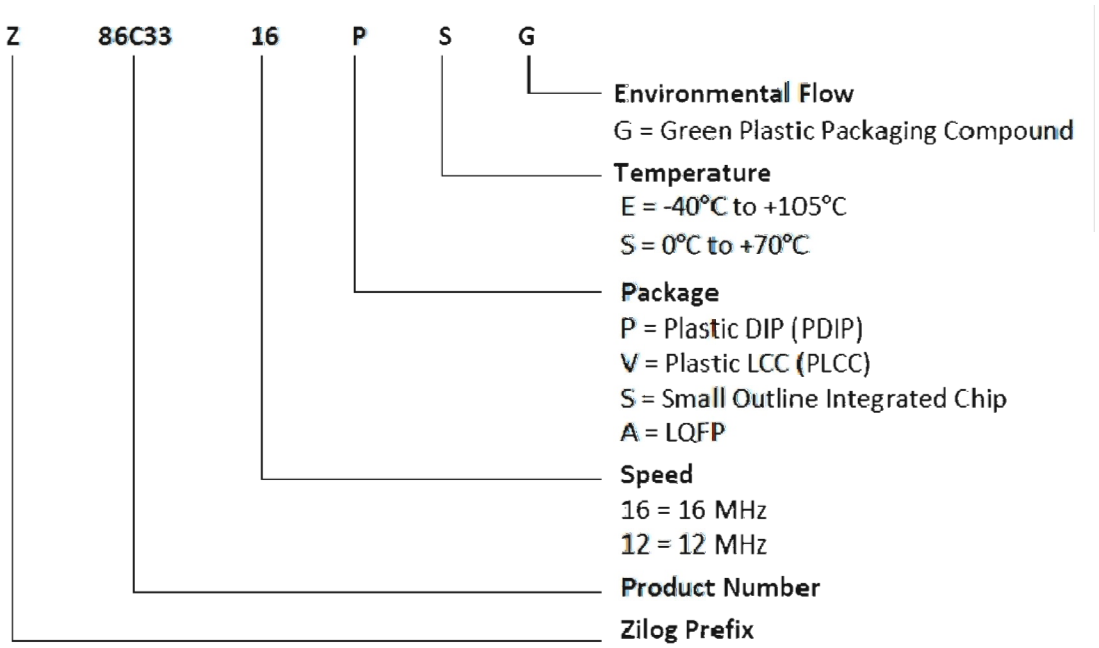
Standard Temperature		Extended Temperature	
28-Pin DIP	28-Pin SOIC	28-Pin DIP	28-Pin SOIC
Z86C3316PSG	Z86C3316SSG		
Z86C3312PSG	Z86C3312SSG	Z86C3312PEG	Z86C3312SEG

Z86C43

Standard Temperature		Extended Temperature
40-Pin DIP	44-Pin PLCC	44-Pin LQFP
Z86C4312PSG	Z86C4316VSG	Z86C4312AEG

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES



Precautions

1. When in ROM Protect Mode, and executing out of External Program Memory, instructions LDC, LDCI, LDE, and LDEI cannot read Internal Program Memory
2. When in ROM Protect Mode, and executing out of Internal Program Memory, instructions LDC, LDCI, LDE, and LDEI can read Internal Program Memory.
3. The device has an oscillator-free WDT reset for the device pins. When the device is reset from a WDT timeout, the reset will force the device pins to their reset default state even if the oscillator is not running.
4. The Port 3 outputs are reset to High State after Reset, except after Stop-Mode Recovery, at which time the outputs remain in the last state.
5. Extended timing is operable.
6. P0/P1/P2/P3 is Low-EMI software programmable.
7. P0/P1/P2 is software programmable for open-drain.
8. Expanded register PCON is Write-Only.
9. WDTMR is writeable only within the first 60 internal system clocks after Reset. Afterward, the WDTMR is write protected.
10. Device functions down to the V_{LV} threshold. At temperatures less than 25°C, the V_{LV} threshold will rise to a maximum V_{DD} of 3.6V.
11. Low-EMI is 25 percent of standard pull-down output driver, and 25 percent of standard pull-up output driver.
12. There is no clock filter on Reset pin.
13. Registers FE Hex (SPH) and FF Hex (SPL) are set to 00 Hex after any reset.
14. When Low EMI OSC is selected (PCON Reg Bit D7=0), the output drive of /DS, /AS, and R//W will also be in Low-EMI Mode.
15. P01M Reg Bit D4, D3 must be set to 00 Hex for Z86C33.
16. Must add a two NOP delay after selecting the P3M bit D1 to 1 before the comparitor output is valid. IRQ0, IRQ1, and IRQ2 should be cleared in IRQ register when the comparitor is enabled or disabled to avoid spurious noise creating a false interrupt.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Customer Support

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To learn more about this product, find additional documentation, or to discover other facets about Zilog product offerings, please visit the Zilog Knowledge Base at https://zilog.com/kb.

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