



THE DATASHEET OF TSM100IDT





TSM100

SINGLE OPERATIONAL AMPLIFIER AND SINGLE COMPARATOR

NOT FOR NEW DESIGN

OPERATIONAL AMPLIFIER

- LOW INPUT OFFSET VOLTAGE : 0.5mV typ.
- MEDIUM BANDWIDTH (unity gain) : 0.9MHz
- LARGE OUTPUT VOLTAGE SWING : 0V to $(V_{CC} - 1.5V)$
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- WIDE POWER SUPPLY RANGE : 5 to 30V ± 2.5 TO $\pm 15V$
- ESD PROTECTION : 2kV

COMPARATOR (OPEN COLLECTOR)

- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mV @ $I_o = 4mA$

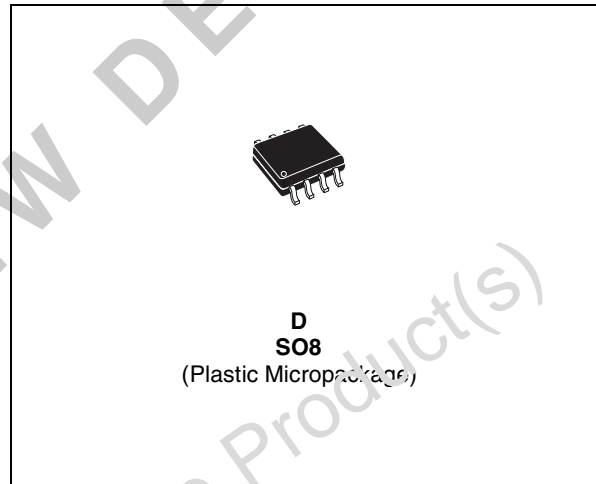
DESCRIPTION

The TSM100 is a monolithic IC that includes one independent op-amp and one independent comparator. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

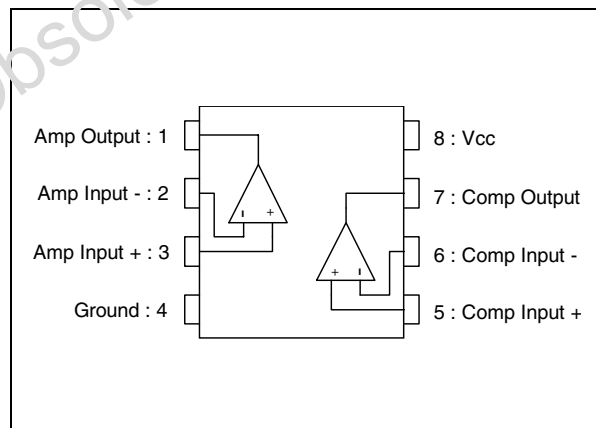
ORDER CODE

Part Number	Temperature Range	Package
		D
TSM100I	-40°C, +105°C	•

D = Small Outline Package (SO) - also available in Tape & Reel (DT)



PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	32	V
V_{id}	Differential Input Voltage	32	V
V_i	Input Voltage	-03. to +32	V
T_{oper}	Operating Free-air Temperature Range	-40 to +105	°C
T_j	Maximum Junction Temperature	150	°C
T_l	Maximum Lead Temperature (10 seconds maximum)	260	°C
R_{thja}	Thermal Resistance Junction to Ambient	175	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Total Supply Current Vcc+ = 5V, no load Vcc+ = 30V, no load		0.9	1.4 1.8	mA

OPERATIONAL AMPLIFIER
 $V_{CC}^+ = +5V$, $V_{CC} = \text{Ground}$, $V_o = 1.4V$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.5	3 4	mV
DV_{io}	Input Offset Voltage Drift		7		$\mu V/^\circ C$
I_{io}	Input Offset Current		2	30	nA
I_{ib}	Input Bias Current		20	150	nA
A_{vd}	Large Signal Voltage Gain $V_{CC} = 15V$, $R_L = 2k$, $V_o = 1.4V$ to $11.4V$	50	100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{CC} = 5V$ to $30V$	65	100		dB
V_{icm}	Input Common Mode Voltage Range $V_{CC} = +30V$ - see note ¹⁾	0		$(V_{CC}^+) - 1.5$	V
CMR	Common Mode Rejection Ratio	65	85		dB
I_{source}	Output Current Source $V_{CC} = +15V$, $V_o = 2V$, $V_{id} = +1V$	20	40		mA
I_o	Short Circuit to Ground $V_{CC} = +15V$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1V$, $V_{CC} = +15V$, $V_o = 2V$ $V_{CC} = +15V$, $V_o = 0.2V$	10 12	20 50		mA μA
V_{OH}	High Level Output Voltage $V_{CC}^+ = 30V$ $T_{amb} = 25^\circ C$, $R_L = 2k$ $T_{amb} = 25^\circ C$, $R_L = 10k$	26 27	27 28		V
V_{OL}	Low Level Output Voltage $R_L = 10k$		5	15	mV
SR	Slew Rate at Unity Gain $V_i = 0.5$ to $3V$, $V_{CC} = 15V$ $R_L = 2k$, $C_L = 100pF$, unity gain	0.2	0.4		$V/\mu s$
GBP	Gain Bandwidth Product $V_{CC} = 30V$, $R_L = 2k$, $C_L = 100pF$ $f = 100kHz$, $V_{in} = 10mV$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1kHz$ $A_v = 20dB$, $R_L = 2k$, $V_{CC} = 30V$ $C_L = 100pF$, $V_o = 2V_{pp}$		0.015		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_s = 100\Omega$ $V_{CC} = 30V$		40		nV/\sqrt{Hz}

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$. But both inputs can go to $V_{CC} + 0.3V$ without damage.

COMPARATOR

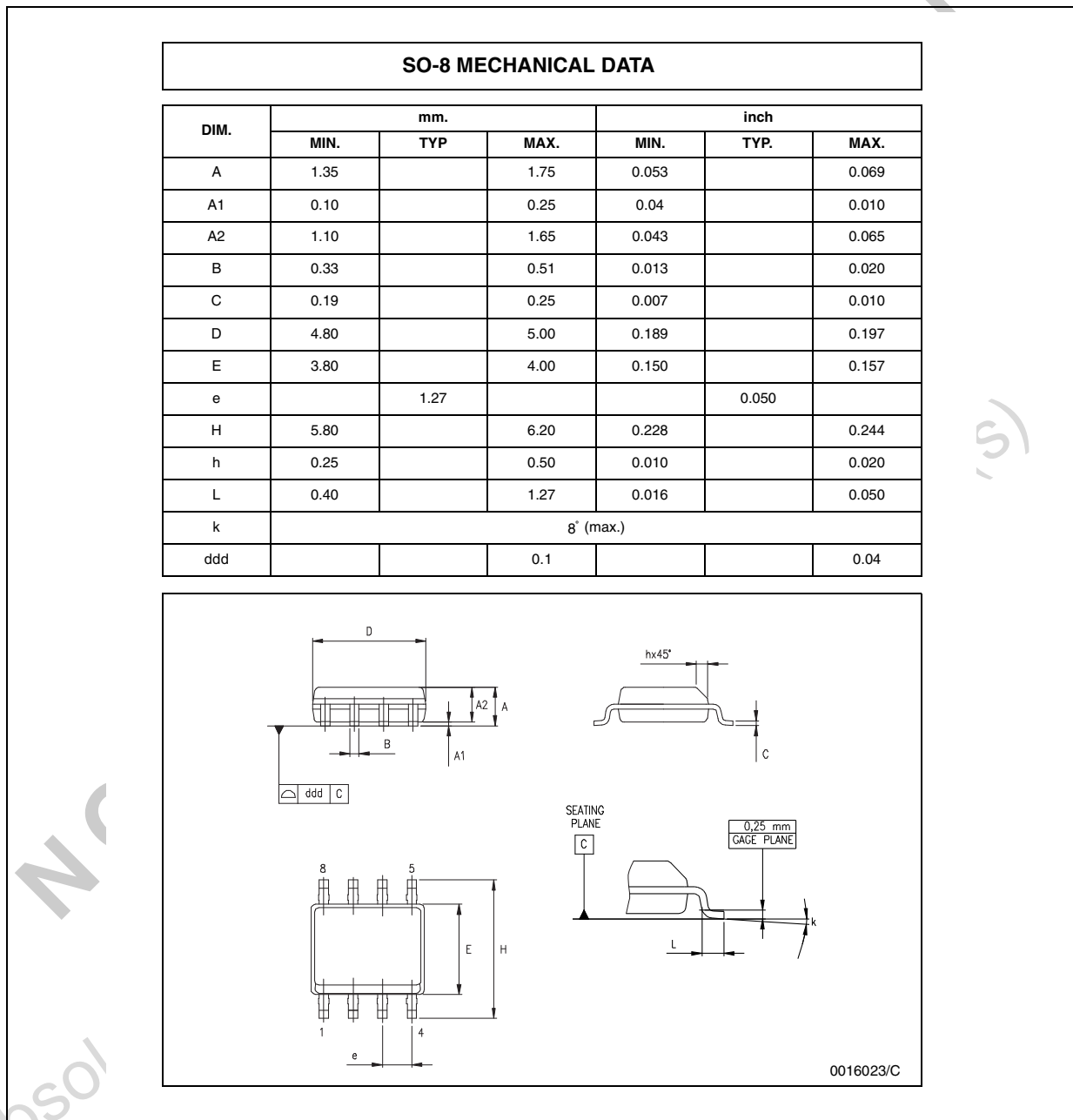
$V_{CC+} = +5V$, $V_{CC} = \text{Ground}$, $T_{amb} = 25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{amb} = 25^{\circ}\text{C}$		1	5	mV
I_{io}	Input Offset Current		5	50	nA
I_{ib}	Input Bias Current		25	250	nA
Avd	Large Signal Voltage Gain $V_{CC} = 15V$, $R_L = 15k$, $V_o = 1V$ to $11V$		200		V/mV
Vicm	Input Common Mode Voltage Range ¹⁾	0		$(V_{CC+}) - 1.5$	V
I_{sink}	Output Sink Current $V_{id} = -1V$, $V_o = 1.5V$	6	16		mA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{sink} = 4mA$		250	400	mV
I_{OH}	High Level Output Current $V_{id} = 1V$, $V_{CC} = V_o = 30V$		0.1		nA
t_{re}	Response Time $R_L = 5.1k$ to V_{CC+} ²⁾		1.3		μs
t_{rel}	Large Signal Response Time $V_i = \text{TTL}$, $V_{ref} = +1.4V$, $R_L = 5.1k$ to V_{CC+}		300		ns

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5V$. But either of both inputs can go to 36V without damage.

2. The response time is specified for a 100mV input step with 5mV overdrive. For larger overdrive signals, 300ns can be obtained

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



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