

TIBPAL20L8-10C, TIBPAL20R4-10C, TIBPAL20R6-10C, TIBPAL20R8-10C HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

SRPS008A – D3336, OCTOBER 1989 – REVISED MARCH 1992

- **High-Performance Operation:**
 f_{max} (no feedback)
 TIBPAL20R' . . . 71.4 MHz
 f_{max} (internal feedback)
 TIBPAL20R' . . . 58.8 MHz
 f_{max} (external feedback)
 TIBPAL20R' . . . 55.5 MHz
 Propagation Delay
 TIBPAL20' . . . 10 ns Max
- **Functionally Equivalent, but Faster Than Existing 24-Pin PLD Circuits**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

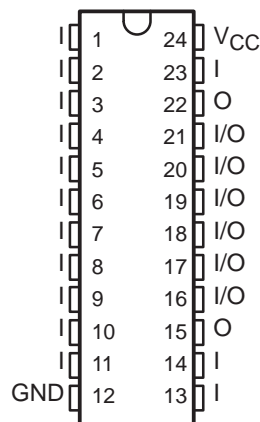
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These *IMPACT-X*™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

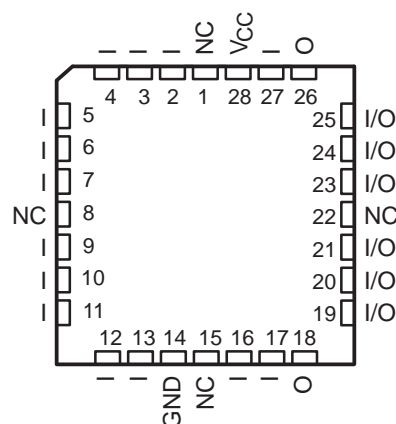
All of the register outputs are set to a low level during power up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C.

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC — No internal connection
Pin assignments in operating mode

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
 PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



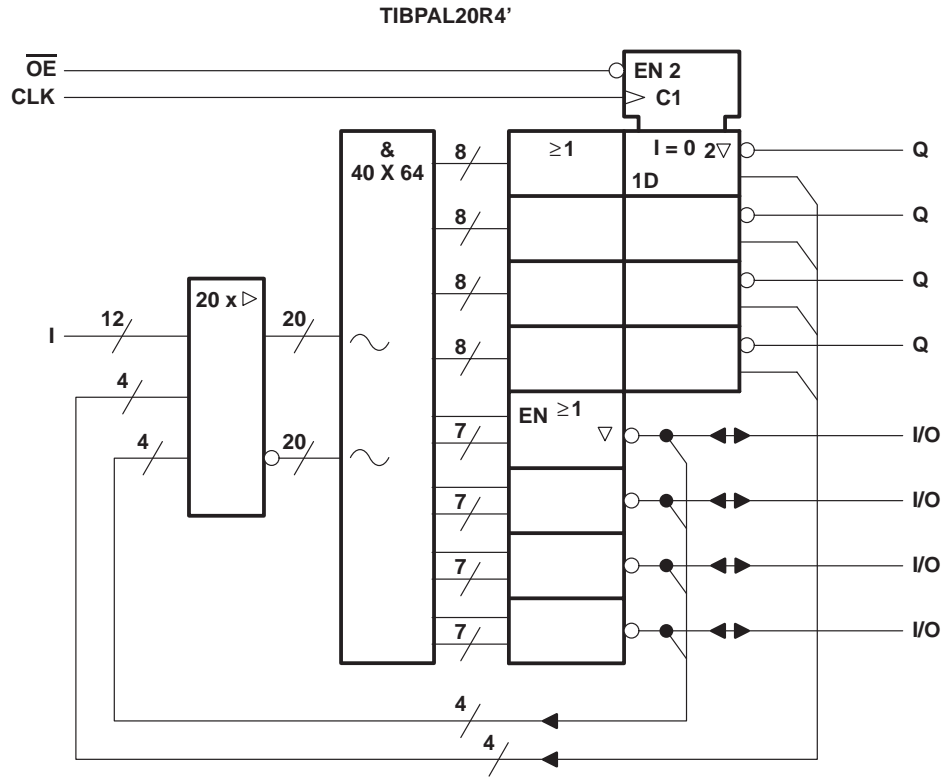
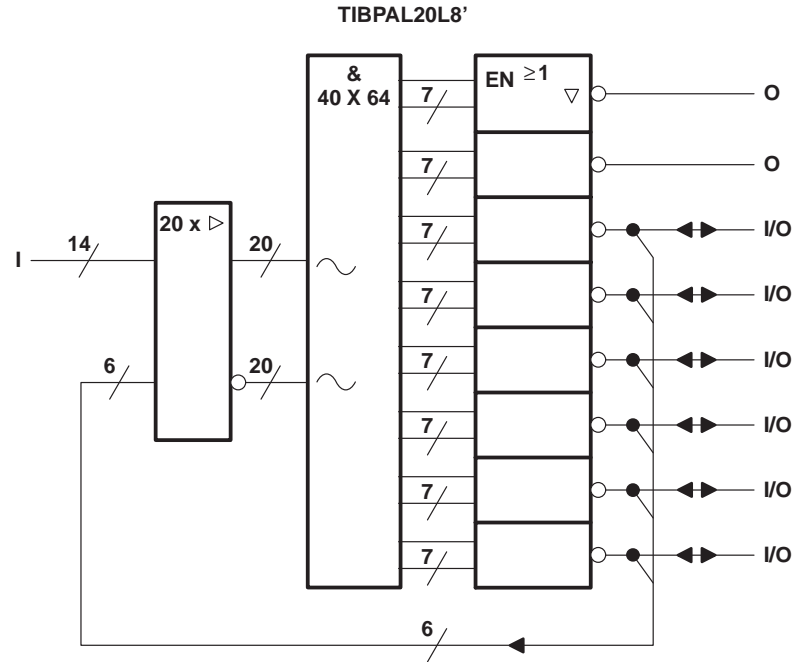
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SRPS008A – D3336, OCTOBER 1989 – REVISED MARCH 1992

functional block diagrams (positive logic)

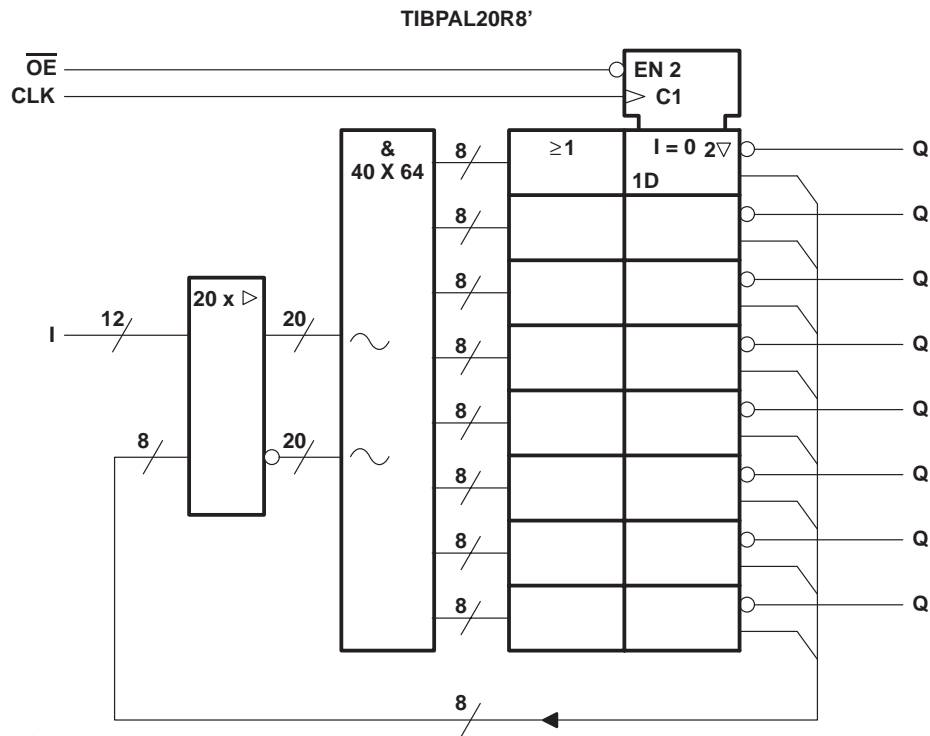
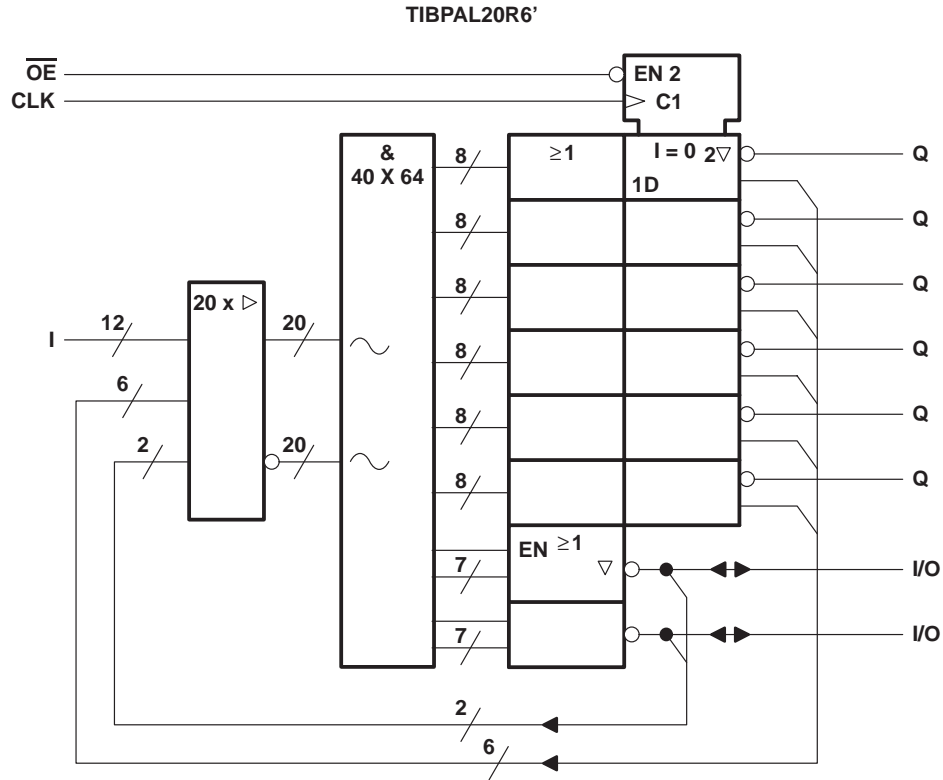


~ denotes fused inputs

TIBPAL20R6-10C, TIBPAL20R8-10C HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

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functional block diagrams (positive logic)

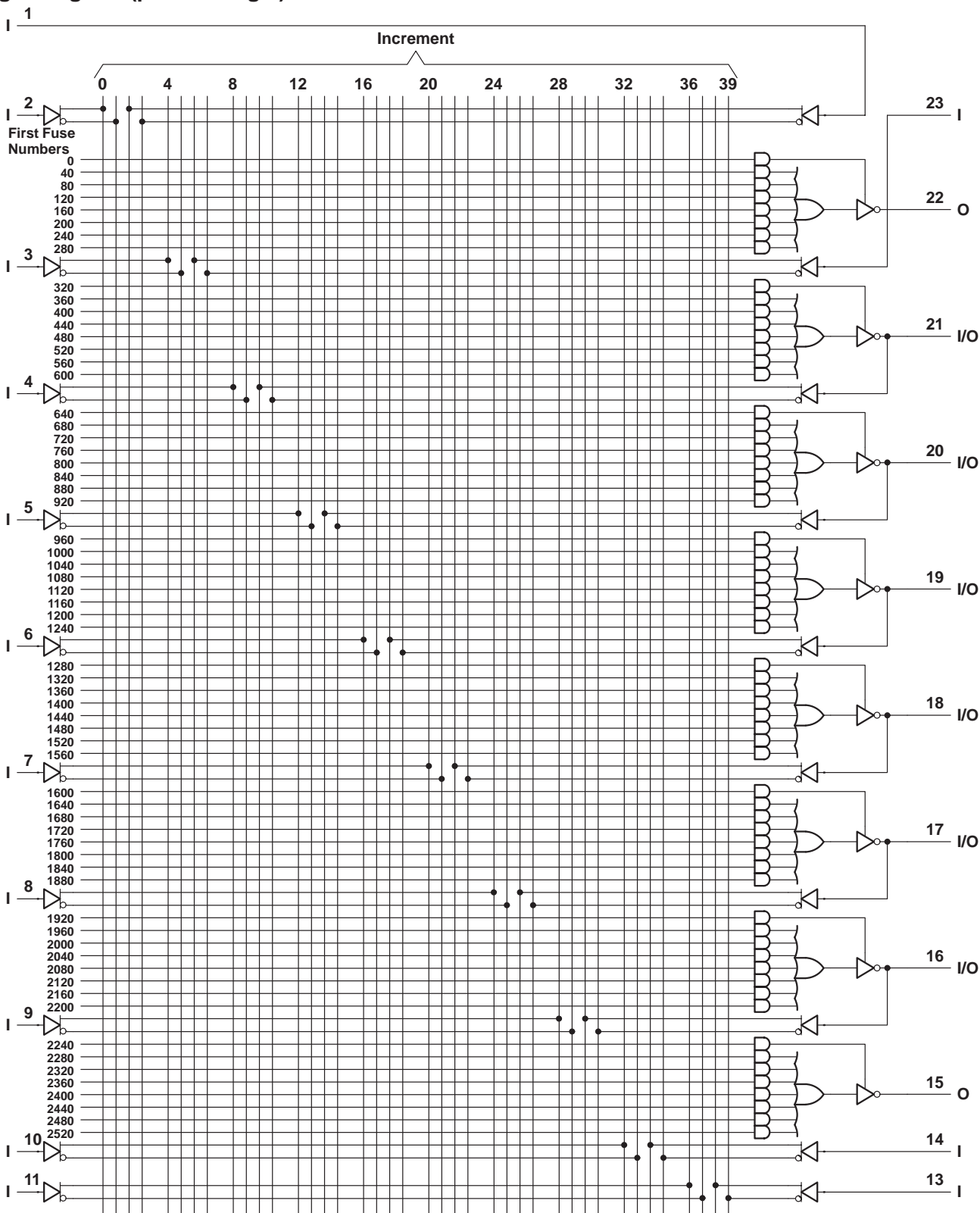


~ denotes fused inputs



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logic diagram (positive logic)

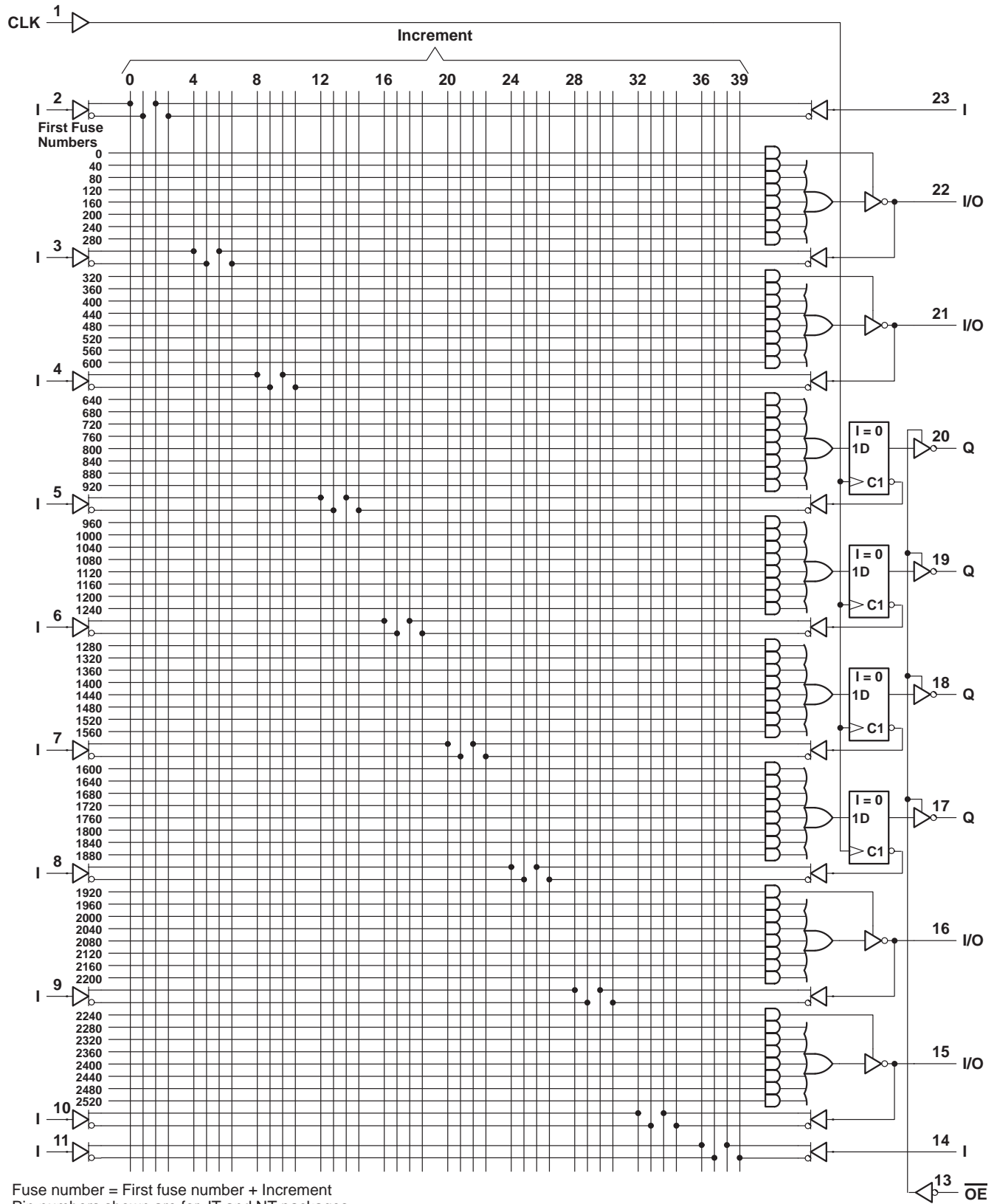


Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

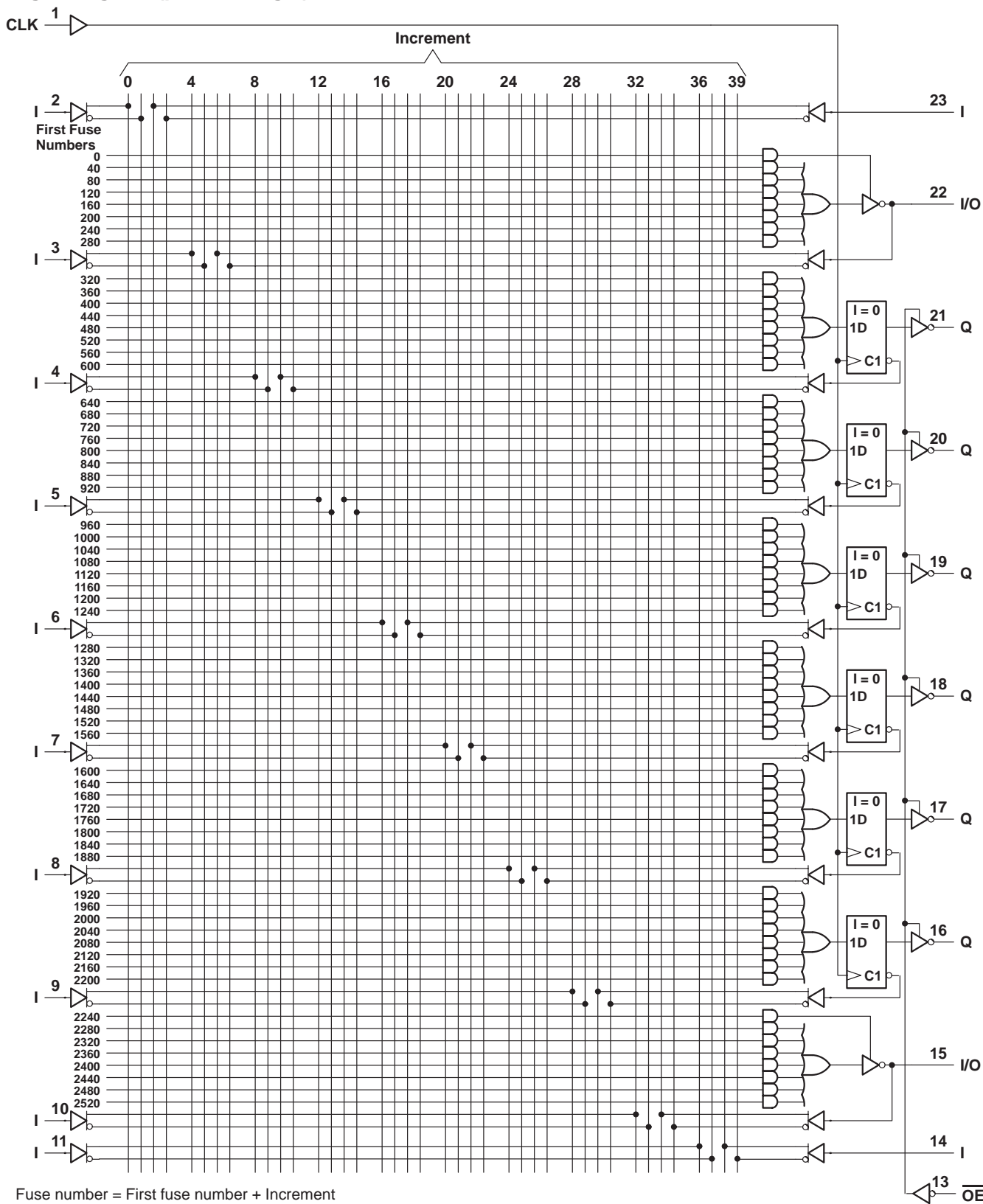
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logic diagram (positive logic)



logic diagram (positive logic)



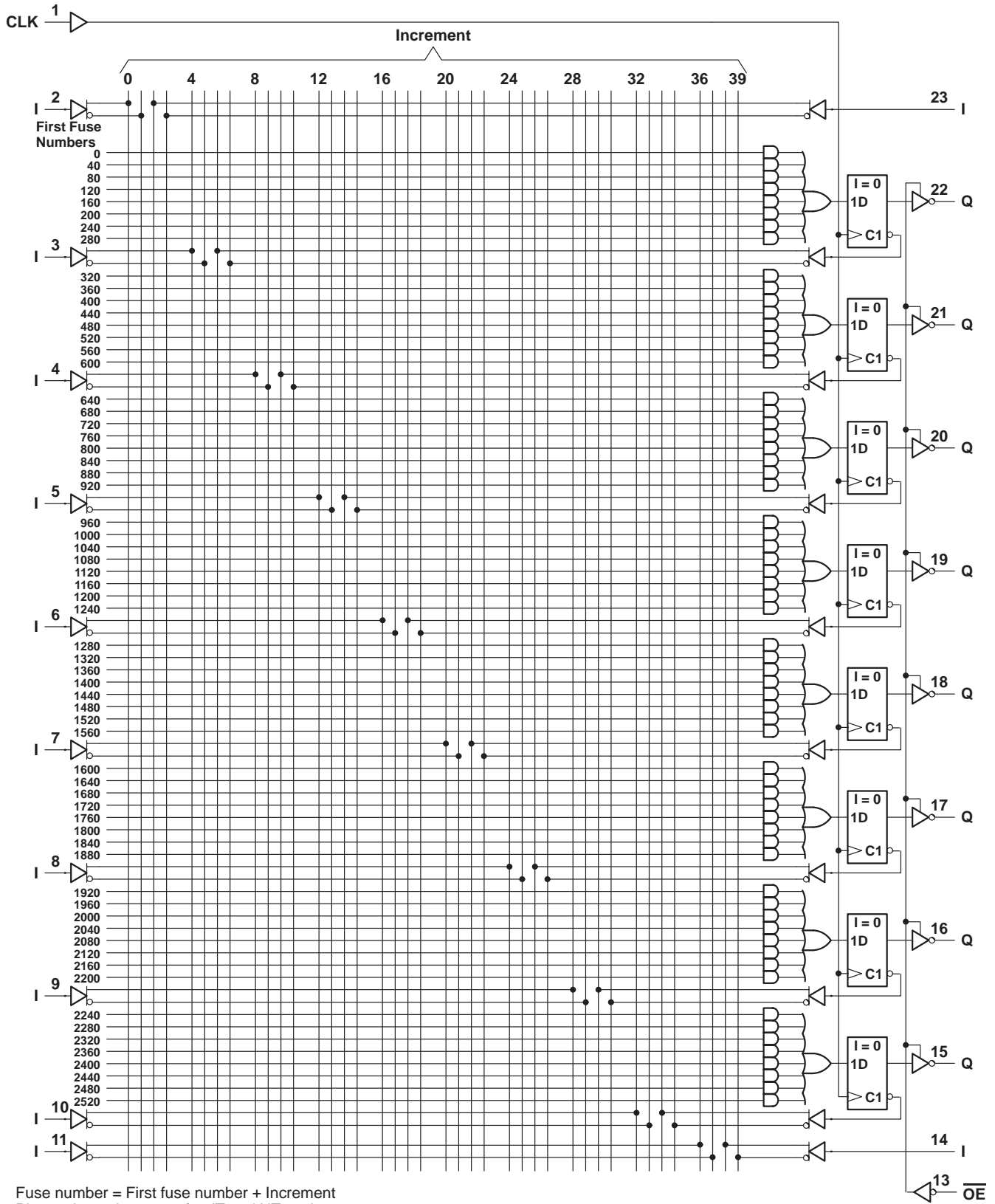
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.



TIBPAL20R8-10C HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

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logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}^{\dagger}	Clock frequency	0		71.4	MHz
t_w^{\dagger}	Pulse duration, clock (see Note 2)	High		7	ns
		Low		7	
t_{su}^{\dagger}	Setup time, input or feedback before clock \uparrow	10			ns
t_h^{\dagger}	Hold time, input or feedback after clock \uparrow	0			ns
T_A	Operating free-air temperature	0	25	75	°C

$^{\dagger} f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.



TIBPAL20L8-10C, TIBPAL20R4-10C, TIBPAL20R6-10C, TIBPAL20R8-10C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = -18 mA		-0.8	-1.5	V
V _{OH}		V _{CC} = 4.75 V,	I _{OH} = -3.2 mA	2.4			V
V _{OL}		V _{CC} = 4.75 V,	I _{OL} = 24 mA		0.3	0.5	V
I _{OZH} ‡	O, Q outputs	V _{CC} = 5.25 V,	V _O = 2.7 V			20	μA
	I/O ports					100	
I _{OZL} ‡	O, Q outputs	V _{CC} = 5.25 V,	V _O = 0.4 V			-20	μA
	I/O ports					-100	
I _I		V _{CC} = 5.25 V,	V _I = 5.5 V			0.2	mA
I _{IH} ‡		V _{CC} = 5.25 V,	V _I = 2.7 V			25	μA
I _{IL} ‡		V _{CC} = 5.25 V,	V _I = 0.4 V			-0.25	mA
I _{OS} §		V _{CC} = 5.25 V,	V _O = 0.5 V	-30	-70	-130	mA
I _{CC}		V _{CC} = 5.25 V, Outputs open,	V _I = 0, OE = V _{IH}			210	mA
C _i		f = 1 MHz,	V _I = 2 V		7		pF
C _o		f = 1 MHz,	V _O = 2 V		8		pF
C _{clk}		f = 1 MHz,	V _{CLK} = 2 V		12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT	
f _{max} ¶	without feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 6	71.4			MHz	
	with internal feedback (counter configuration)			58.8				
	with external feedback			55.5				
t _{pd}	I, I/O	O, I/O			3	8	10	
t _{pd}	CLK↑	Q			2	5	8	ns
t _{pd} #	CLK↑	Feedback input					7	ns
t _{en}	OE↓	Q			2	6	10	ns
t _{dis}	OE↑	Q			2	6	10	ns
t _{en}	I, I/O	O, I/O			3	8	10	ns
t _{dis}	I, I/O	O, I/O			2	8	10	ns
t _{sk(o)}	Skew between registered outputs				0.5		ns	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See section for f_{max} specifications. f_{max} does not apply for TIBPAL20L8'.

This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

|| This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.



programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL} , raise Pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 13 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

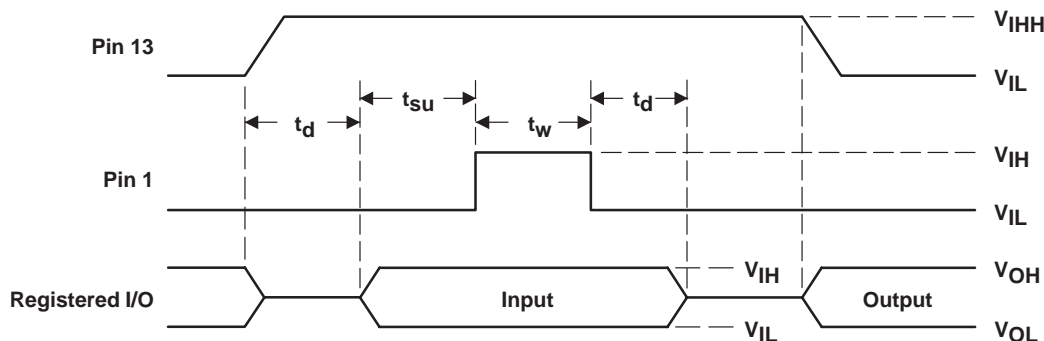
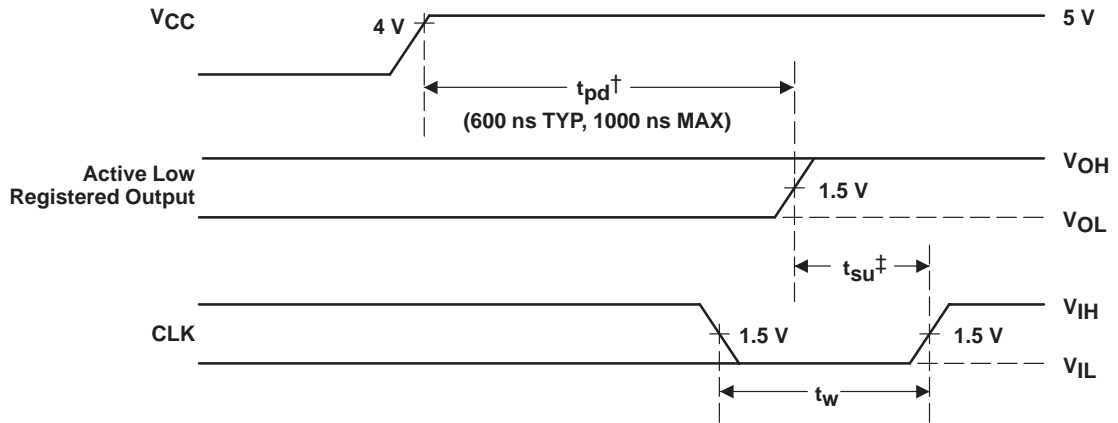


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 v

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
 ‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time (t_{su} + t_h). However, the minimum f_{max} is determined by the minimum clock period (t_w high + t_w low).

$$\text{Thus, } f_{\text{max}} \text{ without feedback} = \frac{1}{(t_{\text{w high}} + t_{\text{w low}})} \text{ or } \frac{1}{(t_{\text{su}} + t_{\text{h}})}$$

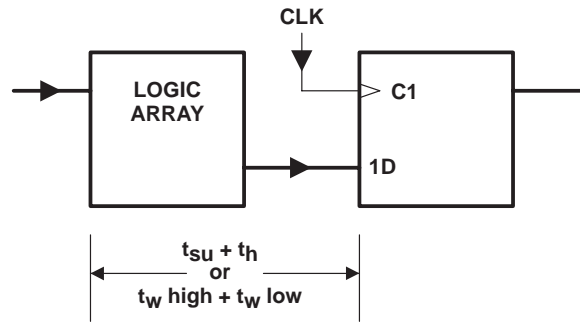


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, } f_{\text{max}} \text{ with internal feedback} = \frac{1}{(t_{\text{su}} + t_{\text{pd CLK-to-FB}})}$$

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

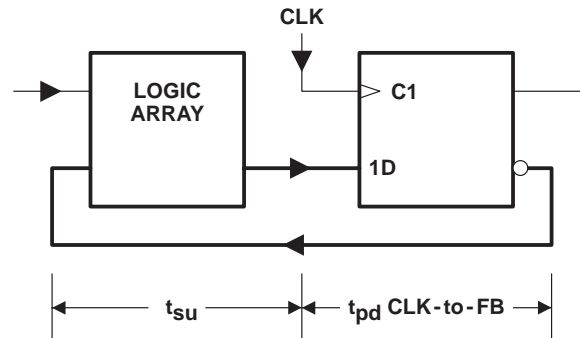


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_{su} + t_{pd} \text{ CLK-to-Q}$).

$$\text{Thus, } f_{\text{max}} \text{ with external feedback} = \frac{1}{(t_{\text{su}} + t_{\text{pd}} \text{ CLK-to-Q})}$$

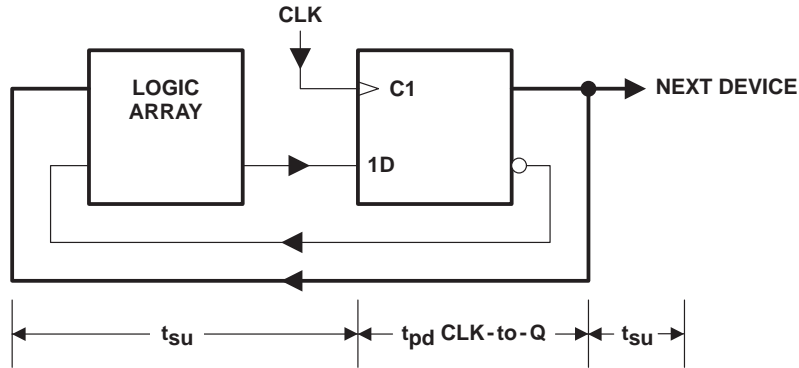
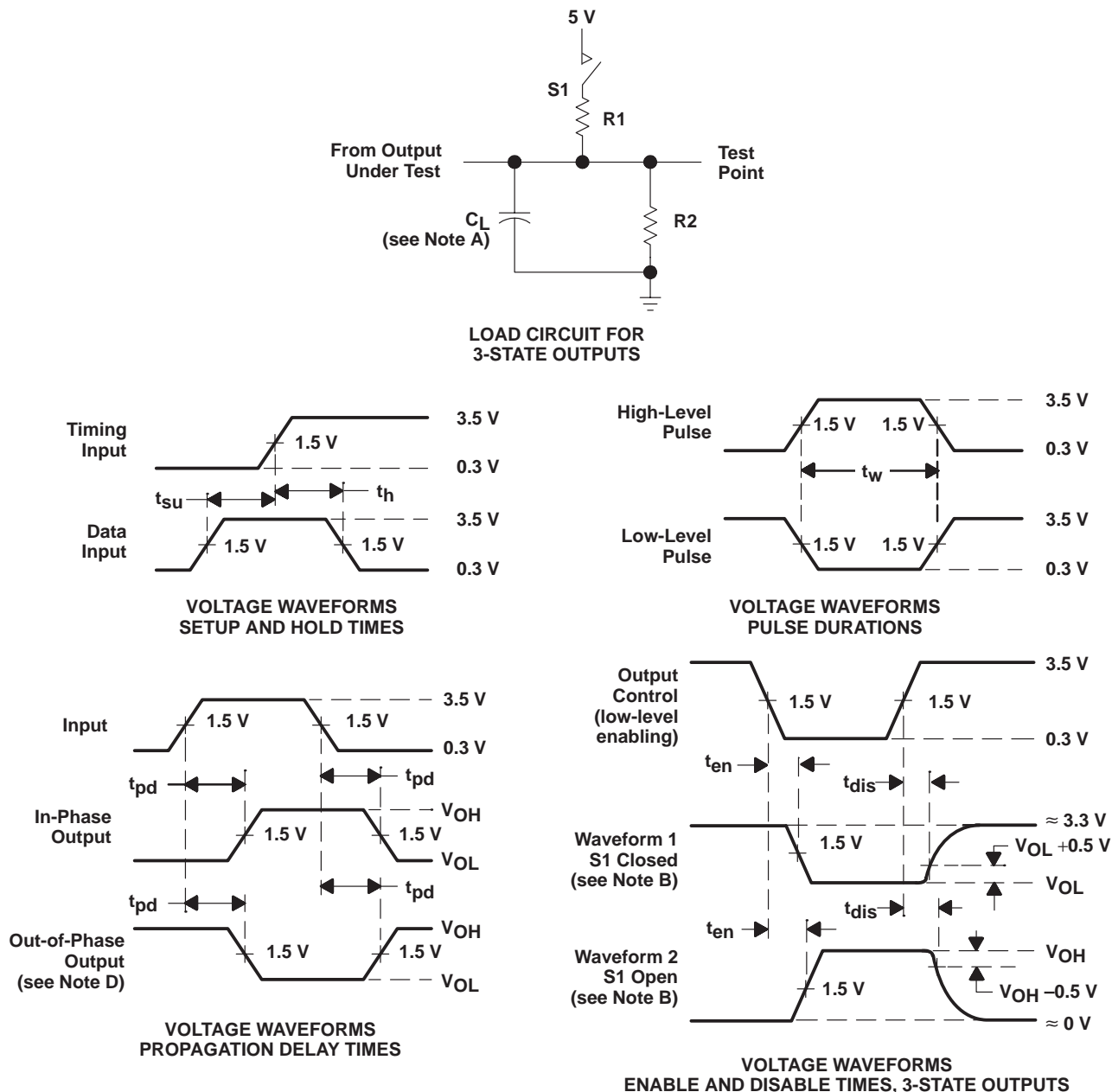


Figure 5. f_{max} With External Feedback

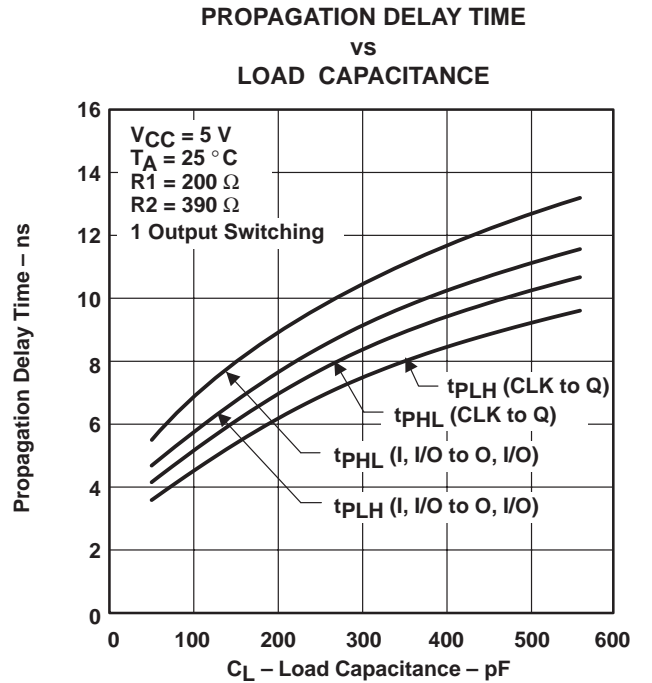
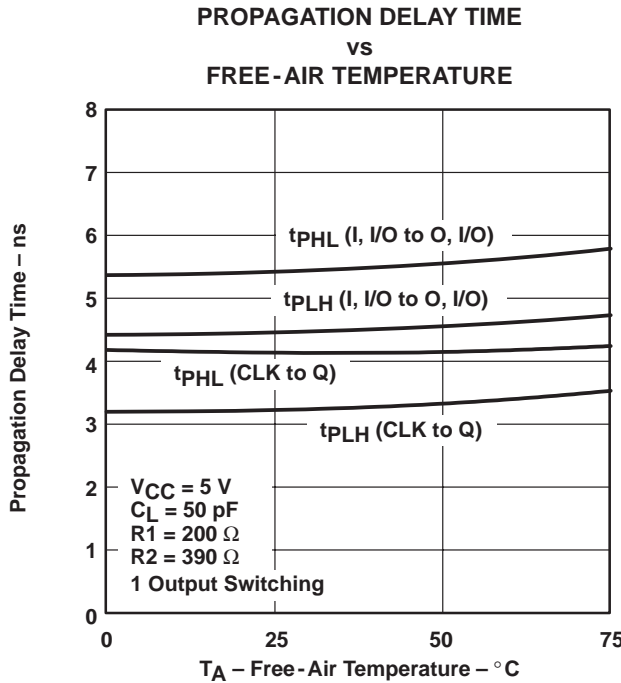
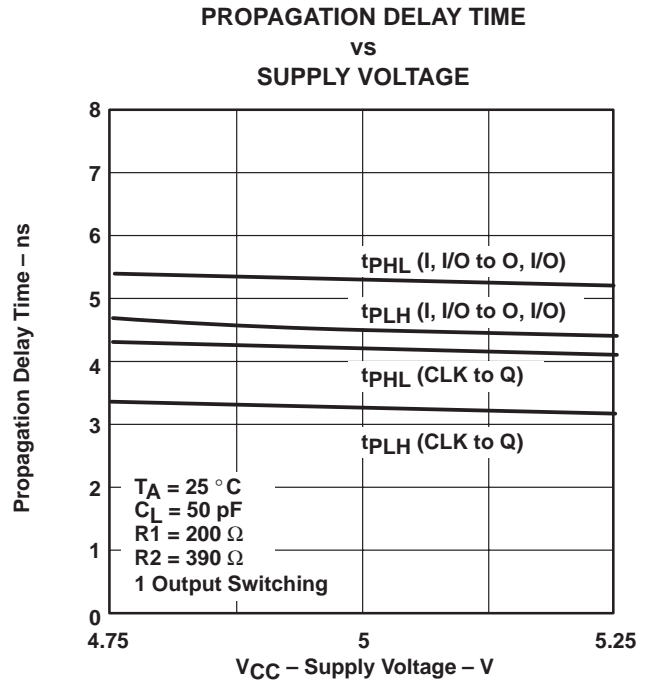
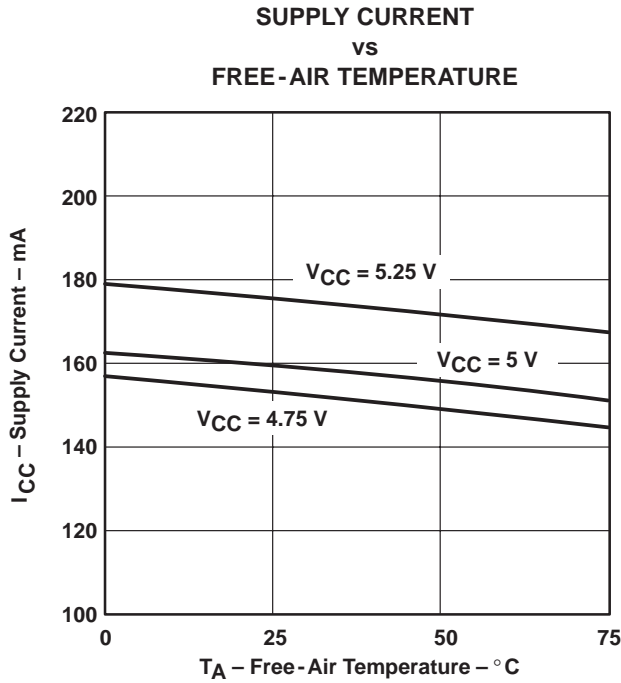
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

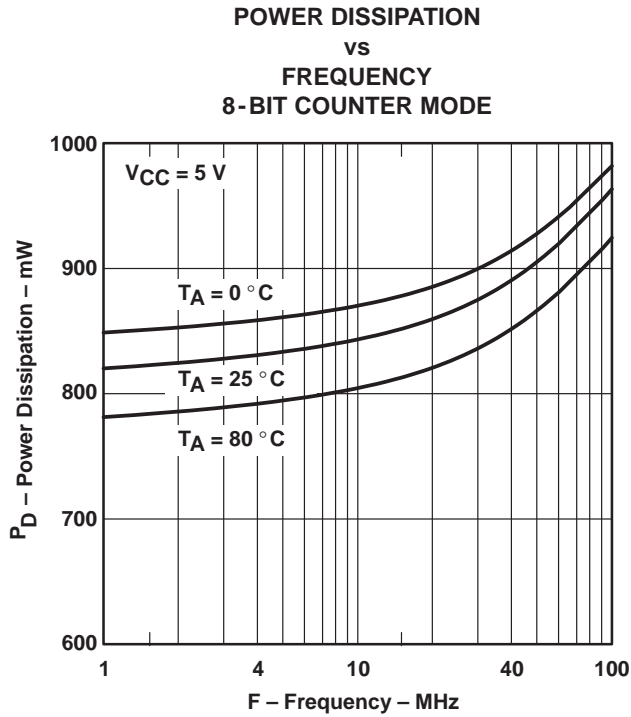


Figure 11

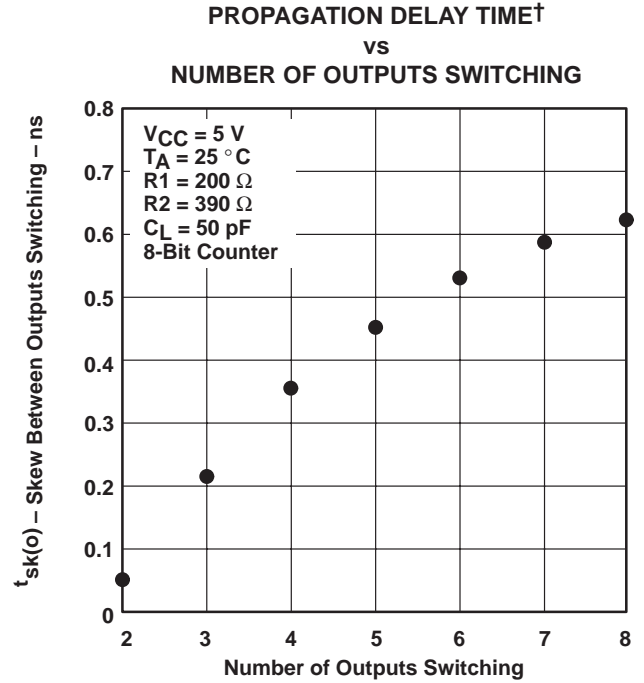


Figure 12

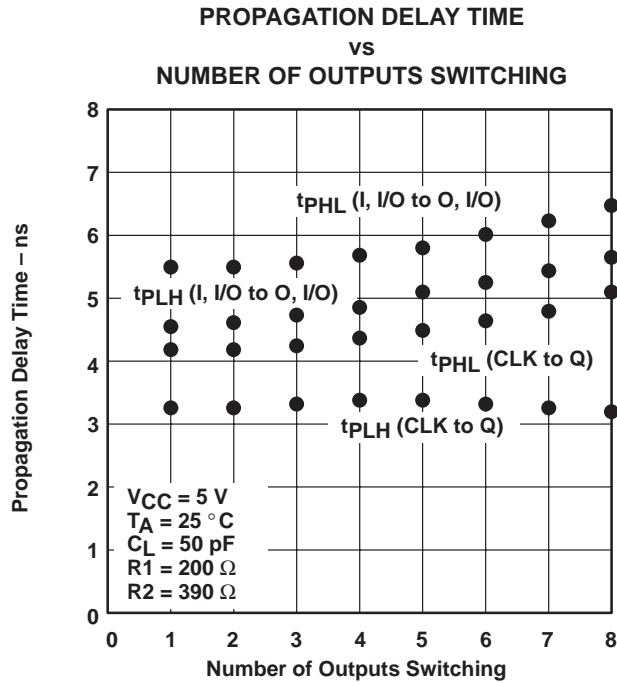


Figure 13

†Outputs switching in the same direction (tPLH compared to tPLH/tPHL to tPHL)

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D0892

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TIBPAL20L8-10CFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIBPAL20L8-10CNT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
TIBPAL20R4-10CFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIBPAL20R4-10CNT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
TIBPAL20R6-10CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL20R6-10CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TIBPAL20R8-10CFN	ACTIVE	PLCC	FN	28	37	TBD	CU SNPB	Level-1-220C-UNLIM
TIBPAL20R8-10CNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

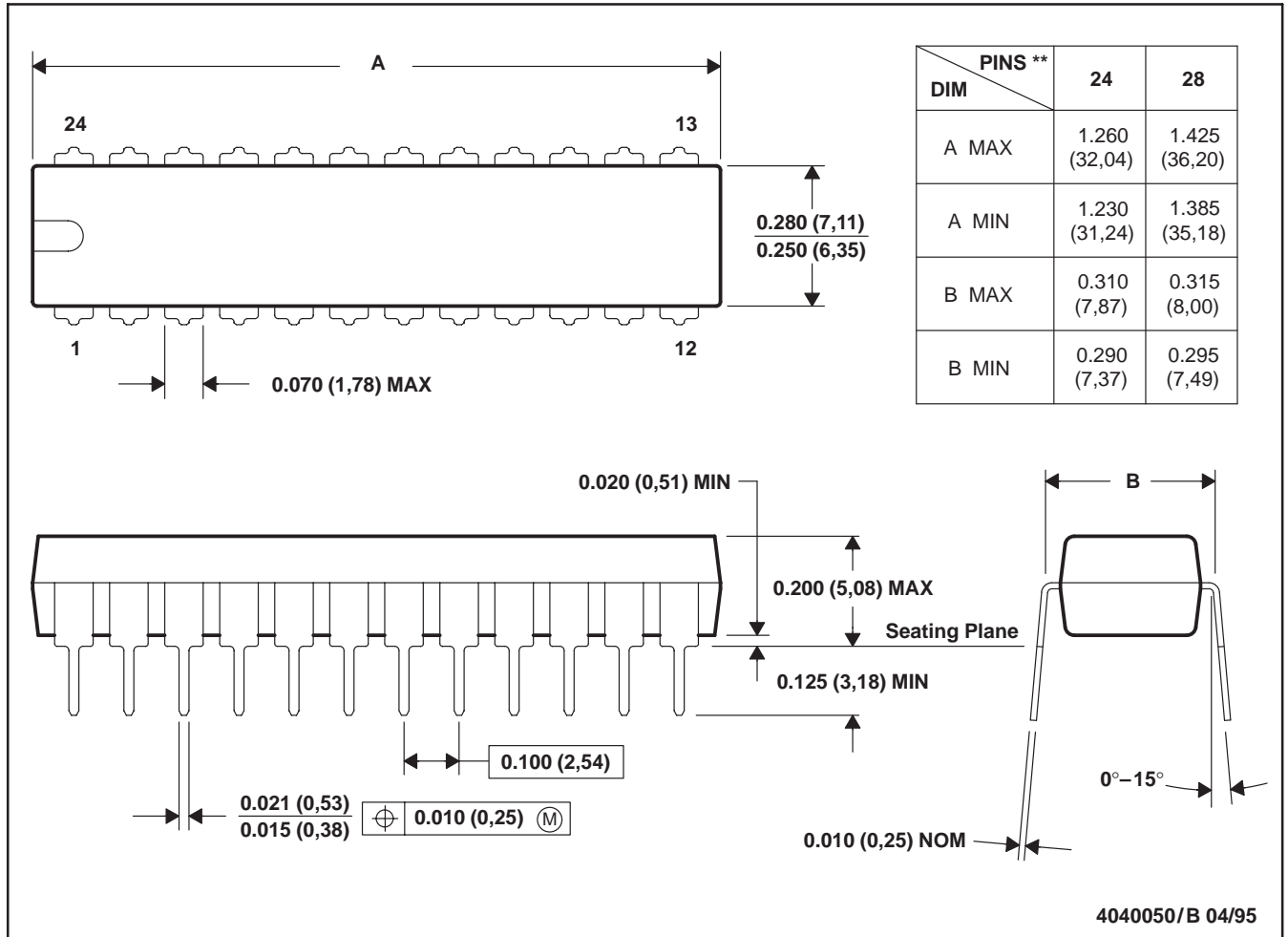
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NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

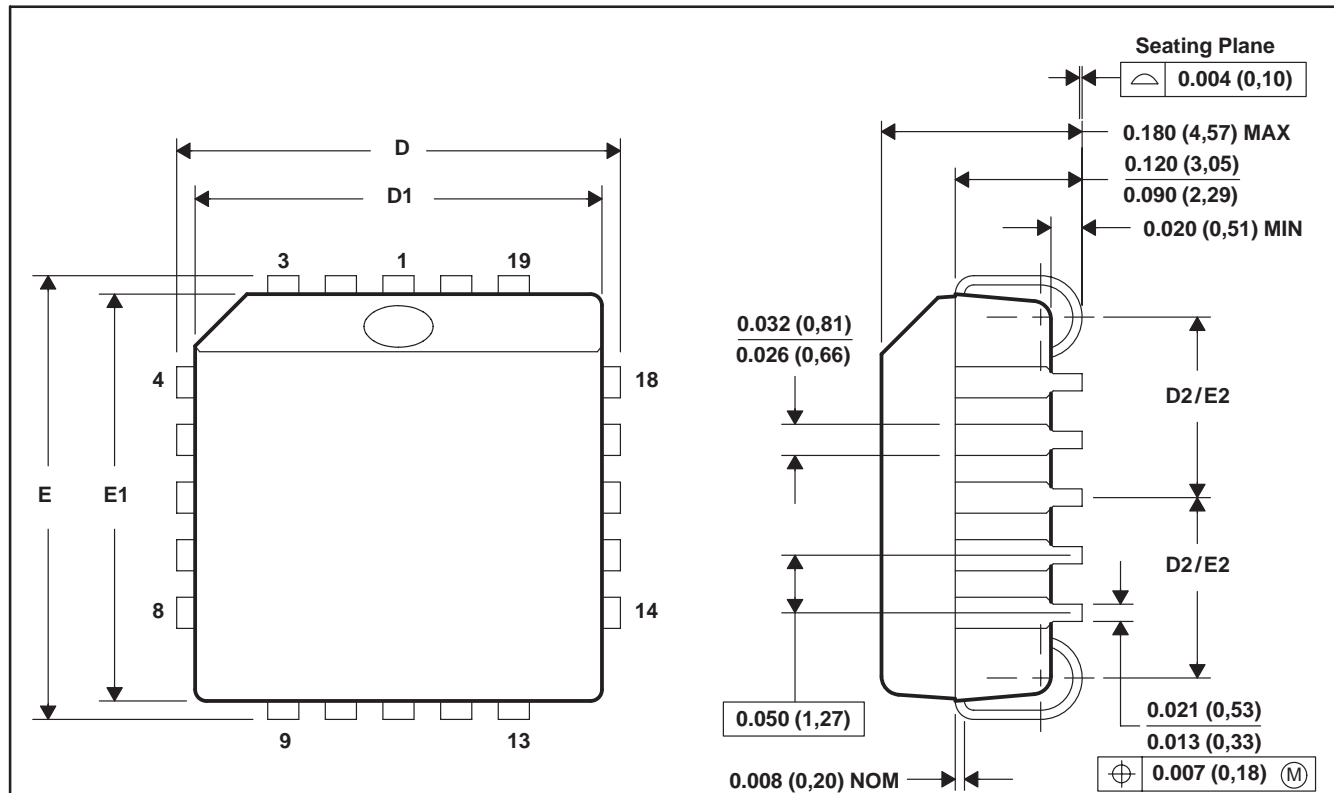


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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