WINSOURCE ELECTRONICS

THE DATASHEET OF

SIP32475DN-T1-GE4

47 mΩ, 1.2 V to 5.5 V, Low Quiescent Current Load Switch in Ultra Thin μDFN-4

DESCRIPTION

The SiP32475 is a compact, ultra thin high side load switch that operates over a input voltage range from 1.2 V to 5.5 V. Designed with a p-channel MOSFET featuring an adaptive charge pump gate drive, the SiP32475 provides 47 mΩ switch on-resistance over a wide input voltage range and maintains a low quiescent current level.

The SiP32475 also features slew rate control, reverse blocking when the switch is off, and output discharge. With guaranteed 1 V control logic high, the SiP32475 can interface directly with a low voltage control I/O, without the need for an extra level shift or driver. The device is logic high enabled and a 2.8 MΩ pulldown resistor is integrated at the logic control EN pin. The slow slew rate of the SiP32475 limits the in-rush current and minimizes the switching noise.

The SiP32475 is available in the μDFN-4L 1 mm x 1 mm package with a 0.3 mm thickness. The device is specified for operation over a temperature range of -40 °C to +85 °C.

FEATURES

- 1.2 V to 5.5 V input voltage range
- 47 mΩ typical on-resistance
- 3 μA quiescent current
- 2 A maximum continuous switch current
- Slew rate controlled turn on: 160 μs
- Guaranteed 1 V logic high over the input voltage range
- Reverse current blocking when the switch is off or V_{IN} is ground
- Integrated output discharge switch
- ESD performance per JESD 22: 4 kV HBM
- Compact μDFN-4L package with 0.3 mm thickness
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- PDAs / smart phones
- Notebook / netbook computers
- Tablet PCs
- Portable media players
- Digital cameras
- GPS navigation devices
- Data storage devices
- Medical and healthcare devices

TYPICAL APPLICATION CIRCUIT

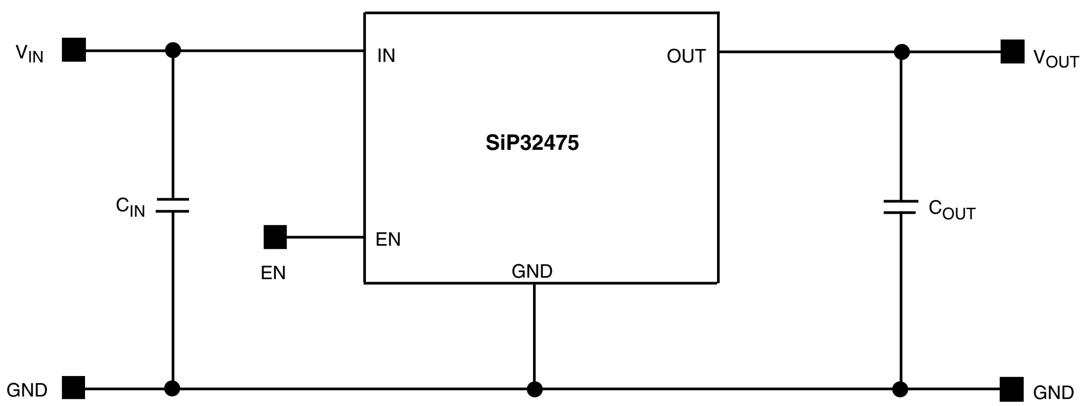


Fig. 1 - Typical Application Circuit

ORDERING INFORMATION					
PART NUMBER	PACKAGE	t_{on} (μs)	$R_{DISCHARGE}$	MARK CODE	TEMPERATURE RANGE
SiP32475DN-T1-GE4	μDFN-4L 1 mm x 1 mm	300	Yes	D	-40 °C to +85 °C

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
Supply input voltage V_{IN}	Reference to GND	-0.3 to 6.5	V
Output voltage V_{OUT}	Reference to GND	-0.3 to 6.5	
Output voltage V_{OUT}	Pulse at 1 ms reference to GND [a]	-1.6	
Enable input voltage EN	Reference to GND	-0.3 to 6.5	
Maximum continuous switch current		2	A
Maximum pulse switch current	Pulse at 1 ms, 10 % duty cycle	2.5	
ESD rating (HBM)		4000	V
Thermal resistance, junction-to-ambient [b]		150	°C/W
Maximum power dissipation [b]	T_A = 25 °C	650	mW
Temperature			
Operating temperature		-40 to +85	°C
Operating junction temperature		125	
Storage temperature		-65 to +150	

Notes

a. Negative current injection up to 300 mA

b. Measured on 2 oz double side layer 1" x 1" board

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
Input voltage (V_{IN})	1.2	-	5.5	V
Output voltage (V_{OUT})	0	-	5.5	

SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V_{IN} = 1.2 V to 5.5 V, T_A = -40 °C to +85 °C (typical values are at 25 °C)	**LIMITS**			**UNIT**
			MIN.	**TYP.**	**MAX.**	
Power Supply						
Quiescent current	I_Q	V_{IN} = 3.3 V, I_{OUT} = 0 mA	-	4.7	7	μA
Shutdown current	I_{SD}	OUT = GND	-	0.001	2	
Off switch current	$I_{DS(off)}$	EN = GND, OUT = GND	-	0.001	2	
Reverse blocking current	$I_{(in)RB}$	Out = 5 V, IN = 1.2 V, EN = 0 V, (measured at IN pin)	-	0.01	1	
		Out = 5 V, IN = 0 V, EN = 0 V, (measured at IN pin)	-	0.12	1	
Switch Resistance						
On resistance	$R_{DS(on)}$	I_{OUT} = 500 mA, V_{IN} = 1.2 V, T_A = 25 °C	-	92	120	mΩ
		I_{OUT} = 500 mA, V_{IN} = 1.5 V, T_A = 25 °C	-	74	90	
		I_{OUT} = 500 mA, V_{IN} = 1.8 V, T_A = 25 °C	-	64	80	
		I_{OUT} = 500 mA, V_{IN} = 3 V, T_A = 25 °C	-	49	60	
		I_{OUT} = 500 mA, V_{IN} = 5 V, T_A = 25 °C	-	47	60	
Discharge switch on resistance	R_{PD}	When V_{IN} = 3 V at 25 °C	-	77	-	Ω
		When V_{IN} = 1.8 V at 25 °C	-	< 200	-	
EN pin pull down resistor	R_{EN}	EN = 1.2 V	1	2.6	6	MΩ
On resistance temperature coefficient	TC_{RDS}		-	2800	-	ppm/°C
On/off Logic						
EN input low voltage	V_{IL}	V_{IN} = 1.5 V	0.4	-	-	V
EN input high voltage	V_{IH}	V_{IN} = 5.5 V	-	-	1	
Switching Speed						
Switch turn-on delay time	t_{on_DLY}	R_{LOAD} = 500 Ω, C_L = 0.1 μF, V_{IN} = 5 V	-	138	-	μs
Switch turn-on rise time	t_r	R_{LOAD} = 500 Ω, C_L = 0.1 μF, V_{IN} = 5 V	-	162	-	
Switch turn-off delay time	t_{off_DLY}	R_{LOAD} = 500 Ω, C_L = 0.1 μF, (50 % V_{IN} to 90 % V_{OUT})	-	3	-	

PIN CONFIGURATION

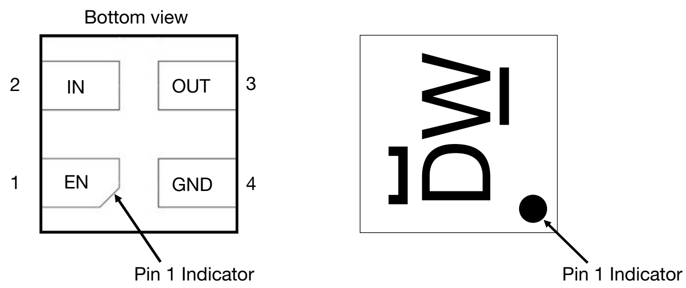


Fig. 2 - µDFN-4L 1 mm x 1 mm

DEVICE MARKING

Line 1 : plant code
Line 2 : D = device part number
W = assembly week
Line 3 : pin 1 dot + fab code

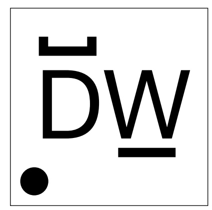


Fig. 3 - µDFN-4L 1 mm x 1 mm

PIN DESCRIPTION		
PIN#	**NAME**	**FUNCTION**
3	OUT	Switch output
2	IN	Switch input
4	GND	Ground connection
1	EN	Switch on/off control. A pull down resistor is integrated

TRUTH TABLE	
EN	**SWITCH**
1	On
0	Off

BLOCK DIAGRAM

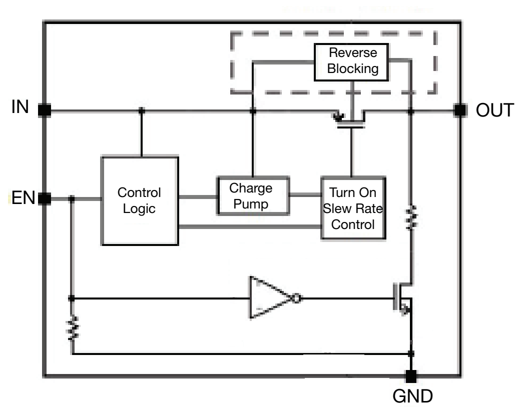


Fig. 4 - Functional Block Diagram

TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)

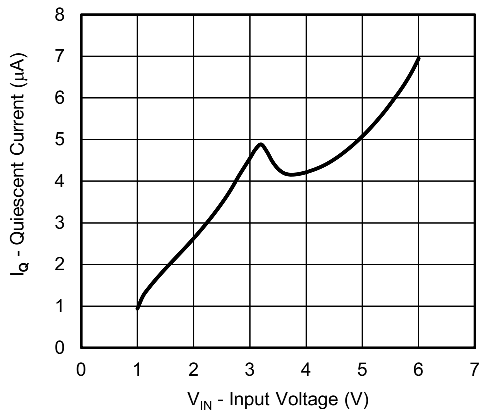


Fig. 5 - Quiescent Current vs. Input Voltage

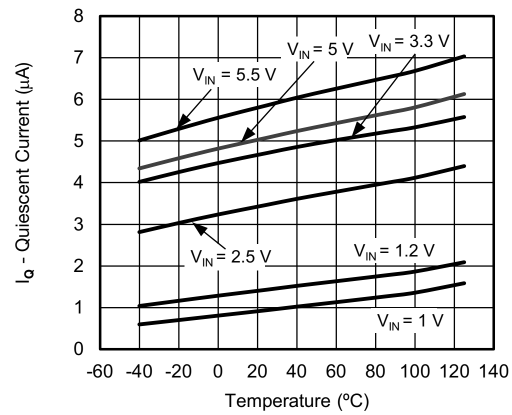


Fig. 8 - Quiescent Current vs. Temperature

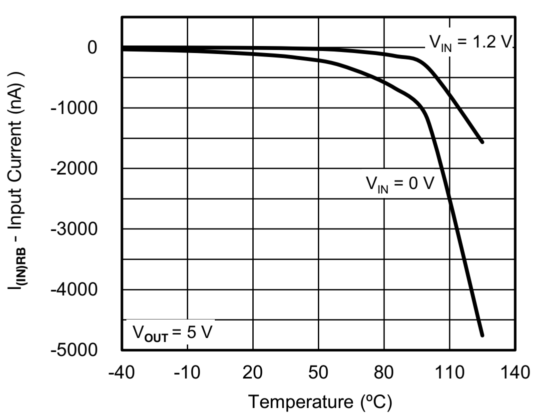


Fig. 6 - Reverse Blocking Current vs. Temperature

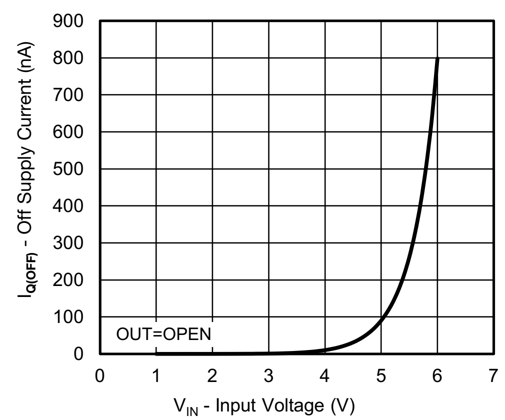


Fig. 9 - Off Supply Current vs. Input Voltage

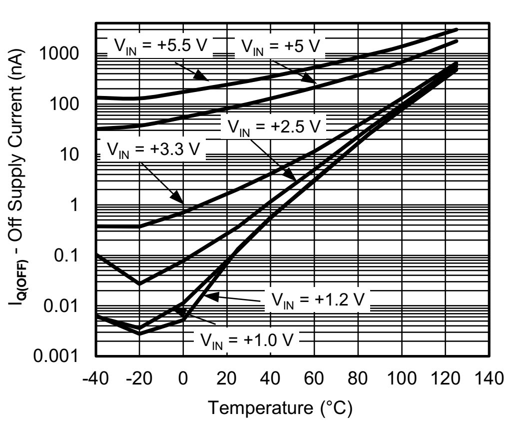


Fig. 7 - Off Supply Current vs. Temperature

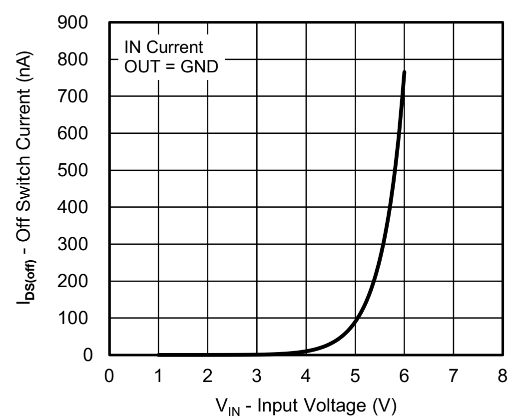


Fig. 10 - Off Switch Current vs. Input Voltage

TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)

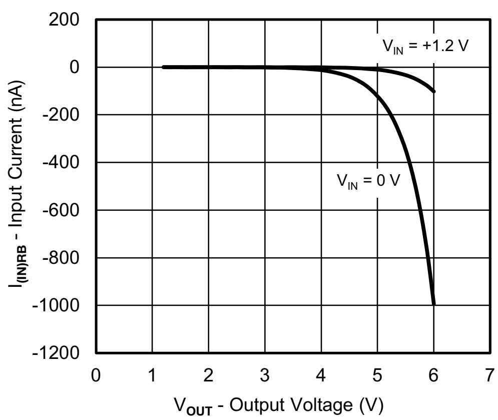


Fig. 11 - Reverse Blocking Current vs. Output Voltage

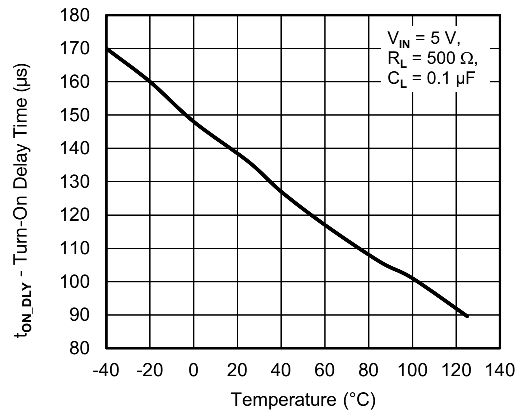


Fig. 14 - Turn-on Delay Time vs. Temperature

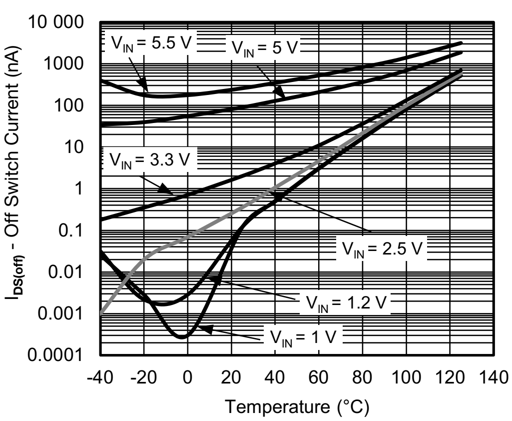


Fig. 12 - Off Switch Current vs. Temperature

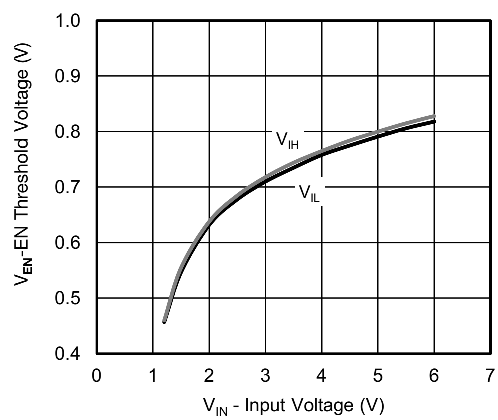


Fig. 15 - EN Threshold Voltage vs. Input Voltage

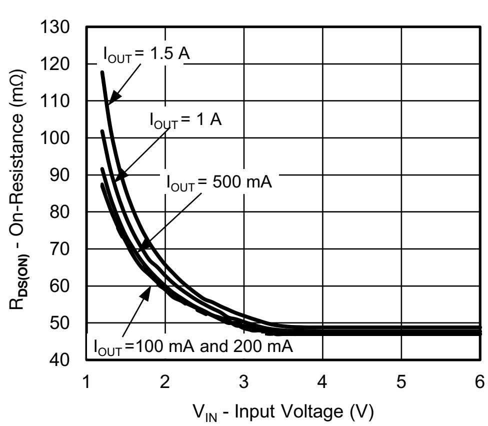


Fig. 13 - $R_{DS(on)}$ vs. Input Voltage

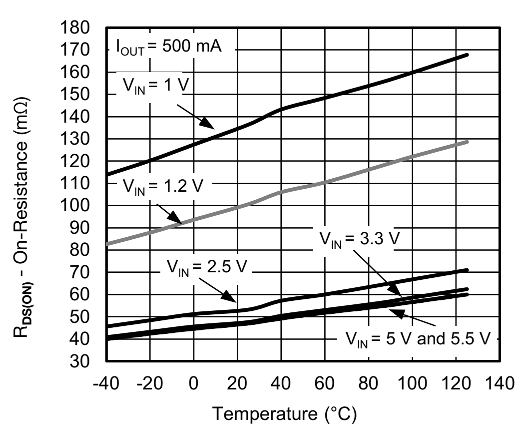


Fig. 16 - $R_{DS(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)

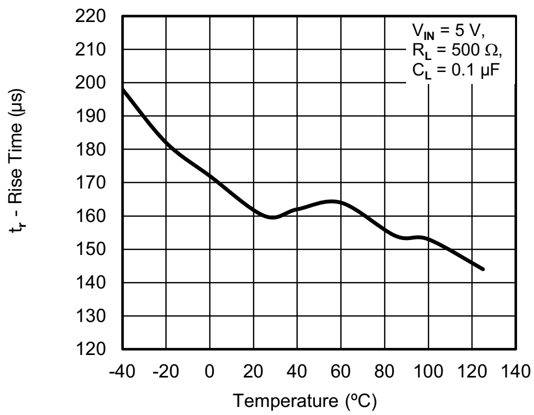


Fig. 17 - Rise Time vs. Temperature

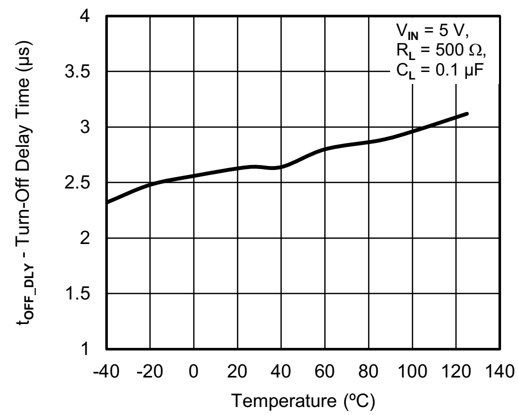


Fig. 18 - Turn-off Delay Time vs. Temperature

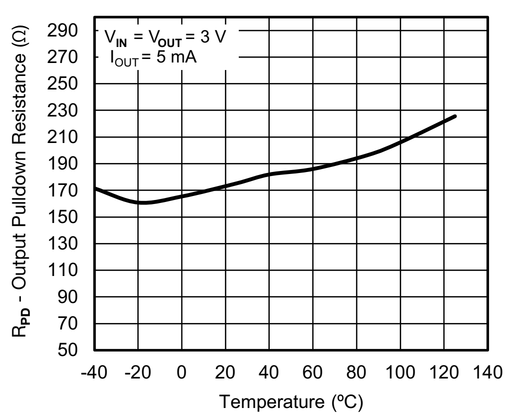
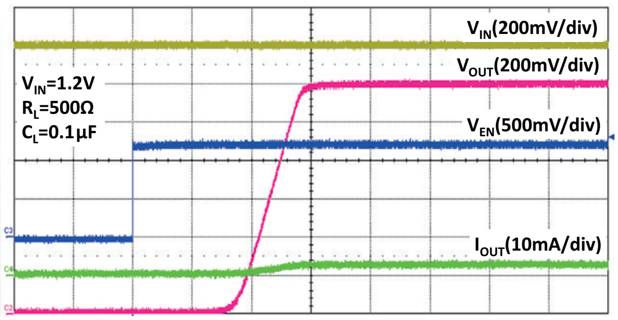


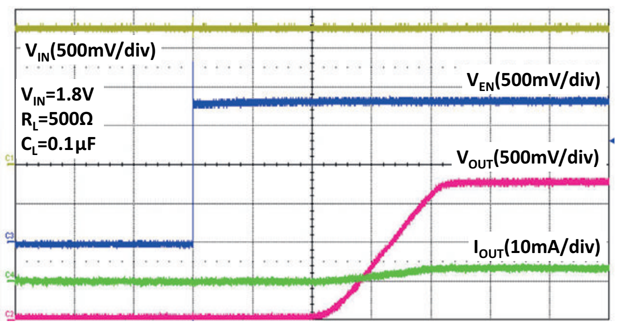
Fig. 19 - Output Pulldown Resistance vs. Temperature

TYPICAL WAVEFORMS



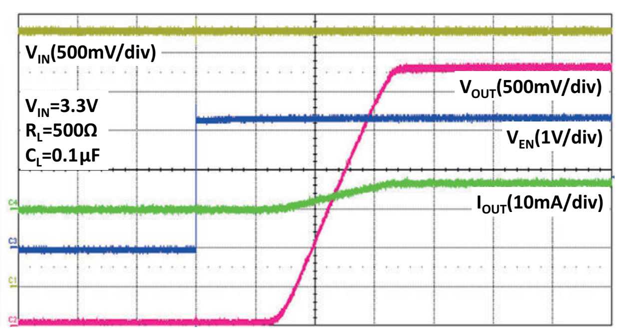
200 µs/div

Fig. 20 - Enable Power Up



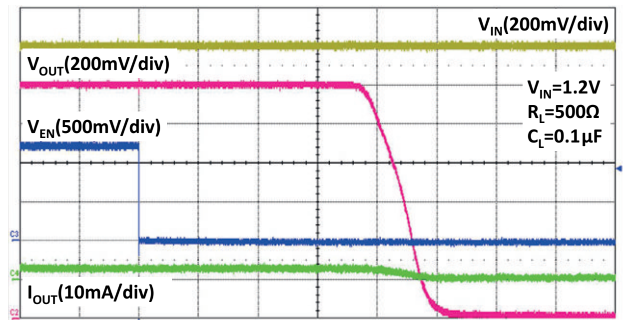
100 µs/div

Fig. 21 - Enable Power Up



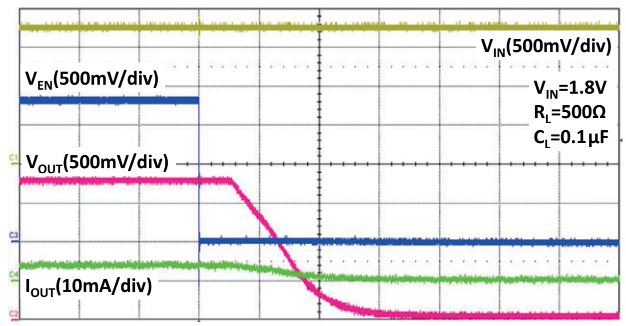
100 µs/div

Fig. 22 - Enable Power Up



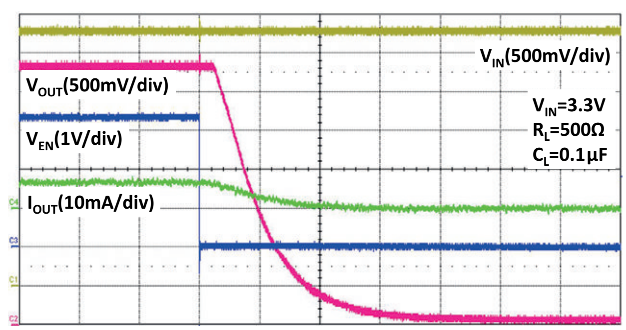
100 µs/div

Fig. 23 - Enable Power Down



20 µs/div

Fig. 24 - Enable Power Down



10 µs/div

Fig. 25 - Enable Power Down

TYPICAL WAVEFORMS

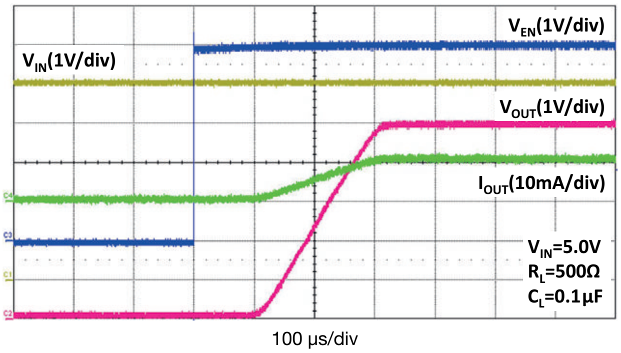


Fig. 26 - Enable Power Up

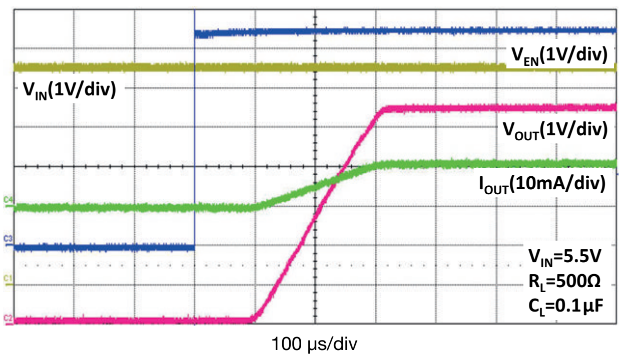


Fig. 27 - Enable Power Up

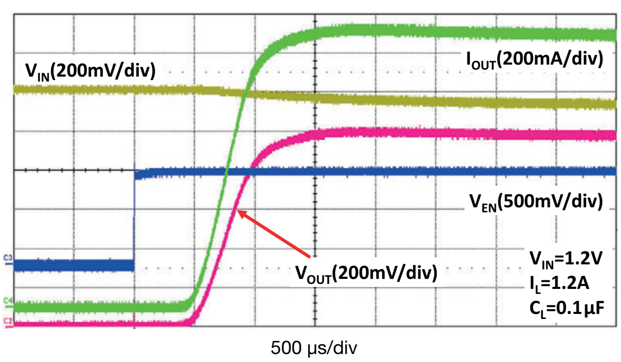


Fig. 28 - Enable Power Up

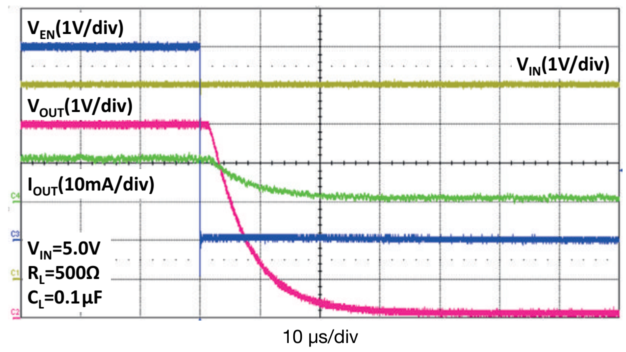


Fig. 29 - Enable Power Down

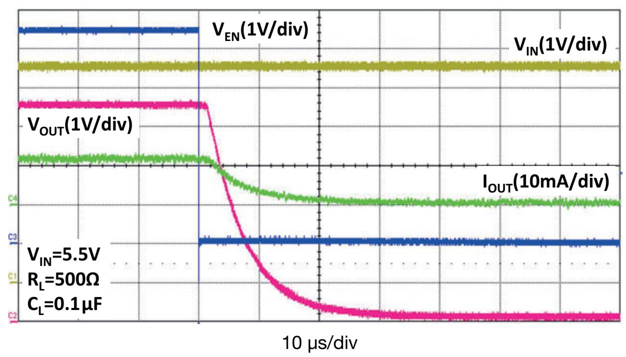


Fig. 30 - Enable Power Down

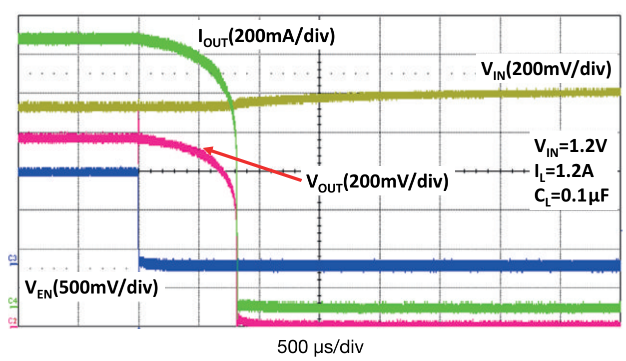


Fig. 31 - Enable Power Down

TYPICAL WAVEFORMS

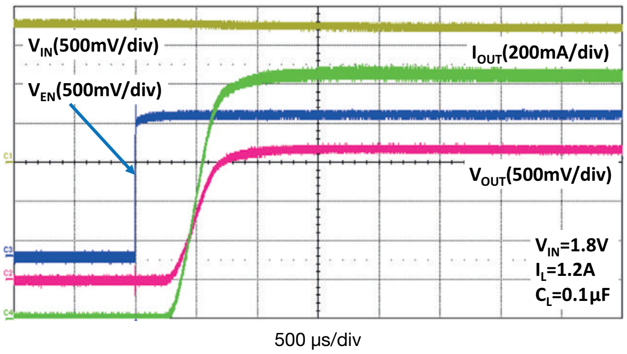


Fig. 32 - Enable Power Up

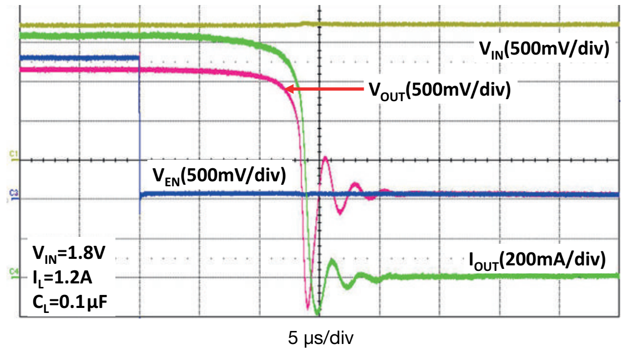


Fig. 35 - Enable Power Down

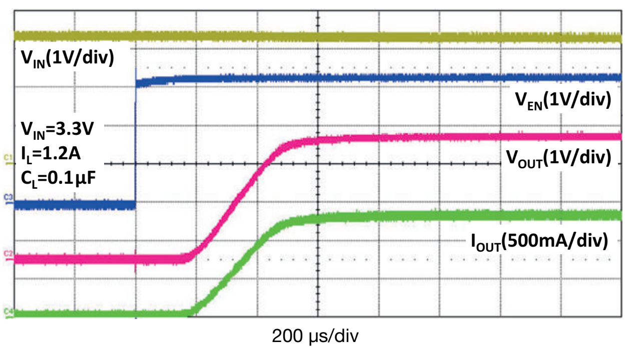


Fig. 33 - Enable Power Up

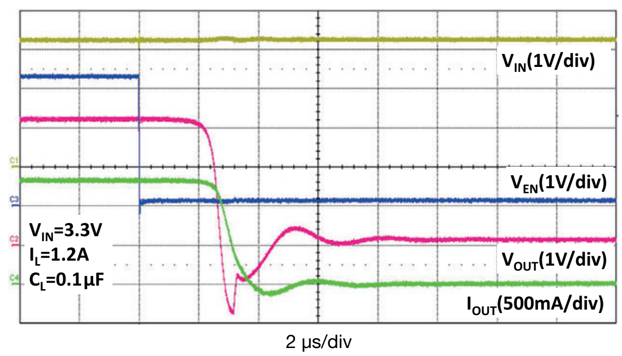


Fig. 36 - Enable Power Down

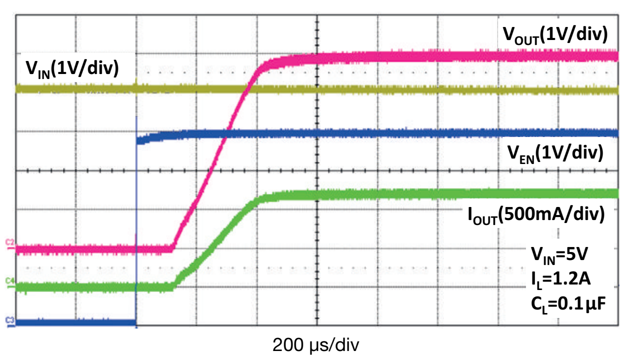


Fig. 34 - Enable Power Up

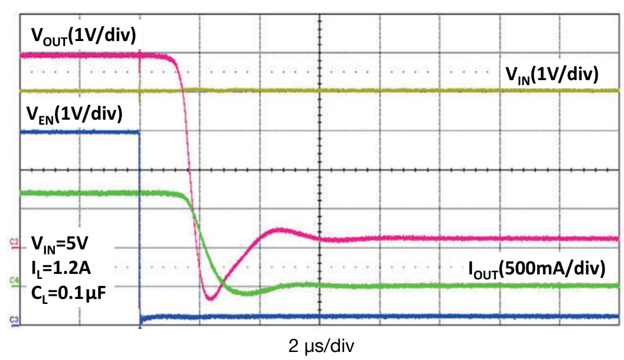


Fig. 37 - Enable Power Down

DETAILED DESCRIPTION

SiP32475 is high side, slew rate controlled, load switch. It incorporates a negative charge pump at the gate to keep the gate to source voltage high when turned on. This keeps the on resistance low at lower input voltages. SiP32475 is designed with slow slew rate to minimize inrush current during turn on. SiP32475 has a reverse blocking circuit, when disabled, to prevent the current from going back to the input when the output voltage is higher than the input voltage. SiP32475 has an output pull down resistor to discharge the output capacitance when the device is off.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 4.7 µF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor across V_{OUT} and GND is recommended to insure proper slew operation. There is inrush current through the output MOSFET and the magnitude of the inrush current depends on the output capacitor, the bigger the C_{OUT} the higher the inrush current. There is no ESR or capacitor type requirement.

Enable

The EN pin is compatible with CMOS logic voltage levels. It requires at least 0.4 V or below to fully shut down the device and 1 V or above to fully turn on the device. There is a 2.6 MΩ resistor connected between EN pin and GND pin.

Protection Against Reverse Voltage Condition

This device contains a reverse blocking circuit. When disabled (V_{EN} less than 0.4 V) this circuit keeps the output current from flowing back to the input when the output voltage is higher than the input voltage.

Thermal Considerations

Due to physical limitations of the layout and assembly of the device the maximum switch current is 2 A as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package.

The maximum power dissipation in any application is dependent on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance, θ_{J-A} = 150 °C/W, and the ambient temperature, T_A, which may be expressed as:

$$P\ (max.) = \frac{T_{J(max.)} - T_A}{\theta_{JA}} = \frac{125 - T_A}{150}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 666 mW.

So long as the load current is below the 2 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C is 120 mΩ at V_{IN} = 1.5 V. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 2800 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 120 mΩ x (1 + 0.0028 x (70 °C - 25 °C)) = 135 mΩ

The maximum current limit is then determined by

$$I_{LOAD(max.)} < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

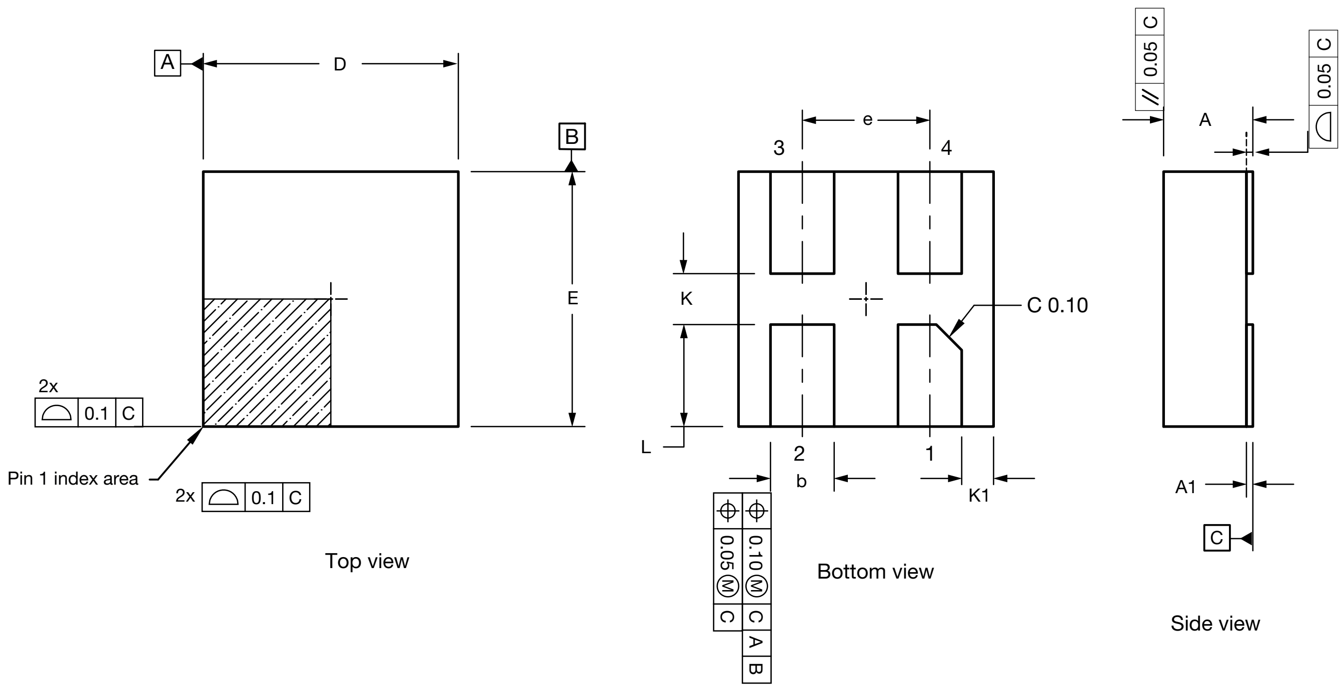
which in this case is 2.2 A. Under the stated input voltage condition, if the 2.2 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

To avoid possible permanent damage to the device and keep a reasonable design margin, it is recommended to operate the device maximum up to 2 A only as listed in the Absolute Maximum Ratings table.

PRODUCT SUMMARY	
Part number	SiP32475
Description	1.2 V to 5.5 V, 47 mΩ, 200 μs rise time, bidirectional off isolation, output discharge
Configuration	Single
Slew rate time (μs)	162
On delay time (μs)	138
Input voltage min. (V)	1.2
Input voltage max. (V)	5.5
On-resistance at input voltage min. (mΩ)	92
On-resistance at input voltage max. (mΩ)	47
Quiescent current at input voltage min. (μA)	1.2
Quiescent current at input voltage max. (μA)	5.5
Output discharge (yes / no)	Yes
Reverse blocking (yes / no)	Yes
Continuous current (A)	2
Package type	μDFN-4L
Package size (W, L, H) (mm)	1.0 x 1.0 x 0.35
Status code	2
Product type	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75792

µDFN-4L 1 mm x 1 mm Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.25	0.30	0.35	0.010	0.012	0.014
A1	0.00	-	0.05	0.000	-	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.50 BSC			0.020 BSC		
K	0.20 Ref.			0.008 Ref.		
K1	0.125 Ref.			0.005 Ref.		
L	0.35	0.40	0.45	0.014	0.016	0.018
ECN: S17-1722-Rev. A, 27-Nov-17 DWG: 6059						

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M-1994
(3) N is the number of terminals
Nd and Ne is the number of terminals in each D and E site respectively
(4) Dimensions b applies to plated terminal and is measured between 0.20 mm and 0.30 mm from terminal tip
(5) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Package warpage max. 0.05 mm

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