



**THE DATASHEET OF
S9S12DP51J4MPVE**



MC9S12DT128

Device User Guide

Covers MC9S12DT128E, MC9S12DG128E,
MC9S12DJ128E, MC9S12DG128, MC9S12DJ128,
MC9S12DB128, MC9S12A128, SC515846, SC515847,
SC515848, SC515849, SC101161DT, SC101161DG,
SC101161DJ, SC102202, SC102203, SC102204,
SC102205

HCS12 Microcontrollers

9S12DT128DGV2/D
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Revision History

| Version Number | Revision Date | Effective Date | Author | Description of Changes |
|----------------|---------------|----------------|--------|--|
| V01.00 | 18 Jun 2001 | 18 June 2001 | | Initial version (parent doc v2.03 dug for dp256). |
| V01.01 | 23 July 2001 | 23 July 2001 | | Updated version after review |
| V01.02 | 23 Sep 2001 | 23 Sep 2001 | | Changed Partname, added pierce mode, updated electrical characteristics some minor corrections |
| V01.03 | 12 Oct 2001 | 12 Oct 2001 | | Replaced Star12 by HCS12 |
| V01.04 | 27 Feb 2002 | 27 Feb 2002 | | Updated electrical spec after MC-Qualification (IOL/IOH), Data for Pierce, NVM reliability New document numbering. Corrected Typos |
| V01.05 | 4 Mar 2002 | 4 Mar 2002 | | Increased VDD to 2.35V, removed min. oscillator startup Removed Document order number except from Cover Sheet |
| V01.06 | 8 July 2002 | 22 July 2002 | | Added: Pull-up columns to signal table, example for PLL Filter calculation, Thermal values for junction to board and package, BGND pin pull-up Part Order Information Global Register Table Chip Configuration Summary Modified: Reduced Wait and Run IDD values Mode of Operation chapter changed leakage current for ADC inputs down to +-1uA Corrected: Interrupt vector table enable register inconsistencies PCB layout for 80QFP VREGEN position |
| V02.00 | 11 Jan 2002 | 11 Jan 2002 | | NEW MASKSET Changed part number from DTB128 to DT128 Functional Changes: ROMCTL changes in Emulation Mode 80 Pin Byteflight package Option available Flash with 2 Bit Backdoor Key Enable Additional CAN0 routing to PJ7,6 Improved BDM with sync and acknowledge capabilities New Part ID number Improvements: Significantly improved NVM reliability data Corrections: Interrupt vector Table |
| V02.01 | 01 Feb 2002 | 01 Feb 2002 | | Updated Block User Guide versions in preface Updated Appendix A Electrical Characteristics |

| Version Number | Revision Date | Effective Date | Author | Description of Changes |
|----------------|---------------|----------------|--------|---|
| V02.02 | 08 Mar 2002 | 08 Mar 2002 | | <p>Changed XCLKS to PE7 in Table 2-2</p> <p>Updated device part numbers in Figure 2-1</p> <p>Updated BDM clock in Figure 3-1</p> <p>Removed SIM description in overview & n_{UPOSC} spec in Table A-15</p> <p>Updated electrical spec of VDD & VDDPLL (Table A-4), IOL/IOH (Table A-6), C_{INS} (Table A-9), C_{IN} (Table A-6 & A-15),</p> <p>Updated interrupt pulse timing variables in Table A-6</p> <p>Updated device part numbers in Figure 2-1</p> <p>Added document numbers on cover page and Table 0-2</p> |
| V02.03 | 14 Mar 2002 | 14 Mar 2002 | | <p>Cleaned up Fig. 1-1, 2-1</p> <p>Updated Section 1.5 descriptions</p> <p>Corrected PE assignment in Table 2-2, Fig. 2-5,6,7.</p> <p>Corrected NVM sizes in Sections 16, 17</p> <p>Added I_{REF} spec for 1ATD in Table A-8</p> <p>Added Blank Check in A.3.1.5 and Table A-11</p> <p>Updated CRG spec in Table A-15</p> |
| V02.04 | 16 Aug 2002 | 16 Aug 2002 | | <p>Added:</p> <p>Pull-up columns to signal table,</p> <p>Example for PLL Filter calculation,</p> <p>Thermal values for junction to board and package,</p> <p>BGND pin pull-up</p> <p>Part Order Information</p> <p>Global Register Table</p> <p>Chip Configuration Summary</p> <p>Device specific info on CRG</p> <p>Modified:</p> <p>Reduced Wait and Run IDD values</p> <p>Mode of Operation chapter</p> <p>Changed leakage current for ADC inputs down to $\pm 1\mu A$</p> <p>Minor modification of PLL frequency/ voltage gain values</p> <p>Corrected:</p> <p>Pin names/functions on 80 pin packages</p> <p>Interrupt vector table enable register inconsistencies</p> <p>PCB layout for 80QFP VREGEN position</p> |
| V02.05 | 12 Sep 2002 | 12 Sep 2002 | | <p>Corrected:</p> <p>Register address mismatches in 1.5.1</p> |
| V02.06 | 06 Nov 2002 | 06 Nov 2002 | | <p>Removed document order no. from Revision History pages</p> <p>Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0/1/4, BDLC, IIC and/or Byteflight</p> <p>Added 2L40K mask set in section 1.6</p> <p>Added OSC User Guide in Preface, "Document References"</p> <p>Added oscillator clock connection to BDM in S12_CORE in fig 3-1</p> <p>Corrected several register and bit names in "Local Enable" column of Table 5.1 Interrupt Vector Locations</p> <p>Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock</p> <p>Added new section: "Oscillator (OSC) Block Description"</p> <p>Corrected in footnote of Table "PLL Characteristics": $f_{OSC} = 4MHz$</p> |

| Version Number | Revision Date | Effective Date | Author | Description of Changes |
|----------------|---------------|----------------|--------|---|
| V02.07 | 29 Jan 2003 | 29 Jan 2003 | | <p>Added 3L40K mask set in section 1.6</p> <p>Corrected register entries in section 1.5.1 “Detailed Memory Map”</p> <p>Updated description for ROMCTL in section 2.3.31</p> <p>Updated section 4.3.3 “Unsecuring the Microcontroller”</p> <p>Corrected and updated device-specific information for OSC (section 8.1) & Byteflight (section 15.1)</p> <p>Updated footnote in Table A-4 “Operating Conditions”</p> <p>Changed reference of VDDM to VDDR in section A.1.8</p> <p>Removed footnote on input leakage current in Table A-6 “5V I/O Characteristics”</p> |
| V02.08 | 26 Feb 2003 | 26 Feb 2003 | | <p>Added part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E in “Preface” and related part number references</p> <p>Removed mask sets 0L40K and 2L40K from Table 1-3</p> |
| V02.09 | 15 Oct 2003 | 15 Oct 2003 | | <p>Replaced references to HCS12 Core Guide by the individual HCS12 Block guides in Table 0-2, section 1.5.1, and section 6; updated Fig.3-1 “Clock Connections” to show the individual HCS12 blocks</p> <p>Corrected PIM module name and document order number in Table 0-2 “Document References”</p> <p>Corrected ECT pulse accumulators description in section 1.2 “Features”</p> <p>Corrected KWP5 pin name in Fig 2-1 112LQFP pin assignments</p> <p>Corrected pull resistor CTRL/reset states for PE7 and PE4-PE0 in Table 2.1 “Signal Properties”</p> <p>Mentioned “S12LRAE” bootloader in Flash section 17</p> <p>Corrected footnote on clamp of TEST pin under Table A-1 “Absolute Maximum Ratings”</p> <p>Corrected minimum bus frequency to 0.25MHz in Table A-4 “Operating Conditions”</p> <p>Replaced “burst programming” by “row programming” in A.3 “NVM, Flash and EEPROM”</p> <p>Corrected blank check time for EEPROM in Table A-11 “NVM Timing Characteristics”</p> <p>Corrected operating frequency in Table A-18 “SPI Master/Slave Mode Timing Characteristics”</p> |
| V02.10 | 6 Feb 2004 | 6 Feb 2004 | | <p>Added A128 information in “Derivative Differences”, 2.1 “Device Pinout”, 2.2 “Signal Properties Summary”, Fig 23-2 & Fig 23-4</p> <p>Added lead-free package option (PVE) in Table 0-2 “Derivative Differences for MC9S12DB128” and Fig 0-1 “Order Partnumber Example”</p> <p>Added an “AEC qualified” row in the “Derivative Differences” tables 0-1 & 0-2.</p> |
| V02.11 | 3 May 2004 | 3 May 2004 | | <p>Added part numbers SC515846, SC515847, SC515848, and SC515849 in “Derivative Differences” tables 0-1 & 0-2, section 2, and section 23.</p> <p>Corrected and added maskset 4L40K in tables 0-1 & 0-2 and section 1.6.</p> <p>Corrected BDLC module availability in DB128 80QFP part in “Derivative Differences” table 0-2.</p> |

| Version Number | Revision Date | Effective Date | Author | Description of Changes |
|----------------|---------------|----------------|--------|---|
| V02.12 | 06 Dec 2004 | 06 Dec 2004 | | Added maskset 0L94R Added items $V_{IH,EXTAL}$, $V_{IL,EXTAL}$, & $V_{HYS,EXTAL}$ in table A-15 "Oscillator characteristics" Removed item "Oscillator" from table A-4 "Operating Conditions" as it is already covered in table "Oscillator Characteristics" |
| V02.13 | 04 Mar 2005 | 04 Mar 2005 | | Amended feature list of A128 in Table 0-1 "Derivative Differences" |
| V02.14 | 28 Apr 2005 | 28 Apr 2005 | | Updated cover page Added part numbers SC101161DT, SC101161DG, SC101161DJ, SC102202, SC102203, SC102204, & SC102205 Added masksets 5L40K & 1L59W Changed T_{Javg} to 85°C in table A-12 "NVM Reliability" & added footnote concerning data retention |
| V02.15 | 05 Oct 2005 | 05 Oct 2005 | | Updated "NVM Reliability" table A-12 format with added data. Added figure A-2 "Typical Endurance vs Temperature" |

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Derivative Differences and Document References

Derivative Differences

(Table 0-1) and (Table 0-2) show the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences¹

| Modules | MC9S12DT128E ³ MC9S12DT128 SC515849 ⁴ SC101161DT ⁵ SC102205 ⁶ | MC9S12DG128E ³ MC9S12DG128 SC515847 ⁴ SC101161DG ⁵ SC102203 ⁶ | MC9S12DJ128E ³ MC9S12DJ128 SC515848 ⁴ SC101161DJ ⁵ SC102204 ⁶ | MC9S12A128 |
|---------------|---|---|---|--|
| # of CANs | 3 | 2 | 2 | 0 |
| CAN4 | ✓ | ✓ | ✓ | X |
| CAN1 | ✓ | X | X | X |
| CAN0 | ✓ | ✓ | ✓ | X |
| J1850/BDLC | X | X | ✓ | X |
| IIC | ✓ | ✓ | ✓ | ✓ |
| Byteflight | X | X | X | X |
| Package | 112 LQFP | 112 LQFP/80 QFP ² | 112 LQFP/80 QFP ² | 112 LQFP/80 QFP ² |
| Package Code | PV | PV/FU | PV/FU | PV/FU |
| Mask set | 1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ | 1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ | 1L40K ³ , 3L40K, 0L94R, 4L40K ⁴ , 1L59W ⁵ , 5L40K ⁶ | 3L40K, 0L94R |
| Temp Options | M, V, C | M, V, C | M, V, C | C |
| AEC qualified | Yes | Yes | Yes | No |
| Notes | An errata exists contact Sales Office | An errata exists contact Sales Office | An errata exists contact Sales Office | An errata exists contact Sales Office |

Table 0-2 Derivative Differences for MC9S12DB128¹

| Modules | MC9S12DB128 SC515846 ⁴ SC102202 ⁶ | MC9S12DB128 SC515846 ⁴ SC102202 ⁶ |
|--------------|---|---|
| # of CANs | 2 | 0 |
| CAN4 | ✓ | X |
| CAN1 | X | X |
| CAN0 | ✓ | X |
| J1850/BDLC | X | X |
| IIC | X | X |
| Byteflight | ✓ | ✓ |
| Package | 112 LQFP | 80 QFP ² |
| Package Code | PV/PVE | FU |

| Modules | MC9S12DB128 SC515846 ⁴ SC102202 ⁶ | MC9S12DB128 SC515846 ⁴ SC102202 ⁶ |
|---------------|---|---|
| Mask set | 3L40K, 0L94R, 4L40K ⁴ , 5L40K ⁶ | 3L40K, 0L94R, 4L40K ⁴ , 5L40K ⁶ |
| Temp Options | M, V, C/M, V | M, V, C |
| AEC qualified | Yes | Yes |
| Notes | An errata exists contact Sales Office | An errata exists contact Sales Office |

NOTE:

- ✓: Available for this device, X: Not available for this device.
- 80 Pin bond-out for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 is the same; MC9S12DB128, SC515846, and SC102202 have a different bond-out.
- Part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E are associated with the mask set 1L40K.
- Part numbers SC515846, SC515847, SC515848, and SC515849 are associated with the mask set 4L40K.
- Part numbers SC101161DT, SC101161DG, SC101161DJ are associated with the mask set 1L59W.
- Part numbers SC102202, SC102203, SC102204, and SC102205 are associated with the mask set 5L40K which is not for volume production.

The following figure provides an ordering number example for the MC9S12D128 devices.

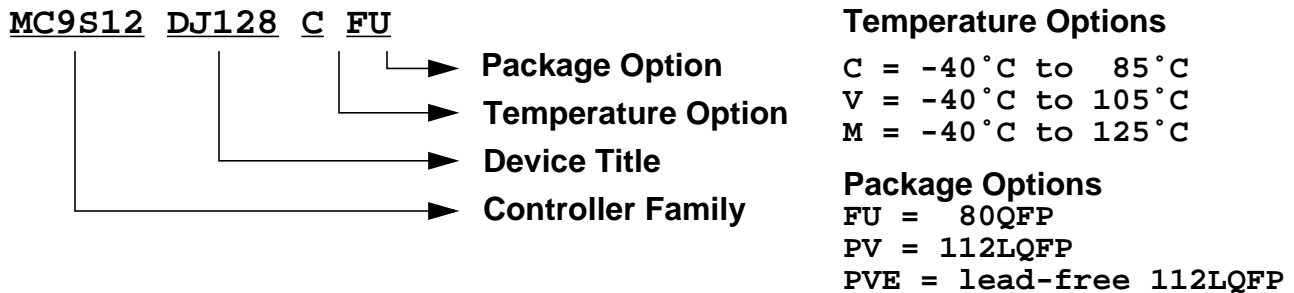


Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Registers**
 - Do not write or read CAN0 registers (after reset: address range \$0140 - \$017F), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write or read CAN1 registers (after reset: address range \$0180 - \$01BF), if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write or read CAN4 registers (after reset: address range \$0280 - \$02BF), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write or read BDLC registers (after reset: address range \$00E8 - \$00EF), if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write or read IIC registers (after reset: address range \$00E0 - \$00E7), if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).

- Do not write or read Byteflight registers (after reset: address range \$0300 - \$035F), if using a derivative without Byteflight registers (see **(Table 0-1)** and **(Table 0-2)**).
- **Interrupts**
 - Fill the four CAN0 interrupt vectors (\$FFB0 - \$FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
 - Fill the four CAN1 interrupt vectors (\$FFA8 - \$FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
 - Fill the four CAN4 interrupt vectors (\$FF90 - \$FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
 - Fill the BDLC interrupt vector (\$FFC2, \$FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
 - Fill the IIC interrupt vector (\$FFC0, \$FFC1) according to your coding policies for unused interrupts, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
 - Fill the four Byteflight interrupt vectors (\$FFA0 - \$FFA7) according to your coding policies for unused interrupts, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).
- **Ports**
 - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
 - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
 - The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
 - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
 - The IIC pin functionality (SCL, SCA) is not available on port PJ7 and PJ6, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
 - The Byteflight pin functionality (BF_PSLM, BF_PERR, BF_PROK, BF_PSYN, TX_BF, RX_BF) is not available on port PM7, PM6, PM5, PM4, PM3 and PM2, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
 - Do not write MODRR3 and MODRR2 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
- **Pins not available in 80 pin QFP package for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204**

- **Port H**
In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+\$0262) to \$FF, or enabling the pull resistors by writing a \$FF to the pull enable register (PERH at Base+\$0264).
- **Port J[1:0]**
Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+\$026C.
- **Port K**
Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+\$000C. Therefore care must be taken not to clear this bit.
- **Port M[7:6]**
PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **Port P6**
PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
- **Port S[7:4]**
PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **PAD[15:8] (ATD1 channels)**
Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!
- **Pins not available in 80 pin QFP package for MC9S12DB128, SC515846, and SC102202**
 - **Port H**
In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+\$0262) to \$FF, or enabling the pull resistors by writing a \$FF to the pull enable register (PERH at Base+\$0264).
 - **Port J[7:6, 1:0]**
Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[7:6, 1:0] by clearing the bits PERJ7, PERJ6, PERJ1 and PERJ0 at Base+\$026C.
 - **Port K**
Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+\$000C. Therefore care must be taken not to clear this bit.
 - **Port M[1:0]**
PM1:0 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
 - **Port P6**
PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.

- **Port S[3:2]**
PS3:2 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **PAD[15:8] (ATD1 channels)**
Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

Document References

The Device User Guide provides information about the MC9S12DT128 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block User Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-3** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-3 Document References

| User Guide | Version | Document Order Number |
|---|---------|-----------------------|
| HCS12 CPU Reference Manual | V02 | S12CPUV2/D |
| HCS12 Module Mapping Control (MMC) Block Guide | V04 | S12MMCV4/D |
| HCS12 Multiplexed External Bus Interface (MEBI) Block Guide | V03 | S12MEBIV3/D |
| HCS12 Interrupt (INT) Block Guide | V01 | S12INTV1/D |
| HCS12 Background Debug Module (BDM) Block Guide | V04 | S12BDMV4/D |
| HCS12 Breakpoint (BKP) Block Guide | V01 | S12BKPV1/D |
| Clock and Reset Generator (CRG) Block User Guide | V04 | S12CRGV4/D |
| Oscillator (OSC) Block User Guide | V02 | S12OSCV2/D |
| Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block User Guide | V01 | S12ECT16B8CV1/D |
| Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block User Guide | V02 | S12ATD10B8CV2/D |
| Inter IC Bus (IIC) Block User Guide | V02 | S12IICV2/D |
| Asynchronous Serial Interface (SCI) Block User Guide | V02 | S12SCIV2/D |
| Serial Peripheral Interface (SPI) Block User Guide | V02 | S12SPIV2/D |
| Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide | V01 | S12PWM8B8CV1/D |
| 128K Byte Flash (FTS128K) Block User Guide | V02 | S12FTS128KV2/D |
| 2K Byte EEPROM (EETS2K) Block User Guide | V01 | S12EETS2KV1/D |
| Byte Level Data Link Controller -J1850 (BDLC) Block User Guide | V01 | S12BDLCV1/D |
| Motorola Scalable CAN (MSCAN) Block User Guide | V02 | S12MSCANV2/D |
| Voltage Regulator (VREG) Block User Guide | V01 | S12VREGV1/D |
| Port Integration Module (PIM_9DTB128) Block User Guide | V02 | S12DTB128PIMV2/D |
| Byteflight (BF) Block User Guide | V01 | S12BFV1/D |

Section 1 Introduction

1.1 Overview

The MC9S12DT128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
 - 16-bit HCS12 CPU
 - i. Upward compatible with M68HC11 instruction set
 - ii. Interrupt stacking and programmer's model identical to M68HC11
 - iii. 20-bit ALU
 - iv. Instruction queue
 - v. Enhanced indexed addressing
 - MEBI (Multiplexed External Bus Interface)
 - MMC (Module Mapping Control)
 - INT (Interrupt control)
 - BKP (Breakpoints)
 - BDM (Background Debug Module)
- CRG (Clock and Reset Generator)
 - Choice of low current Colpitts oscillator or standard Pierce Oscillator
 - PLL
 - COP watchdog
 - real time interrupt
 - clock monitor
- 8-bit and 4-bit ports with interrupt functionality

- Digital filtering
- Programmable rising or falling edge trigger
- Memory
 - 128K Flash EEPROM
 - 2K byte EEPROM
 - 8K byte RAM
- Two 8-channel Analog-to-Digital Converters
 - 10-bit resolution
 - External conversion trigger capability
- Three 1M bit per second, CAN 2.0 A, B software compatible modules
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Enhanced Capture Timer
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels
 - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
 - Programmable period and duty cycle
 - 8-bit 8-channel or 16-bit 4-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
 - Usable as interrupt inputs
- Serial interfaces
 - Two asynchronous Serial Communications Interfaces (SCI)
 - Two Synchronous Serial Peripheral Interface (SPI)
 - Byteflight
- Byte Data Link Controller (BDLC)

- SAE J1850 Class B Data Communications Network Interface
 - Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
 - Compatible with I2C Bus standard
 - Multi-master operation
 - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP and 80-Pin QFP package options
 - I/O lines with 5V input and drive capability
 - 5V A/D converter inputs
 - Operation at 50MHz equivalent to 25MHz Bus Speed
 - Development support
 - Single-wire background debug™ mode
 - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes
 - Special Single-Chip Mode with active Background Debug Mode
 - Special Test Mode (**Freescale use only**)
 - Special Peripheral Mode (**Freescale use only**)

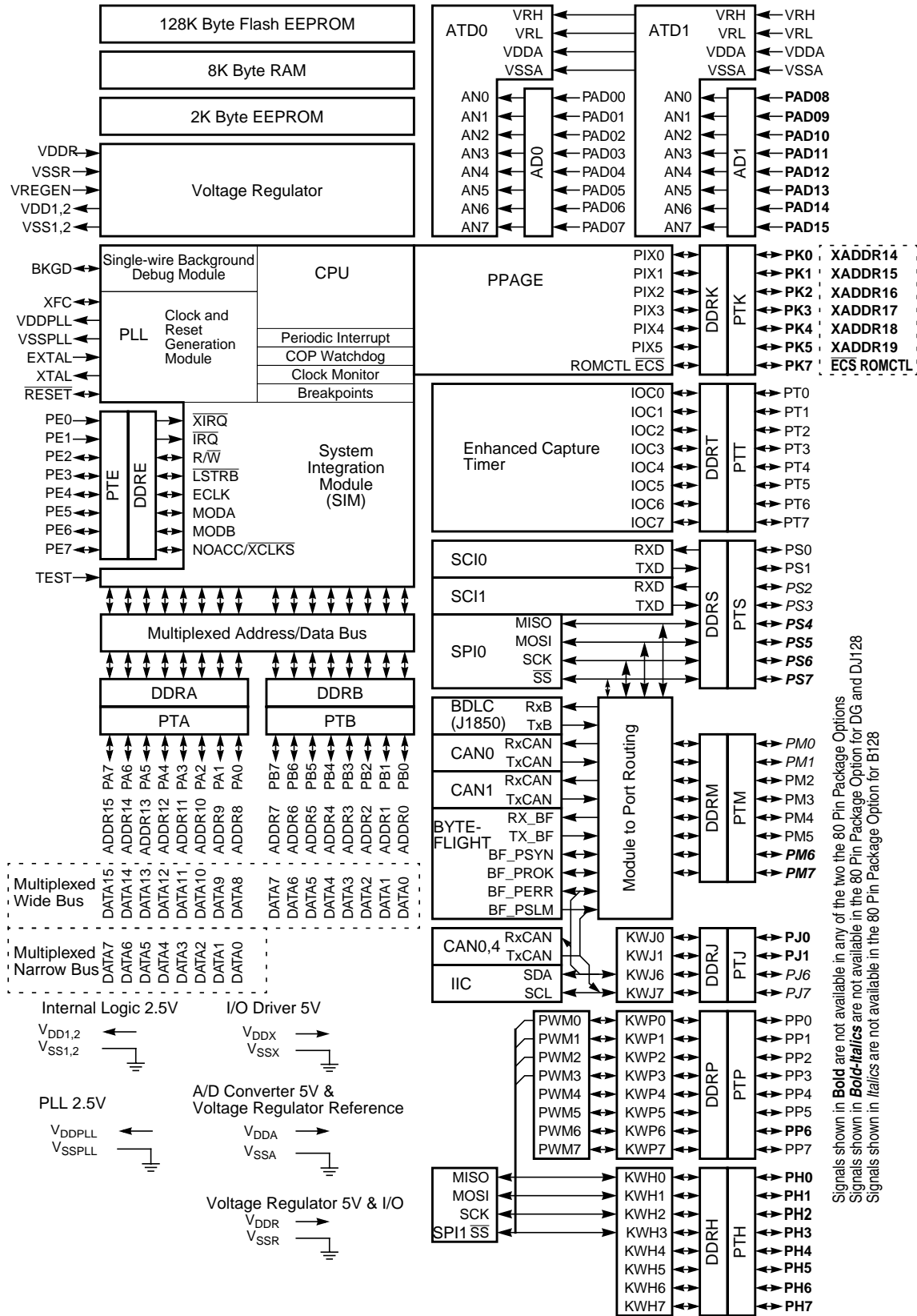
Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DT128 device.

Figure 1-1 MC9S12DT128 Block Diagram



1.5 Device Memory Map

(Table 1-1) and (Figure 1-2) show the device memory map of the MC9S12DT128 after reset. Note that after reset the EEPROM (\$0000 – \$07FF) is hidden by the register space (\$0000 - \$03FF) and the RAM (\$0000 - \$1FFF). The bottom 1K Bytes of RAM (\$0000 - \$03FF) are hidden by the register space.

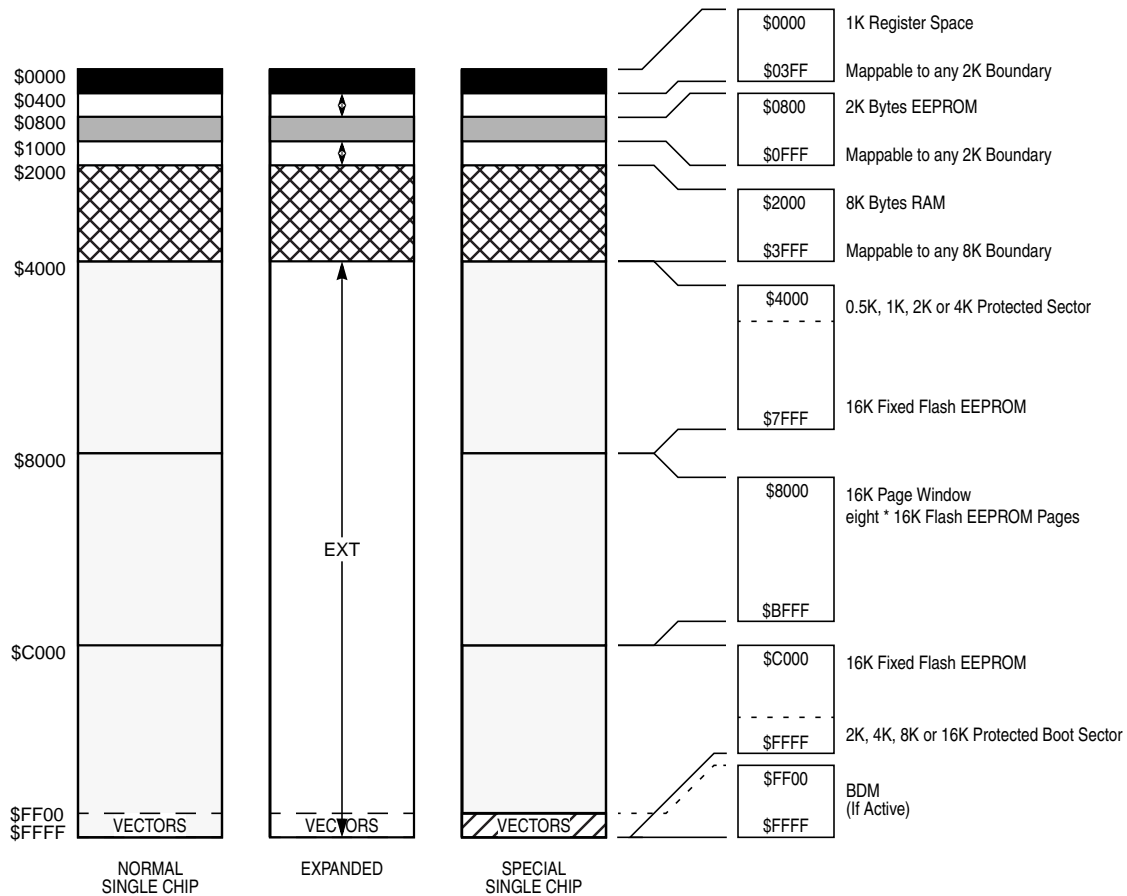
Table 1-1 Device Memory Map

| Address | Module | Size (Bytes) |
|-----------------|--|--------------|
| \$0000 – \$0017 | CORE (Ports A, B, E, Modes, Inits, Test) | 24 |
| \$0018 – \$0019 | Reserved | 2 |
| \$001A – \$001B | Device ID register (PARTID) | 2 |
| \$001C – \$001F | CORE (MEMSIZ, IRQ, HPRIO) | 4 |
| \$0020 – \$0027 | Reserved | 8 |
| \$0028 – \$002F | CORE (Background Debug Module) | 8 |
| \$0030 – \$0033 | CORE (PPAGE, Port K) | 4 |
| \$0034 – \$003F | Clock and Reset Generator (PLL, RTI, COP) | 12 |
| \$0040 – \$007F | Enhanced Capture Timer 16-bit 8 channels | 64 |
| \$0080 – \$009F | Analog to Digital Converter 10-bit 8 channels (ATD0) | 32 |
| \$00A0 – \$00C7 | Pulse Width Modulator 8-bit 8 channels (PWM) | 40 |
| \$00C8 – \$00CF | Serial Communications Interface (SCI0) | 8 |
| \$00D0 – \$00D7 | Serial Communications Interface (SCI1) | 8 |
| \$00D8 – \$00DF | Serial Peripheral Interface (SPI0) | 8 |
| \$00E0 – \$00E7 | Inter IC Bus | 8 |
| \$00E8 – \$00EF | Byte Level Data Link Controller (BDLC) | 8 |
| \$00F0 – \$00F7 | Serial Peripheral Interface (SPI1) | 8 |
| \$00F8 – \$00FF | Reserved | 8 |
| \$0100 – \$010F | Flash Control Register | 16 |
| \$0110 – \$011B | EEPROM Control Register | 12 |
| \$011C – \$011F | Reserved | 4 |
| \$0120 – \$013F | Analog to Digital Converter 10-bit 8 channels (ATD1) | 32 |
| \$0140 – \$017F | Motorola Scalable CAN (CAN0) | 64 |
| \$0180 – \$01BF | Motorola Scalable CAN (CAN1) | 64 |
| \$01C0 – \$01FF | Reserved | 64 |
| \$0200 – \$023F | Reserved | 64 |
| \$0240 – \$027F | Port Integration Module (PIM) | 64 |
| \$0280 – \$02BF | Motorola Scalable CAN (CAN4) | 64 |
| \$02C0 – \$02FF | Reserved | 64 |
| \$0300 – \$035F | Byteflight (BF) | 96 |
| \$0360 – \$03FF | Reserved | 160 |
| \$0000 – \$07FF | EEPROM array | 2048 |
| \$0000 – \$1FFF | RAM array | 8192 |
| \$4000 – \$7FFF | Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start | 16384 |
| \$8000 – \$BFFF | Flash EEPROM Page Window | 16384 |

Table 1-1 Device Memory Map

| Address | Module | Size (Bytes) |
|-----------------|--|--------------|
| \$C000 – \$FFFF | Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at \$FF80 – \$FFFF | 16384 |

Figure 1-2 MC9S12DT128 Memory Map



The address does not show the map after reset, but a useful map. After reset the map is:
 \$0000 – \$03FF: Register Space
 \$0000 – \$1FFF: 8K RAM
 \$0000 – \$07FF: 2K EEPROM (not visible)

1.5.1 Detailed Register Map

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-----------------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0000 | PORTA | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0001 | PORTB | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0002 | DDRA | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0003 | DDRB | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0004 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0005 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0006 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0007 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0008 | PORTE | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | Bit 1 | Bit 0 |
| \$0009 | DDRE | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | Bit 2 | 0 | 0 |
| \$000A | PEAR | Read: Write: | NOACCE | 0 | PIPOE | NECLK | LSTRE | RDWE | 0 | 0 |
| \$000B | MODE | Read: Write: | MODC | MODB | MODA | 0 | IVIS | 0 | EMK | EME |
| \$000C | PUCR | Read: Write: | PUPKE | 0 | 0 | PUPEE | 0 | 0 | PUPBE | PUPAE |
| \$000D | RDRIV | Read: Write: | RDPK | 0 | 0 | RDPE | 0 | 0 | RDPB | RDPA |
| \$000E | EBICTL | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ESTR |
| \$000F | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-----------------|-------|-------|-------|-------|--------|--------|-------|--------|
| \$0010 | INITRM | Read: Write: | RAM15 | RAM14 | RAM13 | RAM12 | RAM11 | 0 | 0 | RAMHAL |
| \$0011 | INITRG | Read: Write: | 0 | REG14 | REG13 | REG12 | REG11 | 0 | 0 | 0 |
| \$0012 | INITEE | Read: Write: | EE15 | EE14 | EE13 | EE12 | EE11 | 0 | 0 | EEON |
| \$0013 | MISC | Read: Write: | 0 | 0 | 0 | 0 | EXSTR1 | EXSTR0 | ROMHM | ROMON |
| \$0014 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

\$0015 - \$0016

INT map 1 of 2 (HCS12 Interrupt)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|------------|-------|-------|-------|-------|-------|-------|-------|
| \$0015 | ITCR | Read: 0 | 0 | 0 | WRINT | ADR3 | ADR2 | ADR1 | ADR0 |
| | | Write: | | | | | | | |
| \$0016 | ITEST | Read: INTE | INTC | INTA | INT8 | INT6 | INT4 | INT2 | INT0 |
| | | Write: | | | | | | | |

\$0017 - \$0017

MMC map 2 of 4 (HCS12 Module Mapping Control)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| \$0017 | MTST1 Test Only | Read: Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | |

\$0018 - \$0019

Reserved

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------------|----------|---------|-------|-------|-------|-------|-------|-------|-------|
| \$0018 - \$0019 | Reserved | Read: 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | |

\$001A - \$001B

Device ID Register ((Table 1-3))

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|------------|-------|-------|-------|-------|-------|-------|-------|
| \$001A | PARTIDH | Read: ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 |
| | | Write: | | | | | | | |
| \$001B | PARTIDL | Read: ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| | | Write: | | | | | | | |

\$001C - \$001D
1-4))

MMC map 3 of 4 (HCS12 Module Mapping Control, (Table

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------------|---------|---------|---------|-------|---------|---------|---------|
| \$001C | MEMSIZ0 | Read: reg_sw0 | 0 | eep_sw1 | eep_sw0 | 0 | ram_sw2 | ram_sw1 | ram_sw0 |
| | | Write: | | | | | | | |
| \$001D | MEMSIZ1 | Read: rom_sw1 | rom_sw0 | 0 | 0 | 0 | 0 | pag_sw1 | pag_sw0 |
| | | Write: | | | | | | | |

\$001E - \$001E

MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|------------|-------|-------|-------|-------|-------|-------|-------|
| \$001E | INTCR | Read: IRQE | IRQEN | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | |

\$001F - \$001F

INT map 2 of 2 (HCS12 Interrupt)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$001F | HPRIO | Write: | PSEL7 | PSEL6 | PSEL5 | PSEL4 | PSEL3 | PSEL2 | PSEL1 | 0 |

\$0020 - \$0027

Reserved

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0020 - \$0027 | Reserved | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

\$0028 - \$002F

BKP (HCS12 Breakpoint)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|-------|--------|-------|
| \$0028 | BKPCT0 | Write: | BKEN | BKFULL | BKBDM | BKTAG | 0 | 0 | 0 | 0 |
| \$0029 | BKPCT1 | Write: | BK0MBH | BK0MBL | BK1MBH | BK1MBL | BK0RWE | BK0RW | BK1RWE | BK1RW |
| \$002A | BKP0X | Write: | 0 | 0 | BK0V5 | BK0V4 | BK0V3 | BK0V2 | BK0V1 | BK0V0 |
| \$002B | BKP0H | Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$002C | BKP0L | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$002D | BKP1X | Write: | 0 | 0 | BK1V5 | BK1V4 | BK1V3 | BK1V2 | BK1V1 | BK1V0 |
| \$002E | BKP1H | Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$002F | BKP1L | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

\$0030 - \$0031

MMC map 4 of 4 (HCS12 Module Mapping Control)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0030 | PPAGE | Write: | 0 | 0 | PIX5 | PIX4 | PIX3 | PIX2 | PIX1 | PIX0 |
| \$0031 | Reserved | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

\$0032 - \$0033

MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0032 | PORTK | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0033 | DDRK | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

\$0034 - \$003F**CRG (Clock and Reset Generator)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------|--------|--------|-------|--------|--------|--------|--------|--------|--------|
| \$0034 | SYNR | Read: | 0 | 0 | SYN5 | SYN4 | SYN3 | SYN2 | SYN1 | SYN0 |
| | | Write: | | | | | | | | |
| \$0035 | REFDV | Read: | 0 | 0 | 0 | 0 | REFDV3 | REFDV2 | REFDV1 | REFDV0 |
| | | Write: | | | | | | | | |
| \$0036 | CTFLG TEST ONLY | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0037 | CRGFLG | Read: | RTIF | PORF | 0 | LOCKIF | LOCK | TRACK | SCMIF | SCM |
| | | Write: | | | | | | | | |
| \$0038 | CRGINT | Read: | RTIE | 0 | 0 | LOCKIE | 0 | 0 | SCMIE | 0 |
| | | Write: | | | | | | | | |
| \$0039 | CLKSEL | Read: | PLLSEL | PSTP | SYSWAI | ROAWAI | PLLWAI | CWAI | RTIWAI | COPWAI |
| | | Write: | | | | | | | | |
| \$003A | PLLCTL | Read: | CME | PLLON | AUTO | ACQ | 0 | PRE | PCE | SCME |
| | | Write: | | | | | | | | |
| \$003B | RTICTL | Read: | 0 | RTR6 | RTR5 | RTR4 | RTR3 | RTR2 | RTR1 | RTR0 |
| | | Write: | | | | | | | | |
| \$003C | COPCTL | Read: | WCOP | RSBCK | 0 | 0 | 0 | CR2 | CR1 | CR0 |
| | | Write: | | | | | | | | |
| \$003D | FORBYP TEST ONLY | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$003E | CTCTL TEST ONLY | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$003F | ARMCOP | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

\$0040 - \$007F**ECT (Enhanced Capture Timer 16 Bit 8 Channels)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0040 | TIOS | Read: | IOS7 | IOS6 | IOS5 | IOS4 | IOS3 | IOS2 | IOS1 | IOS0 |
| | | Write: | | | | | | | | |
| \$0041 | CFORC | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | FOC7 | FOC6 | FOC5 | FOC4 | FOC3 | FOC2 | FOC1 | FOC0 |
| \$0042 | OC7M | Read: | OC7M7 | OC7M6 | OC7M5 | OC7M4 | OC7M3 | OC7M2 | OC7M1 | OC7M0 |
| | | Write: | | | | | | | | |
| \$0043 | OC7D | Read: | OC7D7 | OC7D6 | OC7D5 | OC7D4 | OC7D3 | OC7D2 | OC7D1 | OC7D0 |
| | | Write: | | | | | | | | |
| \$0044 | TCNT (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0045 | TCNT (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0046 | TSCR1 | Read: | TEN | TSWAI | TSFRZ | TFFCA | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0047 | TTOV | Read: | TOV7 | TOV6 | TOV5 | TOV4 | TOV3 | TOV2 | TOV1 | TOV0 |
| | | Write: | | | | | | | | |
| \$0048 | TCTL1 | Read: | OM7 | OL7 | OM6 | OL6 | OM5 | OL5 | OM4 | OL4 |
| | | Write: | | | | | | | | |
| \$0049 | TCTL2 | Read: | OM3 | OL3 | OM2 | OL2 | OM1 | OL1 | OM0 | OL0 |
| | | Write: | | | | | | | | |

\$0040 - \$007F

ECT (Enhanced Capture Timer 16 Bit 8 Channels)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$004A | TCTL3 | Read: | EDG7B | EDG7A | EDG6B | EDG6A | EDG5B | EDG5A | EDG4B | EDG4A |
| | | Write: | | | | | | | | |
| \$004B | TCTL4 | Read: | EDG3B | EDG3A | EDG2B | EDG2A | EDG1B | EDG1A | EDG0B | EDG0A |
| | | Write: | | | | | | | | |
| \$004C | TIE | Read: | C7I | C6I | C5I | C4I | C3I | C2I | C1I | C0I |
| | | Write: | | | | | | | | |
| \$004D | TSCR2 | Read: | TOI | 0 | 0 | 0 | TCRE | PR2 | PR1 | PR0 |
| | | Write: | | | | | | | | |
| \$004E | TFLG1 | Read: | C7F | C6F | C5F | C4F | C3F | C2F | C1F | C0F |
| | | Write: | | | | | | | | |
| \$004F | TFLG2 | Read: | TOF | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0050 | TC0 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0051 | TC0 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0052 | TC1 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0053 | TC1 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0054 | TC2 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0055 | TC2 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0056 | TC3 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0057 | TC3 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0058 | TC4 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0059 | TC4 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$005A | TC5 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$005B | TC5 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$005C | TC6 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$005D | TC6 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$005E | TC7 (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$005F | TC7 (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0060 | PACTL | Read: | 0 | PAEN | PAMOD | PEDGE | CLK1 | CLK0 | PAOVI | PAI |
| | | Write: | | | | | | | | |
| \$0061 | PAFLG | Read: | 0 | 0 | 0 | 0 | 0 | 0 | PAOVF | PAIF |
| | | Write: | | | | | | | | |
| \$0062 | PACN3 (hi) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

\$0040 - \$007F**ECT (Enhanced Capture Timer 16 Bit 8 Channels)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------|-----------------|--------|-------|-------|------------|-----------|-------|-------|-------|
| \$0063 | PACN2 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0064 | PACN1 (hi) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0065 | PACN0 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0066 | MCCTL | Read: Write: | MCZI | MODMC | RDMCL | 0 ICLAT | 0 FLMC | MCEN | MCPR1 | MCPR0 |
| \$0067 | MCFLG | Read: Write: | MCZF | 0 | 0 | 0 | POLF3 | POLF2 | POLF1 | POLF0 |
| \$0068 | ICPAR | Read: Write: | 0 | 0 | 0 | 0 | PA3EN | PA2EN | PA1EN | PA0EN |
| \$0069 | DLYCT | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | DLY1 | DLY0 |
| \$006A | ICOVW | Read: Write: | NOVW7 | NOVW6 | NOVW5 | NOVW4 | NOVW3 | NOVW2 | NOVW1 | NOVW0 |
| \$006B | ICSYS | Read: Write: | SH37 | SH26 | SH15 | SH04 | TFMOD | PACMX | BUFEN | LATQ |
| \$006C | Reserved | Read: Write: | | | | | | | | |
| \$006D | TIMTST Test Only | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | TCBYP | 0 |
| \$006E | Reserved | Read: Write: | | | | | | | | |
| \$006F | Reserved | Read: Write: | | | | | | | | |
| \$0070 | PBCTL | Read: Write: | 0 | PBEN | 0 | 0 | 0 | 0 | PBOVI | 0 |
| \$0071 | PBFLG | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | PBOVF | 0 |
| \$0072 | PA3H | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0073 | PA2H | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0074 | PA1H | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0075 | PA0H | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0076 | MCCNT (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0077 | MCCNT (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0078 | TC0H (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0079 | TC0H (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$007A | TC1H (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$007B | TC1H (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

\$0040 - \$007F

ECT (Enhanced Capture Timer 16 Bit 8 Channels)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$007C | TC2H (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$007D | TC2H (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$007E | TC3H (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$007F | TC3H (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

\$0080 - \$009F

ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|-------|-------|-------|---------|--------|-------|-------|-------|
| \$0080 | ATD0CTL0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0081 | ATD0CTL1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0082 | ATD0CTL2 | Read: | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | Write: | | | | | | | | |
| \$0083 | ATD0CTL3 | Read: | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | Write: | | | | | | | | |
| \$0084 | ATD0CTL4 | Read: | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | Write: | | | | | | | | |
| \$0085 | ATD0CTL5 | Read: | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | Write: | | | | | | | | |
| \$0086 | ATD0STAT0 | Read: | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | Write: | | | | | | | | |
| \$0087 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0088 | ATD0TEST0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0089 | ATD0TEST1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | Write: | | | | | | | | |
| \$008A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$008B | ATD0STAT1 | Read: | CCF7 | CCF6 | CCF5 | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
| | | Write: | | | | | | | | |
| \$008C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$008D | ATD0DIEN | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$008E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$008F | PORTAD0 | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
| | | Write: | | | | | | | | |
| \$0090 | ATD0DR0H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0091 | ATD0DR0L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0080 - \$009F**ATD0 (Analog to Digital Converter 10 Bit 8 Channel)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0092 | ATD0DR1H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0093 | ATD0DR1L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0094 | ATD0DR2H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0095 | ATD0DR2L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0096 | ATD0DR3H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0097 | ATD0DR3L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0098 | ATD0DR4H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0099 | ATD0DR4L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009A | ATD0DR5H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009B | ATD0DR5L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009C | ATD0DR6H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009D | ATD0DR6L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009E | ATD0DR7H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009F | ATD0DR7L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00A0 - \$00C7**PWM (Pulse Width Modulator 8 Bit 8 Channel)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00A0 | PWME | Read: | PWME7 | PWME6 | PWME5 | PWME4 | PWME3 | PWME2 | PWME1 | PWME0 |
| | | Write: | | | | | | | | |
| \$00A1 | PWMPOL | Read: | PPOL7 | PPOL6 | PPOL5 | PPOL4 | PPOL3 | PPOL2 | PPOL1 | PPOL0 |
| | | Write: | | | | | | | | |
| \$00A2 | PWMCLK | Read: | PCLK7 | PCLK6 | PCLK5 | PCLK4 | PCLK3 | PCLK2 | PCLK1 | PCLK0 |
| | | Write: | | | | | | | | |
| \$00A3 | PWMPRCLK | Read: | 0 | PCKB2 | PCKB1 | PCKB0 | 0 | PCKA2 | PCKA1 | PCKA0 |
| | | Write: | | | | | | | | |
| \$00A4 | PWMCAE | Read: | CAE7 | CAE6 | CAE5 | CAE4 | CAE3 | CAE2 | CAE1 | CAE0 |
| | | Write: | | | | | | | | |
| \$00A5 | PWMCTL | Read: | CON67 | CON45 | CON23 | CON01 | PSWAI | PFRZ | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00A6 | PWMTST Test Only | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00A7 | PWMPRSC Test Only | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00A8 | PWMSCLA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

\$00A0 - \$00C7

PWM (Pulse Width Modulator 8 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00A9 | PWMSCLB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00AA | PWMSCNTA Test Only | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00AB | PWMSCNTB Test Only | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00AC | PWMCNT0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00AD | PWMCNT1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00AE | PWMCNT2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00AF | PWMCNT3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00B0 | PWMCNT4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00B1 | PWMCNT5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00B2 | PWMCNT6 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00B3 | PWMCNT7 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00B4 | PWMPER0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00B5 | PWMPER1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00B6 | PWMPER2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00B7 | PWMPER3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00B8 | PWMPER4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00B9 | PWMPER5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BA | PWMPER6 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BB | PWMPER7 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BC | PWMDTY0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BD | PWMDTY1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BE | PWMDTY2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00BF | PWMDTY3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00C0 | PWMDTY4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00C1 | PWMDTY5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

\$00A0 - \$00C7**PWM (Pulse Width Modulator 8 Bit 8 Channel)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|----------|--------|-------|--------|---------|---------|
| \$00C2 | PWMPTY6 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00C3 | PWMPTY7 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00C4 | PWMSDN | Read: | PWMIF | PWMIE | PWMRSTRT | PWMLVL | 0 | PWM7IN | PWM7INL | PWM7ENA |
| | | Write: | | | | | | | | |
| \$00C5 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00C6 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00C7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00C8 - \$00CF**SCI0 (Asynchronous Serial Interface)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|--------|-------|---------|-------|-------|-------|-------|-------|-------|
| \$00C8 | SCI0BDH | Read: | 0 | 0 | 0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | | Write: | | | | | | | | |
| \$00C9 | SCI0BDL | Read: | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | | Write: | | | | | | | | |
| \$00CA | SCI0CR1 | Read: | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | | Write: | | | | | | | | |
| \$00CB | SCI0CR2 | Read: | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| | | Write: | | | | | | | | |
| \$00CC | SCI0SR1 | Read: | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| | | Write: | | | | | | | | |
| \$00CD | SCI0SR2 | Read: | 0 | 0 | 0 | 0 | 0 | BRK13 | TXDIR | RAF |
| | | Write: | | | | | | | | |
| \$00CE | SCI0DRH | Read: | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00CF | SCI0DRL | Read: | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

\$00D0 - \$00D7**SCI1 (Asynchronous Serial Interface)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|--------|-------|---------|-------|-------|-------|-------|-------|-------|
| \$00D0 | SCI1BDH | Read: | 0 | 0 | 0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | | Write: | | | | | | | | |
| \$00D1 | SCI1BDL | Read: | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | | Write: | | | | | | | | |
| \$00D2 | SCI1CR1 | Read: | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | | Write: | | | | | | | | |
| \$00D3 | SCI1CR2 | Read: | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| | | Write: | | | | | | | | |
| \$00D4 | SCI1SR1 | Read: | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| | | Write: | | | | | | | | |

\$00D0 - \$00D7

SCI1 (Asynchronous Serial Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00D5 | SCI1SR2 | Read: | 0 | 0 | 0 | 0 | 0 | BRK13 | TXDIR | RAF |
| | | Write: | | | | | | | | |
| \$00D6 | SCI1DRH | Read: | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00D7 | SCI1DRL | Read: | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

\$00D8 - \$00DF

SPI0 (Serial Peripheral Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|--------|---------|-------|---------|-------|
| \$00D8 | SPI0CR1 | Read: | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| | | Write: | | | | | | | | |
| \$00D9 | SPI0CR2 | Read: | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| | | Write: | | | | | | | | |
| \$00DA | SPI0BR | Read: | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| | | Write: | | | | | | | | |
| \$00DB | SPI0SR | Read: | SPIF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DC | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DD | SPI0DR | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
| | | Write: | | | | | | | | |
| \$00DE | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00E0 - \$00E7

IIC (Inter IC Bus)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|---------------------|---------------------|-------|-------|-------|--------|
| \$00E0 | IBAD | Read: | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | 0 |
| | | Write: | | | | | | | | |
| \$00E1 | IBFD | Read: | IBC7 | IBC6 | IBC5 | IBC4 | IBC3 | IBC2 | IBC1 | IBC0 |
| | | Write: | | | | | | | | |
| \$00E2 | IBCR | Read: | IBEN | IBIE | MS/ \overline{SL} | TX/ \overline{RX} | TXAK | 0 | 0 | IBSWAI |
| | | Write: | | | | | | RSTA | | |
| \$00E3 | IBSR | Read: | TCF | IAAS | IBB | IBAL | 0 | SRW | IBIF | RXAK |
| | | Write: | | | | | | | | |
| \$00E4 | IBDR | Read: | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | Write: | | | | | | | | |
| \$00E5 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00E6 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00E7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00E8 - \$00EF

BDLC (Byte Level Data Link Controller J1850)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|--------|--------|
| \$00E8 | DLCBCR1 | Read: | IMSG | CLKS | 0 | 0 | 0 | 0 | IE | WCM |
| | | Write: | | | | | | | | |
| \$00E9 | DLCBSVR | Read: | 0 | 0 | I3 | I2 | I1 | I0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00EA | DLCBCR2 | Read: | SMRST | DLOOP | RX4XE | NBFS | TEOD | TSIFR | TMIFR1 | TMIFR0 |
| | | Write: | | | | | | | | |
| \$00EB | DLCBDR | Read: | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | Write: | | | | | | | | |
| \$00EC | DLCBARD | Read: | 0 | RXPOL | 0 | 0 | BO3 | BO2 | BO1 | BO0 |
| | | Write: | | | | | | | | |
| \$00ED | DLCBRSR | Read: | 0 | 0 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | | | | | | | | |
| \$00EE | DLCSCR | Read: | 0 | 0 | 0 | BDLCE | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00EF | DLCBSTAT | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IDLE |
| | | Write: | | | | | | | | |

\$00F0 - \$00F7

SPI1 (Serial Peripheral Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|--------|---------|-------|---------|-------|
| \$00F0 | SPI1CR1 | Read: | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| | | Write: | | | | | | | | |
| \$00F1 | SPI1CR2 | Read: | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| | | Write: | | | | | | | | |
| \$00F2 | SPI1BR | Read: | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| | | Write: | | | | | | | | |
| \$00F3 | SPI1SR | Read: | SPIF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00F4 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00F5 | SPI1DR | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
| | | Write: | | | | | | | | |
| \$00F6 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00F7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00F8 - \$00FF

Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00F8 - \$00FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0100 - \$010F

Flash Control Register (fts128k2)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------------|------------------------------|--------|--------|--------|--------|--------|-------|--------|--------|--------|
| \$0100 | FCLKDIV | Read: | FDIVLD | PRDIV8 | FDIV5 | FDIV4 | FDIV3 | FDIV2 | FDIV1 | FDIV0 |
| | | Write: | | | | | | | | |
| \$0101 | FSEC | Read: | KEYEN1 | KEYEN0 | NV5 | NV4 | NV3 | NV2 | SEC1 | SEC0 |
| | | Write: | | | | | | | | |
| \$0102 | FTSTMOD | Read: | 0 | 0 | 0 | WRALL | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0103 | FCNFG | Read: | CBEIE | CCIE | KEYACC | 0 | 0 | 0 | BKSEL1 | BKSEL0 |
| | | Write: | | | | | | | | |
| \$0104 | FPROT | Read: | FPOPEN | NV6 | FPHDIS | FPHS1 | FPHS0 | FPLDIS | FPLS1 | FPLS0 |
| | | Write: | | | | | | | | |
| \$0105 | FSTAT | Read: | CBEIF | CCIF | PVIOL | ACCERR | 0 | BLANK | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0106 | FCMD | Read: | 0 | CMDB6 | CMDB5 | 0 | 0 | CMDB2 | 0 | CMDB0 |
| | | Write: | | | | | | | | |
| \$0107 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0108 | FADDRHI | Read: | 0 | Bit 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0109 | FADDRLO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$010A | FDATAHI | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$010B | FDATALO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$010C - \$010F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0110 - \$011B

EEPROM Control Register (eets2k)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------------------|--------|--------|--------|-------|--------|-------|-------|-------|-------|
| \$0110 | ECLKDIV | Read: | EDIVLD | PRDIV8 | EDIV5 | EDIV4 | EDIV3 | EDIV2 | EDIV1 | EDIV0 |
| | | Write: | | | | | | | | |
| \$0111 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0112 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0113 | ECNFG | Read: | CBEIE | CCIE | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0114 | EPROT | Read: | EPOPEN | NV6 | NV5 | NV4 | EPDIS | EP2 | EP1 | EP0 |
| | | Write: | | | | | | | | |
| \$0115 | ESTAT | Read: | CBEIF | CCIF | PVIOL | ACCERR | 0 | BLANK | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0116 | ECMD | Read: | 0 | CMDB6 | CMDB5 | 0 | 0 | CMDB2 | 0 | CMDB0 |
| | | Write: | | | | | | | | |
| \$0117 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0118 | EADDRHI | Read: | 0 | 0 | 0 | 0 | 0 | 0 | Bit 9 | Bit 8 |
| | | Write: | | | | | | | | |

\$0110 - \$011B

EEPROM Control Register (eets2k)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0119 | EADDRLO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$011A | EDATAHI | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$011B | EDATALO | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

\$011C - \$011F

Reserved for RAM Control Register

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$011C - \$011F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0120 - \$013F

ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | Read: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|-------|-------|-------|---------|--------|-------|-------|-------|
| \$0120 | ATD1CTL0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0121 | ATD1CTL1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0122 | ATD1CTL2 | Read: | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | Write: | | | | | | | | |
| \$0123 | ATD1CTL3 | Read: | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | Write: | | | | | | | | |
| \$0124 | ATD1CTL4 | Read: | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | Write: | | | | | | | | |
| \$0125 | ATD1CTL5 | Read: | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | Write: | | | | | | | | |
| \$0126 | ATD1STAT0 | Read: | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | Write: | | | | | | | | |
| \$0127 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0128 | ATD1TEST0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0129 | ATD1TEST1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | Write: | | | | | | | | |
| \$012A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$012B | ATD1STAT1 | Read: | CCF7 | CCF6 | CCF5 | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
| | | Write: | | | | | | | | |
| \$012C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$012D | ATD1DIEN | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$012E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$012F | PORTAD1 | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
| | | Write: | | | | | | | | |

\$0120 - \$013F

ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0130 | ATD1DR0H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0131 | ATD1DR0L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0132 | ATD1DR1H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0133 | ATD1DR1L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0134 | ATD1DR2H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0135 | ATD1DR2L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0136 | ATD1DR3H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0137 | ATD1DR3L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0138 | ATD1DR4H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0139 | ATD1DR4L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$013A | ATD1DR5H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$013B | ATD1DR5L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$013C | ATD1DR6H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$013D | ATD1DR6L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$013E | ATD1DR7H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$013F | ATD1DR7L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0140 - \$017F

CAN0 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|--------|---------|---------|---------|---------|--------|--------|
| \$0140 | CANOCTL0 | Read: | RXFRM | RXACT | CSWAI | SYNCH | TIME | WUPE | SLPRQ | INITRQ |
| | | Write: | | | | | | | | |
| \$0141 | CANOCTL1 | Read: | CANE | CLKSRC | LOOPB | LISTEN | 0 | WUPM | SLPAK | INITAK |
| | | Write: | | | | | | | | |
| \$0142 | CAN0BTR0 | Read: | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| | | Write: | | | | | | | | |
| \$0143 | CAN0BTR1 | Read: | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| | | Write: | | | | | | | | |
| \$0144 | CAN0RFLG | Read: | WUPIF | CSCIF | RSTAT1 | RSTAT0 | TSTAT1 | TSTAT0 | OVRIF | RXF |
| | | Write: | | | | | | | | |
| \$0145 | CAN0RIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |

\$0140 - \$017F

CAN0 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|-----------------------|--------|--|--------|--------|--------|--------|--------|--------|--------|
| \$0146 | CAN0TFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| \$0147 | CAN0TIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| \$0148 | CAN0TARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| \$0149 | CAN0TAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| \$014A | CAN0TBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| \$014B | CAN0IDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| \$014C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$014D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$014E | CAN0RXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| \$014F | CAN0TXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| \$0150 - \$0153 | CAN0IDAR0 - CAN0IDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$0154 - \$0157 | CAN0IDMR0 - CAN0IDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0158 - \$015B | CAN0IDAR4 - CAN0IDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$015C - \$015F | CAN0IDMR4 - CAN0IDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0160 - \$016F | CAN0RXFG | Read: | FOREGROUND RECEIVE BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |
| \$0170 - \$017F | CAN0TXFG | Read: | FOREGROUND TRANSMIT BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-----------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$xxx0 | Extended ID | Read: | ID28 | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 |
| | Standard ID | Read: | ID10 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 |
| | CANxRIDR0 | Write: | | | | | | | | |
| \$xxx1 | Extended ID | Read: | ID20 | ID19 | ID18 | SRR=1 | IDE=1 | ID17 | ID16 | ID15 |
| | Standard ID | Read: | ID2 | ID1 | ID0 | RTR | IDE=0 | | | |
| | CANxRIDR1 | Write: | | | | | | | | |
| \$xxx2 | Extended ID | Read: | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 | ID7 |
| | Standard ID | Read: | | | | | | | | |
| | CANxRIDR2 | Write: | | | | | | | | |
| \$xxx3 | Extended ID | Read: | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | RTR |
| | Standard ID | Read: | | | | | | | | |
| | CANxRIDR3 | Write: | | | | | | | | |
| \$xxx4- \$xxxB | CANxRDSR0 - CANxRDSR7 | Read: | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | Write: | | | | | | | | |

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|--------------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$xxxC | CANRxDLR | Read: | | | | | DLC3 | DLC2 | DLC1 | DLC0 |
| | | Write: | | | | | | | | |
| \$xxxD | Reserved | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xxxE | CANxRTSRH | Read: | TSR15 | TSR14 | TSR13 | TSR12 | TSR11 | TSR10 | TSR9 | TSR8 |
| | | Write: | | | | | | | | |
| \$xxxF | CANxRTSRL | Read: | TSR7 | TSR6 | TSR5 | TSR4 | TSR3 | TSR2 | TSR1 | TSR0 |
| | | Write: | | | | | | | | |
| \$xx10 | Extended ID CANxTIDR0 | Read: | ID28 | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 |
| | | Write: | | | | | | | | |
| \$xx10 | Standard ID | Read: | ID10 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 |
| | | Write: | | | | | | | | |
| \$xx11 | Extended ID CANxTIDR1 | Read: | ID20 | ID19 | ID18 | SRR=1 | IDE=1 | ID17 | ID16 | ID15 |
| | | Write: | | | | | | | | |
| \$xx11 | Standard ID | Read: | ID2 | ID1 | ID0 | RTR | IDE=0 | | | |
| | | Write: | | | | | | | | |
| \$xx12 | Extended ID CANxTIDR2 | Read: | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 | ID7 |
| | | Write: | | | | | | | | |
| \$xx12 | Standard ID | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xx13 | Extended ID CANxTIDR3 | Read: | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | RTR |
| | | Write: | | | | | | | | |
| \$xx13 | Standard ID | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xx14- \$xx1B | CANxTDSR0 - CANxTDSR7 | Read: | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | Write: | | | | | | | | |
| \$xx1C | CANxTDLR | Read: | | | | | DLC3 | DLC2 | DLC1 | DLC0 |
| | | Write: | | | | | | | | |
| \$xx1D | CONxTTBPR | Read: | PRI07 | PRI06 | PRI05 | PRI04 | PRI03 | PRI02 | PRI01 | PRI00 |
| | | Write: | | | | | | | | |
| \$xx1E | CANxTTSRH | Read: | TSR15 | TSR14 | TSR13 | TSR12 | TSR11 | TSR10 | TSR9 | TSR8 |
| | | Write: | | | | | | | | |
| \$xx1F | CANxTTSRL | Read: | TSR7 | TSR6 | TSR5 | TSR4 | TSR3 | TSR2 | TSR1 | TSR0 |
| | | Write: | | | | | | | | |

\$0180 - \$01BF

CAN1 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|--------|--------|--------|--------|--------|--------|--------|
| \$0180 | CAN1CTL0 | Read: | RXFRM | RXACT | CSWAI | SYNCH | TIME | WUPE | SLPRQ | INITRQ |
| | | Write: | | | | | | | | |
| \$0181 | CAN1CTL1 | Read: | CANE | CLKSRC | LOOPB | LISTEN | 0 | WUPM | SLPAK | INITAK |
| | | Write: | | | | | | | | |
| \$0182 | CAN1BTR0 | Read: | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| | | Write: | | | | | | | | |
| \$0183 | CAN1BTR1 | Read: | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| | | Write: | | | | | | | | |
| \$0184 | CAN1RFLG | Read: | WUPIF | CSCIF | RSTAT1 | RSTAT0 | TSTAT1 | TSTAT0 | OVRIF | RXF |
| | | Write: | | | | | | | | |

\$0180 - \$01BF**CAN1 (Motorola Scalable CAN - MSCAN)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|-----------------------|--------|--|--------|---------|---------|---------|---------|--------|--------|
| \$0185 | CAN1RIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |
| \$0186 | CAN1TFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| \$0187 | CAN1TIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| \$0188 | CAN1TARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| \$0189 | CAN1TAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| \$018A | CAN1TBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| \$018B | CAN1IDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| \$018C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$018D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$018E | CAN1RXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| \$018F | CAN1TXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| \$0190 - \$0193 | CAN1IDAR0 - CAN1IDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$0194 - \$0197 | CAN1IDMR0 - CAN1IDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0198 - \$019B | CAN1IDAR4 - CAN1IDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$019C - \$019F | CAN1IDMR4 - CAN1IDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$01A0 - \$01AF | CAN0RXFG | Read: | FOREGROUND RECEIVE BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |
| \$01B0 - \$01BF | CAN0TXFG | Read: | FOREGROUND TRANSMIT BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |

\$01C0 - \$01FF**Reserved**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$01C0 - \$01FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0200 - \$023F**Reserved**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$020C - \$023F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0240 - \$027F

PIM (Port Integration Module)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|--------|--------|--------|--------|--------|--------|
| \$0240 | PTT | Read: | PTT7 | PTT6 | PTT5 | PTT4 | PTT3 | PTT2 | PTT1 | PTT0 |
| | | Write: | | | | | | | | |
| \$0241 | PTIT | Read: | PTIT7 | PTIT6 | PTIT5 | PTIT4 | PTIT3 | PTIT2 | PTIT1 | PTIT0 |
| | | Write: | | | | | | | | |
| \$0242 | DDRT | Read: | DDRT7 | DDRT6 | DDRT5 | DDRT4 | DDRT3 | DDRT2 | DDRT1 | DDRT0 |
| | | Write: | | | | | | | | |
| \$0243 | RDRT | Read: | RDRT7 | RDRT6 | RDRT5 | RDRT4 | RDRT3 | RDRT2 | RDRT1 | RDRT0 |
| | | Write: | | | | | | | | |
| \$0244 | PERT | Read: | PERT7 | PERT6 | PERT5 | PERT4 | PERT3 | PERT2 | PERT1 | PERT0 |
| | | Write: | | | | | | | | |
| \$0245 | PPST | Read: | PPST7 | PPST6 | PPST5 | PPST4 | PPST3 | PPST2 | PPST1 | PPST0 |
| | | Write: | | | | | | | | |
| \$0246 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0247 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0248 | PTS | Read: | PTS7 | PTS6 | PTS5 | PTS4 | PTS3 | PTS2 | PTS1 | PTS0 |
| | | Write: | | | | | | | | |
| \$0249 | PTIS | Read: | PTIS7 | PTIS6 | PTIS5 | PTIS4 | PTIS3 | PTIS2 | PTIS1 | PTIS0 |
| | | Write: | | | | | | | | |
| \$024A | DDRS | Read: | DDRS7 | DDRS6 | DDRS5 | DDRS4 | DDRS3 | DDRS2 | DDRS1 | DDRS0 |
| | | Write: | | | | | | | | |
| \$024B | RDRS | Read: | RDRS7 | RDRS6 | RDRS5 | RDRS4 | RDRS3 | RDRS2 | RDRS1 | RDRS0 |
| | | Write: | | | | | | | | |
| \$024C | PERS | Read: | PERS7 | PERS6 | PERS5 | PERS4 | PERS3 | PERS2 | PERS1 | PERS0 |
| | | Write: | | | | | | | | |
| \$024D | PPSS | Read: | PPSS7 | PPSS6 | PPSS5 | PPSS4 | PPSS3 | PPSS2 | PPSS1 | PPSS0 |
| | | Write: | | | | | | | | |
| \$024E | WOMS | Read: | WOMS7 | WOMS6 | WOMS5 | WOMS4 | WOMS3 | WOMS2 | WOMS1 | WOMS0 |
| | | Write: | | | | | | | | |
| \$024F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0250 | PTM | Read: | PTM7 | PTM6 | PTM5 | PTM4 | PTM3 | PTM2 | PTM1 | PTM0 |
| | | Write: | | | | | | | | |
| \$0251 | PTIM | Read: | PTIM7 | PTIM6 | PTIM5 | PTIM4 | PTIM3 | PTIM2 | PTIM1 | PTIM0 |
| | | Write: | | | | | | | | |
| \$0252 | DDRM | Read: | DDRM7 | DDRM6 | DDRM5 | DDRM4 | DDRM3 | DDRM2 | DDRM1 | DDRM0 |
| | | Write: | | | | | | | | |
| \$0253 | RDRM | Read: | RDRM7 | RDRM6 | RDRM5 | RDRM4 | RDRM3 | RDRM2 | RDRM1 | RDRM0 |
| | | Write: | | | | | | | | |
| \$0254 | PERM | Read: | PERM7 | PERM6 | PERM5 | PERM4 | PERM3 | PERM2 | PERM1 | PERM0 |
| | | Write: | | | | | | | | |
| \$0255 | PPSM | Read: | PPSM7 | PPSM6 | PPSM5 | PPSM4 | PPSM3 | PPSM2 | PPSM1 | PPSM0 |
| | | Write: | | | | | | | | |
| \$0256 | WOMM | Read: | WOMM7 | WOMM6 | WOMM5 | WOMM4 | WOMM3 | WOMM2 | WOMM1 | WOMM0 |
| | | Write: | | | | | | | | |
| \$0257 | MODRR | Read: | 0 | 0 | MODRR5 | MODRR4 | MODRR3 | MODRR2 | MODRR1 | MODRR0 |
| | | Write: | | | | | | | | |
| \$0258 | PTP | Read: | PTP7 | PTP6 | PTP5 | PTP4 | PTP3 | PTP2 | PTP1 | PTP0 |
| | | Write: | | | | | | | | |

\$0240 - \$027F**PIM (Port Integration Module)**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0259 | PTIP | Read: | PTIP7 | PTIP6 | PTIP5 | PTIP4 | PTIP3 | PTIP2 | PTIP1 | PTIP0 |
| | | Write: | | | | | | | | |
| \$025A | DDRP | Read: | DDRP7 | DDRP6 | DDRP5 | DDRP4 | DDRP3 | DDRP2 | DDRP1 | DDRP0 |
| | | Write: | | | | | | | | |
| \$025B | RDRP | Read: | RDRP7 | RDRP6 | RDRP5 | RDRP4 | RDRP3 | RDRP2 | RDRP1 | RDRP0 |
| | | Write: | | | | | | | | |
| \$025C | PERP | Read: | PERP7 | PERP6 | PERP5 | PERP4 | PERP3 | PERP2 | PERP1 | PERP0 |
| | | Write: | | | | | | | | |
| \$025D | PPSP | Read: | PPSP7 | PPSP6 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSS0 |
| | | Write: | | | | | | | | |
| \$025E | PIEP | Read: | PIEP7 | PIEP6 | PIEP5 | PIEP4 | PIEP3 | PIEP2 | PIEP1 | PIEP0 |
| | | Write: | | | | | | | | |
| \$025F | PIFP | Read: | PIFP7 | PIFP6 | PIFP5 | PIFP4 | PIFP3 | PIFP2 | PIFP1 | PIFP0 |
| | | Write: | | | | | | | | |
| \$0260 | PTH | Read: | PTH7 | PTH6 | PTH5 | PTH4 | PTH3 | PTH2 | PTH1 | PTH0 |
| | | Write: | | | | | | | | |
| \$0261 | PTIH | Read: | PTIH7 | PTIH6 | PTIH5 | PTIH4 | PTIH3 | PTIH2 | PTIH1 | PTIH0 |
| | | Write: | | | | | | | | |
| \$0262 | DDRH | Read: | DDRH7 | DDRH6 | DDRH5 | DDRH4 | DDRH3 | DDRH2 | DDRH1 | DDRH0 |
| | | Write: | | | | | | | | |
| \$0263 | RDRH | Read: | RDRH7 | RDRH6 | RDRH5 | RDRH4 | RDRH3 | RDRH2 | RDRH1 | RDRH0 |
| | | Write: | | | | | | | | |
| \$0264 | PERH | Read: | PERH7 | PERH6 | PERH5 | PERH4 | PERH3 | PERH2 | PERH1 | PERH0 |
| | | Write: | | | | | | | | |
| \$0265 | PPSH | Read: | PPSH7 | PPSH6 | PPSH5 | PPSH4 | PPSH3 | PPSH2 | PPSH1 | PPSH0 |
| | | Write: | | | | | | | | |
| \$0266 | PIEH | Read: | PIEH7 | PIEH6 | PIEH5 | PIEH4 | PIEH3 | PIEH2 | PIEH1 | PIEH0 |
| | | Write: | | | | | | | | |
| \$0267 | PIFH | Read: | PIFH7 | PIFH6 | PIFH5 | PIFH4 | PIFH3 | PIFH2 | PIFH1 | PIFH0 |
| | | Write: | | | | | | | | |
| \$0268 | PTJ | Read: | PTJ7 | PTJ6 | 0 | 0 | 0 | 0 | PTJ1 | PTJ0 |
| | | Write: | | | | | | | | |
| \$0269 | PTIJ | Read: | PTIJ7 | PTIJ6 | 0 | 0 | 0 | 0 | PTIJ1 | PTIJ0 |
| | | Write: | | | | | | | | |
| \$026A | DDRJ | Read: | DDRJ7 | DDRJ6 | 0 | 0 | 0 | 0 | DDRJ1 | DDRJ0 |
| | | Write: | | | | | | | | |
| \$026B | RDRJ | Read: | RDRJ7 | RDRJ6 | 0 | 0 | 0 | 0 | RDRJ1 | RDRJ0 |
| | | Write: | | | | | | | | |
| \$026C | PERJ | Read: | PERJ7 | PERJ6 | 0 | 0 | 0 | 0 | PERJ1 | PERJ0 |
| | | Write: | | | | | | | | |
| \$026D | PPSJ | Read: | PPSJ7 | PPSJ6 | 0 | 0 | 0 | 0 | PPSJ1 | PPSJ0 |
| | | Write: | | | | | | | | |
| \$026E | PIEJ | Read: | PIEJ7 | PIEJ6 | 0 | 0 | 0 | 0 | PIEJ1 | PIEJ0 |
| | | Write: | | | | | | | | |
| \$026F | PIFJ | Read: | PIFJ7 | PIFJ6 | 0 | 0 | 0 | 0 | PIFJ1 | PIFJ0 |
| | | Write: | | | | | | | | |
| \$0270 - \$027F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0280 - \$02BF

CAN4 (Motorola Scalable CAN - MSCAN)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|-----------------------|--------|--|--------|---------|---------|---------|---------|--------|--------|
| \$0280 | CAN4CTL0 | Read: | RXFRM | RXACT | CSWAI | SYNCH | TIME | WUPE | SLPRQ | INITRQ |
| | | Write: | | | | | | | | |
| \$0281 | CAN4CTL1 | Read: | CANE | CLKSRC | LOOPB | LISTEN | 0 | WUPM | SLPAK | INITAK |
| | | Write: | | | | | | | | |
| \$0282 | CAN4BTR0 | Read: | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| | | Write: | | | | | | | | |
| \$0283 | CAN4BTR1 | Read: | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| | | Write: | | | | | | | | |
| \$0284 | CAN4RFLG | Read: | WUPIF | CSCIF | RSTAT1 | RSTAT0 | TSTAT1 | TSTAT0 | OVRIF | RXF |
| | | Write: | | | | | | | | |
| \$0285 | CAN4RIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |
| \$0286 | CAN4TFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| \$0287 | CAN4TIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| \$0288 | CAN4TARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| \$0289 | CAN4TAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| \$028A | CAN4TBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| \$028B | CAN4IDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| \$028C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$028D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$028E | CAN4RXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| \$028F | CAN4TXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| \$0290 - \$0293 | CAN0IDAR0 - CAN0IDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$0294 - \$0297 | CAN0IDMR0 - CAN0IDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0298 - \$029B | CAN0IDAR4 - CAN0IDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$029C - \$029F | CAN0IDMR4 - CAN0IDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$02A0 - \$02AF | CAN4RXFG | Read: | FOREGROUND RECEIVE BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |
| \$02B0 - \$02BF | CAN4TXFG | Read: | FOREGROUND TRANSMIT BUFFER see (Table 1-2) | | | | | | | |
| | | Write: | | | | | | | | |

\$02C0 - \$02FF

Reserved

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$02C0 - \$02FF | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | |

\$0300 - \$035F

Byteflight

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------------|--------------|--------------|--------------|--------------|--------------|---------------------|---------------------|
| \$0300 | BFMCR | Read: INITRQ | Read: MASTER | Read: ALARM | Read: SLPK | Read: SLPRQ | Read: WPULSE | Read: SSWAI | Read: INITAK |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0301 | BFFSIZR | Read: 0 | Read: 0 | Read: 0 | Read: FSIZ4 | Read: FSIZ3 | Read: FSIZ2 | Read: FSIZ1 | Read: FSIZ0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0302 | BFTCR1 | Read: TWX0T7 | Read: TWX0T6 | Read: TWX0T5 | Read: TWX0T4 | Read: TWX0T3 | Read: TWX0T2 | Read: TWX0T1 | Read: TWX0T0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0303 | BFTCR2 | Read: TWX0R7 | Read: TWX0R6 | Read: TWX0R5 | Read: TWX0R4 | Read: TWX0R3 | Read: TWX0R2 | Read: TWX0R1 | Read: TWX0R0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0304 | BFTCR3 | Read: TWX0D7 | Read: TWX0D6 | Read: TWX0D5 | Read: TWX0D4 | Read: TWX0D3 | Read: TWX0D2 | Read: TWX0D1 | Read: TWX0D0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0305 | Reserved | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0306 | BFRISR | Read: RCVFIF | Read: RXIF | Read: SYNAIF | Read: SYNIF | Read: SLMMIF | Read: 0 | Read: XSYNIF | Read: OPTDF |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0307 | BFGISR | Read: TXIF | Read: OVRNIF | Read: ERRIF | Read: SYNEIF | Read: SYNLIF | Read: ILLPIF | Read: LOCKIF | Read: WAKEIF |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0308 | BFRIER | Read: RCVFIE | Read: RXIE | Read: SYNAIE | Read: SYNIE | Read: SLMMIE | Read: 0 | Read: XSYNIE | Read: 0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0309 | BFGIER | Read: TXIE | Read: OVRNIE | Read: ERRIE | Read: SYNEIE | Read: SYNLIE | Read: ILLPIE | Read: LOCKIE | Read: WAKEIE |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030A | BFRIVEC | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: RIVEC3 | Read: RIVEC2 | Read: RIVEC1 | Read: RIVEC0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030B | BFTIVEC | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: TIVEC3 | Read: TIVEC2 | Read: TIVEC1 | Read: TIVEC0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030C | BFFIDAC | Read: FIDAC7 | Read: FIDAC6 | Read: FIDAC5 | Read: FIDAC4 | Read: FIDAC3 | Read: FIDAC2 | Read: FIDAC1 | Read: FIDAC0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030D | BFFIDMR | Read: FIDMR7 | Read: FIDMR6 | Read: FIDMR5 | Read: FIDMR4 | Read: FIDMR3 | Read: FIDMR2 | Read: FIDMR1 | Read: FIDMR0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030E | BFMVR | Read: MVR7 | Read: MVR6 | Read: MVR5 | Read: MVR4 | Read: MVR3 | Read: MVR2 | Read: MVR1 | Read: MVR0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$030F | Reserved | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0310 | BFPCTLBF | Read: PMEREN | Read: 0 | Read: PSLMEN | Read: PERREN | Read: PROKEN | Read: PSYNEN | Read: 0 | Read: BFEN |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0311 | Reserved | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0312 | BFBUFLOCK | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: TXBUFL OCK | Read: RXBUFL OCK |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0313 | Reserved | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 | Read: 0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |
| \$0314 | BFFIDRJ | Read: FIDRJ7 | Read: FIDRJ6 | Read: FIDRJ5 | Read: FIDRJ4 | Read: FIDRJ3 | Read: FIDRJ2 | Read: FIDRJ1 | Read: FIDRJ0 |
| | | Write: | Write: | Write: | Write: | Write: | Write: | Write: | Write: |

\$0300 - \$035F

Byteflight

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|---------------------------|--------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| \$0315 | BFFIDRMR | Read: | FIDRMR 7 | FIDRMR 6 | FIDRMR 5 | FIDRMR 5 | FIDRMR 4 | FIDRMR 3 | FIDRMR 2 | FIDRMR 1 |
| | | Write: | | | | | | | | |
| \$0316 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0317 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0318 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0319 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031B | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$031F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0320 | BFTIDENT | Read: | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| | | Write: | | | | | | | | |
| \$0321 | BFTLEN | Read: | | | | | LEN3 | LEN2 | LEN1 | LEN0 |
| | | Write: | | | | | | | | |
| \$0322 - \$032D | BFTDATA0- BFTDATA11 | Read: | DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |
| | | Write: | | | | | | | | |
| \$032E - \$032F | Reserved | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$0330 | BFRIDENT | Read: | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| | | Write: | | | | | | | | |
| \$0331 | BFRLEN | Read: | | | | | LEN3 | LEN2 | LEN1 | LEN0 |
| | | Write: | | | | | | | | |
| \$0332 - \$033D | BFRDATA0- BFRDATA11 | Read: | DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA 0 |
| | | Write: | | | | | | | | |
| \$033E- \$033F | Reserved | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$0340 | BFFIDENT | Read: | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| | | Write: | | | | | | | | |
| \$0341 | BFFLEN | Read: | | | | | LEN3 | LEN2 | LEN1 | LEN0 |
| | | Write: | | | | | | | | |
| \$0342 - \$034D | BFFDATA0- BFFDATA11 | Read: | DATA 7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |
| | | Write: | | | | | | | | |
| \$034E - \$034F | Reserved | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$0350 - \$035F | BFBUFCTL0 - BFBUFCTL15 | Read: | IFLG | IENA | LOCK | ABTAK | ABTRQ | 0 | 0 | CFG |
| | | Write: | | | | | | | | |

\$0360 - \$03FF**Reserved**

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0360 - \$03FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses \$001A and \$001B after reset). The read-only value is a unique part ID for each revision of the chip. **(Table 1-3)** shows the assigned part ID number.

Table 1-3 Assigned Part ID Numbers

| Device | Mask Set Number | Part ID ¹ |
|-------------|-----------------|----------------------|
| MC9S12DT128 | 1L40K | \$0111 |
| MC9S12DT128 | 3L40K | \$0113 |
| MC9S12DT128 | 4L40K | \$0114 |
| MC9S12DT128 | 0L94R | \$0110 |
| MC9S12DT128 | 1L59W | \$0115 |
| MC9S12DT128 | 5L40K | \$0115 |

NOTES:

- The coding is as follows:
 Bit 15-12: Major family identifier
 Bit 11-8: Minor family identifier
 Bit 7-4: Major mask set revision number including FAB transfers
 Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses \$001C and \$001D after reset). **Table 1-4** shows the read-only values of these registers. Refer to HCS12 Module Mapping Control (MMC) Block Guide for further details.

Table 1-4 Memory size registers

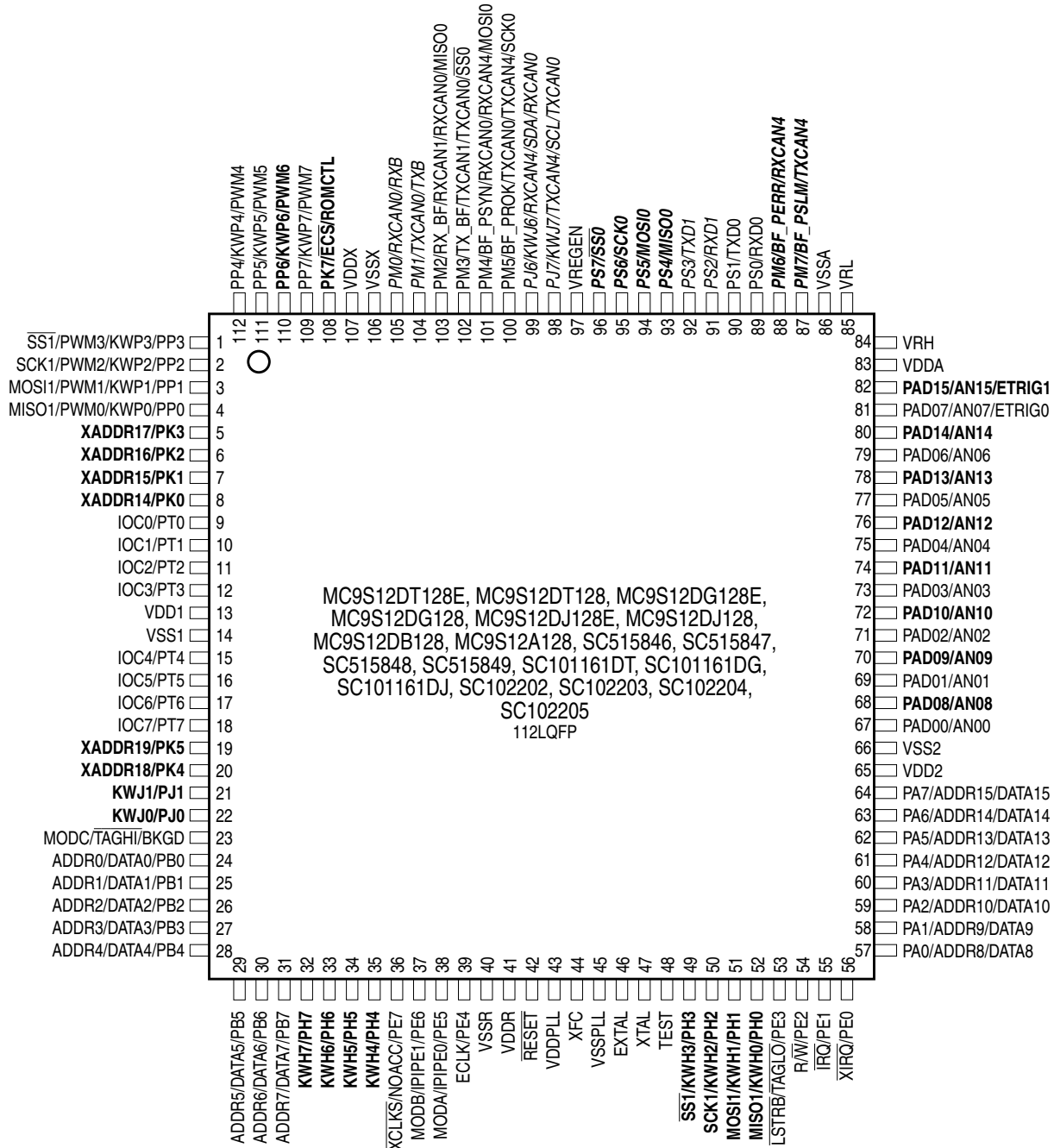
| Register name | Value |
|---------------|-------|
| MEMSIZ0 | \$13 |
| MEMSIZ1 | \$80 |

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12DT128 and its derivatives are available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1**, **Figure 2-2**, and **Figure 2-3** show the pin assignments for different packages.



Signals shown in **Bold** are not available on all the 80 pin package options
 Signals shown in **Bold-Italics** are not available on the MC9S12DJ128E, MC9S12DJ128, MC9S12DG128E, MC9S12DG128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 80 pin package options
 Signals shown in *Italics* are not available on the MC9S12DB128, SC515846, and SC102202 80 pin package options

Figure 2-1 Pin assignments 112 LQFP for MC9S12DT128E, MC9S12DT128, MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12DB128 MC9S12A128, SC515846, SC515847, SC515848, SC515849, SC101161DT, SC101161DG, SC101161DJ, SC102202, SC102203, SC102204, and SC102205

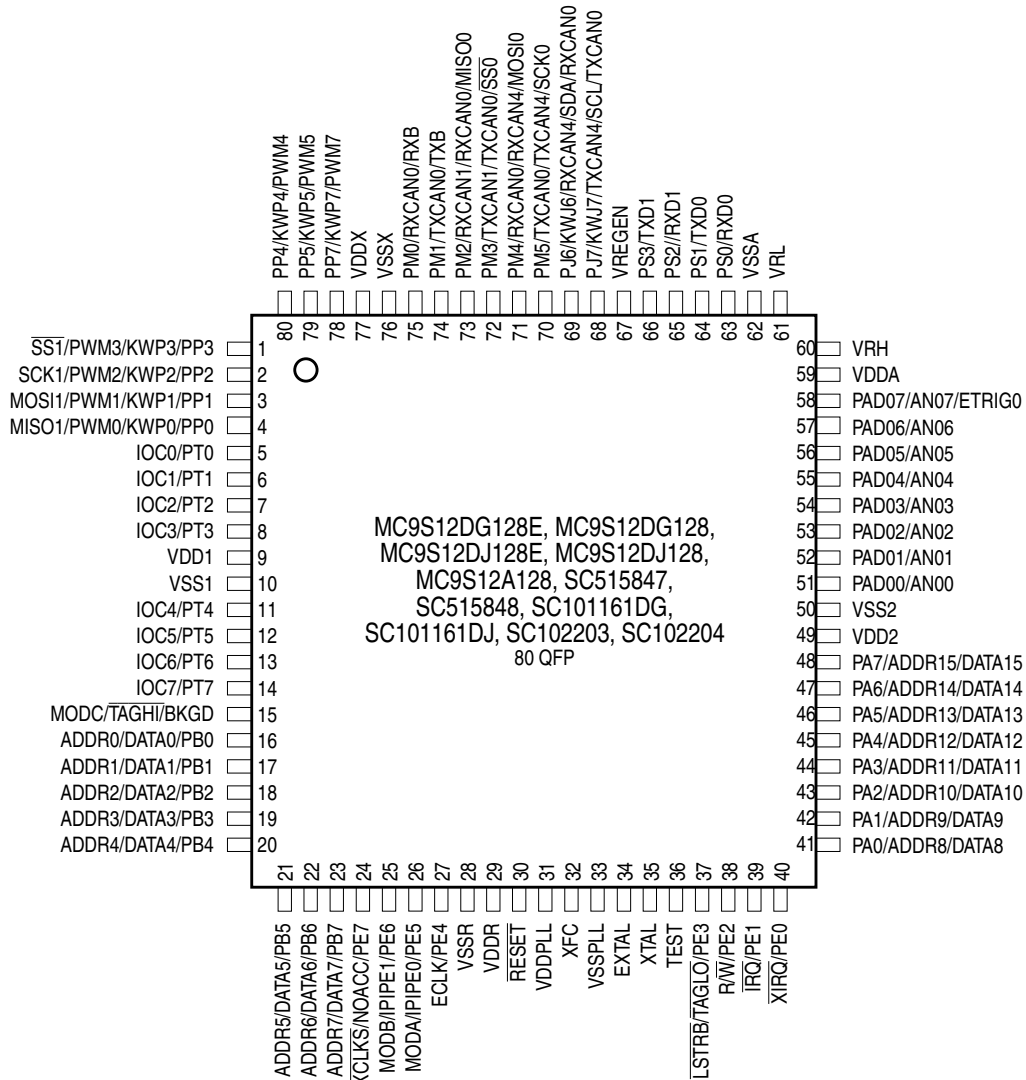


Figure 2-2 Pin Assignments in 80 QFP for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 Bondout

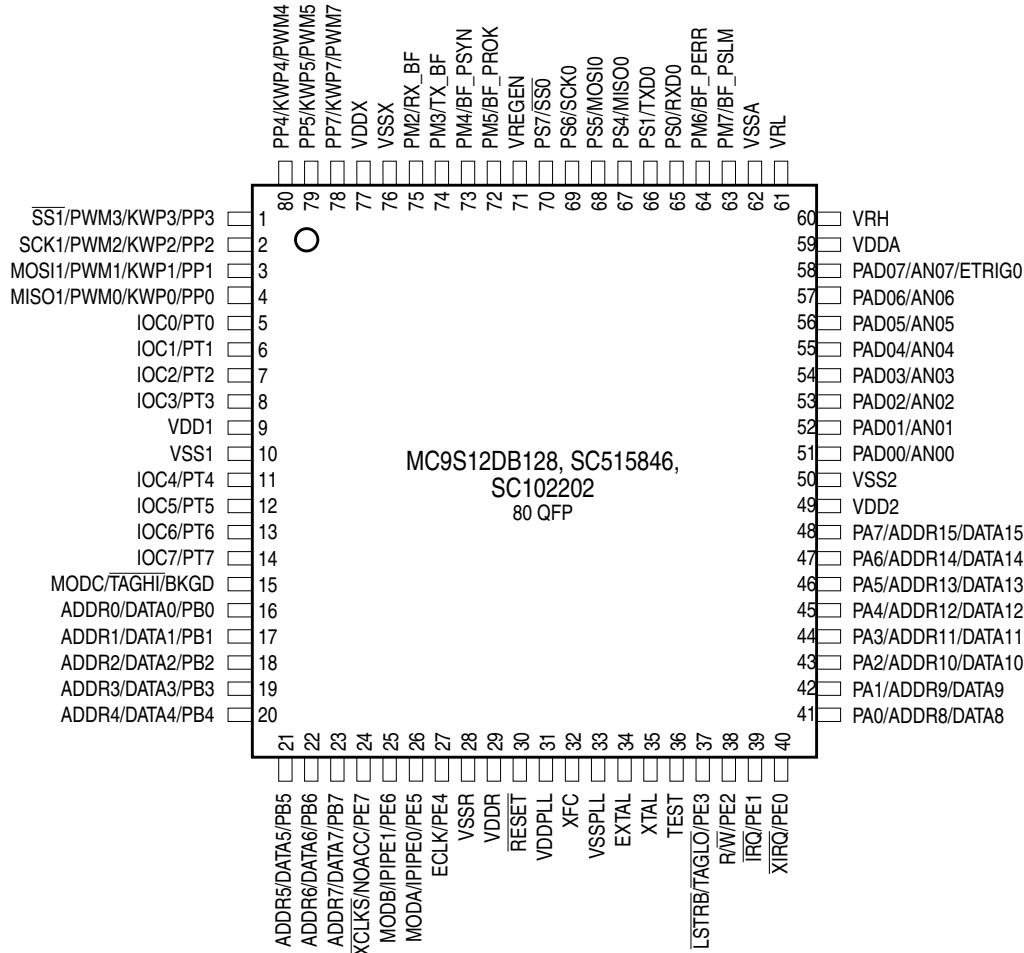


Figure 2-3 Pin Assignments in 80 QFP for MC9S12DB128, SC515846, and SC102202 Bondout

2.2 Signal Properties Summary

(Table 2-1) summarizes the pin functionality. Signals shown in **Bold** are not available on all the 80-pin package options. Signals shown in *Bold-Italics* are not available on the MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 80-pin package options. Signals shown in *Italics* are not available on MC9S12DB128, SC515846, and SC102202 80-pin package options.

Table 2-1 Signal Properties

| Pin Name Function 1 | Pin Name Function 2 | Pin Name Function 3 | Pin Name Function 4 | Pin Name Function 5 | Powered by | Internal Pull Resistor | | Description |
|------------------------|---------------------------|---------------------------|------------------------|------------------------|---------------|---|-------------------------------------|--|
| | | | | | | CTRL | Reset State | |
| EXTAL | — | — | — | — | VDDPLL | NA | NA | Oscillator Pins |
| XTAL | — | — | — | — | VDDPLL | NA | NA | |
| RESET | — | — | — | — | VDDR | None | None | External Reset |
| TEST | — | — | — | — | N.A. | None | None | Test Input |
| VREGEN | — | — | — | — | VDDX | NA | NA | Voltage Regulator Enable Input |
| XFC | — | — | — | — | VDDPLL | NA | NA | PLL Loop Filter |
| BKGD | $\overline{\text{TAGHI}}$ | MODC | — | — | VDDR | Always Up | Up | Background Debug, Tag High, Mode Input |
| PAD[15] | AN1[7] | ETRIG1 | — | — | VDDA | None | None | Port AD Input, Analog Inputs, External Trigger Input (ATD1) |
| PAD[14:8] | AN1[6:0] | — | — | — | VDDA | None | None | Port AD Input, Analog Inputs (ATD1) |
| PAD[7] | AN0[7] | ETRIG0 | — | — | VDDA | None | None | Port AD Input, Analog Inputs, External Trigger Input (ATD0) |
| PAD[6:0] | AN0[6:0] | — | — | — | VDDA | None | None | Port AD Input, Analog Inputs (ATD0) |
| PA[7:0] | ADDR[15:8]/ DATA[15:8] | — | — | — | VDDR | PUCR/ PUPAE | Disabled | Port A I/O, Multiplexed Address/Data |
| PB[7:0] | ADDR[7:0]/ DATA[7:0] | — | — | — | VDDR | PUCR/ PUPBE | Disabled | Port B I/O, Multiplexed Address/Data |
| PE7 | NOACC | $\overline{\text{XCLKS}}$ | — | — | VDDR | PUCR/ PUPEE | Mode depend- ant ¹ | Port E I/O, Access, Clock Select |
| PE6 | IPIPE1 | MODB | — | — | VDDR | While $\overline{\text{RESET}}$ pin low: Down | | Port E I/O, Pipe Status, Mode Input |
| PE5 | IPIPE0 | MODA | — | — | VDDR | | | Port E I/O, Pipe Status, Mode Input |
| PE4 | ECLK | — | — | — | VDDR | PUCR/ PUPEE | Mode depend- ant ¹ | Port E I/O, Bus Clock Output |
| PE3 | $\overline{\text{LSTRB}}$ | $\overline{\text{TAGLO}}$ | — | — | VDDR | | | Port E I/O, Byte Strobe, Tag Low |
| PE2 | R/ $\overline{\text{W}}$ | — | — | — | VDDR | | | Port E I/O, R/ $\overline{\text{W}}$ in expanded modes |
| PE1 | $\overline{\text{IRQ}}$ | — | — | — | VDDR | | Up | Port E Input, Maskable Interrupt |
| PE0 | $\overline{\text{XIRQ}}$ | — | — | — | VDDR | Port E Input, Non Maskable Interrupt | | |
| PH7 | KWH7 | --- | — | — | VDDR | PERH/ PPSH | Disabled | Port H I/O, Interrupt |

| Pin Name Function 1 | Pin Name Function 2 | Pin Name Function 3 | Pin Name Function 4 | Pin Name Function 5 | Powered by | Internal Pull Resistor | | Description |
|---------------------|---------------------|---------------------|---------------------|---------------------|------------|------------------------|-------------|--|
| | | | | | | CTRL | Reset State | |
| PH6 | KWH6 | --- | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt |
| PH5 | KWH5 | --- | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt |
| PH4 | KWH4 | --- | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt |
| PH3 | KWH3 | $\overline{SS1}$ | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt, \overline{SS} of SPI1 |
| PH2 | KWH2 | SCK1 | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt, SCK of SPI1 |
| PH1 | KWH1 | MOSI1 | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt, MOSI of SPI1 |
| PH0 | KWH0 | MISO1 | — | — | VDDR | PERH/PPSH | Disabled | Port H I/O, Interrupt, MISO of SPI1 |
| PJ7 | KWJ7 | TXCAN4 | SCL | TXCAN0 | VDDX | PERJ/PPSJ | Up | Port J I/O, Interrupt, TX of CAN4, SCL of IIC |
| PJ6 | KWJ6 | RXCAN4 | SDA | RXCAN0 | VDDX | PERJ/PPSJ | Up | Port J I/O, Interrupt, RX of CAN4, SDA of IIC |
| PJ[1:0] | KWJ[1:0] | — | — | — | VDDX | PERJ/PPSJ | Up | Port J I/O, Interrupts |
| PK7 | \overline{ECS} | ROMCTL | — | — | VDDX | PUCR/PUPKE | Up | Port K I/O, Emulation Chip Select, ROM Control |
| PK[5:0] | XADDR[19:14] | — | — | — | VDDX | PUCR/PUPKE | Up | Port K I/O, Extended Addresses |
| PM7 | BF_PSLM | TXCAN4 | — | — | VDDX | PERM/PPSM | Disabled | Port M I/O, BF slot mismatch pulse, TX of CAN4 |
| PM6 | BF_PERR | RXCAN4 | — | — | VDDX | PERM/PPSM | Disabled | Port M I/O, BF illegal pulse/message format error pulse, RX of CAN4 |
| PM5 | BF_PROK | TXCAN0 | TXCAN4 | SCK0 | VDDX | PERM/PPSM | Disabled | Port M I/O, BF reception ok pulse, TX of CAN0, CAN4, SCK of SPI0 |
| PM4 | BF_PSYN | RXCAN0 | RXCAN4 | MOSI0 | VDDX | PERM/PPSM | Disabled | Port M I/O, BF sync pulse (Rx/Tx) OK pulse o/p, RX of CAN0, CAN4, MOSI of SPI0 |
| PM3 | TX_BF | TXCAN1 | TXCAN0 | $\overline{SS0}$ | VDDX | PERM/PPSM | Disabled | Port M I/O, TX of BF, CAN1, CAN0, \overline{SS} of SPI0 |
| PM2 | RX_BF | RXCAN1 | RXCAN0 | MISO0 | VDDX | PERM/PPSM | Disabled | Port M I/O, RX of BF, CAN1, CAN0, MISO of SPI0 |

| Pin Name Function 1 | Pin Name Function 2 | Pin Name Function 3 | Pin Name Function 4 | Pin Name Function 5 | Powered by | Internal Pull Resistor | | Description |
|------------------------|------------------------|------------------------|------------------------|------------------------|---------------|---------------------------|-----------------|--|
| | | | | | | CTRL | Reset State | |
| PM1 | TXCAN0 | TXB | — | — | VDDX | PERM/ PPSM | Disabled | Port M I/O, TX of CAN0, RX of BDLC |
| PM0 | RXCAN0 | RXB | — | — | VDDX | PERM/ PPSM | Disabled | Port M I/O, RX of CAN0, RX of BDLC |
| PP7 | KWP7 | PWM7 | — | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 7 of PWM |
| PP6 | KWP6 | PWM6 | — | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 6 of PWM |
| PP5 | KWP5 | PWM5 | — | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 5 of PWM |
| PP4 | KWP4 | PWM4 | — | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 4 of PWM |
| PP3 | KWP3 | PWM3 | $\overline{SS1}$ | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 3 of PWM, \overline{SS} of SPI1 |
| PP2 | KWP2 | PWM2 | SCK1 | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1 |
| PP1 | KWP1 | PWM1 | MOSI1 | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1 |
| PP0 | KWP0 | PWM0 | MISO1 | — | VDDX | PERP/ PPSP | Disabled | Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1 |
| PS7 | $\overline{SS0}$ | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, \overline{SS} of SPI0 |
| PS6 | SCK0 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, SCK of SPI0 |
| PS5 | MOSI0 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, MOSI of SPI0 |
| PS4 | MISO0 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, MISO of SPI0 |
| PS3 | TXD1 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, TXD of SCI1 |
| PS2 | RXD1 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, RXD of SCI1 |
| PS1 | TXD0 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, TXD of SCI0 |
| PS0 | RXD0 | — | — | — | VDDX | PERS/ PPSS | Up | Port S I/O, RXD of SCI0 |
| PT[7:0] | IOC[7:0] | — | — | — | VDDX | PERT/ PPST | Disabled | Port T I/O, Timer channels |

NOTES:

1. Refer to PEAR register description in HCS12 Multiplexed External Bus Interface (MEBI) Block Guide.

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

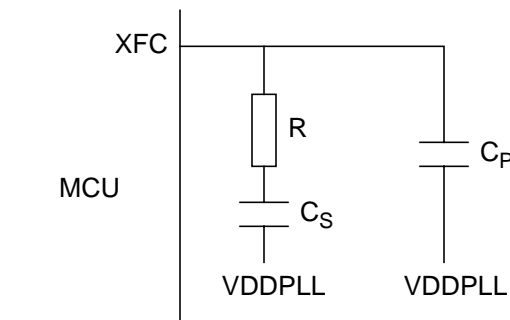


Figure 2-4 PLL Loop Filter Connections

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/ $\overline{\text{TAGHI}}$ /MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin has a permanently enabled pull-up device.

2.3.6 PAD[15] / AN1[7] / ETRIG1 — Port AD Input Pin [15]

PAD15 is a general purpose input pin and analog input of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

2.3.7 PAD[14:8] / AN1[6:0] — Port AD Input Pins [14:8]

PAD14 - PAD8 are general purpose input pins and analog inputs of the analog to digital converter ATD1.

2.3.8 PAD[7] / AN0[7] / ETRIG0 — Port AD Input Pin [7]

PAD7 is a general purpose input pin and analog input of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.9 PAD[6:0] / AN0[6:0] — Port AD Input Pins [6:0]

PAD6 - PAD0 are general purpose input pins and analog inputs of the analog to digital converter ATD0.

2.3.10 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

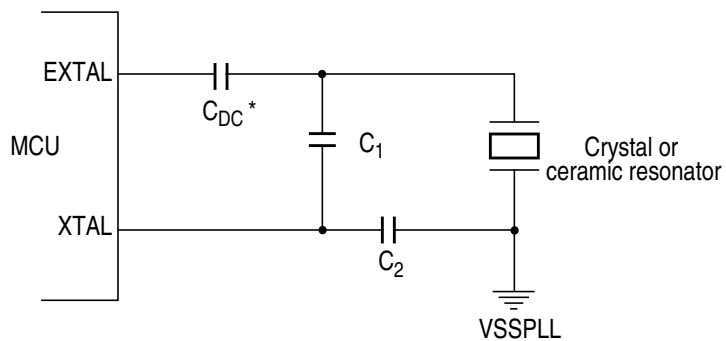
2.3.11 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.12 PE7 / NOACC / \overline{XCLKS} — Port E I/O Pin 7

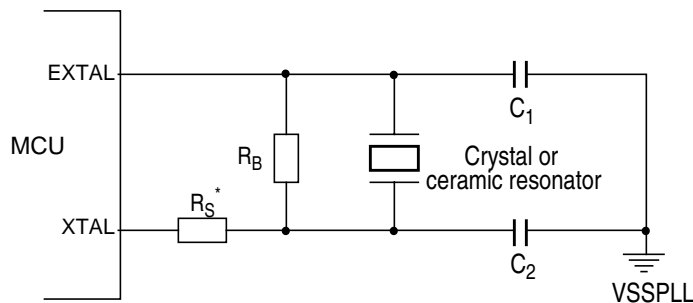
PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.

The \overline{XCLKS} is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of \overline{RESET} . If the input is a logic low the EXTAL pin is configured for an external clock drive. If input is a logic high an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal
 Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC} .

Figure 2-5 Colpitts Oscillator Connections (PE7=1)



* R_S can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-6 Pierce Oscillator Connections (PE7=0)

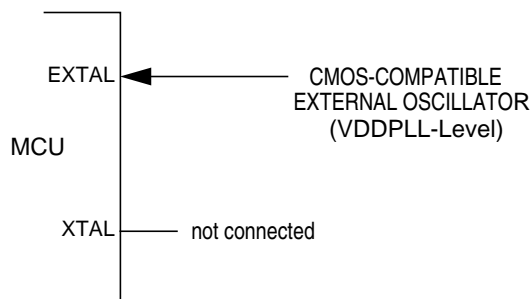


Figure 2-7 External Clock Connections (PE7=0)

2.3.13 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.14 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.15 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.16 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.3.17 PE2 / $\overline{\text{R/W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.18 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.19 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.20 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.21 PH6 / KWH6 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.22 PH5 / KWH5 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.23 PH4 / KWH4 — Port H I/O Pin 2

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.24 PH3 / KWH3 / $\overline{SS1}$ — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin \overline{SS} of the Serial Peripheral Interface 1 (SPI1).

2.3.25 PH2 / KWH2 / SCK1 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.26 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.27 PH0 / KWH0 / MISO1 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.28 PJ7 / KWJ7 / TXCAN4 / SCL / TXCAN0 — PORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for the Motorola Scalable Controller Area Network controller 0 or 4 (CAN0, CAN4) or the serial clock pin SCL of the IIC module.

2.3.29 PJ6 / KWJ6 / RXCAN4 / SDA / RXCAN0 — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXCAN for the Motorola Scalable Controller Area Network controller 0 or 4 (CAN0, CAN4) or the serial data pin SDA of the IIC module.

2.3.30 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.31 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). While configuring MCU expanded modes, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit. For a complete list of modes refer to **4.2 Chip Configuration Summary**.

2.3.32 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.3.33 PM7 / BF_PSLM / TXCAN4 — Port M I/O Pin 7

PM7 is a general purpose input or output pin. It can be configured as the slot mismatch output pulse pin of Byteflight. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 4 (CAN4).

2.3.34 PM6 / BF_PERR / RXCAN4 — Port M I/O Pin 6

PM6 is a general purpose input or output pin. It can be configured as the illegal pulse or message format error output pulse pin of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 4 (CAN4).

2.3.35 PM5 / BF_PROK / TXCAN0 / TXCAN4 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the reception OK output pulse pin of Byteflight. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.36 PM4 / BF_PSYN / RXCAN0 / RXCAN4/ MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the correct synchronisation pulse reception/transmission output pulse pin of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 0 or 4 (CAN0 or CAN4). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM3 / TX_BF / TXCAN1 / TXCAN0 / \overline{SS} — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TX_BF of Byteflight. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the slave select pin \overline{SS} of the Serial Peripheral Interface 0 (SPI0).

2.3.38 PM2 / RX_BF / RXCAN1 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RX_BF of Byteflight. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.3.39 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

2.3.40 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

2.3.41 PP7 / KWP7 / PWM7 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output.

2.3.42 PP6 / KWP6 / PWM6 — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output.

2.3.43 PP5 / KWP5 / PWM5 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output.

2.3.44 PP4 / KWP4 / PWM4 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output.

2.3.45 PP3 / KWP3 / PWM3 / $\overline{SS1}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin \overline{SS} of the Serial Peripheral Interface 1 (SPI1).

2.3.46 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.47 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.48 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.49 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS7 is a general purpose input or output pin. It can be configured as the slave select pin \overline{SS} of the Serial Peripheral Interface 0 (SPI0).

2.3.50 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.51 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.52 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.53 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.54 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.55 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.56 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.57 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12DT128 power and ground pins are described below.

Table 2-2 MC9S12DT128 Power and Ground Connection Summary

| Mnemonic | Pin Number | Nominal Voltage | Description |
|----------|-------------|-----------------|---|
| | 112-pin QFP | | |
| VDD1, 2 | 13, 65 | 2.5V | Internal power and ground generated by internal regulator |
| VSS1, 2 | 14, 66 | 0V | |

| Mnemonic | Pin Number | Nominal Voltage | Description |
|----------|-------------|-----------------|--|
| | 112-pin QFP | | |
| VDDR | 41 | 5.0V | External power and ground, supply to pin drivers and internal voltage regulator. |
| VSSR | 40 | 0V | |
| VDDX | 107 | 5.0V | External power and ground, supply to pin drivers. |
| VSSX | 106 | 0V | |
| VDDA | 83 | 5.0V | Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently. |
| VSSA | 86 | 0V | |
| VRL | 85 | 0V | Reference voltages for the analog-to-digital converter. |
| VRH | 84 | 5.0V | |
| VDDPLL | 43 | 2.5V | Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator. |
| VSSPLL | 45 | 0V | |
| VREGEN | 97 | 5V | Internal Voltage Regulator enable/disable |

NOTE: All VSS pins must be connected together in the application.

2.4.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: No load allowed except for bypass capacitors.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.

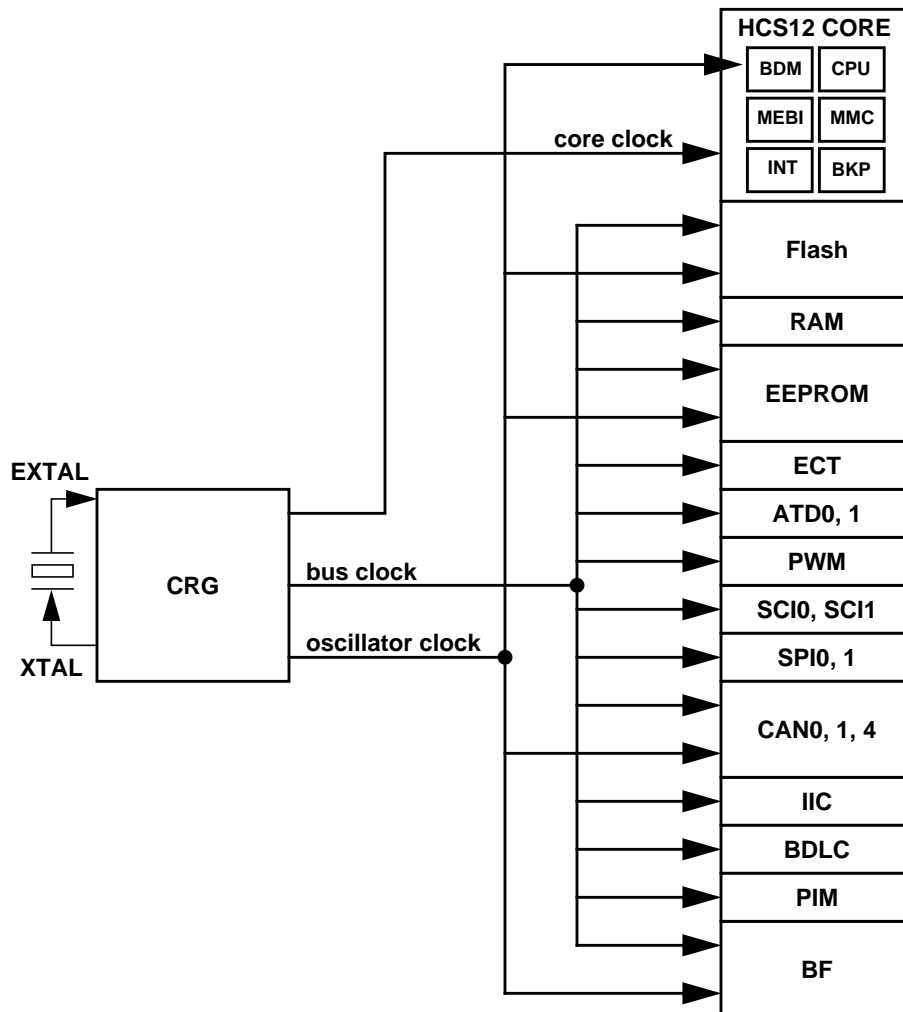


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12DT128. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset ((**Table 4-1**)). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

| BKGD = MODC | PE6 = MODB | PE5 = MODA | PK7 = ROMCTL | ROMON Bit | Mode Description |
|-------------|------------|------------|--------------|-----------|---|
| 0 | 0 | 0 | X | 1 | Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active. |
| 0 | 0 | 1 | 0 | 1 | Emulation Expanded Narrow, BDM allowed |
| | | | 1 | 0 | |
| 0 | 1 | 0 | X | 0 | Special Test (Expanded Wide), BDM allowed |
| 0 | 1 | 1 | 0 | 1 | Emulation Expanded Wide, BDM allowed |
| | | | 1 | 0 | |
| 1 | 0 | 0 | X | 1 | Normal Single Chip, BDM allowed |
| 1 | 0 | 1 | 0 | 0 | Normal Expanded Narrow, BDM allowed |
| | | | 1 | 1 | |
| 1 | 1 | 0 | X | 1 | Special Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used) |
| 1 | 1 | 1 | 0 | 0 | Normal Expanded Wide, BDM allowed |
| | | | 1 | 1 | |

For further explanation on the modes refer to the HCS12 Multiplexed External Bus Interface Block Guide.

Table 4-2 Clock Selection Based on PE7

| PE7 = XCLKS | Description |
|-------------|---|
| 1 | Colpitts Oscillator selected |
| 0 | Pierce Oscillator/external clock selected |

Table 4-3 Voltage Regulator VREGEN

| VREGEN | Description |
|--------|--|
| 1 | Internal Voltage Regulator enabled |
| 0 | Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V |

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode, No BDM possible
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode or via a .sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the CPU Reference Manual for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

(Table 5-1) lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

| Vector Address | Interrupt Source | CCR Mask | Local Enable | HPRIO Value to Elevate |
|----------------|------------------------------------|----------|--------------------------------------|------------------------|
| \$FFFE, \$FFFF | Reset | None | None | – |
| \$FFFC, \$FFFD | Clock Monitor fail reset | None | COPCTL (CME, FCME) | – |
| \$FFFA, \$FFFB | COP failure reset | None | COP rate select | – |
| \$FFF8, \$FFF9 | Unimplemented instruction trap | None | None | – |
| \$FFF6, \$FFF7 | SWI | None | None | – |
| \$FFF4, \$FFF5 | XIRQ / BF High Priority Sync Pulse | X-Bit | None / BFRIER (XSYNIE) | – |
| \$FFF2, \$FFF3 | IRQ | I-Bit | INTCR (IRQEN) | \$F2 |
| \$FFF0, \$FFF1 | Real Time Interrupt | I-Bit | CRGINT (RTIE) | \$F0 |
| \$FFEE, \$FFEF | Enhanced Capture Timer channel 0 | I-Bit | TIE (C0I) | \$EE |
| \$FFEC, \$FFED | Enhanced Capture Timer channel 1 | I-Bit | TIE (C1I) | \$EC |
| \$FFEA, \$FFEB | Enhanced Capture Timer channel 2 | I-Bit | TIE (C2I) | \$EA |
| \$FFE8, \$FFE9 | Enhanced Capture Timer channel 3 | I-Bit | TIE (C3I) | \$E8 |
| \$FFE6, \$FFE7 | Enhanced Capture Timer channel 4 | I-Bit | TIE (C4I) | \$E6 |
| \$FFE4, \$FFE5 | Enhanced Capture Timer channel 5 | I-Bit | TIE (C5I) | \$E4 |
| \$FFE2, \$FFE3 | Enhanced Capture Timer channel 6 | I-Bit | TIE (C6I) | \$E2 |
| \$FFE0, \$FFE1 | Enhanced Capture Timer channel 7 | I-Bit | TIE (C7I) | \$E0 |
| \$FFDE, \$FFDF | Enhanced Capture Timer overflow | I-Bit | TSCR2 (TOF) | \$DE |
| \$FFDC, \$FFDD | Pulse accumulator A overflow | I-Bit | PACTL (PAOVI) | \$DC |
| \$FFDA, \$FFDB | Pulse accumulator input edge | I-Bit | PACTL (PAI) | \$DA |
| \$FFD8, \$FFD9 | SPI0 | I-Bit | SPICR1 (SPIE, SPTIE) | \$D8 |
| \$FFD6, \$FFD7 | SCI0 | I-Bit | SCICR2 (TIE, TCIE, RIE, ILIE) | \$D6 |
| \$FFD4, \$FFD5 | SCI1 | I-Bit | SCICR2 (TIE, TCIE, RIE, ILIE) | \$D4 |
| \$FFD2, \$FFD3 | ATD0 | I-Bit | ATDCTL2 (ASCIE) | \$D2 |
| \$FFD0, \$FFD1 | ATD1 | I-Bit | ATDCTL2 (ASCIE) | \$D0 |
| \$FFCE, \$FFCF | Port J | I-Bit | PIEJ (PIEJ7, PIEJ6, PIEJ1, PIEJ0) | \$CE |
| \$FFCC, \$FFCD | Port H | I-Bit | PIEH (PIEH7-0) | \$CC |

| | | | | |
|---------------------|--------------------------------|-------|---|------|
| \$FFCA, \$FFCB | Modulus Down Counter underflow | I-Bit | MCCTL (MCZI) | \$CA |
| \$FFC8, \$FFC9 | Pulse Accumulator B Overflow | I-Bit | PBCTL (PBOVI) | \$C8 |
| \$FFC6, \$FFC7 | CRG PLL lock | I-Bit | PLLCR (LOCKIE) | \$C6 |
| \$FFC4, \$FFC5 | CRG Self Clock Mode | I-Bit | PLLCR (SCMIE) | \$C4 |
| \$FFC2, \$FFC3 | BDLC | I-Bit | DLCBCR1 (IE) | \$C2 |
| \$FFC0, \$FFC1 | IIC Bus | I-Bit | IBCR (IBIE) | \$C0 |
| \$FFBE, \$FFBF | SPI1 | I-Bit | SPICR1 (SPIE, SPTIE) | \$BE |
| \$FFBC, \$FFBD | Reserved | | | |
| \$FFBA, \$FFBB | EEPROM | I-Bit | ECNFG (CCIE, CBEIE) | \$BA |
| \$FFB8, \$FFB9 | FLASH | I-Bit | FCNFG (CCIE, CBEIE) | \$B8 |
| \$FFB6, \$FFB7 | CAN0 wake-up | I-Bit | CANRIER (WUPIE) | \$B6 |
| \$FFB4, \$FFB5 | CAN0 errors | I-Bit | CANRIER (CSCIE, OVRIE) | \$B4 |
| \$FFB2, \$FFB3 | CAN0 receive | I-Bit | CANRIER (RXFIE) | \$B2 |
| \$FFB0, \$FFB1 | CAN0 transmit | I-Bit | CANTIER (TXEIE[2:0]) | \$B0 |
| \$FFAE, \$FFAF | CAN1 wake-up | I-Bit | CANRIER (WUPIE) | \$AE |
| \$FFAC, \$FFAD | CAN1 errors | I-Bit | CANRIER (CSCIE, OVRIE) | \$AC |
| \$FFAA, \$FFAB | CAN1 receive | I-Bit | CANRIER (RXFIE) | \$AA |
| \$FFA8, \$FFA9 | CAN1 transmit | I-Bit | CANTIER (TXEIE[2:0]) | \$A8 |
| \$FFA6, \$FFA7 | BF Receive FIFO not empty | I-Bit | BFRIER (RCVFIE) | \$A6 |
| \$FFA4, \$FFA5 | BF receive | I-Bit | BFBUFCTL[15:0] (IENA) | \$A4 |
| \$FFA2, \$FFA3 | BF Synchronization | I-Bit | BFRIER (SYNAIE, SYNIE) | \$A2 |
| \$FFA0, \$FFA1 | BF general | I-Bit | BFBUFCTL[15:0] (IENA), BFGIER (OVRNIE, ERRIE, SYNEIE, SYNLIE, ILLPIE, LOCKIE, WAKEIE) BFRIER (SLMMIE) | \$A0 |
| \$FF98, \$FF9F | Reserved | | | |
| \$FF96, \$FF97 | CAN4 wake-up | I-Bit | CANRIER (WUPIE) | \$96 |
| \$FF94, \$FF95 | CAN4 errors | I-Bit | CANRIER (CSCIE, OVRIE) | \$94 |
| \$FF92, \$FF93 | CAN4 receive | I-Bit | CANRIER (RXFIE) | \$92 |
| \$FF90, \$FF91 | CAN4 transmit | I-Bit | CANTIER (TXEIE[2:0]) | \$90 |
| \$FF8E, \$FF8F | Port P Interrupt | I-Bit | PIEP (PIEP7-0) | \$8E |
| \$FF8C, \$FF8D | PWM Emergency Shutdown | I-Bit | PWMSDN (PWMIE) | \$8C |
| \$FF80 to \$FF8B | Reserved | | | |

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

NOTE: *For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Section 6 HCS12 Core Block Description

6.1 CPU Block Description

Consult the CPU Reference Manual for information on the CPU.

6.1.1 Device-specific information

When the CPU Reference Manual refers to cycles this is equivalent to Bus Clock periods. So 1 cycle is equivalent to 1 Bus Clock period.

6.2 HCS12 Module Mapping Control (MMC) Block Description

Consult the MMC Block Guide for information on the HCS12 Module Mapping Control module.

6.2.1 Device-specific information

- INITEE
 - Reset state: \$01
 - Bits EE11-EE15 are "Write once in Normal and Emulation modes and write anytime in Special modes".
- PPAGE
 - Reset state: \$00
 - Register is "Write anytime in all modes".
- MEMSIZ0
 - Reset state: \$13
- MEMSIZ1
 - Reset state: \$80

6.3 HCS12 Multiplexed External Bus Interface (MEBI) Block Description

Consult the MEBI Block Guide for information on HCS12 Multiplexed External Bus Interface module.

6.3.1 Device-specific information

- PUCR
 - Reset state: \$90

6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

6.5 HCS12 Background Debug Module (BDM) Block Description

Consult the BDM Block Guide for information on the HCS12 Background Debug module.

6.5.1 Device-specific information

When the BDM Block Guide refers to *alternate clock* this is equivalent to *oscillator clock*.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block Guide for information on the HCS12 Breakpoint module.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

The Low Voltage Reset feature of the CRG is not available on this device.

Section 8 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

8.1 Device-specific information

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.12 PE / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7**).

Section 9 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block User Guide for information about the Enhanced Capture Timer module. When the ECT_16B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 10 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DT128. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 11 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 12 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12DT128 device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 13 Serial Peripheral Interface (SPI) Block Description

There are two Serial Peripheral Interfaces (SPI1 and SPI0) implemented on MC9S12DT128. Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 14 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 15 Byteflight (BF) Block Description

Consult the BF Block User Guide for information about the 10 Mbps Byteflight module.

15.1 Device-specific information

The read-only Module Version Register (BFMVR) contains the current version number of \$80.

Section 16 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 17 Flash EEPROM 128K Block Description

Consult the FTS128K Block User Guide for information about the flash module.

The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using CAN or SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more details of the S12 LRAE and its implementation, please see the S12 LREA Application Note (AN2546/D).

It is planned that most HC9S12 devices manufactured after Q1 of 2004 will be shipped with the S12 LRAE programmed in the Flash . Exact details of the changeover (ie blank to programmed) for each product will be communicated in advance via GPCN and will be traceable by the customer via datecode marking on the device.

Please contact Freescale Sales if you have any additional questions.

Section 18 EEPROM 2K Block Description

Consult the EETS2K Block User Guide for information about the EEPROM module.

Section 19 RAM Block Description

This module supports single-cycle misaligned word accesses without wait states.

Section 20 MSCAN Block Description

There are three MSCAN modules (CAN4, CAN1 and CAN0) implemented on the MC9S12DT128. Consult the MSCAN Block User Guide for information about the Motorola Scalable CAN Module.

Section 21 Port Integration Module (PIM) Block Description

Consult the PIM_9DTB128 Block User Guide for information about the Port Integration Module.

Section 22 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

Section 23 Printed Circuit Board Layout Proposal

Table 23-1 Suggested External Component Values

| Component | Purpose | Type | Value |
|-----------------------|---------------------|---|---------------|
| C1 | VDD1 filter cap | ceramic X7R | 100 ... 220nF |
| C2 | VDD2 filter cap | ceramic X7R | 100 ... 220nF |
| C3 | VDDA filter cap | ceramic X7R | 100nF |
| C4 | VDDR filter cap | X7R/tantalum | >= 100nF |
| C5 | VDDPLL filter cap | ceramic X7R | 100nF |
| C6 | VDDX filter cap | X7R/tantalum | >= 100nF |
| C7 | OSC load cap | | |
| C8 | OSC load cap | | |
| C9 / C _S | PLL loop filter cap | See PLL specification chapter | |
| C10 / C _P | PLL loop filter cap | | |
| C11 / C _{DC} | DC cutoff cap | Colpitts mode only, if recommended by quartz manufacturer | |
| R1 / R | PLL loop filter res | See PLL Specification chapter | |
| R2 / R _B | | Pierce mode only | |
| R3 / R _S | | | |
| Q1 | Quartz | | |

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1 – C6).
- Central point of the ground star should be the VSSR pin.

- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Figure 23-1 Recommended PCB Layout for 112LQFP Colpitts Oscillator

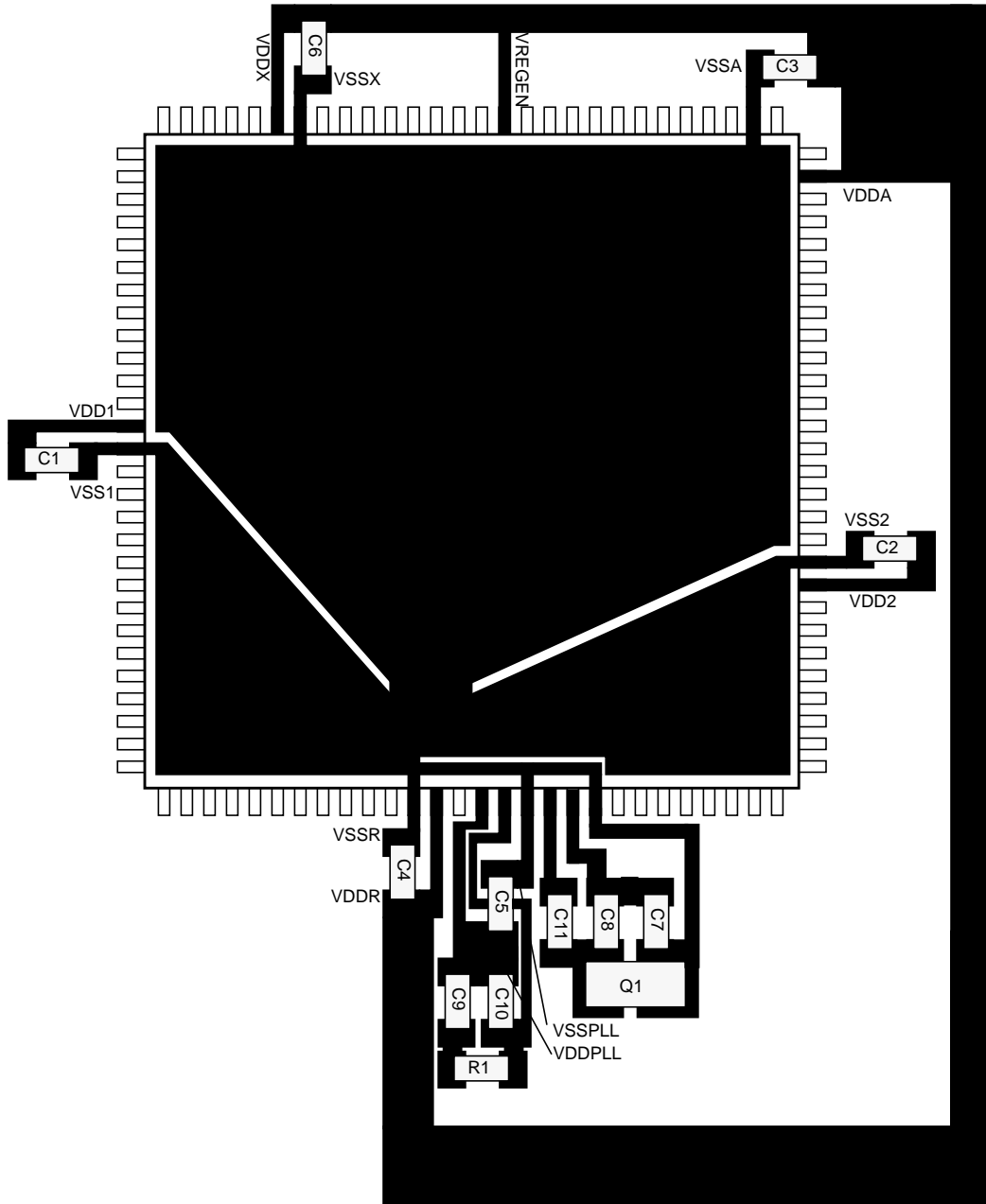


Figure 23-2 Recommended PCB Layout for 80QFP (MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204) Colpitts Oscillator

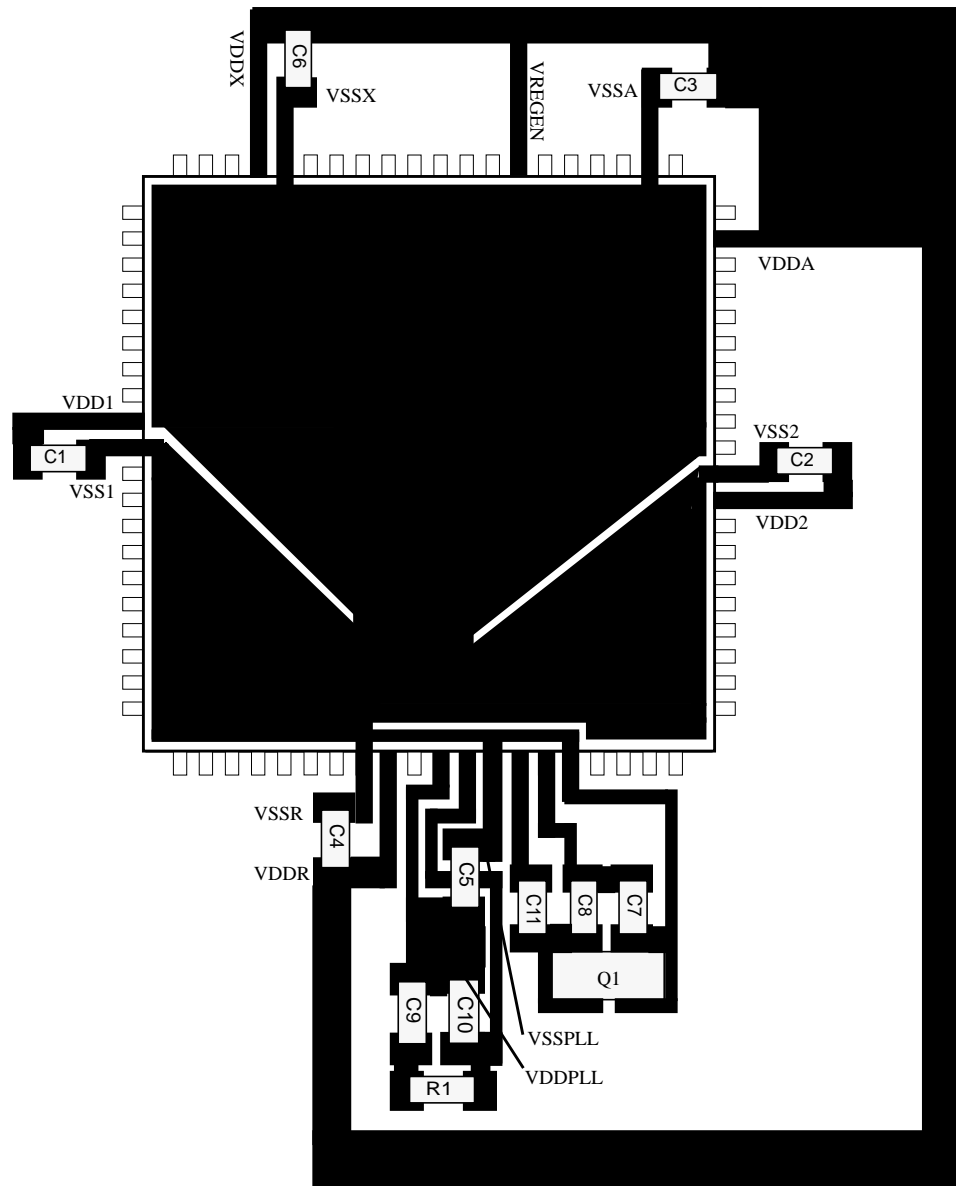


Figure 23-3 Recommended PCB Layout for 112LQFP Pierce Oscillator

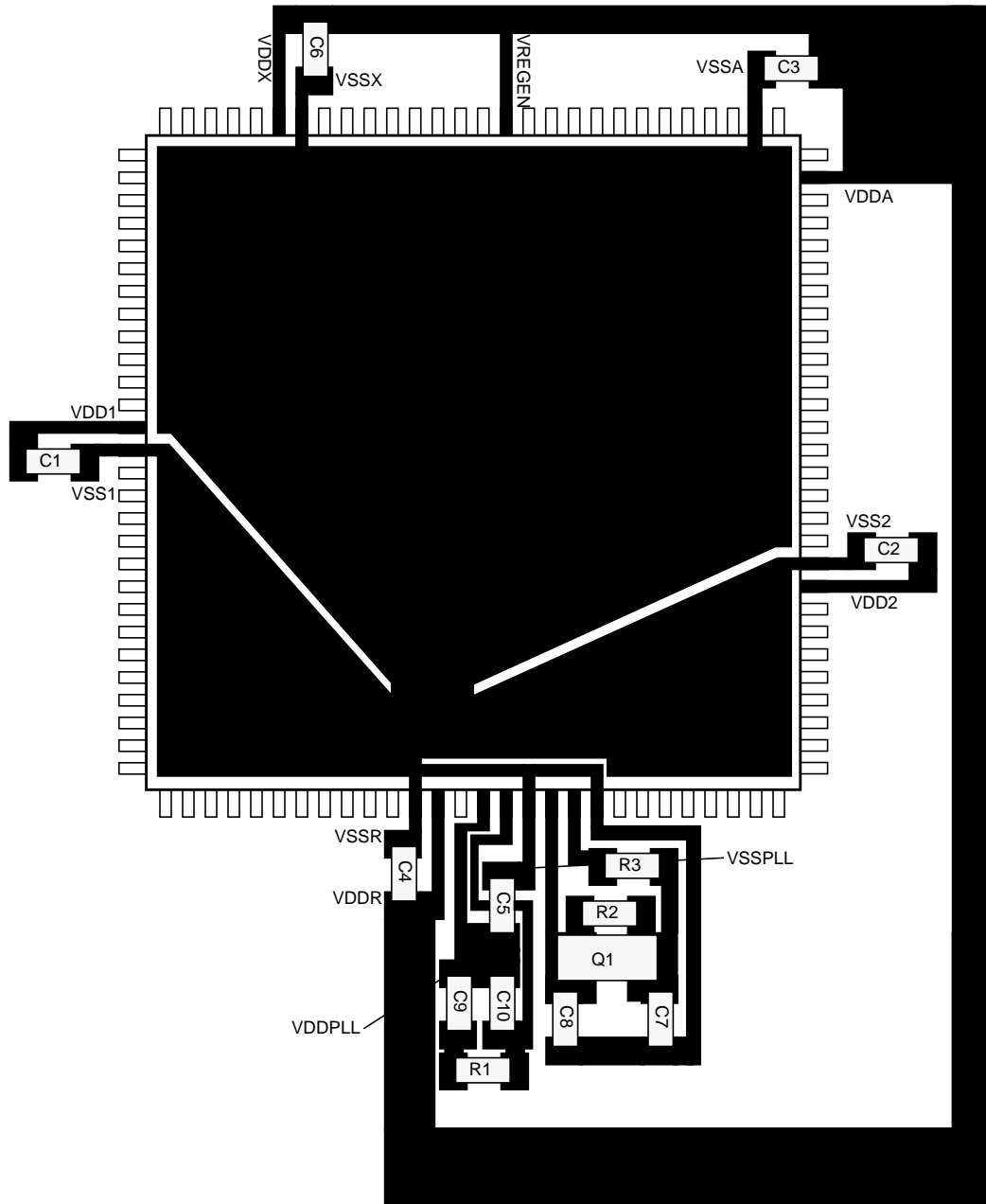


Figure 23-4 Recommended PCB Layout for 80QFP (MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204) Pierce Oscillator

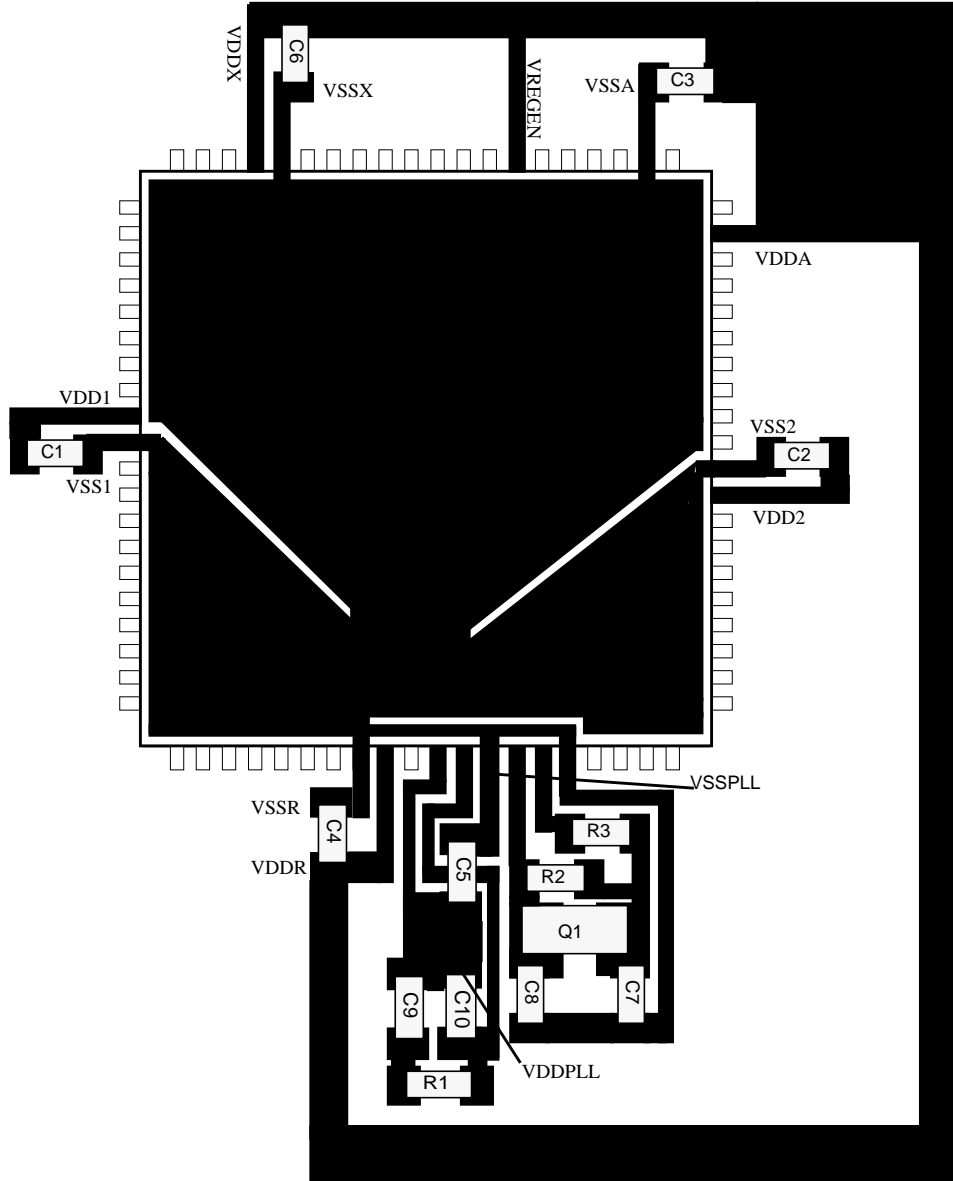
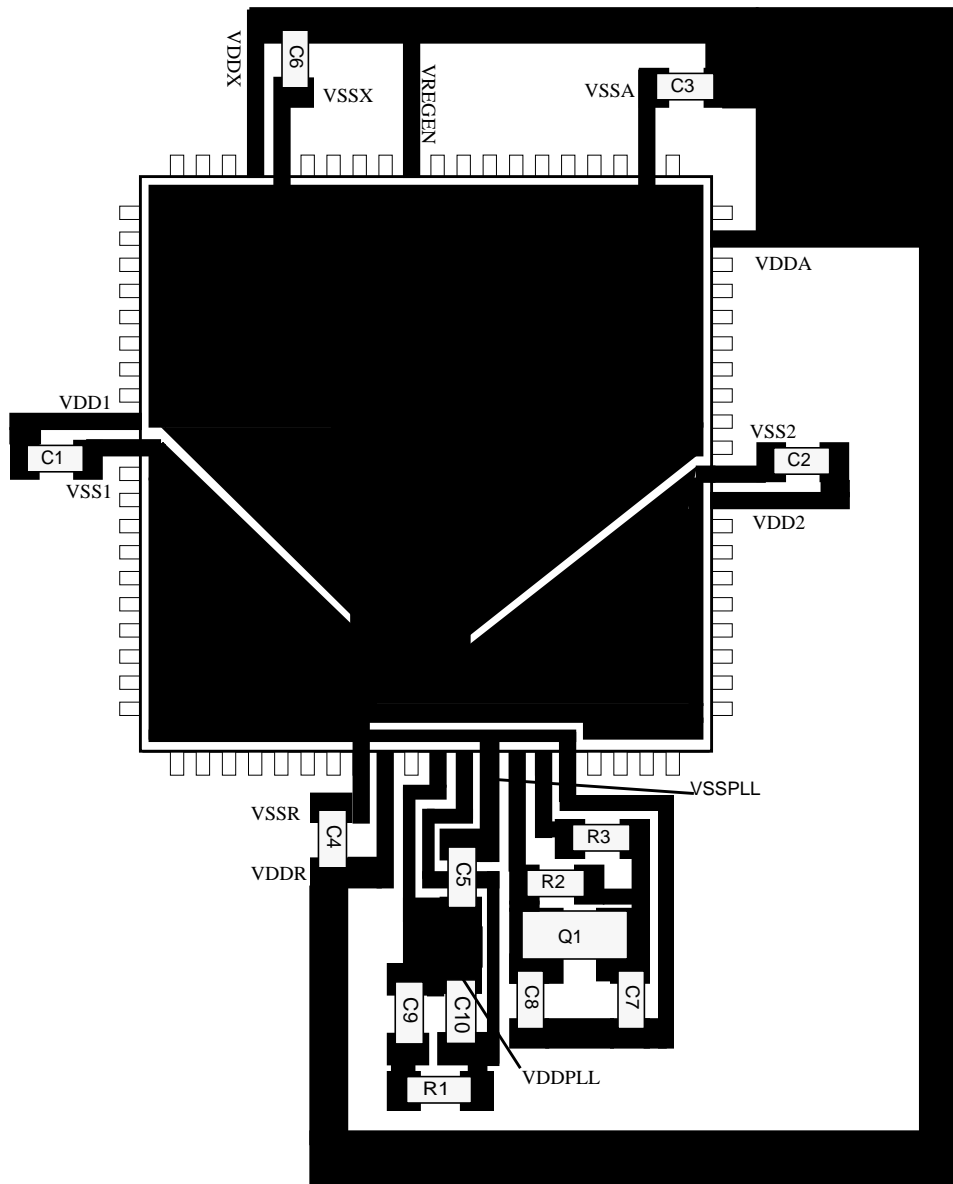


Figure 23-5 Recommended PCB Layout for 80QFP (MC9S12DB128, SC515846, and SC102202) Pierce Oscillator



Appendix A Electrical Characteristics

A.1 General

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12DT128 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator, PLL and internal logic.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs. The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This class is made up by the two VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5} , the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings¹

| Num | Rating | Symbol | Min | Max | Unit |
|-----|---|------------------|-------|------|------|
| 1 | I/O, Regulator and Analog Supply Voltage | V_{DD5} | -0.3 | 6.0 | V |
| 2 | Digital Logic Supply Voltage ² | V_{DD} | -0.3 | 3.0 | V |
| 3 | PLL Supply Voltage ⁽²⁾ | V_{DDPLL} | -0.3 | 3.0 | V |
| 4 | Voltage difference VDDX to VDDR and VDDA | ΔV_{DDX} | -0.3 | 0.3 | V |
| 5 | Voltage difference VSSX to VSSR and VSSA | ΔV_{SSX} | -0.3 | 0.3 | V |
| 6 | Digital I/O Input Voltage | V_{IN} | -0.3 | 6.0 | V |
| 7 | Analog Reference | V_{RH}, V_{RL} | -0.3 | 6.0 | V |
| 8 | XFC, EXTAL, XTAL inputs | V_{ILV} | -0.3 | 3.0 | V |
| 9 | TEST input | V_{TEST} | -0.3 | 10.0 | V |
| 10 | Instantaneous Maximum Current Single pin limit for all digital I/O pins ³ | I_D | -25 | +25 | mA |
| 11 | Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL ⁴ | I_{DL} | -25 | +25 | mA |
| 12 | Instantaneous Maximum Current Single pin limit for TEST ⁵ | I_{DT} | -0.25 | 0 | mA |
| 13 | Storage Temperature Range | T_{stg} | -65 | 155 | °C |

NOTES:

- Beyond absolute maximum ratings device might be damaged.
- The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
- All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA} .
- Those pins are internally clamped to V_{SSPLL} and V_{DDPLL} .
- This pin is clamped low to V_{SSX} , but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|---|--------|-------------|------|
| Human Body | Series Resistance | R1 | 1500 | Ohm |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulse per pin positive negative | – | – 3 3 | |
| Machine | Series Resistance | R1 | 0 | Ohm |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulse per pin positive negative | – | – 3 3 | |
| Latch-up | Minimum input voltage limit | | –2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

Table A-3 ESD and Latch-Up Protection Characteristics

| Num | C | Rating | Symbol | Min | Max | Unit |
|-----|---|---|-----------|--------------|-----|------|
| 1 | C | Human Body Model (HBM) | V_{HBM} | 2000 | – | V |
| 2 | C | Machine Model (MM) | V_{MM} | 200 | – | V |
| 3 | C | Charge Device Model (CDM) | V_{CDM} | 500 | – | V |
| 4 | C | Latch-up Current at 125°C positive negative | I_{LAT} | +100 –100 | – | mA |
| 5 | C | Latch-up Current at 27°C positive negative | I_{LAT} | +200 –200 | – | mA |

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J . For power dissipation

calculations refer to **Section A.1.8 Power Dissipation and Thermal Characteristics**.

Table A-4 Operating Conditions

| Rating | Symbol | Min | Typ | Max | Unit |
|--|-----------------|-------------------|-----|------|------|
| I/O, Regulator and Analog Supply Voltage | V_{DD5} | 4.5 | 5 | 5.25 | V |
| Digital Logic Supply Voltage ¹ | V_{DD} | 2.35 | 2.5 | 2.75 | V |
| PLL Supply Voltage ¹ | V_{DDPLL} | 2.25 | 2.5 | 2.75 | V |
| Voltage Difference VDDX to VDDR and VDDA | Δ_{VDDX} | -0.1 | 0 | 0.1 | V |
| Voltage Difference VSSX to VSSR and VSSA | Δ_{VSSX} | -0.1 | 0 | 0.1 | V |
| Bus Frequency | f_{bus} | 0.25 ² | - | 25 | MHz |
| MC9S12DT128C | | | | | |
| Operating Junction Temperature Range | T_J | -40 | - | 100 | °C |
| Operating Ambient Temperature Range ³ | T_A | -40 | 27 | 85 | °C |
| MC9S12DT128V | | | | | |
| Operating Junction Temperature Range | T_J | -40 | - | 120 | °C |
| Operating Ambient Temperature Range ³ | T_A | -40 | 27 | 105 | °C |
| MC9S12DT128M | | | | | |
| Operating Junction Temperature Range | T_J | -40 | - | 140 | °C |
| Operating Ambient Temperature Range ³ | T_A | -40 | 27 | 125 | °C |

NOTES:

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J .

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [$^{\circ}\text{C}/\text{W}$]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **(Table A-7)** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics¹

| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
|-----|---|--|---------------|-----|-----|-----|------|
| 1 | T | Thermal Resistance LQFP112, single sided PCB ² | θ_{JA} | – | – | 54 | °C/W |
| 2 | T | Thermal Resistance LQFP112, double sided PCB with 2 internal planes ³ | θ_{JA} | – | – | 41 | °C/W |
| 3 | T | Junction to Board LQFP112 | θ_{JB} | – | – | 31 | °C/W |
| 4 | T | Junction to Case LQFP112 | θ_{JC} | – | – | 11 | °C/W |
| 5 | T | Junction to Package Top LQFP112 | Ψ_{JT} | – | – | 2 | °C/W |
| 6 | T | Thermal Resistance QFP 80, single sided PCB | θ_{JA} | – | – | 51 | °C/W |
| 7 | T | Thermal Resistance QFP 80, double sided PCB with 2 internal planes | θ_{JA} | – | – | 41 | °C/W |
| 8 | T | Junction to Board QFP80 | θ_{JB} | – | – | 27 | °C/W |
| 9 | T | Junction to Case QFP80 | θ_{JC} | – | – | 14 | °C/W |
| 10 | T | Junction to Package Top QFP80 | Ψ_{JT} | – | – | 3 | °C/W |

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|--|------------------------|----------------------|-----|----------------------|---------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Input High Voltage | V_{IH} | $0.65 \cdot V_{DD5}$ | – | | V |
| | T | Input High Voltage | V_{IH} | – | – | $V_{DD5} + 0.3$ | |
| 2 | P | Input Low Voltage | V_{IL} | – | – | $0.35 \cdot V_{DD5}$ | V |
| | T | Input Low Voltage | V_{IL} | $V_{SS5} - 0.3$ | – | – | V |
| 3 | C | Input Hysteresis | V_{HYS} | | 250 | | mV |
| 4 | P | Input Leakage Current (pins in high ohmic input mode) $V_{in} = V_{DD5}$ or V_{SS5} | I_{in} | -1.0 | – | 1.0 | μA |
| 5 | C | Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2.0mA$ | V_{OH} | $V_{DD5} - 0.8$ | – | – | V |
| | P | Full Drive $I_{OH} = -10.0mA$ | | | | | |
| 6 | C | Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +2.0mA$ | V_{OL} | – | – | 0.8 | V |
| | P | Full Drive $I_{OL} = +10.0mA$ | | | | | |
| 7 | P | Internal Pull Up Device Current, tested at V_{IL} Max. | I_{PUL} | – | – | -130 | μA |
| 8 | C | Internal Pull Up Device Current, tested at V_{IH} Min. | I_{PUH} | -10 | – | – | μA |
| 9 | P | Internal Pull Down Device Current, tested at V_{IH} Min. | I_{PDH} | – | – | 130 | μA |
| 10 | C | Internal Pull Down Device Current, tested at V_{IL} Max. | I_{PDL} | 10 | – | – | μA |
| 11 | D | Input Capacitance | C_{in} | | 6 | – | pF |
| 12 | T | Injection current ¹ Single Pin limit Total Device Limit. Sum of all injected currents | I_{ICS} I_{ICP} | -2.5 -25 | – | 2.5 25 | mA |
| 13 | P | Port H, J, P Interrupt Input Pulse filtered ² | t_{PULSE} | | | 3 | μs |
| 14 | P | Port H, J, P Interrupt Input Pulse passed ² | t_{PULSE} | 10 | | | μs |

NOTES:

1. Refer to **Section A.1.4 Current Injection**, for more details
2. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|--|--|------------|-----|--|-----------------------------|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Run supply currents Single Chip, Internal regulator enabled | I_{DD5} | | | 55 | mA |
| 2 | P P | Wait Supply current All modules enabled, PLL on only RTI enabled ⁽¹⁾ | I_{DDW} | | | 30 5 | mA |
| 3 | C P C C C P C P C P | Pseudo Stop Current (RTI and COP disabled) ^{1, 2} -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | I_{DDPS} | | 370 400 450 550 600 650 800 850 1200 | 500 1600 2100 5000 | μA |
| 4 | C C C C C C C C | Pseudo Stop Current (RTI and COP enabled) ^{(1), (2)} -40°C 27°C 70°C 85°C 105°C 125°C 140°C | I_{DDPS} | | 570 600 650 750 850 1200 1500 | | μA |
| 5 | C P C C P C P C P | Stop Current ⁽²⁾ -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | I_{DD5} | | 12 25 100 100 130 160 200 350 400 600 | 100 1200 1700 5000 | μA |

NOTES:

1. PLL off, Oscillator in Colpitts Mode
2. At those low power dissipation levels $T_J = T_A$ can be assumed

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **(Table A-8)** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|---|---|---|------------------------------|--------------------------|------|--------------------------|-------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | D | Reference Potential Low High | V_{RL} V_{RH} | V_{SSA} $V_{DDA}/2$ | | $V_{DDA}/2$ V_{DDA} | V V |
| 2 | C | Differential Reference Voltage ¹ | $V_{RH}-V_{RL}$ | 4.50 | 5.00 | 5.25 | V |
| 3 | D | ATD Clock Frequency | f_{ATDCLK} | 0.5 | | 2.0 | MHz |
| 4 | D | ATD 10-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV10} T_{CONV10} | 14 7 | | 28 14 | Cycles μs |
| 5 | D | ATD 8-Bit Conversion Period Clock Cycles ⁽²⁾ Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV8} T_{CONV8} | 12 6 | | 26 13 | Cycles μs |
| 6 | D | Stop Recovery Time ($V_{DDA}=5.0$ Volts) | t_{SR} | | | 20 | μs |
| 7 | P | Reference Supply current (Both ATD modules on) | I_{REF} | | | 0.75 | mA |
| 8 | P | Reference Supply current (Only one ATD module on) | I_{REF} | | | 0.375 | mA |

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors – source resistance, source capacitance and current injection – have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **(Table A-6)** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq 1\text{LSB}$, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of \$3FF (\$FF in 8-bit mode) for analog inputs greater than V_{RH} and \$000 for values less than V_{RL} unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9 ATD Electrical Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|---|------------------------|------|-----|-----------|------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | C | Max input Source Resistance | R_S | - | - | 1 | K Ω |
| 2 | T | Total Input Capacitance Non Sampling Sampling | C_{INN} C_{INS} | | | 10 22 | pF |
| 3 | C | Disruptive Analog Input Current | I_{NA} | -2.5 | | 2.5 | mA |
| 4 | C | Coupling Ratio positive current injection | K_p | | | 10^{-4} | A/A |
| 5 | C | Coupling Ratio negative current injection | K_n | | | 10^{-2} | A/A |

A.2.3 ATD accuracy

(Table A-10) specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

| Conditions are shown in (Table A-4) unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$ | | | | | | | |
|---|---|-------------------------------------|--------|------|------|-----|--------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | 10-Bit Resolution | LSB | | 5 | | mV |
| 2 | P | 10-Bit Differential Nonlinearity | DNL | -1 | | 1 | Counts |
| 3 | P | 10-Bit Integral Nonlinearity | INL | -2.5 | ±1.5 | 2.5 | Counts |
| 4 | P | 10-Bit Absolute Error ¹ | AE | -3 | ±2.0 | 3 | Counts |
| 5 | P | 8-Bit Resolution | LSB | | 20 | | mV |
| 6 | P | 8-Bit Differential Nonlinearity | DNL | -0.5 | | 0.5 | Counts |
| 7 | P | 8-Bit Integral Nonlinearity | INL | -1.0 | ±0.5 | 1.0 | Counts |
| 8 | P | 8-Bit Absolute Error ⁽¹⁾ | AE | -1.5 | ±1.0 | 1.5 | Counts |

NOTES:

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^n DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

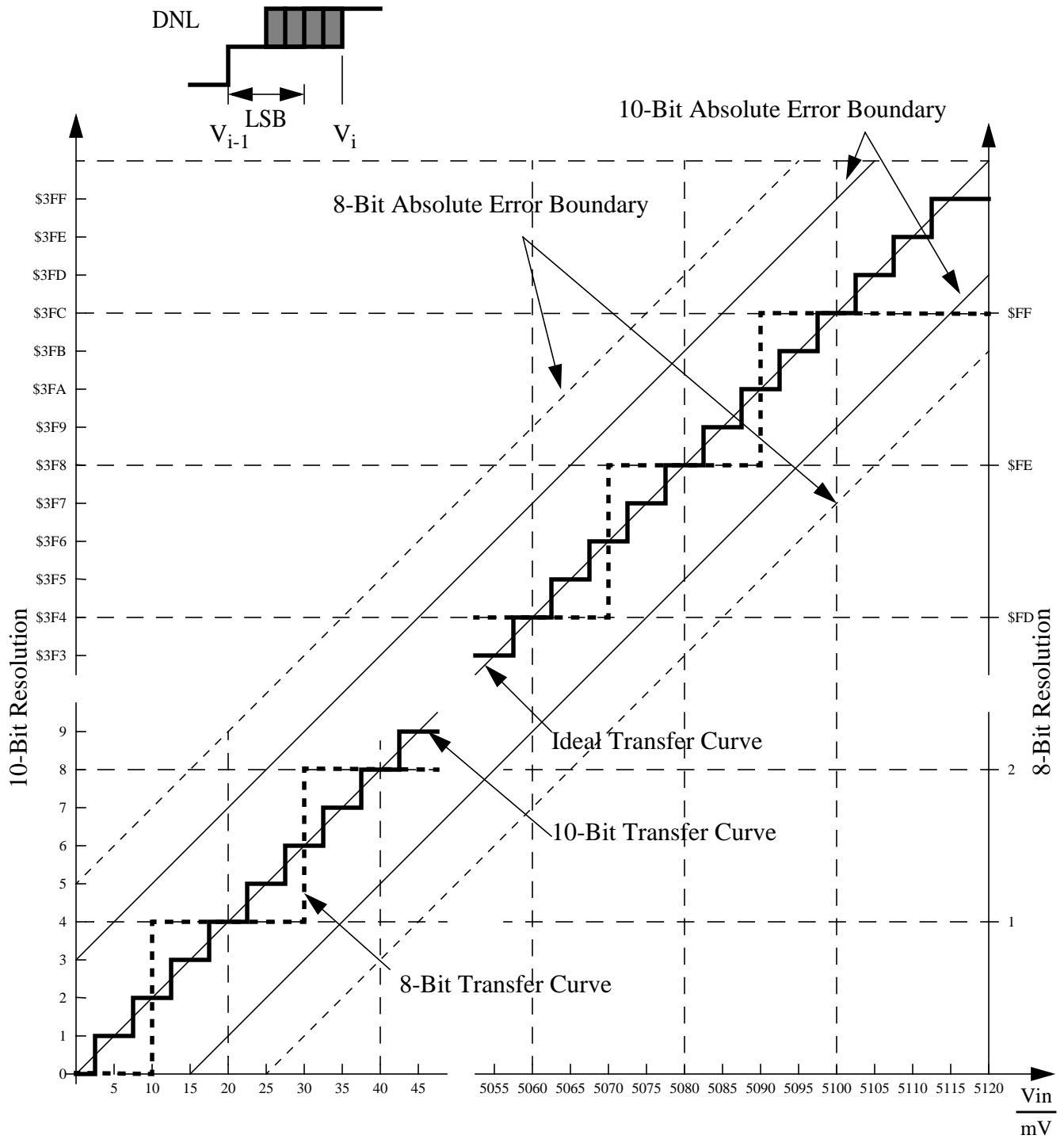


Figure A-1 ATD Accuracy Definitions

NOTE: *Figure A-1 shows only definitions, for specification values refer to **Table A-10**.*

A.3 NVM, Flash and EEPROM

NOTE: Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP} .

The minimum program and erase times shown in **(Table A-11)** are calculated for maximum f_{NVMOP} and maximum f_{bus} . The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{\text{swpgm}} = 9 \cdot \frac{1}{f_{\text{NVMOP}}} + 25 \cdot \frac{1}{f_{\text{bus}}}$$

A.3.1.2 Row Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{\text{bwpgm}} = 4 \cdot \frac{1}{f_{\text{NVMOP}}} + 9 \cdot \frac{1}{f_{\text{bus}}}$$

The time to program a whole row is:

$$t_{\text{brpgm}} = t_{\text{swpgm}} + 31 \cdot t_{\text{bwpgm}}$$

Row programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx \text{location} \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11 NVM Timing Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|--|--------------|----------------------|-----|-----------------------|-----------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | D | External Oscillator Clock | f_{NVMOSC} | 0.5 | | 50 ¹ | MHz |
| 2 | D | Bus frequency for Programming or Erase Operations | f_{NVMBUS} | 1 | | | MHz |
| 3 | D | Operating Frequency | f_{NVMOP} | 150 | | 200 | kHz |
| 4 | P | Single Word Programming Time | t_{swpgm} | 46 ² | | 74.5 ³ | μ s |
| 5 | D | Flash Row Programming consecutive word ⁴ | t_{bwpgm} | 20.4 ⁽²⁾ | | 31 ⁽³⁾ | μ s |
| 6 | D | Flash Row Programming Time for 32 Words ⁽⁴⁾ | t_{brpgm} | 678.4 ⁽²⁾ | | 1035.5 ⁽³⁾ | μ s |
| 7 | P | Sector Erase Time | t_{era} | 20 ⁵ | | 26.7 ⁽³⁾ | ms |
| 8 | P | Mass Erase Time | t_{mass} | 100 ⁽⁵⁾ | | 133 ⁽³⁾ | ms |
| 9 | D | Blank Check Time Flash per block | t_{check} | 11 ⁶ | | 32778 ⁷ | t_{cyc} |
| 10 | D | Blank Check Time EEPROM per block | t_{check} | 11 ⁽⁶⁾ | | 1034 ⁽⁷⁾ | t_{cyc} |

NOTES:

- Restrictions for oscillator in crystal mode apply!
- Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus} .
- Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus} . Refer to formulae in Sections **Section A.3.1.1 Single Word Programming-** **Section A.3.1.4 Mass Erase** for guidance.
- Row Programming operations are not applicable to EEPROM
- Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP} .
- Minimum time, if first word in the array is not blank
- Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

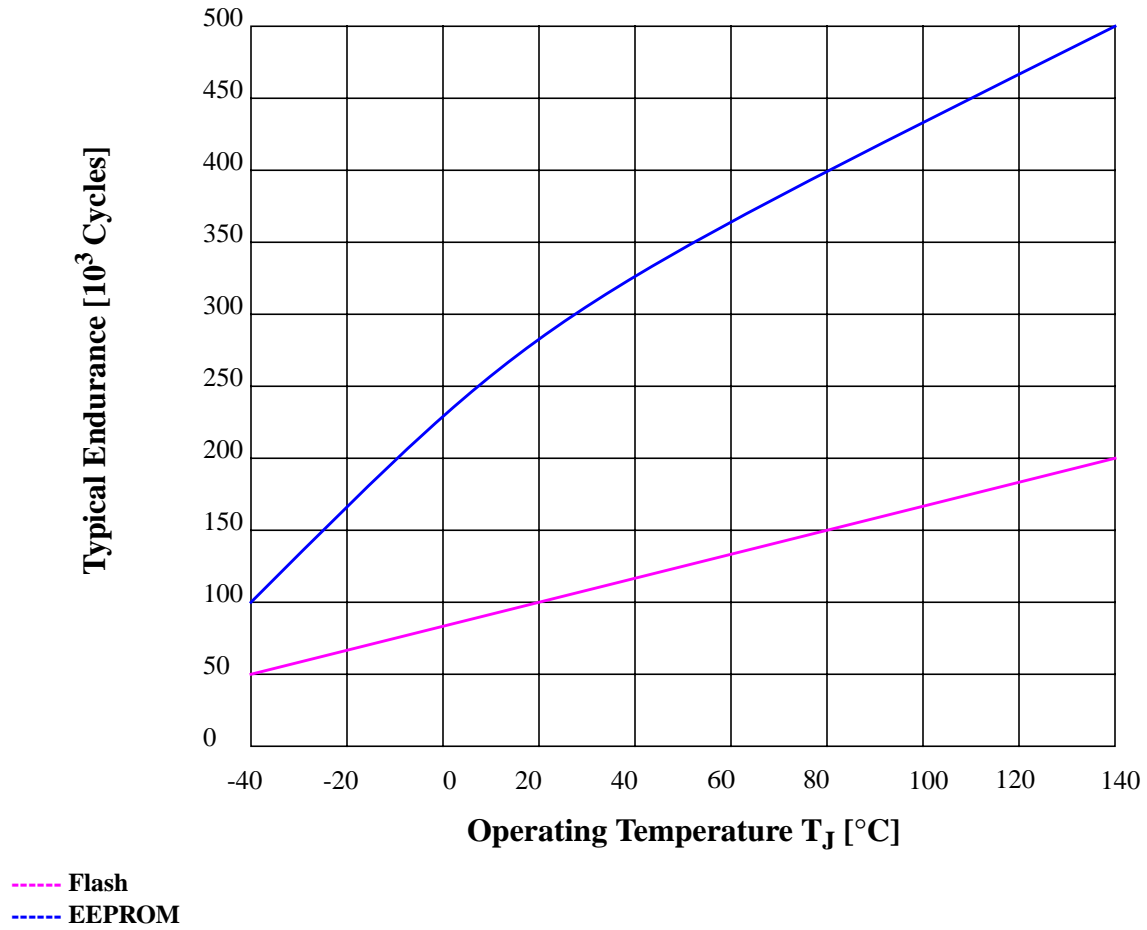
Table A-12 NVM Reliability Characteristics¹

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|--|--------------|---------|-------------|-----|--------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| Flash Reliability Characteristics | | | | | | | |
| 1 | C | Data retention after 10,000 program/erase cycles at an average junction temperature of $T_{Javg} \leq 85^{\circ}\text{C}$ | t_{FLRET} | 15 | 100^2 | — | Years |
| 2 | C | Data retention with <100 program/erase cycles at an average junction temperature $T_{Javg} \leq 85^{\circ}\text{C}$ | | 20 | 100^2 | — | |
| 3 | C | Number of program/erase cycles ($-40^{\circ}\text{C} \leq T_J \leq 0^{\circ}\text{C}$) | n_{FL} | 10,000 | — | — | Cycles |
| 4 | C | Number of program/erase cycles ($0^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$) | | 10,000 | $100,000^3$ | — | |
| EEPROM Reliability Characteristics | | | | | | | |
| 5 | C | Data retention after up to 100,000 program/erase cycles at an average junction temperature of $T_{Javg} \leq 85^{\circ}\text{C}$ | t_{EEPRET} | 15 | 100^2 | — | Years |
| 6 | C | Data retention with <100 program/erase cycles at an average junction temperature $T_{Javg} \leq 85^{\circ}\text{C}$ | | 20 | 100^2 | — | |
| 7 | C | Number of program/erase cycles ($-40^{\circ}\text{C} \leq T_J \leq 0^{\circ}\text{C}$) | n_{EEP} | 10,000 | — | — | Cycles |
| 8 | C | Number of program/erase cycles ($0^{\circ}\text{C} < T_J \leq 140^{\circ}\text{C}$) | | 100,000 | $300,000^3$ | — | |

NOTES:

- T_{Javg} will not exceed 85°C considering a typical temperature profile over the lifetime of a consumer, industrial or automotive application.
- Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, please refer to Engineering Bulletin EB618.
- Spec table quotes typical endurance evaluated at 25°C for this product family, typical endurance at various temperature can be estimated using the graph below. For additional information on how Freescale defines Typical Endurance, please refer to Engineering Bulletin EB619.

Figure A-2 Typical Endurance vs Temperature



A.4 Voltage Regulator

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed.

Table A-13 Voltage Regulator Recommended Load Capacitances

| Rating | Symbol | Min | Typ | Max | Unit |
|-----------------------------|-----------------|-----|-----|-----|------|
| Load Capacitance on VDD1, 2 | C_{LVDD} | | 220 | | nF |
| Load Capacitance on VDDPLL | $C_{LVDDfcPLL}$ | | 220 | | nF |

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

(Table A-14) summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-14 Startup Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|---|-------------|------|-----|------|-----------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | T | POR release level | V_{PORR} | | | 2.07 | V |
| 2 | T | POR assert level | V_{PORA} | 0.97 | | | V |
| 3 | D | Reset input pulse width, minimum input time | PW_{RSTL} | 2 | | | t_{osc} |
| 4 | D | Startup from Reset | n_{RST} | 192 | | 196 | n_{osc} |
| 5 | D | Interrupt pulse width, \overline{IRQ} edge-sensitive mode | PW_{IRQ} | 20 | | | ns |
| 6 | D | Wait recovery startup time | t_{WRS} | | | 14 | t_{cyc} |

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc} .

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when V_{DD5} is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{WRS} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. By asserting the \overline{XCLKS} input during reset this oscillator can be bypassed allowing the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC} . The device also features a clock monitor. A

Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA} .

Table A-15 Oscillator Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|--|-----------------|------------------------|-------|------------------------|---------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1a | C | Crystal oscillator range (Colpitts) | f_{OSC} | 0.5 | | 16 | MHz |
| 1b | C | Crystal oscillator range (Pierce) ¹ | f_{OSC} | 0.5 | | 40 | MHz |
| 2 | P | Startup Current | i_{OSC} | 100 | | | μA |
| 3 | C | Oscillator start-up time (Colpitts) | t_{UOSC} | | 8^2 | 100^3 | ms |
| 4 | D | Clock Quality check time-out | t_{CQOUT} | 0.45 | | 2.5 | s |
| 5 | P | Clock Monitor Failure Assert Frequency | f_{CMFA} | 50 | 100 | 200 | KHz |
| 6 | P | External square wave input frequency ⁴ | f_{EXT} | 0.5 | | 50 | MHz |
| 7 | D | External square wave pulse width low | t_{EXTL} | 9.5 | | | ns |
| 8 | D | External square wave pulse width high | t_{EXTH} | 9.5 | | | ns |
| 9 | D | External square wave rise time | t_{EXTR} | | | 1 | ns |
| 10 | D | External square wave fall time | t_{EXTF} | | | 1 | ns |
| 11 | D | Input Capacitance (EXTAL, XTAL pins) | C_{IN} | | 7 | | pF |
| 12 | C | DC Operating Bias in Colpitts Configuration on EXTAL Pin | V_{DCBIAS} | | 1.1 | | V |
| 13 | P | EXTAL Pin Input High Voltage ⁴ | $V_{IH,EXTAL}$ | $0.75 \cdot V_{DDPLL}$ | | | V |
| | T | EXTAL Pin Input High Voltage ⁴ | $V_{IH,EXTAL}$ | | | $V_{DDPLL} + 0.3$ | V |
| 14 | P | EXTAL Pin Input Low Voltage ⁴ | $V_{IL,EXTAL}$ | | | $0.25 \cdot V_{DDPLL}$ | V |
| | T | EXTAL Pin Input Low Voltage ⁴ | $V_{IL,EXTAL}$ | $V_{SSPLL} - 0.3$ | | | V |
| 15 | C | EXTAL Pin Input Hysteresis ⁴ | $V_{HYS,EXTAL}$ | | 250 | | mV |

NOTES:

1. Depending on the crystal a damping series resistor might be necessary
2. $f_{osc} = 4\text{MHz}$, $C = 22\text{pF}$.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. $\overline{XCLKS} = 0$ during reset

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL's Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

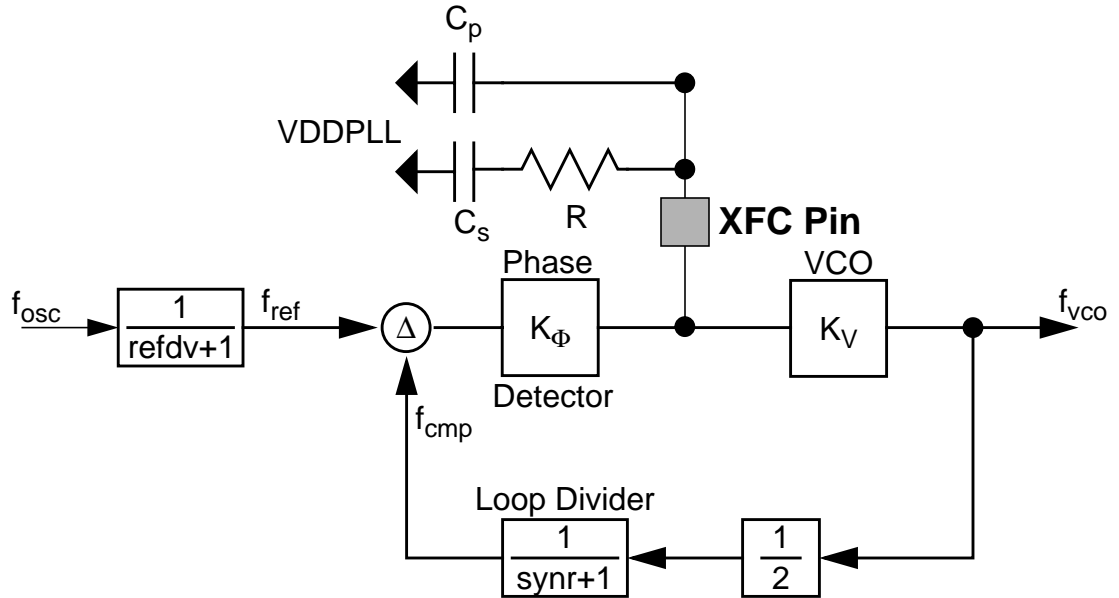


Figure A-3 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1 , f_1 and i_{ch} from **(Table A-16)**.

The grey boxes show the calculation for $f_{VCO} = 50\text{MHz}$ and $f_{ref} = 1\text{MHz}$. E.g., these frequencies are used for $f_{OSC} = 4\text{MHz}$ and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{VCO})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60 - 50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (\text{synr} + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C=10\text{KHz}$:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} = 2 \cdot \pi \cdot 50 \cdot 10\text{kHz} / (316.7\text{Hz}/\Omega) = 9.9\text{k}\Omega \approx 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) = 5.19\text{nF} \approx 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-3**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-4**.

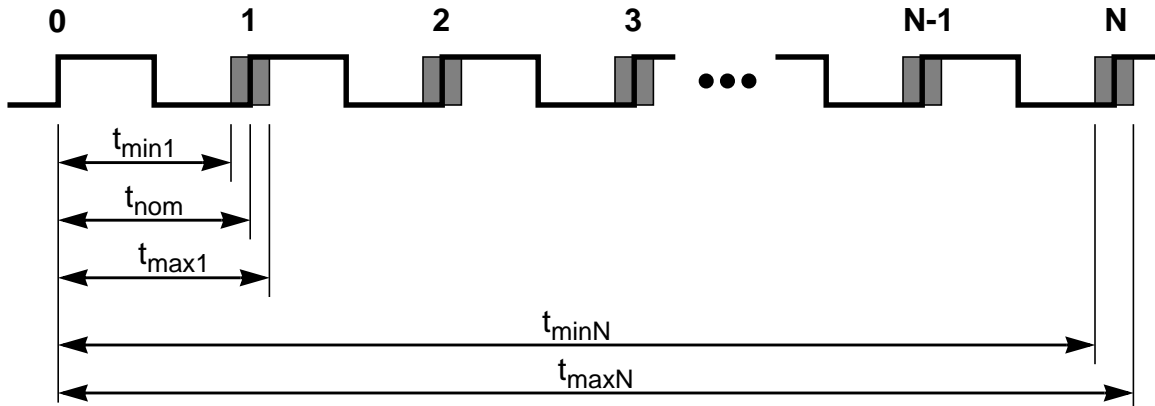


Figure A-4 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For $N < 100$, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

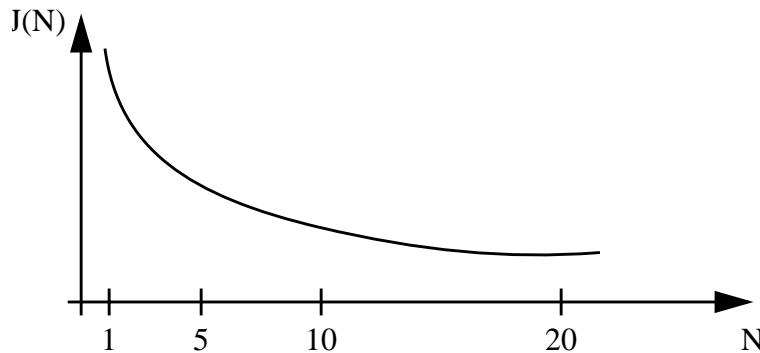


Figure A-5 Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-16 PLL Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|--|---|--|-------------------|-----|------|------|------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Self Clock Mode frequency | f_{SCM} | 1 | | 5.5 | MHz |
| 2 | D | VCO locking range | f_{VCO} | 8 | | 50 | MHz |
| 3 | D | Lock Detector transition from Acquisition to Tracking mode | $ \Delta_{trk} $ | 3 | | 4 | % ¹ |
| 4 | D | Lock Detection | $ \Delta_{Lock} $ | 0 | | 1.5 | % ⁽¹⁾ |
| 5 | D | Un-Lock Detection | $ \Delta_{unt} $ | 0.5 | | 2.5 | % ⁽¹⁾ |
| 6 | D | Lock Detector transition from Tracking to Acquisition mode | $ \Delta_{unt} $ | 6 | | 8 | % ⁽¹⁾ |
| 7 | C | PLLON Total Stabilization delay (Auto Mode) ² | t_{stab} | | 0.5 | | ms |
| 8 | D | PLLON Acquisition mode stabilization delay ⁽²⁾ | t_{acq} | | 0.3 | | ms |
| 9 | D | PLLON Tracking mode stabilization delay ⁽²⁾ | t_{al} | | 0.2 | | ms |
| 10 | D | Fitting parameter VCO loop gain | K_1 | | -100 | | MHz/V |
| 11 | D | Fitting parameter VCO loop frequency | f_1 | | 60 | | MHz |
| 12 | D | Charge pump current acquisition mode | $ i_{ch} $ | | 38.5 | | μA |
| 13 | D | Charge pump current tracking mode | $ i_{ch} $ | | 3.5 | | μA |
| 14 | C | Jitter fit parameter 1 ⁽²⁾ | j_1 | | | 1.1 | % |
| 15 | C | Jitter fit parameter 2 ⁽²⁾ | j_2 | | | 0.13 | % |

NOTES:

1. % deviation from target frequency
2. $f_{OSC} = 4\text{MHz}$, $f_{BUS} = 25\text{MHz}$ equivalent $f_{VCO} = 50\text{MHz}$: REFDV = #03, SYNRR = #018, Cs = 4.7nF, Cp = 470pF, Rs = 10K Ω .

A.6 MSCAN

Table A-17 MSCAN Wake-up Pulse Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted | | | | | | | |
|---|---|---------------------------------------|-----------|-----|-----|-----|---------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | MSCAN Wake-up dominant pulse filtered | t_{WUP} | | | 2 | μs |
| 2 | P | MSCAN Wake-up dominant pulse pass | t_{WUP} | 5 | | | μs |

A.7 SPI

A.7.1 Master Mode

Figure A-6 and Figure A-7 illustrate the master mode timing. Timing values are shown in (Table A-18).

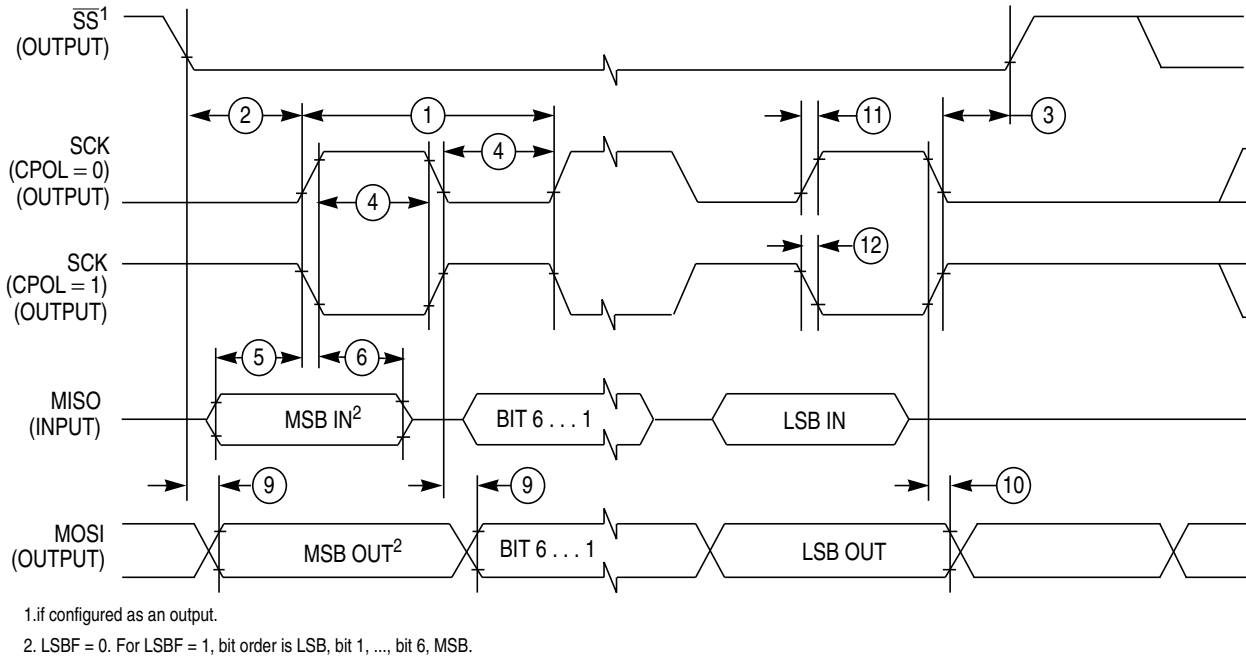
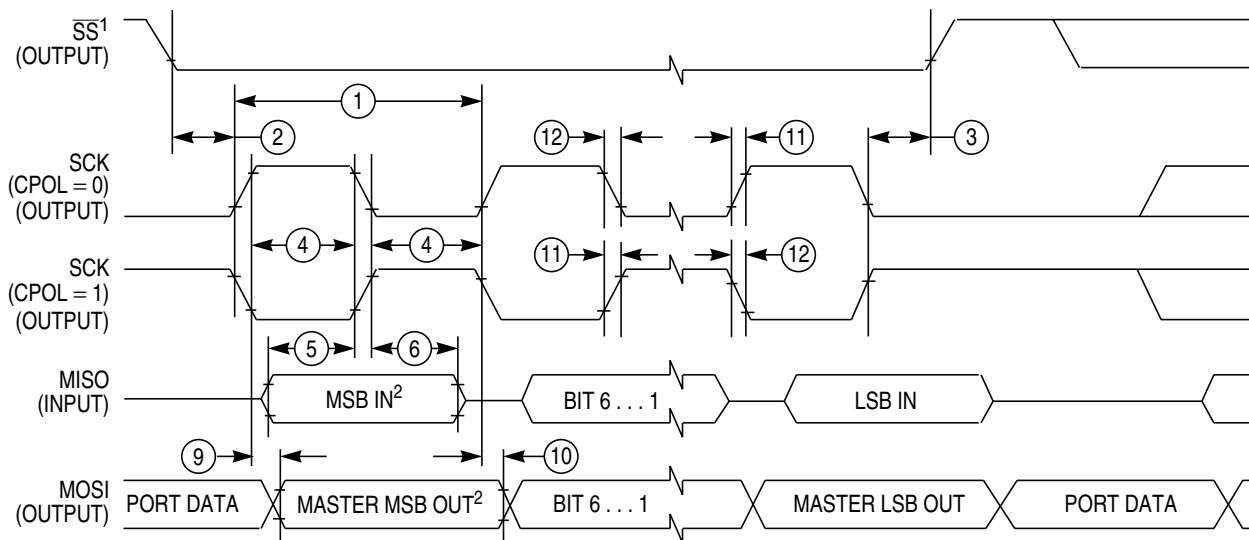


Figure A-6 SPI Master Timing (CPHA = 0)



1. If configured as output
 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7 SPI Master Timing (CPHA =1)

Table A-18 SPI Master Mode Timing Characteristics¹

Conditions are shown in (Table A-4) unless otherwise noted, C_{LOAD} = 200pF on all outputs

| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
|-----|---|--|-------------------|-----------------------|-----|-----------------------|------------------|
| 1 | P | Operating Frequency | f _{op} | DC | | 1/2 | f _{bus} |
| 1 | P | SCK Period t _{sck} = 1./f _{op} | t _{sck} | 4 | | 2048 | t _{bus} |
| 2 | D | Enable Lead Time | t _{lead} | 1/2 | | — | t _{sck} |
| 3 | D | Enable Lag Time | t _{lag} | 1/2 | | | t _{sck} |
| 4 | D | Clock (SCK) High or Low Time | t _{wsck} | t _{bus} - 30 | | 1024 t _{bus} | ns |
| 5 | D | Data Setup Time (Inputs) | t _{su} | 25 | | | ns |
| 6 | D | Data Hold Time (Inputs) | t _{hi} | 0 | | | ns |
| 9 | D | Data Valid (after SCK Edge) | t _v | | | 25 | ns |
| 10 | D | Data Hold Time (Outputs) | t _{ho} | 0 | | | ns |
| 11 | D | Rise Time Inputs and Outputs | t _r | | | 25 | ns |
| 12 | D | Fall Time Inputs and Outputs | t _f | | | 25 | ns |

NOTES:

1. The numbers 7, 8 in the column labeled "Num" are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in (Table A-19).

A.7.2 Slave Mode

Figure A-8 and Figure A-9 illustrate the slave mode timing. Timing values are shown in (Table A-19).

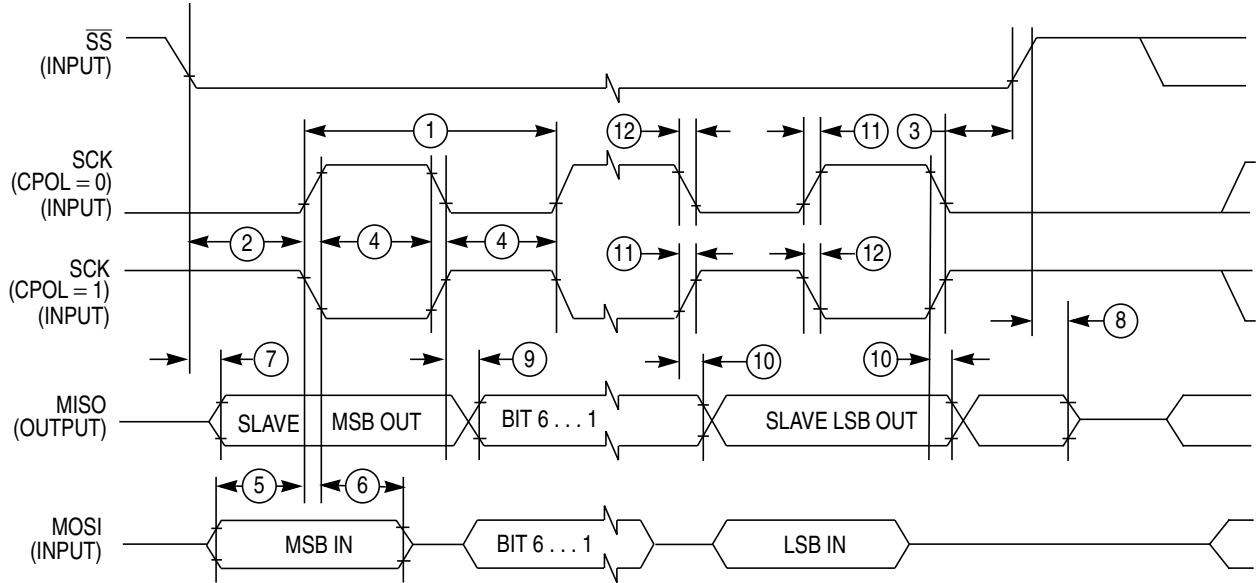


Figure A-8 SPI Slave Timing (CPHA = 0)

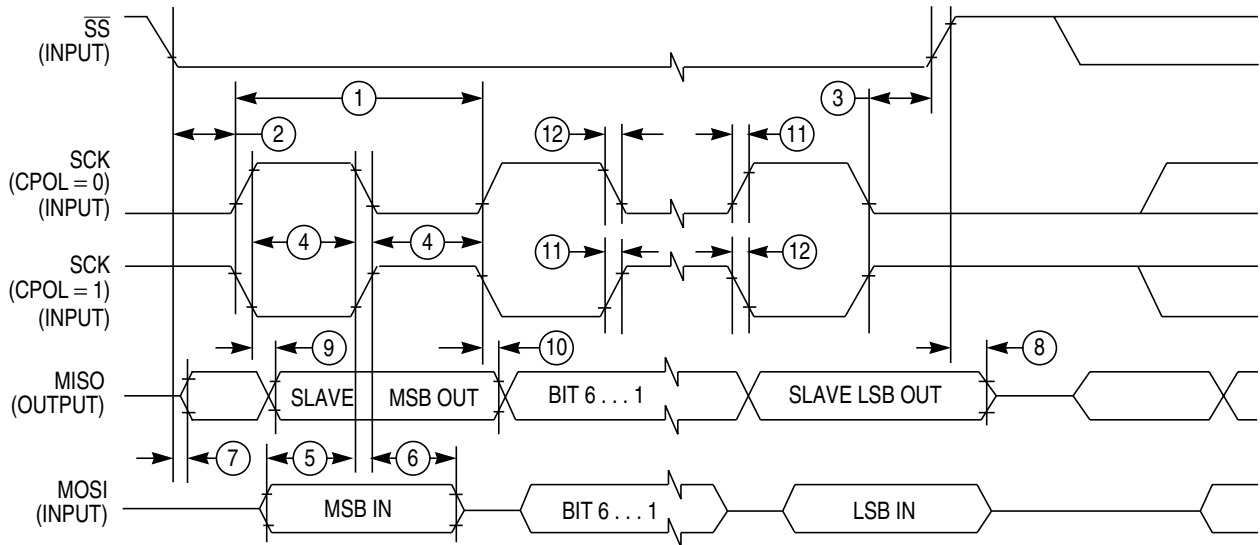


Figure A-9 SPI Slave Timing (CPHA = 1)

Table A-19 SPI Slave Mode Timing Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted, CLOAD = 200pF on all outputs | | | | | | | |
|--|---|----------------------------------|------------|----------------|-----|------|-----------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Operating Frequency | f_{op} | DC | | 1/4 | f_{bus} |
| 1 | P | SCK Period $t_{sck} = 1./f_{op}$ | t_{sck} | 4 | | 2048 | t_{bus} |
| 2 | D | Enable Lead Time | t_{lead} | 1 | | | t_{cyc} |
| 3 | D | Enable Lag Time | t_{lag} | 1 | | | t_{cyc} |
| 4 | D | Clock (SCK) High or Low Time | t_{wsck} | $t_{cyc} - 30$ | | | ns |
| 5 | D | Data Setup Time (Inputs) | t_{su} | 25 | | | ns |
| 6 | D | Data Hold Time (Inputs) | t_{hi} | 25 | | | ns |
| 7 | D | Slave Access Time | t_a | | | 1 | t_{cyc} |
| 8 | D | Slave MISO Disable Time | t_{dis} | | | 1 | t_{cyc} |
| 9 | D | Data Valid (after SCK Edge) | t_v | | | 25 | ns |
| 10 | D | Data Hold Time (Outputs) | t_{ho} | 0 | | | ns |
| 11 | D | Rise Time Inputs and Outputs | t_r | | | 25 | ns |
| 12 | D | Fall Time Inputs and Outputs | t_f | | | 25 | ns |

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-10** with the actual timing values shown on table (**Table A-20**). All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Multiplexed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

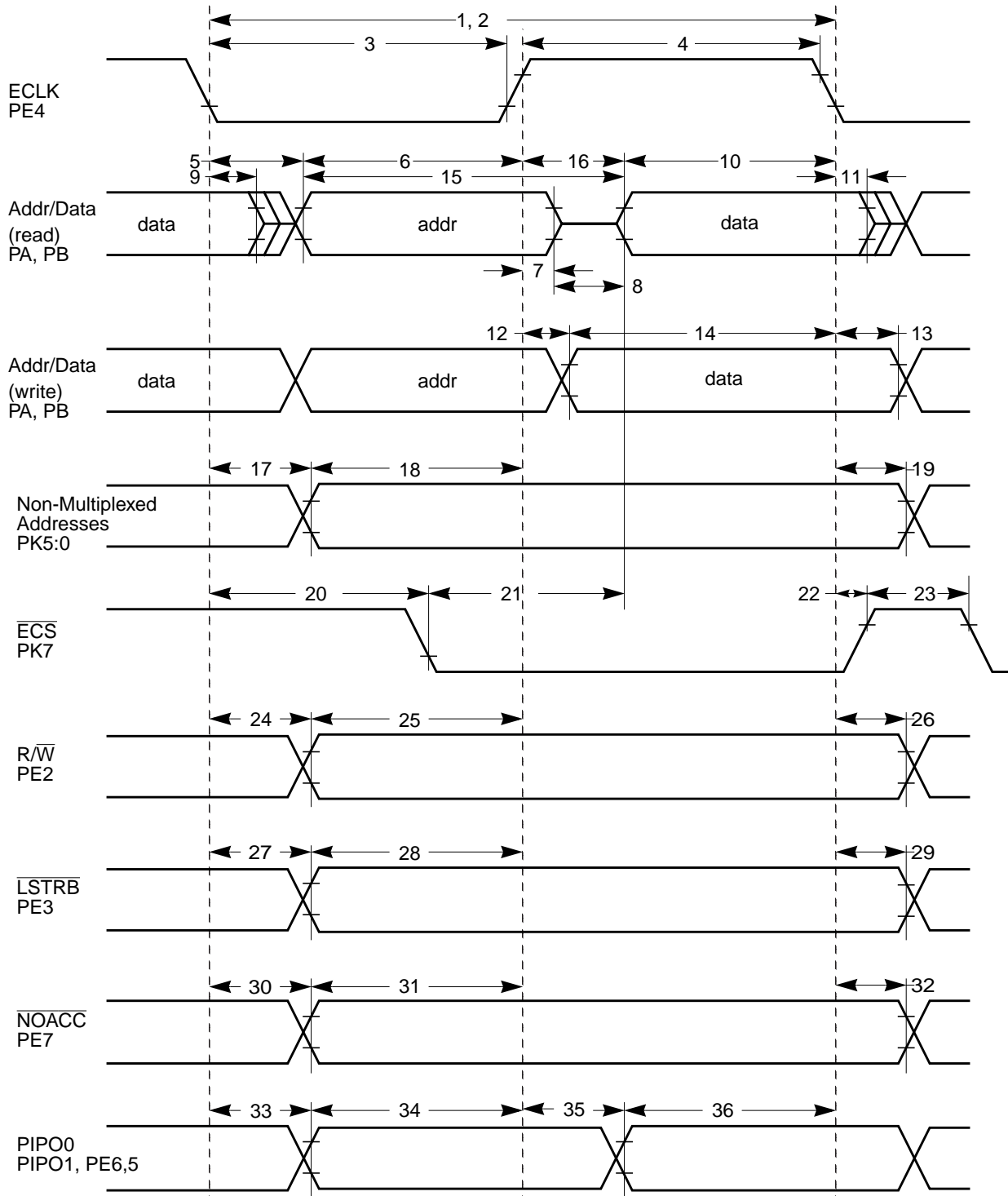


Figure A-10 General External Bus Timing

Table A-20 Expanded Bus Timing Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted, $C_{LOAD} = 50pF$ | | | | | | | |
|---|---|--|------------|-----|-----|------|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Frequency of operation (E-clock) | f_o | 0 | | 25.0 | MHz |
| 2 | P | Cycle time | t_{cyc} | 40 | | | ns |
| 3 | D | Pulse width, E low | PW_{EL} | 19 | | | ns |
| 4 | D | Pulse width, E high ¹ | PW_{EH} | 19 | | | ns |
| 5 | D | Address delay time | t_{AD} | | | 8 | ns |
| 6 | D | Address valid time to E rise ($PW_{EL}-t_{AD}$) | t_{AV} | 11 | | | ns |
| 7 | D | Muxed address hold time | t_{MAH} | 2 | | | ns |
| 8 | D | Address hold to data valid | t_{AHDS} | 7 | | | ns |
| 9 | D | Data hold to address | t_{DHA} | 2 | | | ns |
| 10 | D | Read data setup time | t_{DSR} | 13 | | | ns |
| 11 | D | Read data hold time | t_{DHR} | 0 | | | ns |
| 12 | D | Write data delay time | t_{DDW} | | | 7 | ns |
| 13 | D | Write data hold time | t_{DHW} | 2 | | | ns |
| 14 | D | Write data setup time ⁽¹⁾ ($PW_{EH}-t_{DDW}$) | t_{DSW} | 12 | | | ns |
| 15 | D | Address access time ⁽¹⁾ ($t_{cyc}-t_{AD}-t_{DSR}$) | t_{ACCA} | 19 | | | ns |
| 16 | D | E high access time ⁽¹⁾ ($PW_{EH}-t_{DSR}$) | t_{ACCE} | 6 | | | ns |
| 17 | D | Non-multiplexed address delay time | t_{NAD} | | | 6 | ns |
| 18 | D | Non-muxed address valid to E rise ($PW_{EL}-t_{NAD}$) | t_{NAV} | 15 | | | ns |
| 19 | D | Non-multiplexed address hold time | t_{NAH} | 2 | | | ns |
| 20 | D | Chip select delay time | t_{CSD} | | | 16 | ns |
| 21 | D | Chip select access time ⁽¹⁾ ($t_{cyc}-t_{CSD}-t_{DSR}$) | t_{ACCS} | 11 | | | ns |
| 22 | D | Chip select hold time | t_{CSH} | 2 | | | ns |
| 23 | D | Chip select negated time | t_{CSN} | 8 | | | ns |
| 24 | D | Read/write delay time | t_{RWD} | | | 7 | ns |
| 25 | D | Read/write valid time to E rise ($PW_{EL}-t_{RWD}$) | t_{RWV} | 14 | | | ns |
| 26 | D | Read/write hold time | t_{RWH} | 2 | | | ns |
| 27 | D | Low strobe delay time | t_{LSD} | | | 7 | ns |
| 28 | D | Low strobe valid time to E rise ($PW_{EL}-t_{LSD}$) | t_{LSV} | 14 | | | ns |
| 29 | D | Low strobe hold time | t_{LSH} | 2 | | | ns |
| 30 | D | NOACC strobe delay time | t_{NOD} | | | 7 | ns |
| 31 | D | NOACC valid time to E rise ($PW_{EL}-t_{NOD}$) | t_{NOV} | 14 | | | ns |

Table A-20 Expanded Bus Timing Characteristics

| Conditions are shown in (Table A-4) unless otherwise noted, C _{LOAD} = 50pF | | | | | | | |
|--|---|--|------------------|-----|-----|-----|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 32 | D | NOACC hold time | t _{NOH} | 2 | | | ns |
| 33 | D | IPIPO[1:0] delay time | t _{P0D} | 2 | | 7 | ns |
| 34 | D | IPIPO[1:0] valid time to E rise (PW _{EL} -t _{P0D}) | t _{P0V} | 11 | | | ns |
| 35 | D | IPIPO[1:0] delay time ⁽¹⁾ (PW _{EH} -t _{P1V}) | t _{P1D} | 2 | | 25 | ns |
| 36 | D | IPIPO[1:0] valid time to E fall | t _{P1V} | 11 | | | ns |

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DT128 packages.

B.2 112-pin LQFP package

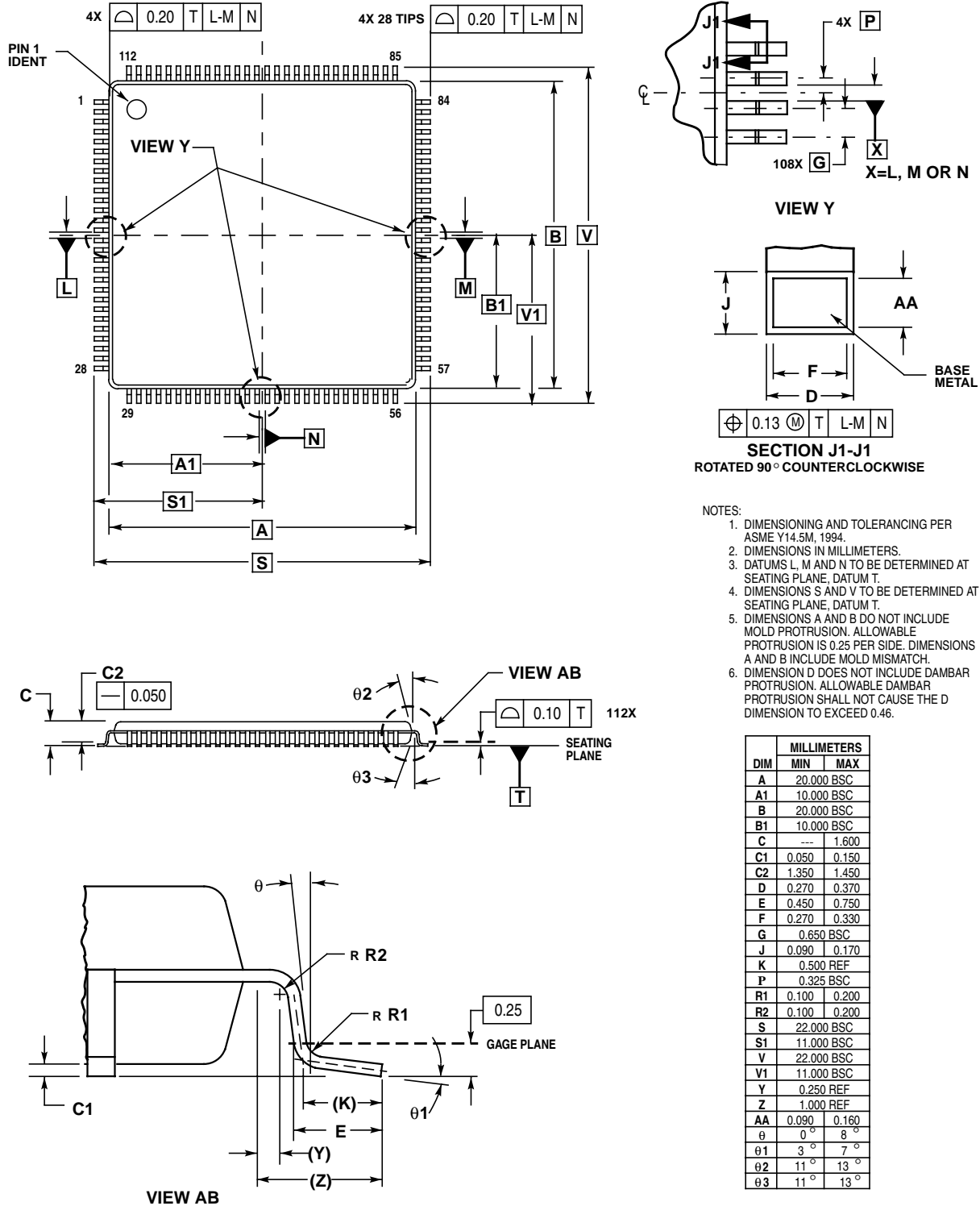


Figure 23-6 112-pin LQFP mechanical dimensions (case no. 987)

B.3 80-pin QFP package

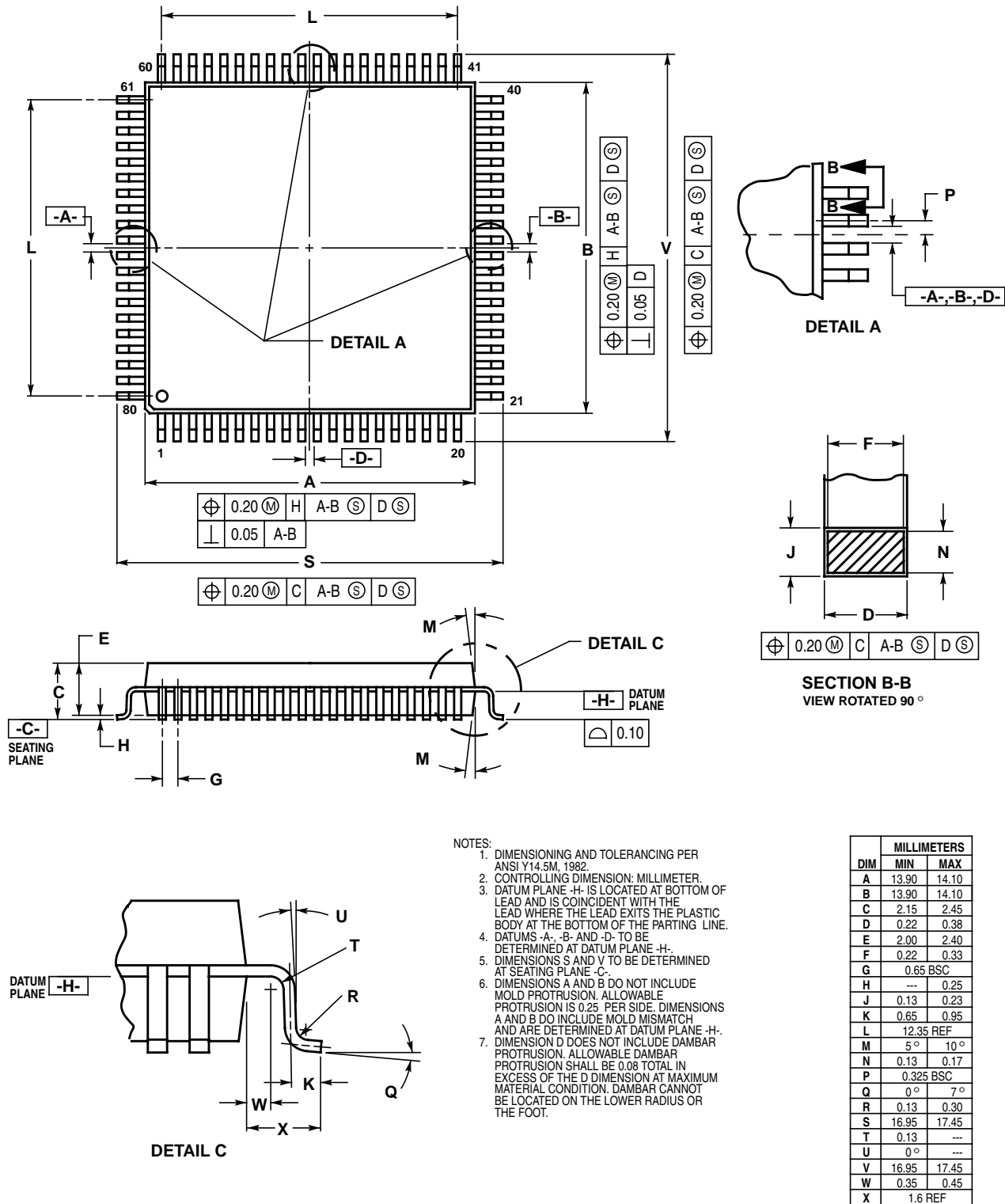


Figure 1 80-pin QFP Mechanical Dimensions (case no. 841B)

User Guide End Sheet

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