THE DATASHEET OF

PT6462A

PT6460 Series

EXCALIBUR

14-A 5-V Input Adjustable Integrated Switching Regulator

SLTS178B - JANUARY 2003 - REVISED JUNE 2003

Features

- 5 V Input
- 14 A Output Current
- Low-Profile (8mm)
- DSP Compatible
- >90 % Efficiency
- Adjustable Output Voltage
- On/Off Inhibit
- Pre-Bias Start-up Capability
- Over-Current Protection
- Output Remote Sense
- Optional Output Capacitor
- Small Footprint (0.64 in², Suffix 'N')
- Surface Mount Compatible
- IPC Lead Free 2

Description

The PT6460 Excalibur™ series of integrated switching regulators (ISRs) combines outstanding power density with a comprehensive list of features. They are an ideal choice for applications where board space is a premium and performance cannot be compromised. These modules provide a full 14 A of output current, yet are housed in a low-profile, 12-pin, package that is almost half the size of the previous product generation. The integral copper case construction requires no heatsink, and offers the advantages of solderability and a small footprint (0.64 in² for suffix 'N'). Both through-hole and surface mount pin configurations are available.

The PT6460 series operates from a 5-V input bus and provides a convenient point-of-load power source for the industry's latest high-performance DSPs and microprocessors. The series includes output voltage options as low as 1.0 VDC.

Other features include external output voltage adjustment, on/off inhibit, pre-bias startup, short circuit protection, and an output remote sense.

Ordering Information

PT6461❒	= 3.3 Volts
PT6462❒	= 2.5 Volts
PT6463❒	= 2.0 Volts
PT6464❒	= 1.8 Volts
PT6465❒	= 1.5 Volts
PT6466❒	= 1.2 Volts
PT6467❒	= 1.0 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(EPH)
Horizontal	**A**	(EPJ)
SMD	**C**	(EPK)

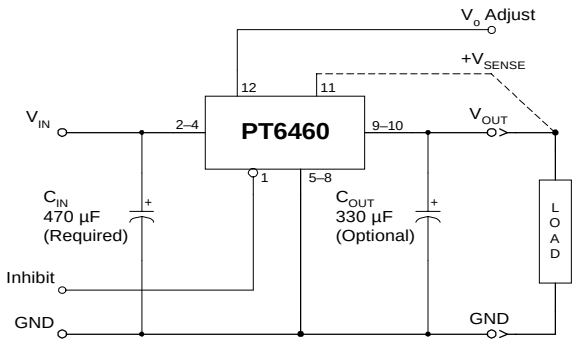
(Reference the applicable package code drawing for the dimensions and PC board layout)

Pin-Out Information

Pin	Function
1	Inhibit*
2	V_{in}
3	V_{in}
4	V_{in}
5	GND
6	GND
7	GND
8	GND
9	V_{out}
10	V_{out}
11	(+)Sense
12	V_o Adjust

** Denotes negative logic:*
Open = Output enabled
Ground = Output disabled

Standard Application



C_{in} = Required 470 µF
C_{out} = Optional 330 µF

Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =5 V, C_{in} =470 µF, C_{out} =0 µF, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	PT6460 SERIES Min	Typ	Max	Units
Output Current	I_o	V_{in} =5 V	0	—	14	A
Input Voltage Range	V_{in}	Over I_o range	4.5	—	5.5	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±10	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3	%V_o
Efficiency	η	I_o =10 A PT6461 (3.3 V)	—	94	—	%
		PT6462 (2.5 V)	—	93	—	
		PT6463 (2.0 V)	—	91	—	
		PT6464 (1.8 V)	—	90	—	
		PT6465 (1.5 V)	—	88	—	
		PT6466 (1.2 V)	—	86	—	
		PT6467 (1.0 V)	—	84	—	
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	—	25	—	mVpp
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, C_{out} =330 µF				
	t_{tr}	Recovery Time	—	50	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	100	—	mV
Over-Current Threshold	I_{TRIP}	Reset, followed by auto-recovery	—	27.5	—	A
Output Voltage Adjust	V_o adj		—	±15 (1)	—	%
Switching Frequency	f_s	Over V_{in} and I_o ranges	—	300	—	kHz
Inhibit Control (pin1)		Referenced to GND (pins 5–8)				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (2)	V
Input Low Voltage	V_{IL}		–0.2	—	0.8	
Input Low Current	I_{IL}	Pin 1 to GND	—	–10	—	µA
Inhibit Input Current	I_{in} inhibit	Pin 1 to GND	—	5	—	mA
External Input Capacitance	C_{in}		470 (3)	—	—	µF
External Output Capacitance	C_{out}		0	330 (4) (5)	3,300	µF
Operating Temperature Range	T_a	Over V_{in} range	–40 (5)	—	85 (6)	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case	—	—	215 (7)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign	8.0	—	—	10^6 Hrs
Mechanical Shock		Mil-STD-883D, Method 2002.3 Half Sine, mounted to a fixture	—	500	—	G
Mechanical Vibration		Mil-STD-883D, Method 2007.2, Suffix N	—	20 (8)	—	G
		20-2000 Hz, PCB mounted Suffixes A, C	—	20 (8)	—	
Weight	—	—	—	10	—	grams
Flammability	—	Materials meet UL 94V-0				

Notes: *(1) This is a typical value. For the adjustment limits of a specific model consult the related application note on output voltage adjustment.*
(2) The Inhibit control (pin 1) has an internal pull-up, and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended to control this input. See application notes for more information.
(3) A 470 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimumm of 0.7 Arms of ripple current.
(4) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.
(5) For operation below 0 °C, C_{OUT} should have stable characteristics. Use either low-ESR tantalum or Oscon® type capacitors.
(6) See SOA curves or consult factory for the appropriate derating.
(7) During solder reflow of SMD package version do not elevate the module case, pins, or internal component temperature above a peak of 215 °C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).
(8) The case pins on the through-hole package types (suffixes N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Descriptions

V_{IN}: The positive supply voltage input for the module with respect to the common *GND*.

V_{OUT}: This is the regulated output voltage from the module with respect to the common *GND*.

GND: The common node to which the input, output, and external control signals are referenced.

Inhibit*: This is an open-collector (open-drain) negative logic input that is referenced to *GND*. Pulling this pin low disables the module's output voltage. If *Inhibit** is left open-circuit, the output will be active whenever a valid input source is applied.

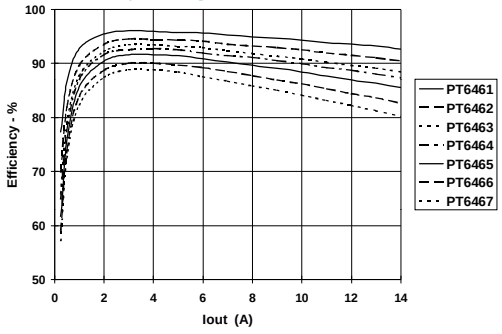
V_o Adjust: This pin is used to trim the output voltage over a typical range of ±15 % of nominal. The adjustment method uses an external resistor. The resistor is connected from *V_o Adjust* to either the *GND* or *(+)Sense*, in order to adjust the output either up or down, respectively. Consult the related application note for the adjust limits on a specific part.

Vsense: An external remote sense input is provided to allow the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vsense* should be connected to V_{OUT}. If desired, *Vsense* may also be left open circuit.

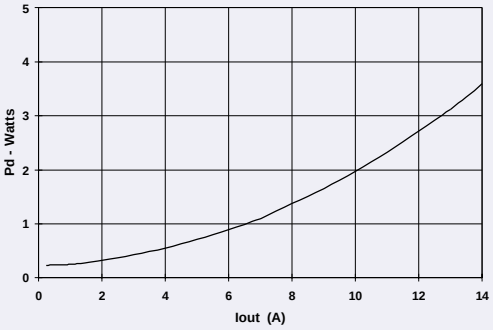
Typical Characteristics

Performance Data; V_{in} =5.0 V (See Note A)

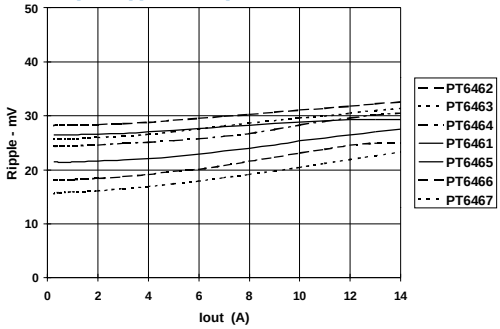
Efficiency vs Output Current



Power Dissipation vs Output Current



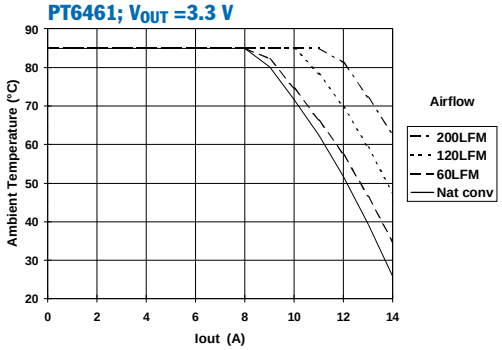
Output Ripple vs Output Current



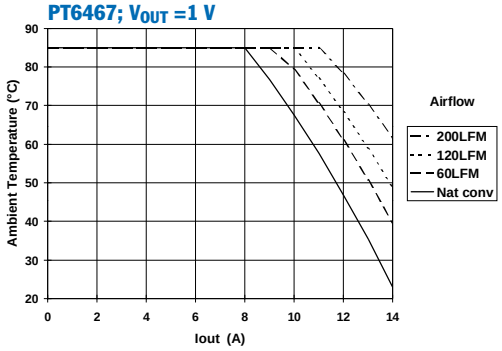
Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*

Safe Operating Curve, V_{in} =5 V (See Note B)

PT6461; V_{OUT} =3.3 V



PT6467; V_{OUT} =1 V



Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

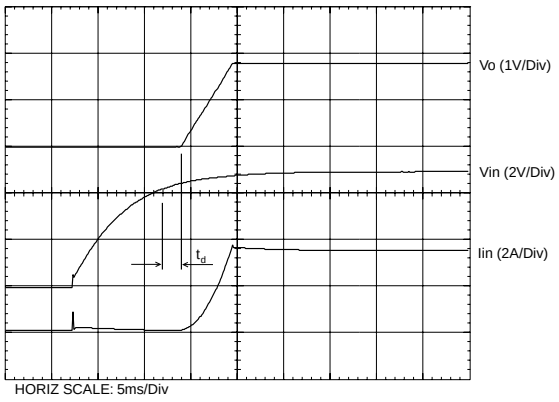
Operating Features and System Considerations for the PT6460 & PT6470 Regulator Series

The PT6460 (5-V input) and the PT6470 (3.3-V input) series of integrated switching regulators (ISRs) provide step-down voltage conversion for output loads of up to 14 A.

Power up & Soft-Start Timing

Following either the application of a valid input source voltage, or the removal of a ground signal to the *Inhibit** control pin (with input power applied), the regulator will initiate a soft-start power up. A soft start slows the rate at which the output voltage rises and introduces a short time delay, t_d (approximately 2 ms), into the power-up sequence. Figure 1-1 shows the power-up characteristic of a PT6464 (5-V input, 1.8-V output) with a 8.5-A load.

Figure 1-1



Over-Current Protection

To protect against load faults, these ISRs incorporate output over-current protection. Applying a load that exceeds the over-current threshold (see data sheet specifications) will cause the regulated output to shut down. Following shutdown the ISR will periodically attempt to recover by initiating a soft-start power-up. This is often described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Output Remote Sense

The *(+)Sense* pin allows the regulator to compensate for limited amounts of 'IR' voltage drop in the positive output connection resistance. This is the voltage drop incurred in the PCB trace between *Vout* (pins 9 & 10) of the regulator and the load some distance away. Connecting *(+)Sense* to the positive load terminal improves the voltage regulation at the load, particularly when the load current fluctuates. Although not recommended, leaving *(+)Sense* disconnected will not damage the regulator or the load circuitry. An internal 10 Ω resistor, connected between the sense pin and the output, keeps the output voltage in regulation.

With the sense pin connected, the difference between the voltage measured between V_{out} and *GND* at the regulator, and that measured from *(+)Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to 0.3 V maximum.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connections they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Pre-Bias Startup

In complex digital systems an external voltage can sometimes be present at the output of the regulator during power up. For example, this voltage may be backfed through a dual-supply logic component such as an FPGA or ASIC. Another path might be via a clamp diode (to a lower supply voltage) as part of a power-up sequencing implementation.

Although the PT6460 (5-V input) and PT6470 (3.3-V input) series of regulators will sink current under steady-state conditions, they will not do so during startup. This feature allows these regulators to start up while an external voltage is simultaneously applied to the output. To facilitate this feature the input voltage must always be greater than or equal to the output voltage throughout the power-up and power-down sequence. Startup includes both the application of a valid input source voltage, or the removal of a ground signal from the *Inhibit** control (pin 1) with a valid input source applied. The output of the regulator is also effectively off (tri-state), during the period that the *Inhibit** control is held low.

Note: If the pre-bias is greater than the nominal regulation voltage, the module will begin sinking current at the end of its soft-start power-up sequence. This could overstress the regulator if the current exceeds its rated output.

Capacitor Recommendations for the PT6460 & PT6470 Regulator Series

Input Capacitor:

The recommended input capacitor is determined by a minimum of 470 µF capacitance and 700 mA minimum ripple current rating.

Ripple current and <100 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of 2× (maximum DC voltage + AC ripple). This is necessary to insure reliability for input voltage bus applications.

Output Capacitors (Optional):

The ESR of the capacitors should be less than 150 mΩ. Electrolytic capacitors have marginal ripple performance at frequencies greater than 400 kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Preferred low ESR type capacitor part numbers are identified in Table 2-1.

Tantalum Capacitors(Optional Output Capacitors)

Tantalum type capacitors can be used for the output but only the AVX TPS, Sprague 593D/594/595, or Kemet T495/T510 series. These capacitors are recommended over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation, and lower ripple current capability. The TAJ series is less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0 °C.

Capacitor Table

Table 2-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 2-1: Input/Output Capacitors

Capacitor Vendor/ Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value(µF)	(ESR) Equivalent Series Resistance	Maximum Ripple Current @105°C (Irms)	Physical Size (mm)	Input Bus	Output Bus	Vendor Part Number
Panasonic FC (Radial)	16 V 10 V	470 560	0.09 Ω 0.09 Ω	755 mA 755 mA	10x12.5 10×12.5	1 1	1 1	EEUFC1C471 EEUFC1A561
 FK (SMT)	25 V 35 V	470 470	0.08 Ω 0.06 Ω	850 mA 1100 mA	10x10.2 12.5×13.5	1 1	1 1	EEVFK1E471P EEVFK1V471Q
United Chemi-con LXZ/LXV FX	 16 V 10 V 10 V	 470 680 680	 0.090 Ω 0.090 Ω 0.015 Ω	 760 mA 770 mA 4735 mA	 10x12.5 10x12.5 10×10.5	 1 1 1	 1 1 1	 LXZ16VB471M10X12LL LXZ10VB681M10X12LL 10FX680M
Nichicon PL/PM NX Series (SMT)	16 V 16 V 10 V	330 470 330	0.12÷2=0.06 Ω 0.09 Ω 0.024 Ω	745 mA 770 mA 3770 mA	10x12.5 10x15 10x8	2 1 2	1 1 1	UPM1C331MPH6 UPM1C 471MPH6 PNX1A330MCAR1GS
Sanyo-Os-con SP SVP (SMT)	10 V 10 V	470 560	0.015 Ω 0.013 Ω	>4500 mA >5200 mA	10×10.5 11×12.7	1 1	1 1	10SP470M 10SVP560M
AVX Tantalum TPS (SMT)	10 V 10 V	470 470	0.045 Ω 0.060 Ω	1723 mA 1826 mA	7.3L×5.7W ×4.1H	1 1	1 1	TPSE477M010R0045 TPSV477M010R0060
Kemet Polymer Tantalum T520/T530 (SMT)	10 V 10 V	330 330	0.040 Ω 0.015 Ω	1800 mA >3800 mA	4.3W×7.3L ×4.0H	2 2	1 1	T520X337M010AS T530X337M010AS
Sprague Tantalum 594D (SMT)	10 V	680	0.090 Ω	1660 mA	7.2L×6W ×4.1H	1	1	595D687X0010R2T

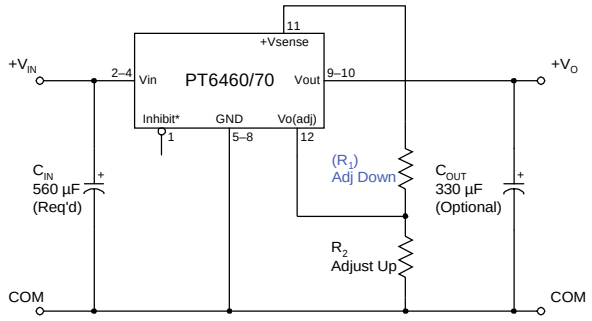
Adjusting the Output Voltage of the PT6460 & PT6470 ISR Series

The output voltage of the PT6460 (5-V input) and the PT6470 (3.3-V input) series of power modules may be adjusted higher or lower than the pre-set voltage. The adjustment method requires a single external resistor. The value of the resistor can either be calculated using the formulas given below, or simply selected from the range of values given in Table 3-2. Table 3-1 gives the allowable adjustment range for each model as V_a (min) and V_a (max). Refer to Figure 3-1 for the placement of the required resistor. Resistor R_1 adjusts the output voltage up, and the resistor (R_2) adjusts it down.

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_2, between *V_o Adjust* (pin 12) and *GND* (pin 5).

Adjust Down: Add a resistor (R_1), between *V_o Adjust* (pin 12) and *+Vsense* (pin 11).

Figure 3-1



The values of (R_1) [adjust down], and R_2 [adjust up], can be calculated using the following formulas. Refer to Figure 3-1 for the placement of the required resistor; either (R_1) or R_2 as appropriate.

$$(R_1) = \frac{R_o\,(V_a - 0.8)}{V_o - V_a} - R_s \quad k\Omega$$

$$R_2 = \frac{0.8\,R_o}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value from Table 3-1
R_s = The series resistance from Table 3-1

Notes:

1. Use a 1 % (or better) tolerance resistor in either the (R_1) or R_2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adj to either GND or V_{out}. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. If the remote sense feature is not being used, the adjust resistor (R_1) can also be connected to *V_{out}*, (pins 9–10) instead of *$+V_{sense}$*.
4. The PT6472 may not be adjusted higher than the nominal output voltage of 2.5 V. There is insufficient input voltage to allow for any increase in output voltage.

Table 3-1

ISR OUTPUT VOLTAGE ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt. Nos.							
5-V Bus:	**PT6461**	**PT6462**	**PT6463**	**PT6464**	**PT6465**	**PT6466**	**PT6467**
3.3-V Bus:	**N/A**	**PT6472**	**PT6473**	**PT6474**	**PT6475**	**PT6476**	**PT6477**
V_o (nom)	3.3 V	2.5 V	2.0 V	1.8 V	1.5 V	1.2 V	1 V
V_a (min)	2.6 V	2.0 V	1.66 V	1.52 V	1.31 V	1.1 V	0.95 V
V_a (max)	3.63 V	2.8 V *	2.32 V	2.1 V	1.82 V	1.52 V	1.32 V
R_o (kΩ)	10.2	10.7	10.0	10.2	9.76	10.0	10.2
R_s (kΩ)	24.9	24.9	24.9	24.9	24.9	24.9	24.9

** The PT6472 may not be adjusted higher than its nominal output voltage of 2.5 V. See note 4*

Table 3-2

ISR ADJUSTMENT RESISTOR VALUES									
Series Pt. Nos.									
5.0V Bus:	**PT6461**	**PT6462**			**PT6463**	**PT6464**	**PT6465**	**PT6466**	**PT6467**
3.3V Bus:	**N/A**	**PT6472**			**PT6473**	**PT6474**	**PT6475**	**PT6476**	**PT6477**
V_o (nom)	**3.3 V**	**2.5 V**			**2.0 V**	**1.8 V**	**1.5 V**	**1.2 V**	**1.0V**
V_a (req.d)				**V_a (req.d)**					
3.60	2.3 kΩ			2.300	1.8 kΩ				
3.55	7.7 kΩ			2.250	7.1 kΩ				
3.50	15.9 kΩ			2.200	15.1 kΩ				
3.45	29.5 kΩ			2.150	28.4 kΩ				
3.40	56.7 kΩ			2.100	55.1 kΩ	2.3 kΩ			
3.35	138.0 kΩ			2.050	135.0 kΩ	7.7 kΩ			
3.30				2.000		15.9 kΩ			
3.25	(475.0) kΩ			1.950	(205.0) kΩ	29.5 kΩ			
3.20	(220.0) kΩ			1.900	(85.1) kΩ	56.7 kΩ			
3.15	(135.0) kΩ			1.850	(45.1) kΩ	138.0 kΩ			
3.10	(92.4) kΩ			1.800	(25.1) kΩ		1.1 kΩ		
3.05	(66.9) kΩ			1.750	(13.1) kΩ	(169.0) kΩ	6.3 kΩ		
3.00	(49.9) kΩ			1.700	(5.1) kΩ	(66.9) kΩ	14.1 kΩ		
2.95	(37.5) kΩ			1.650		(32.9) kΩ	27.2 kΩ		
2.90	(28.6) kΩ			1.600		(15.9) kΩ	53.2 kΩ		
2.85	(21.6) kΩ			1.550		(5.7) kΩ	131.0 kΩ		
2.80	(15.9) kΩ	3.6 kΩ		1.500				1.8 kΩ	
2.75	(11.3) kΩ	9.3 kΩ		1.475			(239.0) kΩ	4.2 kΩ	
2.70	(7.4) kΩ	17.9 kΩ		1.450			(102.0) kΩ	7.1 kΩ	
2.65	(4.1) kΩ	32.2 kΩ		1.425			(56.4) kΩ	10.7 kΩ	
2.60	(1.3) kΩ	60.7 kΩ		1.400			(33.7) kΩ	15.1 kΩ	
2.550		146.0 kΩ		1.375			(20.0) kΩ	20.8 kΩ	
2.500				1.350			(10.9) kΩ	28.4 kΩ	
2.450	See note 4	(328.0) kΩ		1.325			(4.4) kΩ	39.1 kΩ	
2.400		(146.0) kΩ		1.300				55.1 kΩ	2.3 kΩ
2.350		(85.7) kΩ		1.275				81.8 kΩ	4.8 kΩ
2.300		(55.3) kΩ		1.250				135.0 kΩ	7.7 kΩ
2.250		(37.2) kΩ		1.225				295.0 kΩ	11.4 kΩ
2.200		(25.0) kΩ		1.200					15.9 kΩ
2.150		(16.4) kΩ		1.175				(125.0) kΩ	21.7 kΩ
2.100		(9.9) kΩ		1.150				(45.1) kΩ	29.5 kΩ
2.050		(4.8) kΩ		1.125				(18.4) kΩ	40.4 kΩ
2.000		(0.8) kΩ		1.100				(5.1) kΩ	56.7 kΩ
				1.075					83.9 kΩ
				1.050					138.0 kΩ
				1.025					302.0 kΩ
				1.000					
				0.975					(46.5) kΩ
				0.950					(5.7) kΩ

R_1 = Black R_2 = (Blue)

Using the Inhibit Control of the PT6460 & PT6470 Series of Step-Down ISRs

The PT6460 (5-V input) and the PT6470 (3.3-V input) series of integrated switching regulators (ISRs) provide step-down voltage conversion for output loads of up to 14 A. For applications that require the output voltage to be held off, these ISRs incorporate an *Inhibit** control (pin 1). The *Inhibit** control input can be used for power-up sequencing or whenever there is a requirement for the output voltage from the ISR to be turned off.

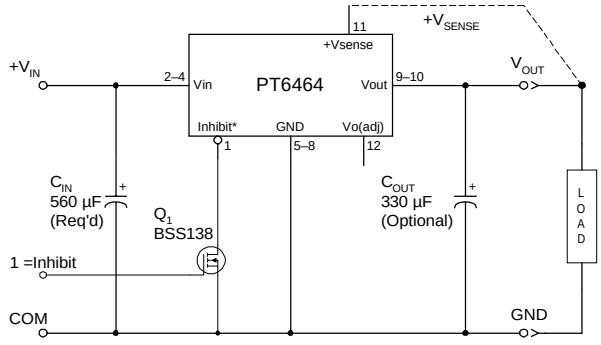
The ISR functions normally with pin 1 open circuit, providing a regulated output whenever a valid source voltage is applied between V_{in} (pins 2–3) and *GND* (pins 5–8). When a low-level ground signal is applied to pin 1, the regulator output is turned off [2] and the input current is significantly reduced [3].

Figure 4-1 shows the typical application of the *Inhibit** function. Note the discrete transistor, Q_1. The *Inhibit** control has its own internal pull-up to V_{in} potential. An open-collector or open-drain device is recommended to control this input [1]. The voltage thresholds are given in Table 4-1.

Table 4-1; Inhibit Control Requirements

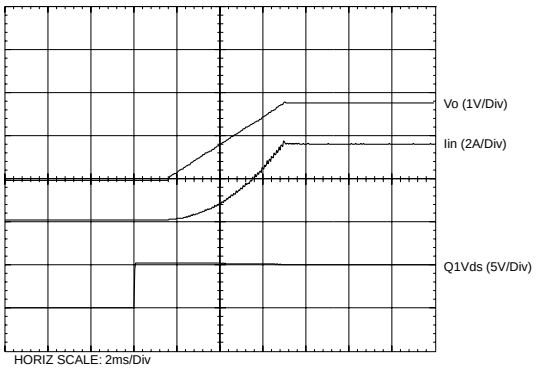
Parameter	Min	Typ	Max
Enable (V_{IH})	V_{in} – 0.5 V	—	Open
Disable (V_{IL})	–0.2 V	—	+0.8 V
I_{IL}	—	–0.2 mA	—

Figure 4-1



Turn-On Time: In the circuit of Figure 4-1, turning Q_1 on applies a low-voltage to the *Inhibit** control (pin 1) and disables the output of the regulator [2]. If Q_1 is then turned off, the ISR executes a soft-start power up. Power up consists of a short delay (approx. 2 msec), followed by a period in which the output voltage rises to the full regulation voltage. The module produces a regulated output voltage within 10 msec. Figure 4-2 shows the typical rise in both the output voltage and input current for a PT6464 (1.8 V), following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 5VDC input voltage, and 8.5-A load.

Figure 4-2



Notes:

1. Use an open-collector device with a breakdown voltage of at least 10 V (preferably a discrete transistor) for the *Inhibit** control input. A pull-up resistor is not necessary. To disable the output voltage the control pin should be pulled low to less than +0.8 VDC.
2. When a ground signal is applied to the *Inhibit** control (pin 1) the module output is effectively turned off (tri-state). The output voltage decays to zero as the load impedance discharges the output capacitors.
3. When the output is disabled via the *Inhibit** pin, the input current is reduced to approximately 5 to 10 mA.

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