



**THE DATASHEET OF
PI74ALVCH16501A**



18-Bit Universal Bus Transceiver With 3-State Outputs

Product Features

- PI74ALVCH16501 is designed for low voltage operation
- $V_{CC} = 2.3V$ to $3.6V$
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce)
< $0.8V$ at $V_{CC} = 3.3V, T_A = 25^\circ C$
- Typical V_{OHV} (Output V_{OH} Undershoot)
< $2.0V$ at $V_{CC} = 3.3V, T_A = 25^\circ C$
- Bus Hold retains last active bus state during 3-STATE eliminating the need for external pullup resistors
- Industrial operation at $-40^\circ C$ to $+85^\circ C$
- Packages available:
 - 48-pin 240 mil wide plastic TSSOP (A)
 - 48-pin 300 mil wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The 18-bit PI74ALVCH16501 universal bus transceiver is designed for 2.3V to 3.6V V_{CC} operation.

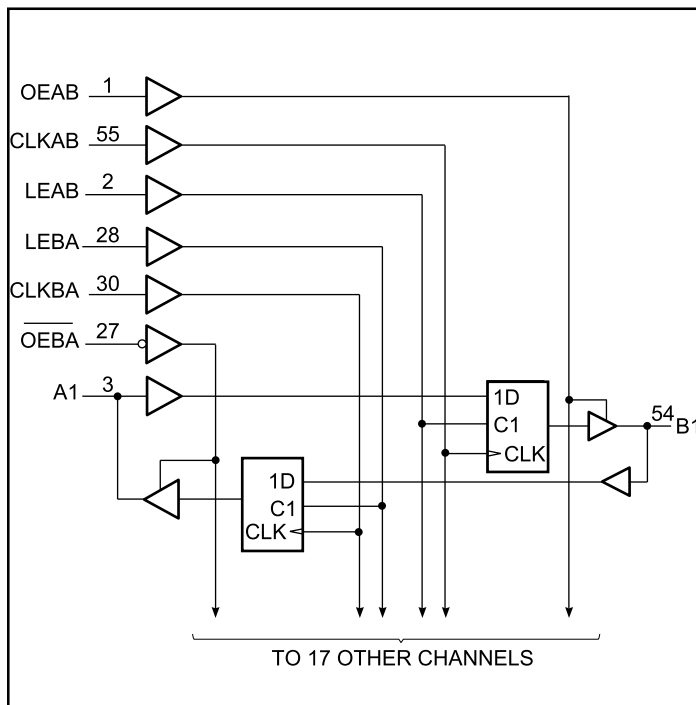
Data flow in each direction is controlled by Output Enable (OEAB and \overline{OEBA}), Latched Enable (LEAB and LEBA), and CLOCK (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is LOW, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CLKBA. The Output Enables are complementary (OEAB is active HIGH and \overline{OEBA} is active LOW).

To ensure the high-impedance state during power up or power down, OEBA should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Logic Block Diagram



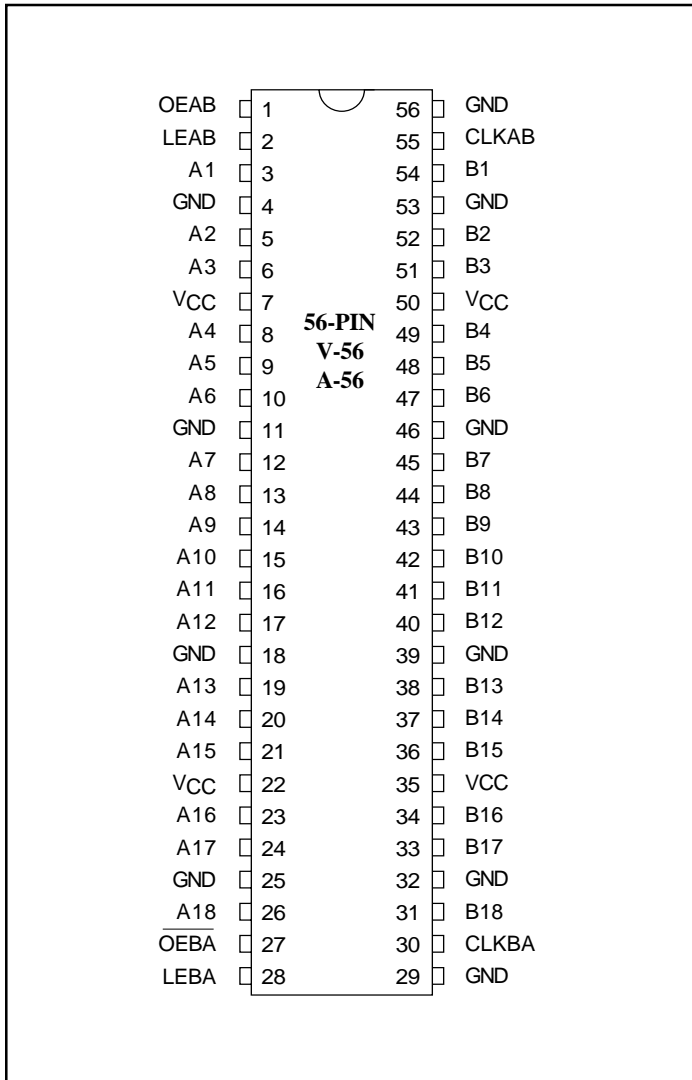
Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active HIGH)
LE	Latch Enable (Active HIGH)
CLK	Clock Input (Active HIGH)
Ax	Data I/O
Bx	Data I/O
GND	Ground
Vcc	Power

Truth Table^{(1)†}

Inputs				Output B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B0‡
H	L	L	X	B0§

Product Pin Configuration



Notes:

1. H=High Signal Level
L=Low Signal Level
Z=High Impedance
↑=LOW-to-HIGH Transition
- † A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA.
- ‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB is HIGH before LEAB goes LOW.
- § Output level before the indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Input Voltage Range, V_{IN}	-0.5V to $V_{CC} + 0.5V$
Output Voltage Range, V_{OUT}	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage	-0.5V to +5.0V
DC Output Current	100 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions⁽¹⁾

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 2.7V$ to $3.6V$	2.0			
V_{IL}	Input LOW Voltage	$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 2.7V$ to $3.6V$			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	High-level Output Current	$V_{CC} = 2.3V$			-12	mA
		$V_{CC} = 2.7V$			-12	
		$V_{CC} = 3.0V$			-24	
I_{OL}	Low-level Output Current	$V_{CC} = 2.3V$			12	
		$V_{CC} = 2.7V$			12	
		$V_{CC} = 3.0V$			24	
T_A	Operating Free-Air Temperature		-40		85	°C

Note:

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

Parameters	Test Conditions	$V_{CC}^{(1)}$	Min.	Typ. ⁽²⁾	Max.	Units
V_{OH}	$I_{OH} = -100 \mu\text{A}$	Min. to Max.	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$	$V_{IH} = 1.7\text{V}$	2.3V	2.0		
	$I_{OH} = -12 \text{ mA}$	$V_{IH} = 1.7\text{V}$	2.3V	1.7		
		$V_{IH} = 2.0\text{V}$	2.7V	2.2		
	$I_{OH} = -24 \text{ mA}$	$V_{IH} = 2.0\text{V}$	3.0V	2.4		
V_{OL}	$I_{OL} = 100 \mu\text{A}$	Min. to Max.			0.2	V
	$I_{OL} = 6 \text{ mA}$	$V_{IL} = 0.7\text{V}$	2.3V		0.4	
	$I_{OL} = 12 \text{ mA}$	$V_{IL} = 0.7\text{V}$	2.3V		0.7	
		$V_{IL} = 0.8\text{V}$	2.7V		0.4	
	$I_{OL} = 24 \text{ mA}$	$V_{IL} = 0.8\text{V}$	3.0V		0.55	
I_I	$V_I = V_{CC}$ or GND	3.6V			± 5	μA
I_I (Hold) ⁽³⁾	$V_I = 0.7\text{V}$	2.3V	45			
	$V_I = 1.7\text{V}$		-45			
	$V_I = 0.8\text{V}$	3.0V	75			
	$V_I = 2.0\text{V}$		-75			
	$V_I = 0$ to 3.6V	3.6V			± 500	
$I_{OZ}^{(4)}$	$V_O = V_{CC}$ or GND	3.6V			± 10	
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6V		40	
ΔI_{CC}	One input at $V_{CC} - 0.6\text{V}$, Other inputs at V_{CC} or GND	3V to 3.6V			750	
C_I Control Inputs	$V_I = V_{CC}$ or GND	3.3V		4		pF
C_{IO} A or B ports	$V_O = V_{CC}$ or GND	3.3V		8		pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient and maximum loading.
3. Bus Hold maximum dynamic current required to switch the input from one state to another.
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description	Conditions ⁽¹⁾	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f _{CLOCK}	Clock frequency	C _L = 50pF R _L = 500Ω	0	150	0	150	0	150	MHz
t _w Pulse Duration	LE high		3.3		3.3		3.3		ns
	CLK high or low		3.3		3.3		3.3		
t _{SU} Setup time	Data before CLK ↑		2.2		2.1		1.7		
	Data before LE ↓, CLK high		1.9		1.6		1.5		
	Data before LE ↓, CLK low		1.3		1.1		1.0		
t _H Hold time	Data after CLK ↑		0.6		0.6		0.7		
	Data after LE ↓, CLK high or low		1.4		1.7		1.4		
Δt/Δv ⁽²⁾	Input Transition Rise or Fall	0	10	0	10	0	10	ns/V	

Notes:

1. See test circuit and waveforms.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics Over Operating Range⁽¹⁾

Parameters	From (Input)	To (Output)	Conditions ⁽¹⁾	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Units
				Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f _{MAX}			C _L = 50pF R _L = 500Ω	150		150		150		MHz
t _{PD}	A or B	B or A		1.2	5.4		4.5	1	3.9	ns
	LE	A or B		1.6	6.3		5.3	1.3	4.6	
	CLK	A or B		1.7	6.7		5.6	1.4	4.9	
t _{EN}	OEAB	B		1.1	6.3		5.3	1.0	4.6	
t _{DIS}	OEAB	B		2.2	6.4		5.7	1.4	5.0	
t _{EN}	OEBA	A		1.4	6.8		6.0	1.1	5.0	
t _{DIS}	OEBA	A		2.0	5.5		4.6	1.3	4.2	

Notes:



1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Units
			Typical		
C _{PD} Power Dissipation Capacitance	Outputs Enabled	C _L = 50pF, f = 10 MHz	44	54	pF
	Outputs Disabled		6	6	

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