



**THE DATASHEET OF
PCKV857ADGG,518**



DATA SHEET

PCKV857A

100-250 MHz differential
1:10 clock driver

Product data
Supersedes data of 2002 Dec 13

2003 Jul 31

100-250 MHz differential 1:10 clock driver

PCKV857A

FEATURES

- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications as per JEDEC specifications
- 1-to-10 differential clock distribution
- Very low skew (< 100 ps) and jitter (< 100 ps)
- Operation from 2.2 V to 2.7 V V_{DD} and 2.3 V to 2.7 V V_{DD}
- SSTL_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTV16877 or SSTV16857
- Designed for DDR 266, 300, and 333 DIMM applications
- Available in TSSOP-48 and TVSOP-48 packages

DESCRIPTION

The PCKV857A is a high-performance, low-skew, low-jitter zero delay buffer designed for 2.5 V V_{DD} and 2.5 V V_{DD} operation and differential data input and output levels.

The PCKV857A is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs ($Y[0:9]$, $\overline{Y}[0:9]$) and one differential pair feedback clock outputs (FB_{OUT} , $\overline{\text{FB}}_{\text{OUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FB_{IN} , $\overline{\text{FB}}_{\text{IN}}$), and the analog power input (V_{DD}). When $\overline{\text{PWRDWN}}$ is HIGH, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is LOW, all outputs are disabled to HIGH impedance state (3-State), and the PLL is shut down (LOW power mode). The device also enters the LOW power mode when the input frequency falls below 20 MHz. An input frequency detection circuit will detect the LOW frequency condition and after applying a > 20 MHz input signal, the detection circuit turns on the PLL again and enables the outputs.

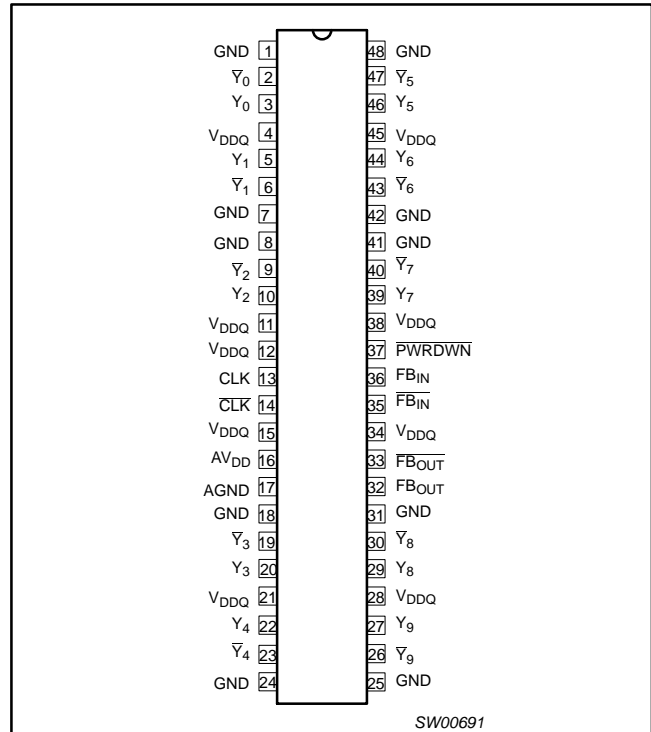
When V_{DD} is grounded, the PLL is turned off and bypassed for test purposes. The PCKV857A is also able to track spread spectrum clocking for reduced EMI.

The PCKV857A is characterized for operation from 0 to +70 °C.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	PCKV857ADGG	SOT362-1
48-Pin Plastic TSSOP (TVSOP)	0 to +70 °C	PCKV857ADGV	SOT480-1

PIN CONFIGURATION



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PIN DESCRIPTION

PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	SSTL_2 ground pins
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	$Y_n, \bar{Y}_n, FB_{OUT}, \overline{FB_{OUT}}$	SSTL_2 differential outputs
4, 11, 12, 15, 21, 28, 34, 38, 46	V_{DDQ}	SSTL_2 power pins
13, 14, 35, 36	$CLK_{IN}, \overline{CLK_{IN}}, FB_{IN}, \overline{FB_{IN}}$	SSTL_2 differential inputs
16	AV_{DD}	Analog power
17	AGND	Analog ground
37	PWRDWN	Power-down control input

FUNCTION TABLE

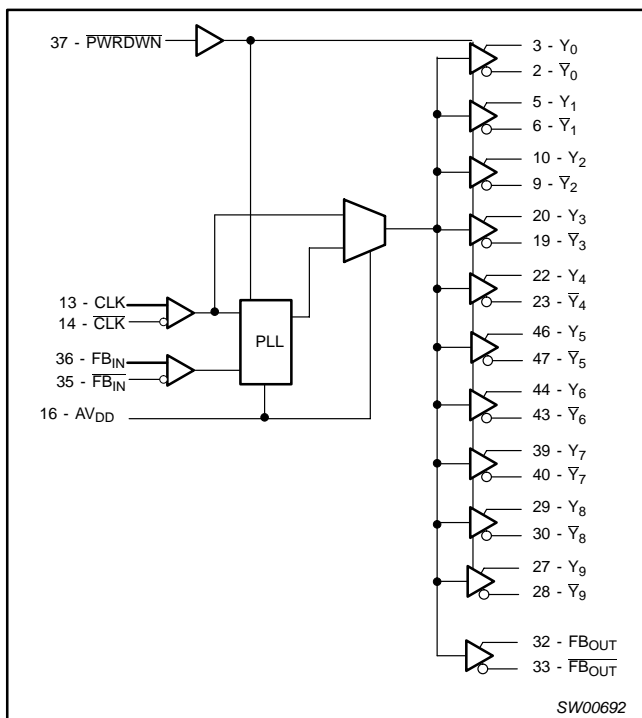
INPUTS			OUTPUTS				PLL ON/OFF
PWRDWN	CLK	CLK	Y_n	\bar{Y}_n	FB_{OUT}	$\overline{FB_{OUT}}$	
L	L	H	Z	Z	Z^1	Z^1	OFF
L	H	L	Z	Z	Z^1	Z^1	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X^2	< 20 MHz	< 20 MHz	Z	Z	Z^1	Z^1	OFF

NOTES:

H = HIGH voltage level
 L = LOW voltage level
 Z = HIGH impedance OFF-state
 X = don't care

- Subject to change. May cause conflict with FB_{IN} pins.
- Additional feature that senses when the clock input is less than 20 MHz and places the part in sleep mode.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V _{DDQ}	Supply voltage range		0.5	3.6	V
AV _{DD}	Supply voltage range		0.5	3.6	V
V _I	Input voltage range	see Notes 2 and 3	-0.5	V _{DDQ} + 0.5	V
V _O	Output voltage range	see Notes 2 and 3	-0.5	V _{DDQ} + 0.5	V
I _{IK}	Input clamp current	V _I < 0 or V _I > V _{DDQ}	—	±50	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{DDQ}	—	±50	mA
I _O	Continuous output current	V _O = 0 to V _{DDQ}	—	±50	mA
	Continuous current to GND or V _{DDQ}		—	±100	mA
T _{stg}	Storage temperature range		-65	+150	°C

NOTES:

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 3.6 V maximum.

RECOMMENDED OPERATING CONDITIONS¹

SYMBOL	PARAMETER		CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
V _{DDQ}	Supply voltage range			2.3	—	2.7	V
AV _{DD}	Supply voltage range			2.2	—	2.7	V
V _{IL}	LOW-level input voltage	CLK, $\overline{\text{CLK}}$, FB _{IN} , $\overline{\text{FB}}_{\text{IN}}$		—	—	V _{DDQ} /2 - 0.18	V
		PWRDWN		-0.3	—	0.7	
V _{IH}	HIGH-level input voltage	CLK, $\overline{\text{CLK}}$, FB _{IN} , $\overline{\text{FB}}_{\text{IN}}$		V _{DDQ} /2 + 0.18	—	—	V
		PWRDWN		1.7	—	V _{DDQ} + 0.3	
	DC input signal voltage		Note 2	-0.3	—	V _{DDQ}	V
V _{ID}	DC differential input signal voltage	CLK, FB _{IN}	Note 3	0.36	—	V _{DDQ} + 0.6	V
	AC differential input signal voltage	CLK, FB _{IN}	Note 3	0.7	—	V _{DDQ} + 0.6	V
V _{OX}	Output differential cross-voltage		Note 4	V _{DDQ} /2 - 0.2	V _{DDQ} /2	V _{DDQ} /2 + 0.2	V
V _{IX}	Input differential cross-voltage		Note 4	V _{DDQ} /2 - 0.2	—	V _{DDQ} /2 + 0.2	V
I _{OH}	HIGH-level output current			—	—	-12	mA
I _{OL}	LOW-level output current			—	—	12	mA
SR	Input slew rate			1	—	4	V/ns
T _{amb}	Operating free-air temperature			0	—	70	°C

NOTES:

- Unused inputs must be held HIGH or LOW to prevent them from floating.
- DC input signal voltage specifies the allowable DC execution of differential input.
- Differential input signal voltage specifies the differential voltage |V_{TR} - V_{CP}| required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level.
- Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IK}	Input voltage, all inputs	$V_{DDQ} = 2.3 \text{ V}$, $I_I = -18 \text{ mA}$	—	—	-1.2	V
V_{OH}	HIGH-level output voltage	$V_{DDQ} = \text{min to max}$, $I_{OH} = -1 \text{ mA}$	$V_{DDQ} - 0.1$	—	—	V
		$V_{DDQ} = 2.3 \text{ V}$, $I_{OH} = -12 \text{ mA}$	1.7	—	—	V
V_{OL}	LOW-level output voltage	$V_{DDQ} = \text{min to max}$, $I_{OL} = 1 \text{ mA}$	—	—	0.1	V
		$V_{DDQ} = 2.3 \text{ V}$, $I_{OL} = 12 \text{ mA}$	—	—	0.6	V
I_I	Input current	$V_{DDQ} = 2.7 \text{ V}$, $V_I = 0 \text{ V to } 2.7 \text{ V}$	—	—	± 10	μA
I_{OZ}	HIGH-impedance-state output current	$V_{DDQ} = 2.7 \text{ V}$, $V_O = V_{DDQ}$ or GND	—	—	± 10	μA
I_{DDPD}	Power-down current on $V_{DDQ} + AV_{DD}$	CLK and $\overline{\text{CLK}} = 0 \text{ MHz}$, PWRDWN = LOW; Σ of I_{DD} and A_{DD}	—	30	100	μA
I_{DD}	Dynamic current on V_{DDQ}	$f_O = 67 \text{ MHz to } 190 \text{ MHz}$	—	200	300	mA
A_{DD}	Supply current on AV_{DD}	$f_O = 67 \text{ MHz to } 190 \text{ MHz}$	—	8	10	mA
C_I	Input capacitance	$V_{CC} = 2.5 \text{ V}$, $V_I = V_{CC}$ or GND	2	2.8	3	pF

NOTE:

1. This is intended to operate in the SSTL_2 type IV unterminated mode without series resistors on the outputs.
2. All typical values are at respective nominal V_{DDQ} .
3. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing.

TIMING REQUIREMENTS

Over recommended ranges of supply voltage and operating free-air temperature.

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{CK}	Operating clock frequency	100	250	MHz
	Input clock duty cycle	40	60	%
	Stabilization time ¹	100	—	μs

NOTE:

1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power-up.

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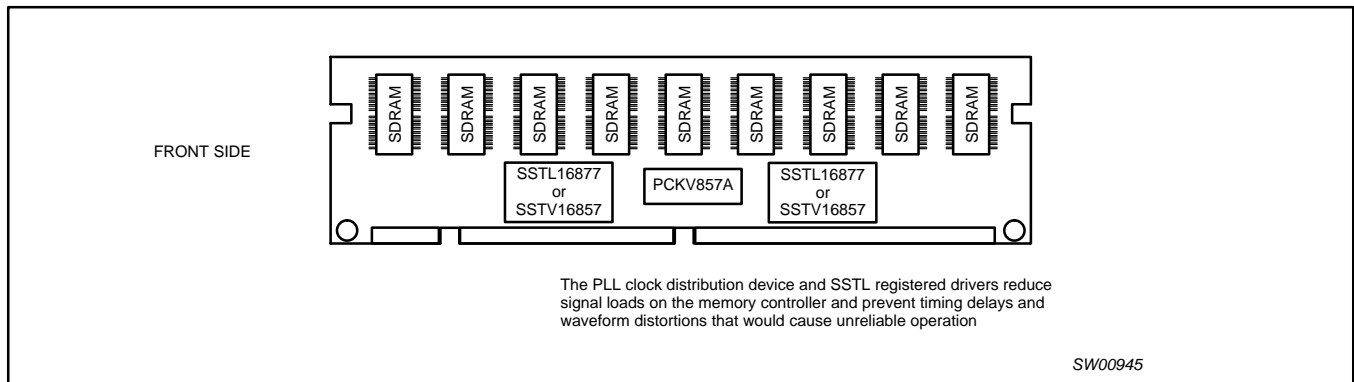
AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ k Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
$t_{(O)}$	Static phase offset	Figure 1		-350	0	350	ps
$t_{SK(O)}$	Output clock skew	Figure 2		—	—	150	ps
$t_{SLR(O)}$	Output clock slew rate	Figure 3		1	—	2	V/ns
$t_{JIT(PER)}$	Jitter (period)	Figure 4	$f_O = 67$ MHz to 200 MHz	-75	—	75	ps
$t_{JIT(CC)}$	Jitter (cycle-to-cycle)	Figure 5	$f_O = 67$ MHz to 200 MHz	-75	—	75	ps
$t_{JIT(HPER)}$	Half-period jitter	Figure 6		-75	—	75	ps
t_{PLH}^1	LOW to HIGH level propagation delay		Test mode/CLK to any output	—	3.7	—	ns
t_{PHL}^1	HIGH to LOW level propagation delay		Test mode/CLK to any output	—	3.7	—	ns

NOTE:

1. Refers to transition of noninverting output.



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AC WAVEFORMS

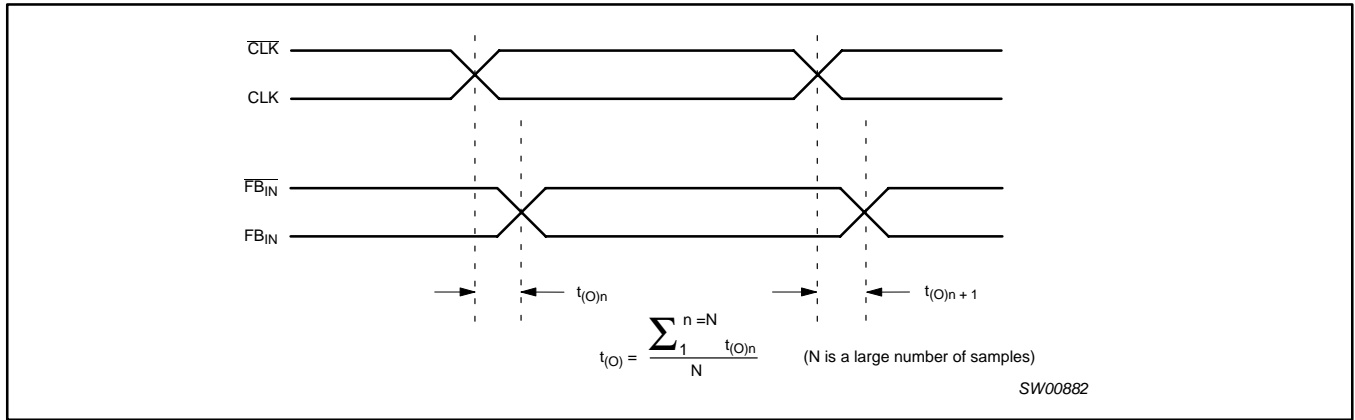


Figure 1. Static phase offset

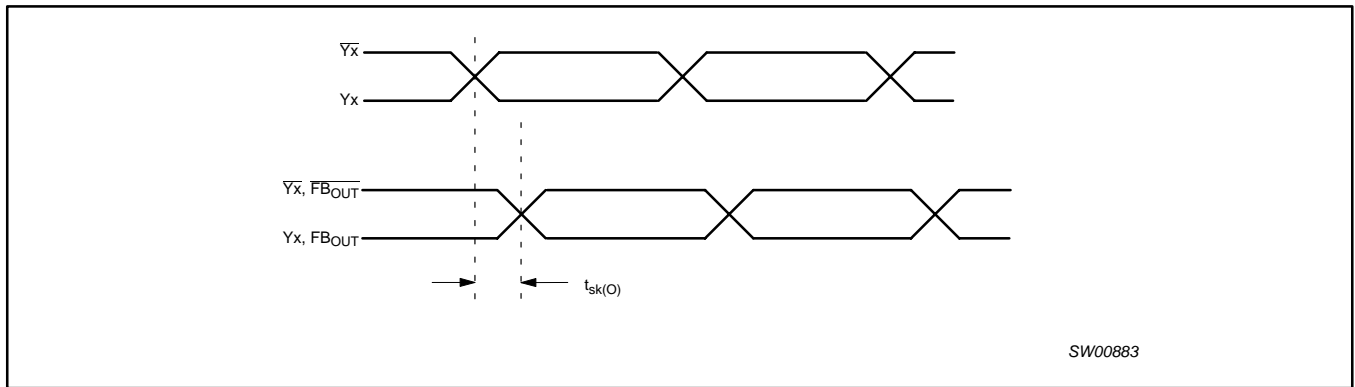


Figure 2. Output skew

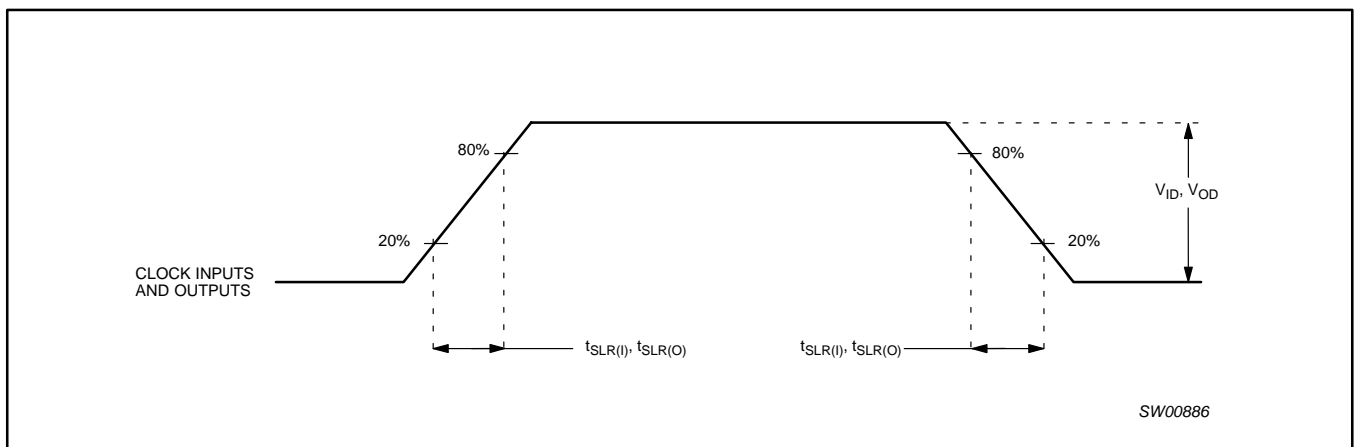


Figure 3. Input and output slew rates

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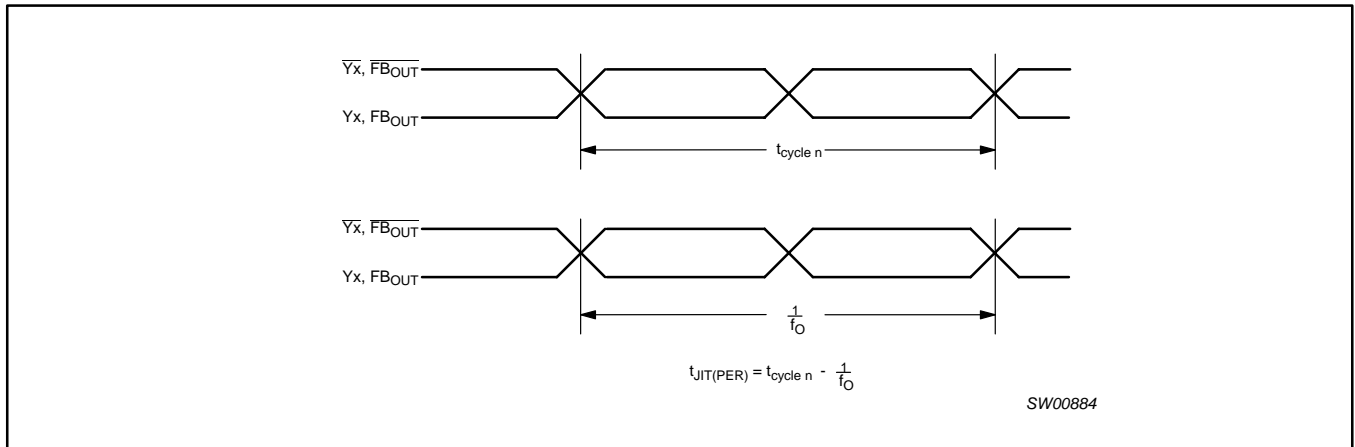


Figure 4. Period jitter

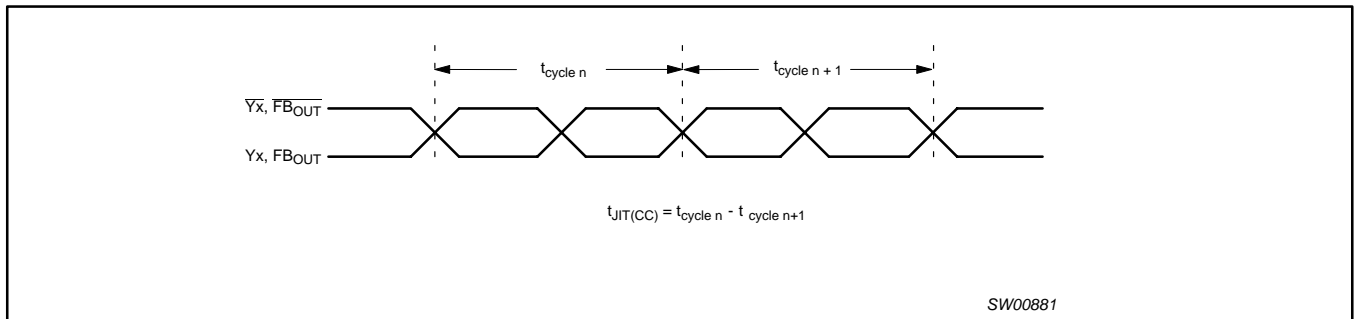


Figure 5. Cycle-to-cycle jitter

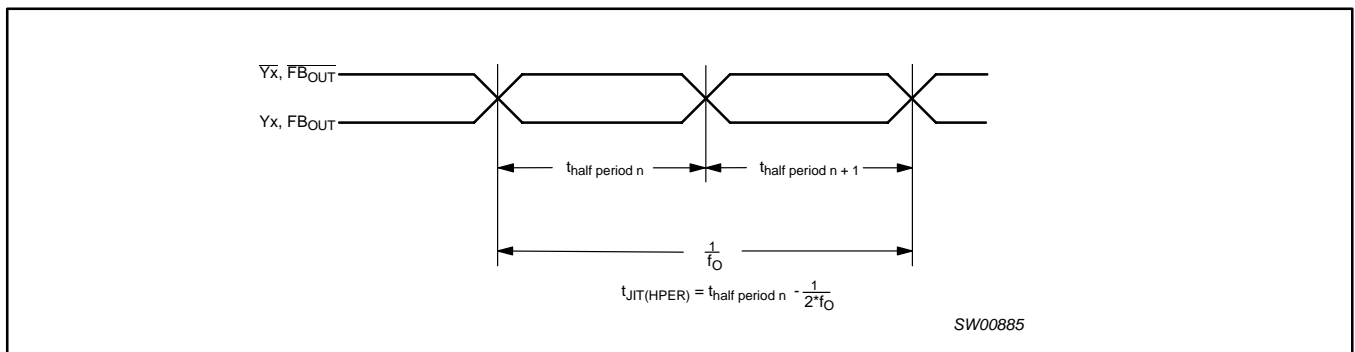


Figure 6. Half-period jitter

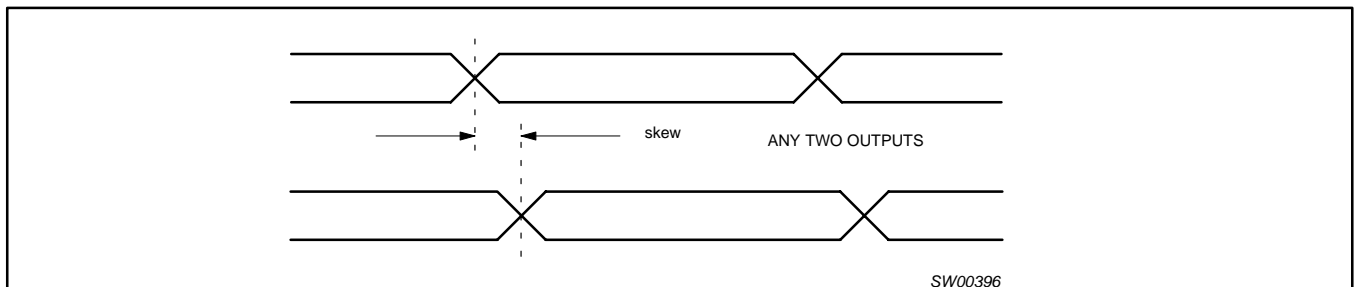


Figure 7. Skew between any two outputs.

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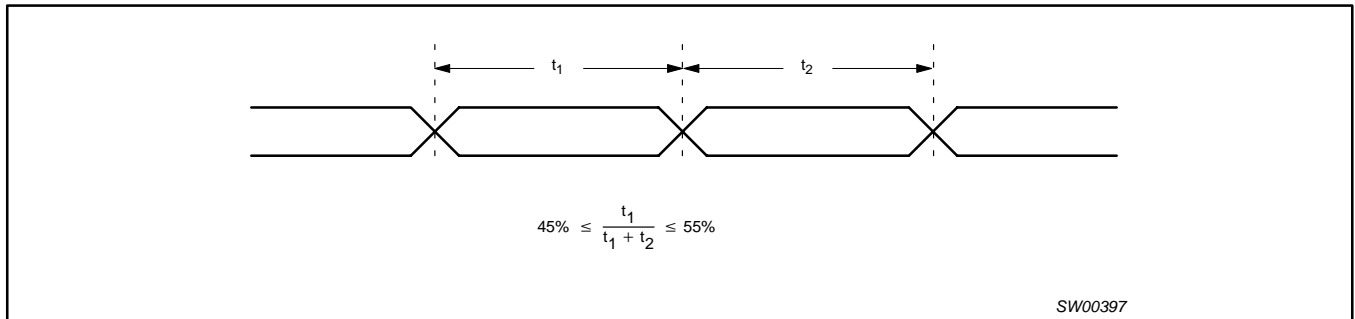


Figure 8. Duty cycle limits and measurement

TEST CIRCUIT

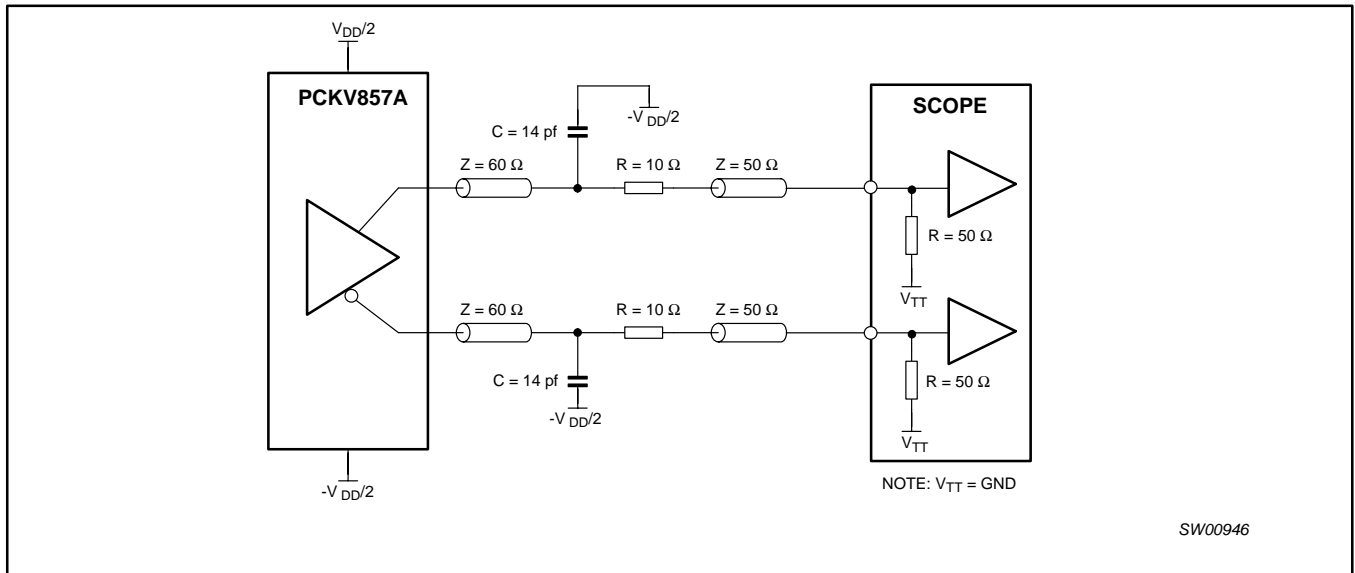


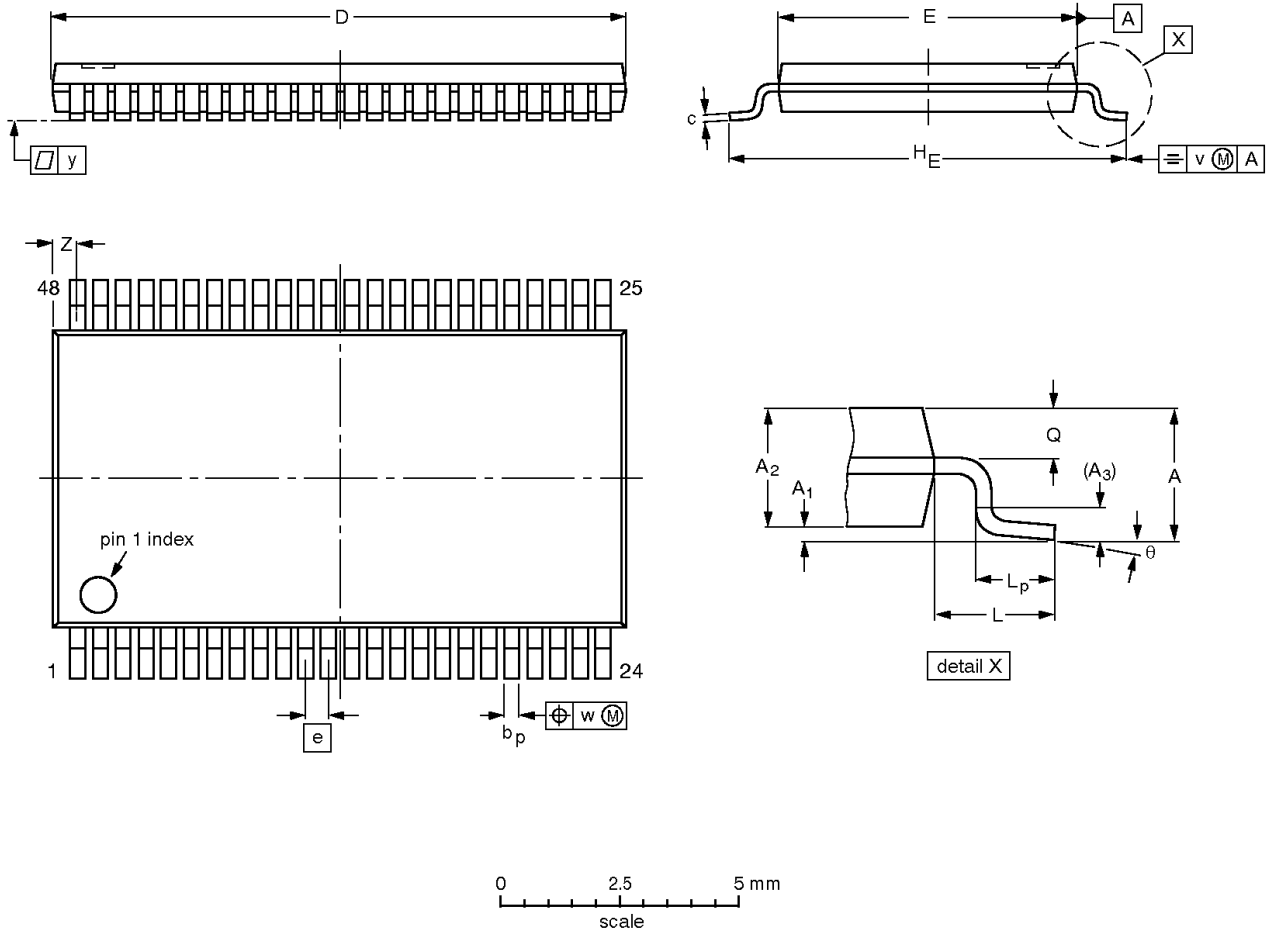
Figure 9. Output load test circuit

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

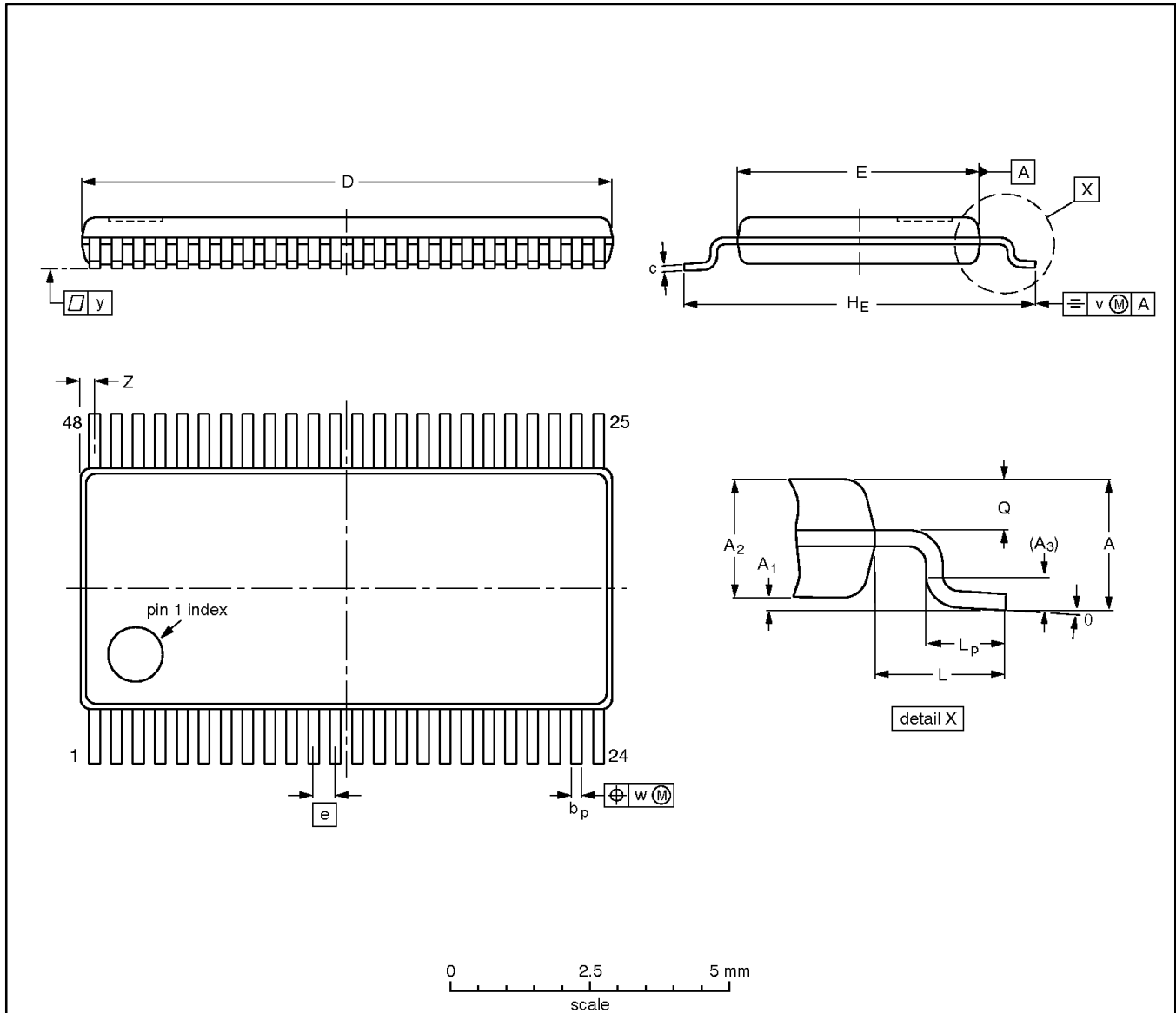
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

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TSSOP48: plastic thin shrink small outline package; 48 leads;
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.80 9.60	4.50 4.30	0.40	6.60 6.20	1.00	0.70 0.50	0.40 0.30	0.20	0.07	0.08	0.40 0.10	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT480-1		MO-153				97-03-20 99-12-27

100-250 MHz differential 1:10 clock driver

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REVISION HISTORY

Rev	Date	Description
_2	20030731	Product data (9397 750 11759); ECN 853-2394 30057 dated 18 June 2003. Supersedes data of 2002 Decemaber 13 (9397 750 10867). Modifications: <ul style="list-style-type: none">• Minor changes or corrections to existing product specifications.
_1	20021213	Product data (9397 750 10867); ECN 853-2394 29181 of 13 December 2002.

100-250 MHz differential 1:10 clock driver

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Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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