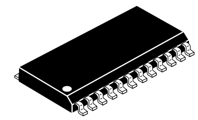
THE DATASHEET OF

NCV7685DQR2G

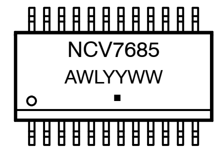
12 Channels 60 mA LED Linear Current Driver I²C Controllable for Automotive Applications

NCV7685



SSOP24−NB EP
CASE 940AQ

MARKING DIAGRAM



NCV7685 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7685DQR2G	SSOP24−EP (Pb−Free)	2500/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

The NCV7685 consists of twelve linear programmable constant current sources with common reference. The part is designed for use in the regulation and control of LED for automotive applications. The NCV7685 allows 128 different duty cycle levels adjustable using pulse width modulation (PWM) independently for each output channel programmable via I²C serial interface. PWM frequency can be chosen in four different configurations up to 1200 Hz. The device can be used with micro−controller applications using the I²C bus or in stand−alone applications where a choice could be done in between two different static configuration settings. The IC also provides 3.3 V voltage reference to the application for loads up to 1 mA.

LED brightness level is easily programmed using an external resistor. Each channel has an internal circuitry to detect open−load conditions with an optional auto−recovery mode. If one driver is in open−load condition, all other channels could be turned off according to the programmable bit setting.

The device is available in small body size SSOP24−EP package.

Features

- 12 Common Current Programmable Sources up to 60 mA
- Independent PWM Duty Cycle Control for each Channel via PC
- Common PWM Duty Cycle Control via I²C
- On−Chip 150, 300, 600 and 1200 Hz PWM
- Open LED String Diagnostics
- Low Dropout Operation for Pre−Regulator Applications
- Single Resistor for Current Set Point
- Voltage Reference 3.3 V/1 mA
- 8 Bits I²C Interface with CRC8 Error Detection
- OTP Bank for Stand−Alone Operation (2 Configurations)
- Output Enable Pin
- Detection and Protection Against Open Load and Under−Voltage
- Over Temperature Detection and Protection
- Low Emission with Spread Spectrum Oscillator
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- SSOP24−EP Packaging

Applications

- Dashboard Applications
- Rear Combination Lamps (RCL)
- Daytime Running Lights (DRL)
- Fog Lights
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Turn Signal and Other Externally Modulated Applications

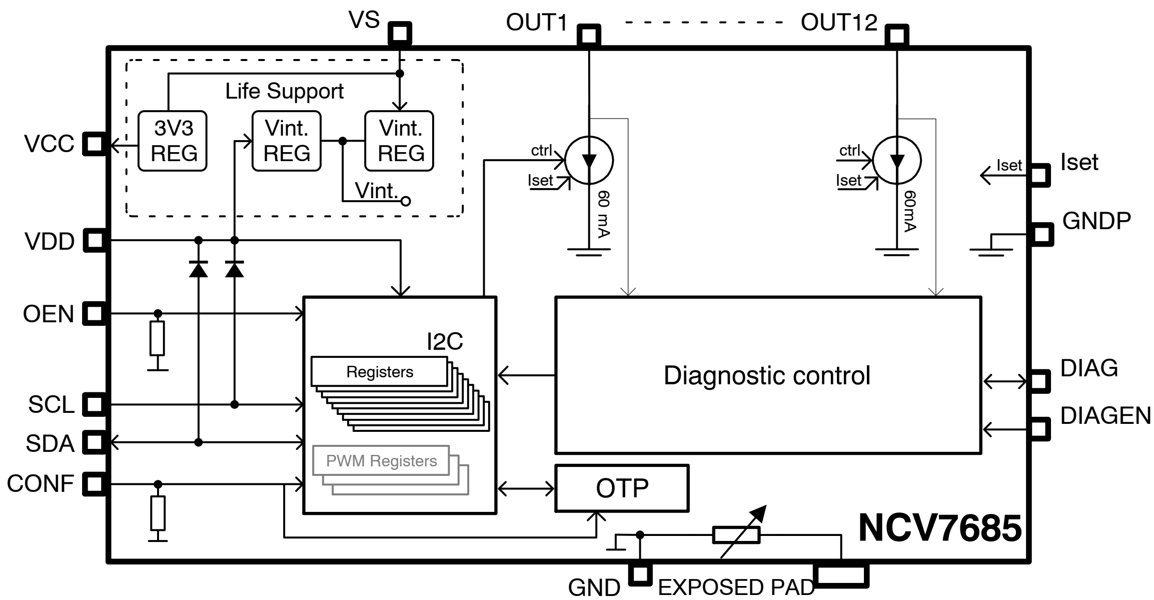


Figure 1. Block Diagram

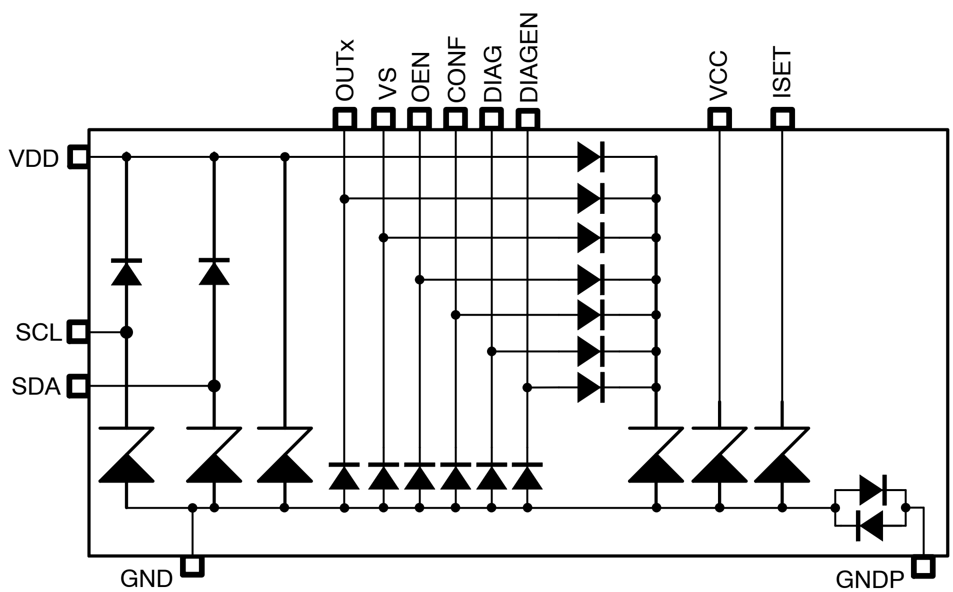


Figure 2. ESD Schematic

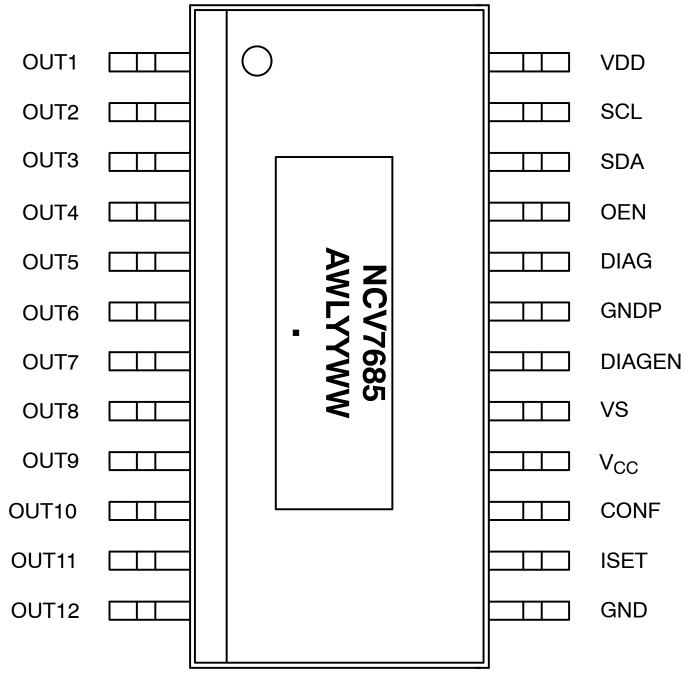


Figure 3. Pinout Diagram

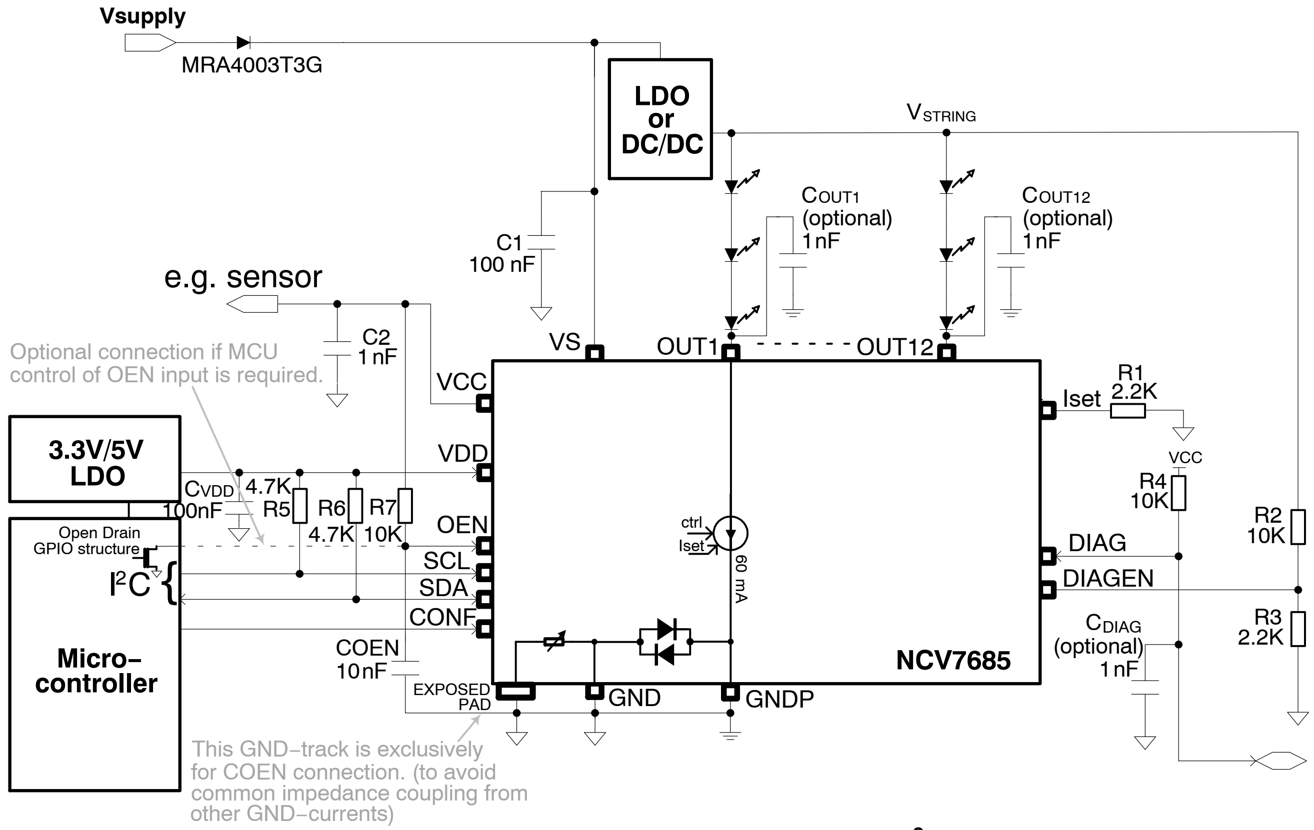


Figure 4. Application Diagram with Micro−controller (I^{2}C Mode)

The device is powered−up with both VS and VDD. Both must be in the recommended operating range.

– At power−up, the device loads the selected SAM register. (like in Stand Alone Mode)
– Because VDD is supplied, communication through the I^{2}C lines (SCL−and SDA−pins) is allowed
– I^{2}C mode must be activated by setting I2CFLAG in the I2C_CONF register.

NOTE: The NCV7685 may not start−up when VDD is kept between 1 V and VDDUV_R (2.9V)

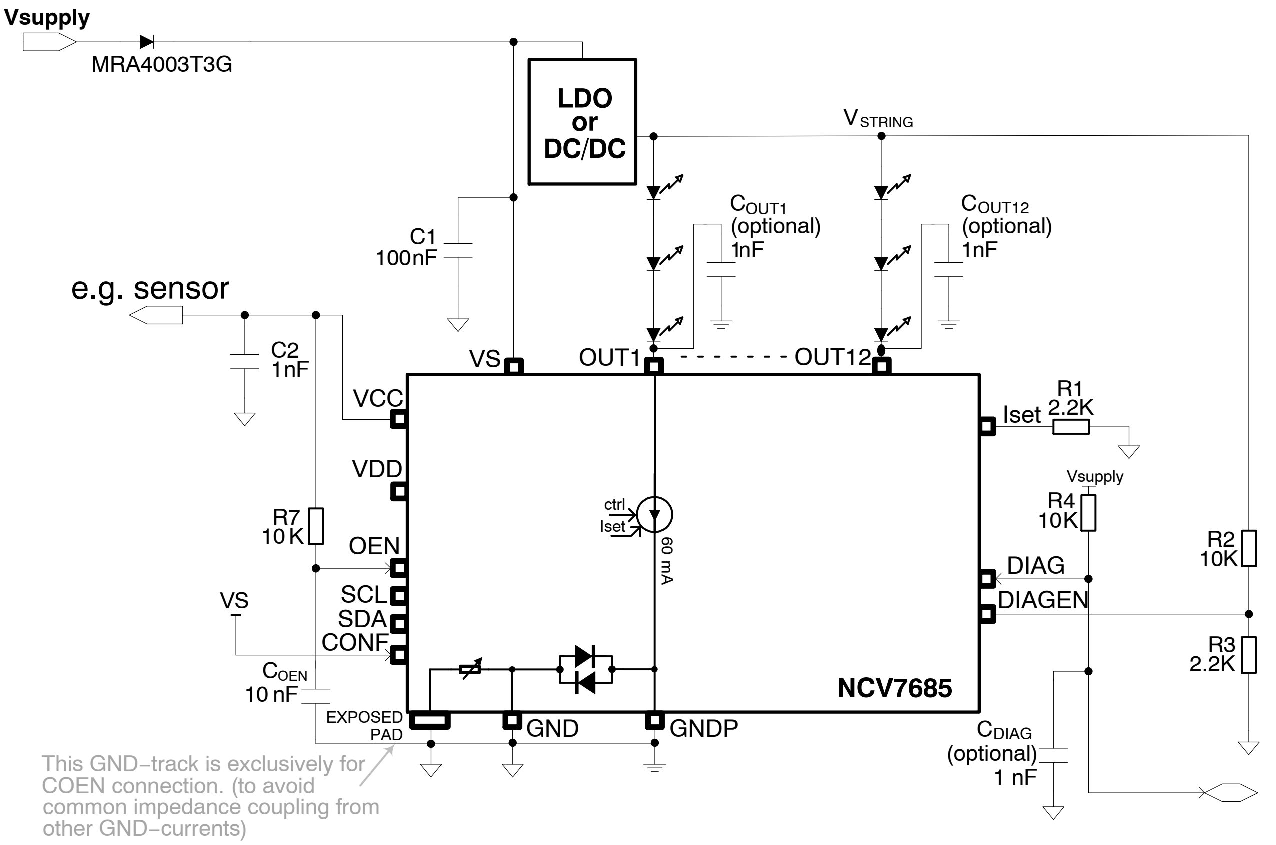


Figure 5. Application Diagram without Micro−controller (Stand Alone Mode)

The device is powered−up with only VS in the recommended operating range while VDD input is open or VDD is connected to GND.

- At power−up, the device loads the selected SAM register.
- Because VDD is not supplied, communication through the I^2C lines (SCL−and SDA−pins) is not allowed.
- The I^2C pins (SCL−and SDA−pins) must be left NC or connected to GND as those pins are internally protected via internal diodes to VDD−pin (See Figure 2)

NOTE: The NCV7685 may not start−up when VDD is kept between 1 V and VDDUV_R (2.9 V).

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Label	Description
1	OUT1	Channel 1 Current Output to LED
2	OUT2	Channel 2 Current Output to LED
3	OUT3	Channel 3 Current Output to LED
4	OUT4	Channel 4 Current Output to LED
5	OUT5	Channel 5 Current Output to LED
6	OUT6	Channel 6 Current Output to LED
7	OUT7	Channel 7 Current Output to LED
8	OUT8	Channel 8 Current Output to LED
9	OUT9	Channel 9 Current Output to LED
10	OUT10	Channel 10 Current Output to LED
11	OUT11	Channel 11 Current Output to LED
12	OUT12	Channel 12 Current Output to LED
13	GND	Signal Ground
14	ISET	Current Setting/EoL Enable Pin
15	CONF	Stand Alone Mode Selection Bank

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin #	Label	Description
16	VCC	3.3 V Voltage Reference Output (Needs External Decoupling Capacitor)
17	VS	Supply Voltage Input
18	DIAGEN	Diagnostic Voltage Sensing Node for V_{STRING} Via Resistor Divider
19	GNDP	Power Ground for output drivers
20	DIAG	Open−drain diagnostic input/output. Reporting Open Circuit and thermal shutdown. Normal Operation = HIGH
21	OEN	Output Enable Input
22	SDA	I^2C Serial Data
23	SCL	I^2C Serial Clock
24	VDD	Digital Supply Voltage Input
epad	epad	True Ground Do NOT Connect to PCB Traces other than GND

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Power supply voltage: Continuous supply voltage Transient Voltage (t < 500 ms, “load dump”)	V_{MAX}_VS	 −0.3 −0.3	 28 40	 V V
Input pin voltage (DIAGEN, DIAG, CONF, OEN)	V_{MAX}_INx	−0.3	40	V
Continuous Output Pin voltage Transient Voltage (t < 500 ms, “load dump”) or during PWM period = OFF	V_{MAX}_OUTx	−0.3 −0.3	28 40	V V
Stabilized supply voltage	V_{MAX}_VCC	−0.3	3.6	V
Digital input supply voltage	V_{MAX}_VDD	−0.3	5.5	V
DC voltage at pins (VDD, SCL, SDA)	V_{MAX}_IO	−0.3	5.5	V
DC voltage at pin ISET	V_{MAX}_ISET	−0.3	3.6	V
Maximum Ground Current	I_{MAX}_GNDP	−	750	mA
ESD Capability (Note 2) ESD Voltage, HBM (Human Body Model); (100 pF, 1500 Ω) − All pins − Output pins OUTx to GND ESD according to CDM (Charge Device Model) − All pins − Corner pins ESD according to MM (Machine Mode) − All pins	 ESD_{HBM} ESD_{CDM} ESD_{MM}	 ±2 ±4 ±500 ±750 ±150		 kV kV V V V
Moisture sensitivity (SSOP24−EP) (Note 3)		MSL2		
Storage Temperature		−55 to 150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model
   ESD MM according to AEC−Q100
3. For additional information, see or download **onsemi**’s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D, and Application Note AND8003/D.

Table 3. RECOMMENDED OPERATING RANGES

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 4) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage (VS) – parametric operation	VS_OP	5	18	V
Analog Supply Voltage – functional extended operation (Note 5)	VS_EXT	5	28	V
Analog Supply Voltage – slope (Note 6)	VS_SLOPE	10	10000	V/ms
OEN pin voltage during first 10 μs until VCC is activated (Note 7)	OEN_start	0	5	mV
Digital Supply Voltage (VDD)	VDD	3.15	5.5	V
Ambient Temperature	T_A	−40	125	°C
OTP Zap Ambient Temperature	T_{A_ZAP}	10	30	°C
Parametric operating junction temperature range (Note 8)	T_{JP}	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes and application diagrams, in which the device is operated by the customer, etc. No more than 20 cumulated hours in life time above T_{JP}.
5. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating range.
6. Analog supply slopes should be kept within specified range while VS < 5 V in order to guarantee safe start−up. However, if there is a need to exceed this value, please contact onsemi in order to mutually agree on the application.
7. Max slope on OEN pin must be secured accordingly to OEN paragraph to guarantee safe startup.
8. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.

Table 4. THERMAL CHARACTERISTICS

Parameter	Value	Unit
Package Thermal Resistance (SSOP24−EP) (Note 9)		
– Junction to Ambient, $R_{\theta JA}$	45.8	°C/W
– Junction to Board, $R_{\theta JB}$	8.8	°C/W
– Junction to Case (Top), $R_{\theta JC}$	10.1	°C/W

9. Values represent thermal resistances under natural convection are obtained in a simulation on a JEDEC−standard, 2S2P; High Effective Thermal Conductivity Test Board as specified in JESD51−7, in an environment described in JESD51−2a.

Table 5. ELECTRICAL CHARACTERISTICS

(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, −40°C ≤ T_J ≤ 150°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GENERAL						
Supply Under−Voltage	VSUV	VS rising	3.8	4.1	4.4	V
Supply range during OTP zapping	VS_OTPzap	2.5 V ≤ ISET ≤ 3.3 V; VS current peak capability ≥ 70 mA	13	–	18	V
Supply Under−Voltage hysteresis	VSUVhys		–	200	–	mV
Supply Current (Vs)	Is(error mode)	all OUTx OFF except channel in open load SCL = SDA = 0; Iout_VCC = 0 mA	–	1.2	1.5	mA
		Iout_VCC = 1 mA	–	2.2	2.5	mA
	Is(active)	Active Mode VS = 16 V, Vcc unloaded OUTx = 1 V, R1 = 2 kΩ	–	7	10	mA
Digital supply current	IDD	I^2C mode, VS = 12 V	–	0.24	2	mA
VDD Under Voltage detection	VDDUV_R	VDD rising, while VS in operating range	–	–	2.9	V
	VDDUV_F	VDD falling, while VS in operating range	2	–	–	V

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, −40°C ≤ T_J ≤ 150°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CURRENT SOURCE OUTPUTS						
Output current	IOUThot	OUTx = 1 V, T_J = 150°C	50	55	60	mA
	IOUTcold	OUTx = 0.5 V, T_J = −40°C	50	55	60	mA
Current Matching from channel to channel	ImatchCold	T_J = −40°C (Note 10)	−7	0	7	%
	Imatch	T_J = 25°C (Note 10)	−6	0	6	%
	ImatchHot	T_J = 150°C (Note 10)	−5	0	5	%
Current Slew Rate	ISRx	10% to 90%	–	30	–	mA/μs
Open Circuit Detection Threshold	OLDT	IOUTx > 20 mA	30	50	70	% of output current
Open load recovery in auto−recovery mode	OLR		5	10	15	mA
VOLTAGE REFERENCE						
Output Voltage Tolerance	V_VCC	I_VCC ≤ 1 mA	3.20	3.30	3.45	V
Output Current	Iout_VCC		–	–	−1	mA
Load Capacitor	Cload_VCC	ESR < 200 mΩ	0.9	1.0	2.5	nF
INPUTS: OEN, CONF						
Input Low Level	VinL		0.7	1.0	–	V
Input High Level	VinH		–	1.25	1.66	V
Input Hysteresis	Vin_hyst		100	250	400	mV
Input Pull−down Resistor	Rin_pd		120	200	280	kΩ
INPUTS: SCL, SDA						
Input Low Level	VinL		–	–	0.3 × VDD	V
Input High Level	VinH		0.7 × VDD	–	–	V
Input Hysteresis	Vin_hyst		0.05 × VDD	–	–	V
Output Current	Iout_SDA	V (SDA) = 0.4 V	3	–	–	mA
DIAGEN PIN						
VS Diagnostic Enable Threshold	VDiagenTH		1.9	2.0	2.1	V
Input Pull−down Resistor	Rdiagen_pd		120	200	280	kΩ
DIAG PIN						
Output Low Level	VoutL	Diagnostic Activated, Idiag = 1 mA	–	0.2	0.4	V
Diagnostic Reset Voltage	DiagRes		1.65	1.80	1.95	V
Filter Time to Set the DIAG Fail Pin in Failure Mode	tp_DIAG	Idiag = 1 mA	–	10	20	μs
DIAG Output Leakage	DIAG_leak	VDIAG = 5 V	–	–	10	μA
ISET INPUT PIN						
Global Current Setting	VISET		0.94	1.0	1.06	V
IOUT ISET Factor	K		–	100	–	–

10. Matching formulas:

$$\left[\frac{2IOUTx(min)}{IOUTx(min) + IOUTx(max)} - 1\right] \times 100 \text{ and } \left[\frac{2IOUTx(max)}{IOUTx(min) + IOUTx(max)} - 1\right] \times 100$$

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, −40°C ≤ T_J ≤ 150°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup−up Time to 90% of the ISET Regulated Value	tsetupISET	VS > 5 V	–	–	50	μs
INTERNAL PWM CONTROL UNIT (OUT1− OUT12)						
PWM1 Frequency, I^2C Mode	PWM1	Configuration Via I^2C	132	150	168	Hz
PWM2 Frequency, I^2C Mode	PWM2	Configuration Via I^2C	264	300	336	Hz
PWM3 Frequency, I^2C Mode	PWM3	Configuration Via I^2C	528	600	672	Hz
PWM4 Frequency, I^2C Mode	PWM4	Configuration Via I^2C	1056	1200	1344	Hz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. THERMAL WARNING AND THERMAL SHUTDOWN PROTECTION

Symbol	Parameter	Min	Typ	Max	Unit
Tjwar_on	Thermal Warning Threshold (Junction Temperature)	–	TSD−30	–	°C
TSD	Thermal Shutdown Threshold (Junction Temperature) T_J Increasing	160	–	180	°C
Tjsd_hys	Thermal Shutdown Hysteresis	10	–	15	°C

General

The NCV7685 is a twelve channel LED driver. Each output can drive currents up to 60 mA/channel and are programmable via an external resistor. The target applications for the device are in automotive rear lighting systems and dashboard applications. The device can be used with micro−controller applications using the I^2C bus or in stand−alone applications. In both cases it is mandatory to supply the LED channels by an external ballast transistor, or by an LDO or a DC/DC to have low voltage drop on the outputs which will lead to a decrease in power dissipation in the device. In order to have very low electromagnetic emission, this device has an embedded spread spectrum oscillator.

Output Current Programming (I_{SET}/I_{OUTx})

The maximum current can be defined with the Iset input pin. The equations below can be used to calculate this maximum output current:

$$Iset = 1\ V/R1 \quad \text{(eq. 1)}$$

$$IOUTx = K \times Iset \quad \text{(eq. 2)}$$

Example:
R1 = 2 kΩ
using eq. 1 → Iset = 500 μA
and using eq. 2 → IOUTx = 50 mA

To avoid potential disturbances when all drivers are activated at the same time, a typical activation delay of 400 ns between groups of two consecutive outputs is implemented (see Figure 6).

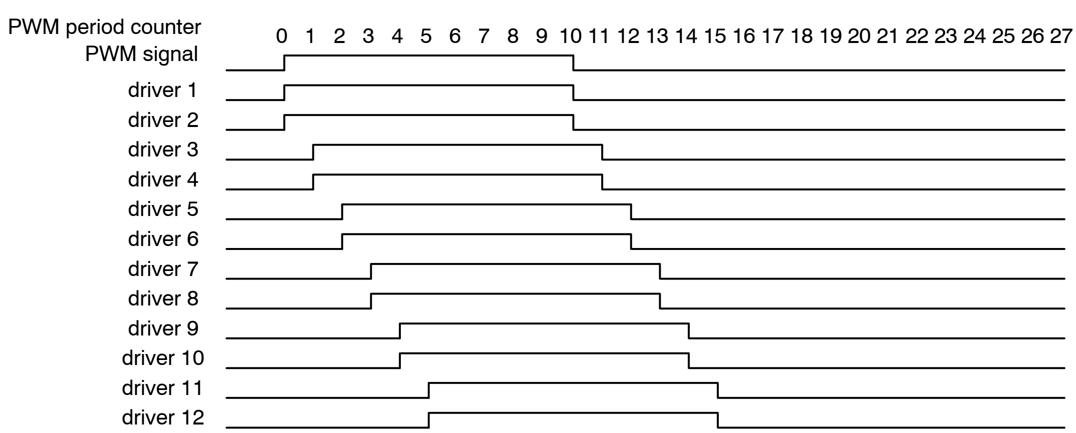


Figure 6.

Power Supply and Voltage Reference (VS, V_{CC}, V_{DD})

VS is the analog power supply input of the device. VS supply is monitored with respect to the crossing of VSUV level (typ. 4.1 V). When VS rises above VSUV, the device starts the power−up state. When VS is above the VS_OP minimum level (typ. 5 V), the device can work properly.

VCC is a voltage reference providing 3.3 V derived from the VS main supply. It is able to deliver up to 1 mA and is primarily intended to supply 3.3 V loads. If VCC output reference is not used, then the VCC capacitor can be omitted.

VDD is the digital power supply input of the device.

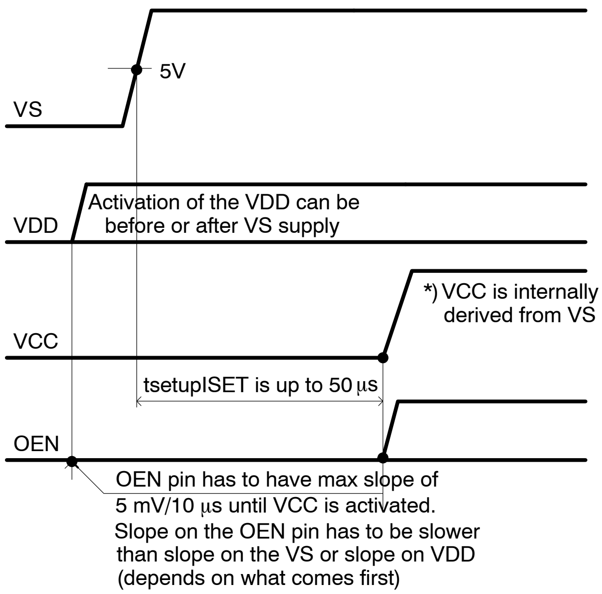


Figure 7. Power−up Sequence for OEN pin

Ground Connections (GND: Pin 13 and GNDP Pin 19)

The device ground connection is split to two pins called GND and GNDP. Both pins have to be connected on the application PCB.

Chip Select for OTP Programing (Using I_{SET})

The device can be programmed using the I^2C bus in End of Line cases. When the voltage on the ISET pin is pulled higher than 2.5 V, the device can be set in OTP control mode via the I^2C bus. During normal mode where only an external ISET resistor is connected to the I_{SET} pin, the access to the OTP registers is not possible. Zapping is only possible with VS above 13 V. The outputs are disabled as soon as 2.5 V is applied to the ISET pin. After the ID_LOCK_OTP I2C message is properly received, no further OTP zapping is possible.

Output Enable (OEN)

When the OEN input voltage is high, all output channels are programmed according to the I2C or SAM configuration. When OEN voltage is below 0.7 V, all outputs are disabled in the SAM or I2C mode regardless on the registers setting. If the OEN pin is left floating, the internal pull down resistor will cause switching off all channels. The OEN pin has to have max slope of 5 mV for first 10 μs until VCC is activated. The recommended examples are shown in Figure 4 and Figure 5. The Figure 11 shows the example of the driving multiple NCV7685 drivers from one MCU.

Configuration (CONF)

When the CONF input voltage will be below 0.7 V the configuration 1 will be selected (One Time Programmable OTP 1 register called SAM_CONF_1) and when the CONF input voltage will be above 1.66 V the configuration 2 will be selected (OTP 2 register called SAM_CONF_2). There is ability to change the configuration in error mode (either with CONF in SAM or through I^2C in I2C mode).

I^2C Bus (SCL, SDA)

The I^2C bus consists of two wires, Serial Data (SDA) and Serial Clock (SCL), carrying information between the devices connected on the bus. Each device connected to the bus is recognized by a unique address and operates as either a transmitter or receiver, depending on the function of the device. The NCV7685 can both receive and transmit data with CRC8 error detection algorithm. The NCV7685 is a slave device.

SDA is a bi−directional line connected to a positive supply voltage via an external pull−up resistor. When the bus is free both lines are HIGH. The output stages of the devices connected to the bus must have an open drain to perform the wired−AND function. Data on the I^2C bus can be transferred up to 400 kb/s.

Diagnostic Enabling (DIAGEN)

The device is capable to detect for each independent channel an open load condition. Versus the number of LEDs and the Vstring voltage supply, a wrong open load condition can be detected if the fault detection is activated when there is not enough voltage across the LEDs. This threshold can be programmable thanks to an external divider connected to the DIAGEN pin. When the divided voltage is below a typical value of 2 V, the LED diagnostic is disabled. When the divided voltage is above the typical value of 2 V, the LED diagnostic is enabled.

Diagnostic Feedback (DIAG)

The DIAG is an open drain output pin who can alert a microcontroller as soon as one of the outputs is in error mode (DIAG Low = open load or thermal shut−down or I_{SET} shorted). Forcing the DIAG pin below 1.8 V will force a fault condition if the DIAGEN input pin is above a typical value of 2 V. If the DIAGEN input pin is below the typical value of 2 V then forcing the DIAG input pin will not have any effect.

Due to certain sensitivity on the DIAG pin during the startup, it is recommended to have the pull−up resistor connected to the VCC supply. In case if the application deviate from the proposal mentioned in the Figure 4 or Figure 5, the power−up sequence has to follow the timing diagrams in the Figure 8 or Figure 9.

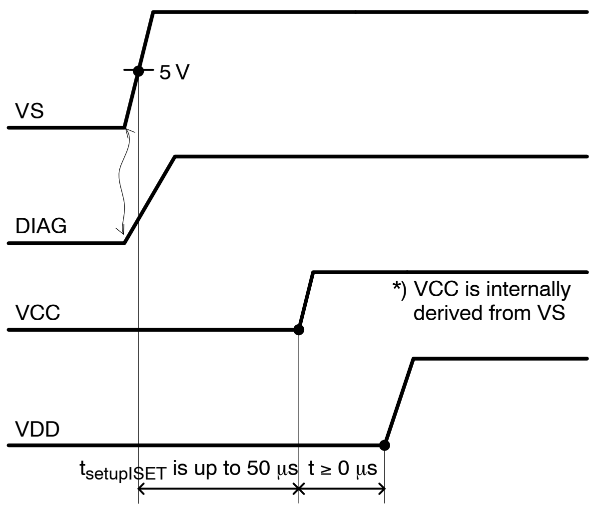


Figure 8. Power−up Sequence for DIAG pin. VS is supplied first, VDD comes up later.

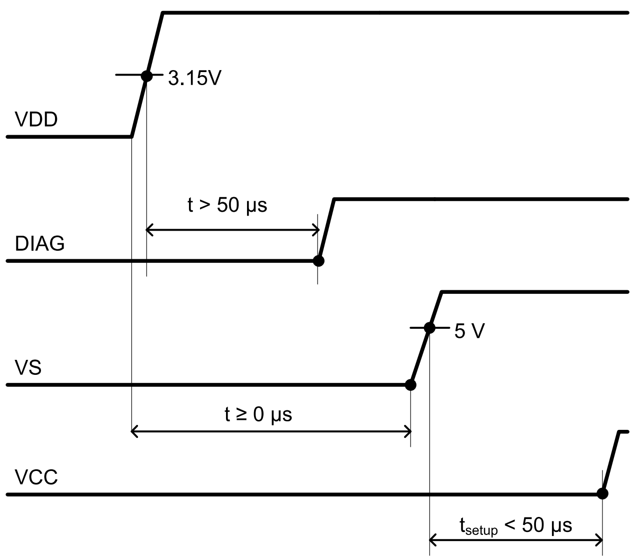


Figure 9. Power−up Sequence for DIAG pin. VDD is supplied first, VS comes up later or equal.

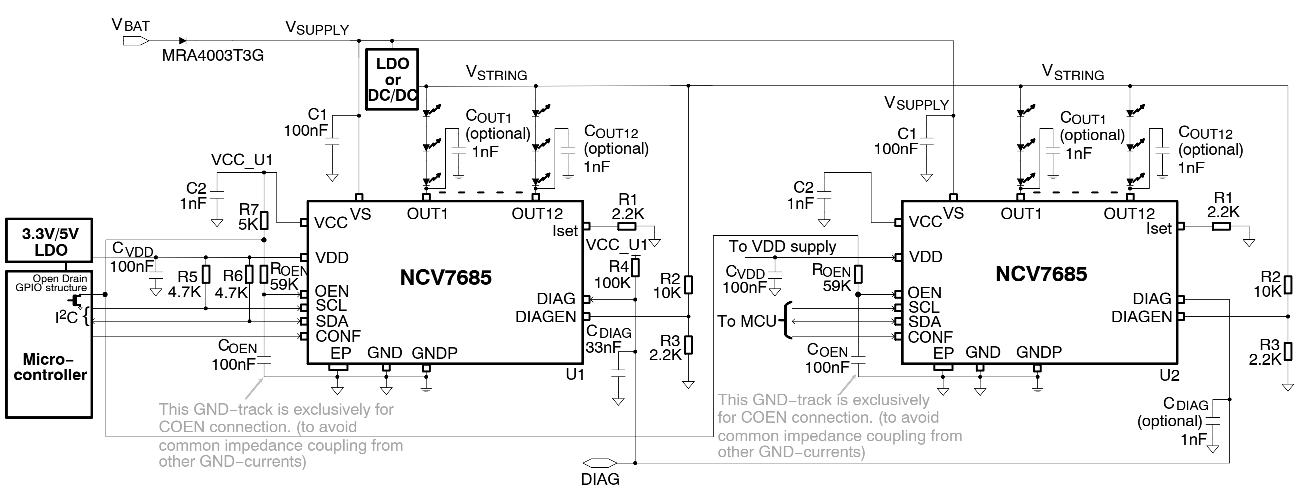


Figure 10. Example of using Multiple NCV7685 Drivers Controlled from One MCU

Parallel Outputs

The maximum rating per output is 60 mA. In order to increase system level LED string current, parallel combinations of any number of outputs is allowed. Combining all 12 outputs will allow for a maximum system level string current design of 720 mA.

Required Time Delay for OTP Zapping

As soon as the ID_LOCK_OTP message is received, the I2C acknowledge is immediately sent out to the MCU. However, the internal circuitries still requires 500 µs time delay to complete the OTP zapping of one OTP bit. Therefore, no I2C confirmation is send. The number of OTP bits that are zapped corresponds with each change from the default values. It is needed 16.5 ms in total to successfully finish the zapping sequence of all 32 customer bits + one internal bit. The verification of the OTP banks can be done by readout of the ID_READ_OTP I2C message after zapping delay.

DIGITAL PART AND I2C REGISTERS

The I^{2}C bus consists of two wires, serial data (SDA) and serial clock (SCL), carrying information between the devices connected on the bus. Each device connected to the bus is recognized by a unique address. The NCV7685 can both receive and transmit data with CRC8 error detection algorithm. The NCV7685 is a slave device only. Generation of the signals on the I^{2}C bus is always the responsibility of the master device.

They are multiple kinds of message structure possible versus ID code received.

Table 7. IDENTIFIER ADDRESSING (ID) MESSAGE

Name	ID	Access type	Name of Register Addressed
ID_I2C_CONF	00	W	I2C_CONF
ID_PWM	01	W	PWM_DUTY
ID_PWM_CONF	02	W	PWM_CONF, PWM_DUTY_EN
ID_PWM_ALL	03	W	PWM_D1, PWM_D2, PWM_D3, PWM_D4, PWM_D5, PWM_D6, PWM_D7, PWM_D8, PWM_D9, PWM_D10, PWM_D11, PWM_D12
ID_WRITEALL	04	W	I2C_CONF, PWM_CONF, PWM_DUTY_EN
ID_STATUS	08	R	I2C_STATUS
ID_FAULT	09	R	FAULT_STATUS
ID_READALL	0A	R	I2C_CH_STATUS, I2C_STATUS, FAULT_STATUS
ID_SET_OTP	20	W	SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET
ID_LOCK_OTP	21	W	SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET
ID_READ_OTP	28	R	ID_VERS_1, ID_VERS_2, SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET

There are three kinds of registers, Hard Coding, OTP and volatile registers.

Hard Coding Registers:
- ID_VERS_1
- ID_VERS_2

OTP Registers:
- ADD_SAM_SET
- SAM_CONF_1
- SAM_CONF_2

Volatile Registers:
- I2C_CONF
- I2C_STATUS
- I2C_CH_STATUS
- FAULT_STATUS
- PWM_DUTY
- PWM_D1 – PWM_D12
- PWM_DUTY_EN
- PWM_CONF

Format of the I2C frames

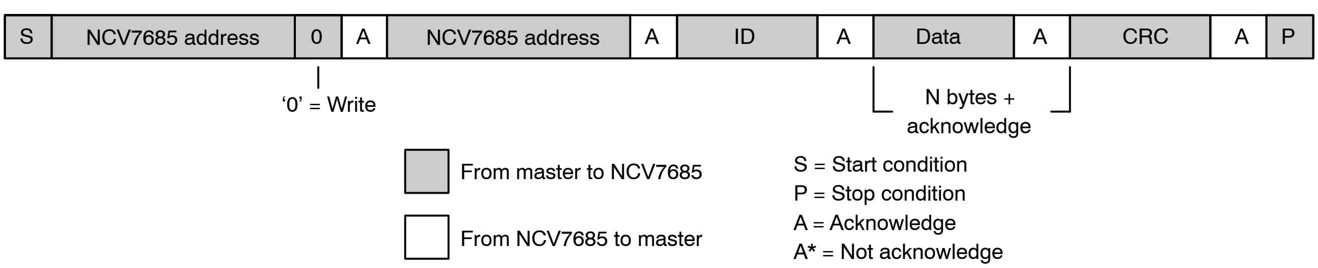


Figure 11. Format of I2C Write Access Frames

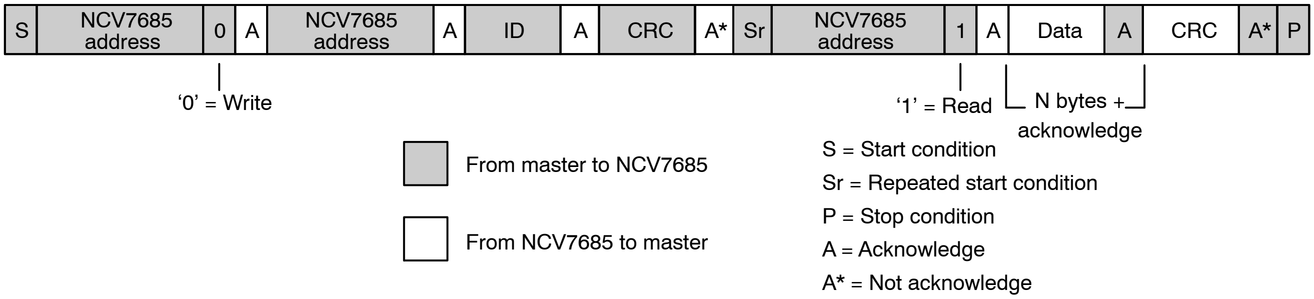


Figure 12. Format of I2C Read Access Frames

Remark: CRC byte is not transmitted when CRC protection is turned off (ERREN = 0)

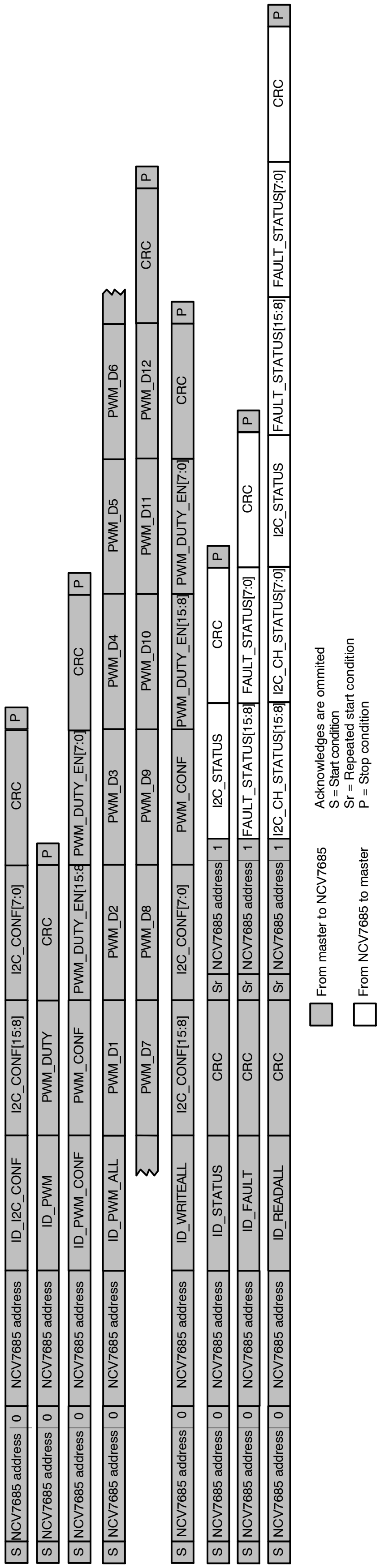


Figure 13. Format of I2C Frames

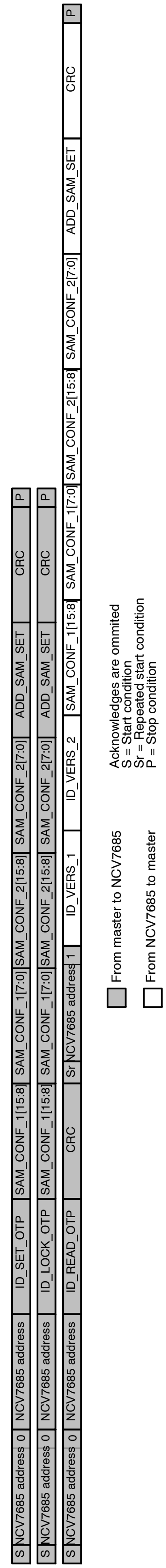


Figure 14. Format of I2C OTP Frames

There is a safety mechanism implemented by repeating the address. Since the I^2C address is 7 bits long, first bit of the second address byte starts with a "0" in the repeated byte (see tables below).

Table 8.

1st byte							
7	6	5	4	3	2	1	0
I^2C device Address							R/W Bit
2nd byte							
7	6	5	4	3	2	1	0
I^2C device Address							0

CRC ERROR DETECTION ALGORITHM

The CRC protection is turned off by default. It can be enabled by activation of the OTP ERREN bit (ERREN = 1). The every I^2C byte including both addresses with R/W flag are calculated using CRC8 algorithms. The CRC polynomial is following: $x^8 + x^5 + x^3 + x^2 + x + 1$.

Example of the CRC used in the I^2C message with I2C_CONF byte = 0xCFFF and with I^2C address 0x60 (0xC0) is 0x2E.

HARD CODING REGISTERS

Table 9. HARD CODING REGISTERS

Bit	D7	D6	D5	D4	D3	D2	D1	D0
ID_VERS_1								
Access type	R	R	R	R	R	R	R	R
Bit name	ID1[7:0]							
Reset value	0	1	0	0	0	0	1	1
ID_VERS_2								
Access type	R	R	R	R	R	R	R	R
Bit name	ID2[7:0]							
Reset value	0	0	0	0	0	1	0	0

11. ID1[7:0] = 43h (**onsemi** device identifier)
ID2[7:0] = 04h (The actual version)

OTP REGISTERS

Table 10. ADD_SAM_SET

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit name	AUTOR	DETONLY	ERREN	ADD[4:0]				
Reset value	0	1	0	0	0	0	0	0

ADD[4:0] are the programmable BUS address registers (in I2C mode ADD[6:5] = 11).

AUTOR: When AUTOR=1 (and DIAGEN is high), open load diagnosis is performed. When a fault is detected, the DIAG pin is set and LED driver imposes a low current on the faulty branch alone, switching off the others. When fault is recovered, LED driver returns to normal operation after resetting the DIAG pin. If the DIAG pin is triggered externally, LED driver outputs are switched off and the low power mode is entered.

DETONLY: When DETONLY=1, open load diagnostic is performed. When a fault is detected, the DIAG pin is set without taking any action on the current regulation. When fault is recovered, DIAG is reset. If the DIAG pin is triggered externally, no action is taken.

When *AUTOR = DETONLY = 0,* no diagnostic performed

When *AUTOR = DETONLY = 1,* no change (same as previously setting).

ERREN: When ERREN = 1, CRC error detection algorithm is activated for I^2C communication.

Table 11. SAM_CONF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SAM_CONF_1																
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit name	–	–	–	–	SAM1conf[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAM_CONF_2																
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit name	–	–	–	–	SAM2conf[11:0]											
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

12. SAM1conf[x] = 0 means channel is OFF and SAM1conf[x] = 1 means channel is ON
SAM2conf[x] = 0 means channel is OFF and SAM2conf[x] = 1 means channel is ON

VOLATILE REGISTERS

Table 12. I2C_CONF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Bit name	I2CFLAG	I2CautoR	I2CdOnly	PWMEN	I2Cconf[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The NCV7685 is in I^2C mode when I2CFLAG=1 and when VDD is in the operating range. Standalone mode is activated by resetting the I2CFLAG which can be done with one of the following methods:

- method 1: By writing “0” on I2CFLAG−bit through I^2C communication.
- method 2: By generating undervoltage on VDD (VDD < VDDUV_F) while VS remains in operating range.
- method 3: By generating POR by switching off both VS and VDD supply and then power−on again.
- VS and VDD supply have reached their off−state when both have their capacitors discharged to below 1 V.

I2CautoR: When I2CautoR=1 (and DIAGEN is high), open load diagnosis is performed. When a fault is detected, the DIAG pin is set and LED driver imposes a low current on the faulty branch alone, switching off the others. When fault is recovered, LED driver returns to normal operation after resetting the DIAG pin. If the DIAG pin is triggered externally, LED driver outputs are switched off and the low power mode is entered. Whenever the device is configured in autorecovery (AUTOR in standalone mode or I2CautoR in I2C mode), it is not allowed to put PWMDUTY = 0 or PWMDx = 0 to a channel which has detected an open load.

I2CdOnly: When I2CdOnly =1, open load diagnostic is performed. When a fault is detected, the DIAG pin is set without taking any action on the current regulation. When fault is recovered, DIAG is reset. If the DIAG pin is triggered externally, no action is taken.

When *I2CautoR* = *I2CdOnly* = *0*, no diagnostic performed.

When *I2CautoR* = *I2CdOnly* = *1*, no change (same as previously setting).

PWMEN: When PWMEN = 1, PWM is activated, when PWMEN = 0 the content of the complete register PWM_DUTY_EN is not reset and PWM is disabled.

I2Cconf[x] = 0 means channel is OFF and I2Cconf[x] = 1 means channel is ON.

Table 13. I2C_STATUS

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R	R	R	R	R	R	R	R
Bit name	SC_Iset	I2Cerr	UV	diagRange	TW	TSD	DIAGERR	OL
Reset value	0	0	0	0	0	0	0	0

SC_Iset: SC_Iset = 1 means there is short−circuit on the external resistor on I_{SET} pin and drivers are switched OFF and DIAG pin is set. SC_Iset=0 no short−circuit.

I2Cerr: I2Cerr=1 means an error has been detected during the I2C communication, I2Cerr=0 means no error during I2C communication has been detected.

UV: the device is in under voltage condition (VS is below VSUV threshold, all channels OFF).

diagRange: when diagRange = 1 the divided voltage is above the typical value of 2 V (LED diagnostic is enabled), diagRange = 0 means the divided voltage is below the typical value of 2 V (LED diagnostic is disabled).

TW: when TW=1 the device is in the thermal warning range (typ 140°C), this flag is just a warning no action is foreseen on the output drivers. TW=0 means the device is below the thermal warning range.

TSD: when TSD = 1 the device is in the Thermal shutdown range, TSD = 0 means the device is below the thermal shutdown range.

DIAGERR: DIAGERR = 1 means an error is detected by DIAG pin forced externally.

OL: OL = 1 means at least one channel is in Open Load condition, OL = 0 no Open Load.

Table 14.

SC_Iset	set when a short−circuit on the external resistor on I_{SET} pin, latched if permanent after 10 μs. Reset in case of short−circuit disappear permanently for at least 10μs.
I2Cerr	set if an error has been detected during the I2C communication. Reset on register reading.
UV	set when device is in under voltage condition (VS is below VSUV, all channels OFF).
diagRange	set when divided voltage is above the VDiagenTH threshold. Reset when the divided voltage is below the VDiagenTH threshold.
TW	set when junction temperature is above the Tjwar_on threshold. Reset on register reading AND temperature is below the (Tjwar_on − Tjsd_hys) threshold
TSD	set when junction temperature is above the TSD threshold. Reset on register reading AND temperature is below the TSD − Tjsd_hys) threshold
DIAGERR	set by DIAG pin forced low externally, latched if permanent after 10 μs. Reset in case DIAG pin is not forced permanently for at least 10 μs.
OL	set in Open Load condition and DIAGEN is high, latched if permanent after 10 μs. Reset if Open Load disappear permanently for at least 10 μs. Fault information is maintained on falling DIAGEN threshold exceeded

Table 15. I2C_CH_STATUS

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit name	I2CFLAG	I2CautoR	I2CdOnly	PWMEN	I2C_CH_STATUS[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2CFLAG: same as I2C_CONF register
I2CautoR: same as I2C_CONF register
I2CdOnly: same as I2C_CONF register
PWMEN: same as I2C_CONF register
I2C_CH_STATUS[11:0]: same as I2C_CONF[11:0] bits in I2C mode or same as SAM_CONF_1[11:0], SAM_CONF_2[11:0] bits in Standalone mode.

Remark: When NCV7685 is configured in I2C mode and output channel OUTx is configured to operate in PWM mode, I2C_CH_STATUS[x] shall contain value ‘1’.

Table 16. FAULT_STATUS

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit name	–	–	–	–	FAULT[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FAULT[11:0]: when FAULT[x] = 1 the OUTx channel is in fault mode (Open Load latched when the duration is longer than 10 μs), when FAULT[x] = 0 the OUTx channel is working properly. The register is reset on each read operation.

Table 17. PWM_DUTY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	W	W	W	W	W	W	W
Bit Name	–	PWMDUTY[6:0]						
Reset Value	0	0	0	0	0	0	0	0

PWMDUTY[6:0]: logarithmic (or linear) common dimming for all channels via embedded PWM generator (128 steps). Following formula applies when logarithmic dimming is selected: Duty_Cycle_Percent = $100 \times \alpha^{(N-i)}$ where $\alpha = 0.9471$ and $N = 127$ rounded with an accuracy of 400 ns.

When PWMDUTY = 127 all channels ar fully switched on.

When PWMDUTY = 0 all channels are switched off.

Whenever the device is configured in autorecovery (AUTOR in standalone mode or I2CautoR in I2C mode), it is not allowed to put PWMDUTY = 0 or PWMDx = 0 to a channel which has detected an open load.

Transmitting PWM_DUTY via I^2C will cause setting the value to all channels.

Table 18. PWM_Dx

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	W	W	W	W	W	W	W
Bit Name	–	PWMDx[6:0]						
Reset Value	0	0	0	0	0	0	0	0

PWMDx[6:0]: logarithmic (or linear) independent PWM dimming for each OUTx channel via embedded PWM generator (128 steps). Following formula applies when logarithmic dimming is selected: Duty_Cycle_Percent = $100 \times \alpha^{(N-i)}$ where $\alpha = 0.9471$ and $N = 127$ rounded with an accuracy of 400 ns.

When PWMDx = 127 the OUTx channel is fully switched on.

When PWMDx = 0 the OUTx channel is switched off.

Whenever the device is configured in autorecovery (AUTOR in standalone mode or I2CautoR in I2C mode), it is not allowed to put PWMDUTY = 0 or PWMDx = 0 to a channel which has detected an open load.

To set independent PWM Duty Cycle value to each channel simultaneously, all twelve PWM_Dx bytes has to be transferred via I^2C bus in ID_PWM_ALL message. If PWM_DUTY register is updated, all PWM_Dx bytes will be overwritten by the same value from PWM_DUTY register.

Table 19. PWM_DUTY_EN

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	–	–	–	–	W	W	W	W	W	W	W	W	W	W	W	W
Bit name	–	–	–	–	PWMDUTYen[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWMDUTYen[11 :0] : when PWMDUTYen[x] = 1, PWM dimming is enabled for OUTx channel, when PWMGAINen[x] = 0 means PWM dimming is disabled for OUTx channel. When the PWM dimming is disabled, the output channel is programmed according to the I2Cconf[x] settings.

Table 20. PWM_CONF

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	W	W	W	W	W	W	W	W
Bit Name	–	–	–	–	–	PWMLIN	PWMF2	PWMF1
Reset Value	0	0	0	0	0	0	0	0

PWMLIN bit shall select between between logarithmic (PWMLIN=0) and linear (PWMLIN=1) translation of PWMDUTY bits to duty cycle of internal PWM signal.

PWMF2 and *PWMF1* bits set typical PWM frequency settings according to the Table 21.

Table 21. TYPICAL PWM FREQUENCY SETTINGS

PWMF2	PWMF1	typ. PWM frequency [Hz]
0	0	150
0	1	300
1	0	600
1	1	1200

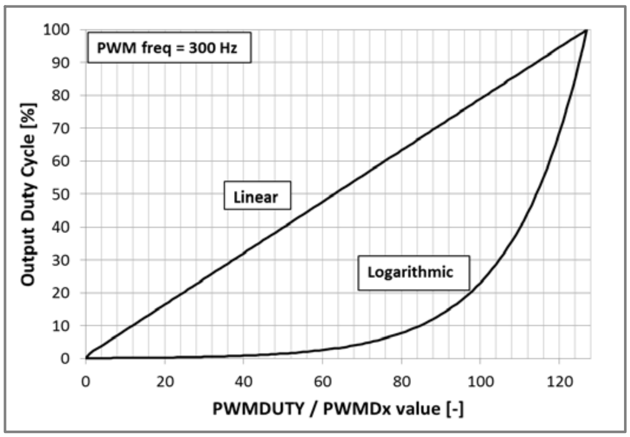


Figure 15. Output Duty Cycle vs. Register Setting

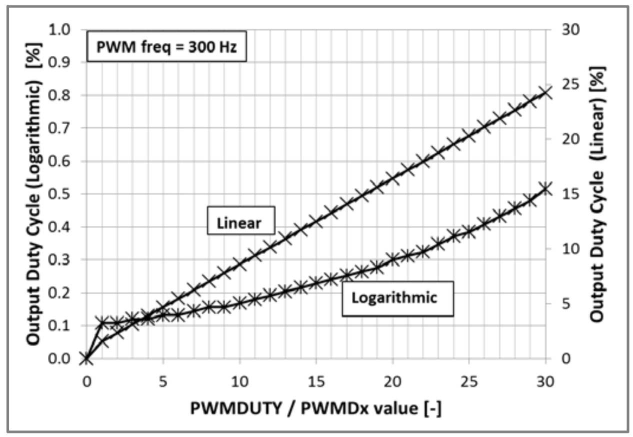
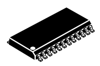


Figure 16. Output Duty Cycle vs. Register Setting – Detail



SCALE 1:1

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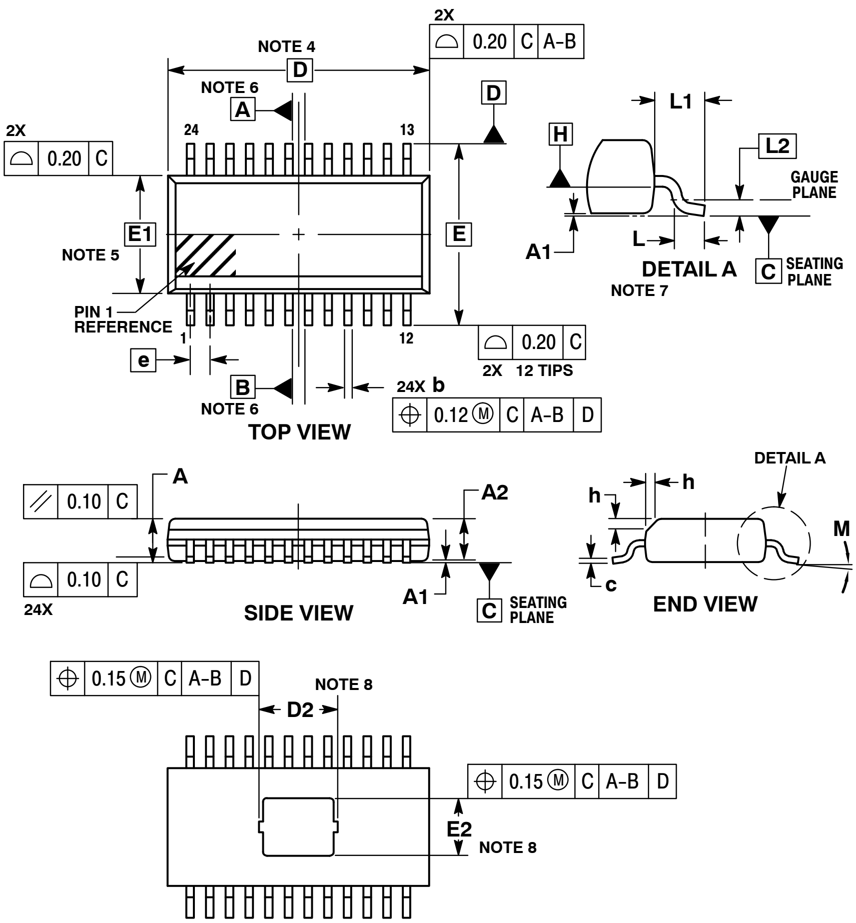
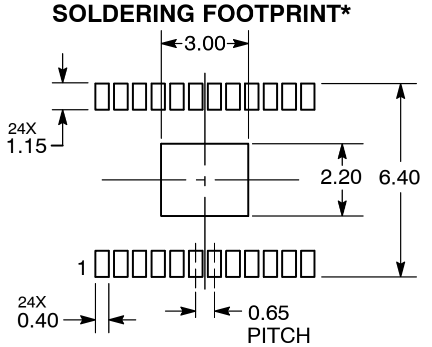


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	2.50	2.70
E	6.00 BSC	
E1	3.90 BSC	
E2	1.80	2.00
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

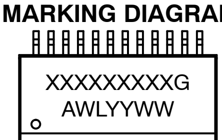
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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