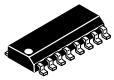
THE DATASHEET OF

NB4N507ADG

www.win-source.net 0086-755-83957316

3.3 V/5 V, 50 MHz to 200 MHz PECL Clock Synthesizer

NB4N507A



SOIC−16
D SUFFIX
CASE 751B−05

Description

The NB4N507A is a precision clock synthesizer which generates a very low jitter differential PECL output clock. It produces a clock output based on an integer multiple of an input reference frequency.

The NB4N507A accepts a standard fundamental mode crystal, using Phase−Locked−Loop (PLL) techniques, will produce output clocks up to 200 MHz. In addition, the PLL circuitry will produce a 50% duty cycle square−wave clock output (see Figure 7).

The NB4N507A can be programmed to generate a selection of input reference frequency multiples. An exact 155.52 MHz output clock can be generated from a 19.44 MHz crystal and the x8 multiplier selection. The NB4N507A is intended for low output jitter clock generation.

The PECL outputs are 15 mA open collector and must be DC loaded and AC terminated. See Figures 4 and 6.

Features

- Input Crystal Frequency of 10 − 27 MHz
- Enable Usage of Common Low−Cost Crystal
- Differential PECL Output Clock Frequencies up to 200 MHz
- Duty Cycle of 48%/52%
- Operating Range: V_{CC} = 3.0 V to 5.5 V
- Ideal for SONET Applications and Oscillator Manufacturers
- Available in Die Form
- Packaged in 16−Pin Narrow SOIC
- Pb−Free Packages are Available*

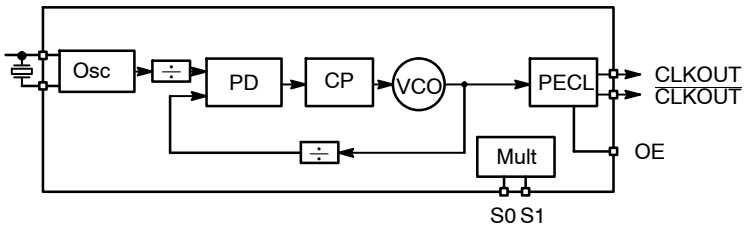
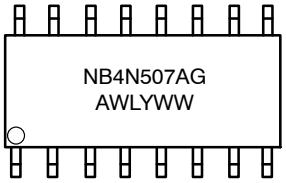


Figure 1. Simplified Logic Block Diagram

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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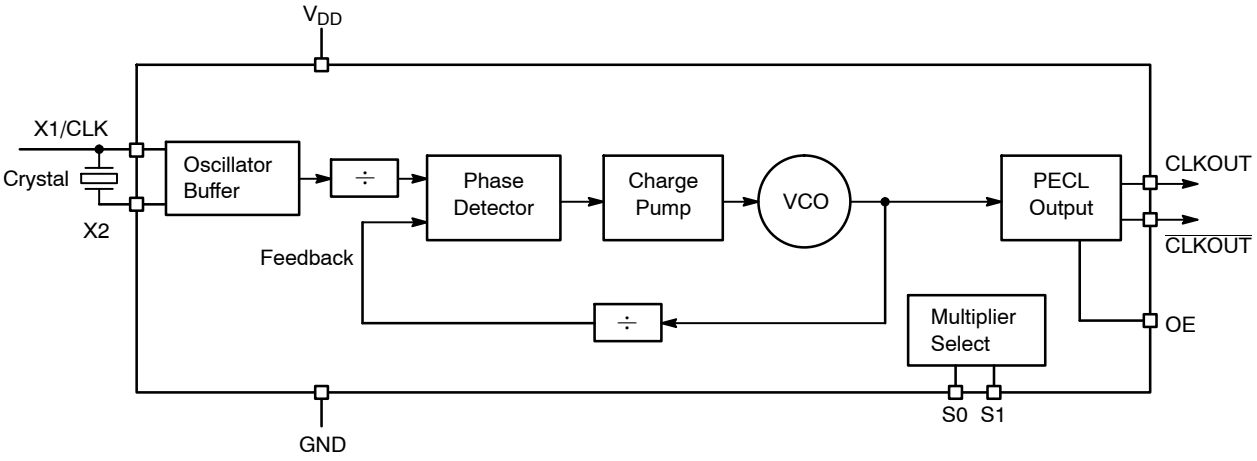

Figure 2. NB4N507A Logic Diagram

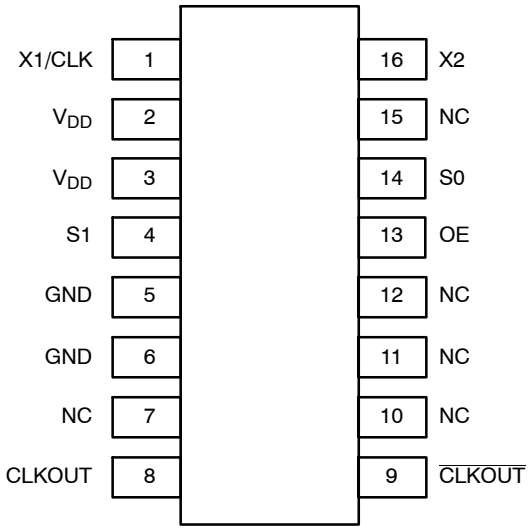

Figure 3. 16−Pin SOIC (Top View)

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1	S0	Multiplier
L	L	9.72X*
L	M	10X
L	H	12X
M	L	6.25X
M	M	8X
M	H	5X
H	L	NA
H	M	3X
H	H	4X

*Example Crystal = 16 MHz, f_{CLKOUT} = 155.52 MHz
L = GND
H = V_{DD}
M = OPEN

Table 2. OE, OUTPUT ENABLE FUNCTION

OE	Function
0	Disable
1	Enable

Table 3. PIN DESCRIPTION

Pin # SOIC−16	Name	I/O	Description
1	X1/CLK	Crystal Input	Crystal or Clock Input
2,3	V_{DD}	Power Supply	Positive Supply Voltage (3.0 V to 5.5 V)
4	S1	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to V_{DD} ÷ 2
5,6	GND	Power Supply	Negative Supply Voltage
7,10,11,12, 15	NC	No Connect	Pin 10 does not require an external resistor. The NB4N507A will function with or without a resistor on Pin 10.
8	CLKOUT	PECL Output*	Non−inverted differential PECL clock output.
9	$\overline{\text{CLKOUT}}$	PECL Output*	Inverted differential PECL clock output.
13	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the CLKOUT/$\overline{\text{CLKOUT}}$ Outputs. Outputs are enabled when HIGH or when left open; OE pin has internal pullup resistor. Disables both outputs when LOW. CLKOUT goes LOW, $\overline{\text{CLKOUT}}$ goes HIGH.
14	S0	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to V_{DD} ÷ 2
16	X2	Crystal Input	Crystal Input

*The PECL Outputs are 15 mA open collector and must be DC loaded and AC terminated. See Figures 4, 5 and 6.

Table 4. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model Charged Device Model	> 1 kV > 150 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	1145 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		6	V
V_I	Input Voltage			GND − 0.5 ≤ V_I ≤ V_{DD} + 0.5	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−16	100 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	SOIC−16	33 to 36	°C/W
T_{sol}	Wave Solder Pb Pb−Free	< 3 sec @ 248°C < 3 sec @ 260°C		265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, GND = 0 V, T_A = −40°C to +85°C (Note 3))

Symbol	Characteristic		Min	Typ	Max	Unit
I_{DD}	Power Supply Current (does not include output load resistor current)	V_{DD} = 5 V V_{DD} = 3.3 V	15 10	27 23	35 30	mA mA
V_{OH}	Output HIGH Voltage (Notes 5 & 6)	V_{DD} = 5 V V_{DD} = 3.3 V	3.95 2.57	4.05 2.67	4.15 2.77	V
V_{OL}	Output LOW Voltage (Notes 5 & 6)	V_{DD} = 5 V V_{DD} = 3.3 V	3.12 1.90	3.20 2.00	3.30 2.10	V
V_{IH}	Input HIGH Voltage (Note 4)	S0, S1, X1/CLK OE	V_{DD} − 0.5 2.0		V_{DD}	V
V_{IL}	Input LOW Voltage,(Note 4)	S0, S1, X1/CLK OE	0		0.5 0.8	V
C_x	Internal Crystal Capacitance, X1 & X2			0		pF
C_{in}	Input Capacitance, S0, S1, OE			5.0		pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. PECL output parameters vary 1:1 with V_{DD}.
4. S0 and S1 default to V_{DD} ÷ 2 when left open.

Table 7. AC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, GND = 0 V, T_A = −40°C to +85°C (Note 5))

Symbol	Characteristic	Min	Typ	Max	Unit
f_{Xtal}	Crystal Input Frequency (Note 7)	10		27	MHz
f_{CLK}	Input Clock Frequency (Note 8)	5		52	MHz
f_{OUT}	Output Frequency Range	50		200	MHz
$V_{out\ pk-pk}$	Output Amplitude	550	680		mV
DC	Clock Output Duty Cycle (Note 8)	48		52	%
PLL_{BW}	PLL Bandwidth (Note 8)	10			kHz
$t_{jitter\ (pd)}$	Period Jitter (RMS, 1σ, 10,000 Cycles)			10	ps
$t_{jitter\ (pd)}$	Period Jitter (Peak−to−Peak, 10,000 Cycles)			±20	ps
tr/tf	Output Rise and Fall Times (Note 8)	50	270	500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. PECL outputs loaded with external resistors for proper operation (see Figures 4, 5 and 6).
6. V_{OH} and V_{OL} can be set by the external resistors, which can be modified.
7. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where CL is the specified crystal load capacitance: Crystal caps (pF) = (CL−5) x 2. So, for a crystal with 16 pF load capacitance, use two 22 pF caps, including board trace capacitance (see Figure 7).
8. Guaranteed by design and characterization.

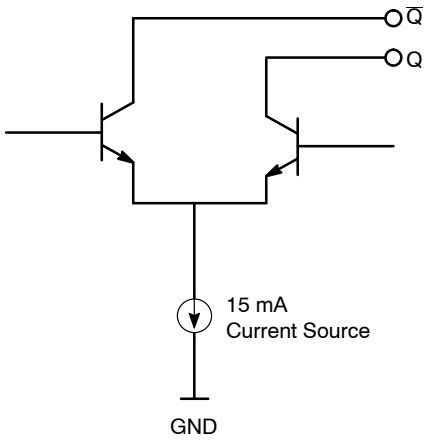

Figure 4. Output Structure

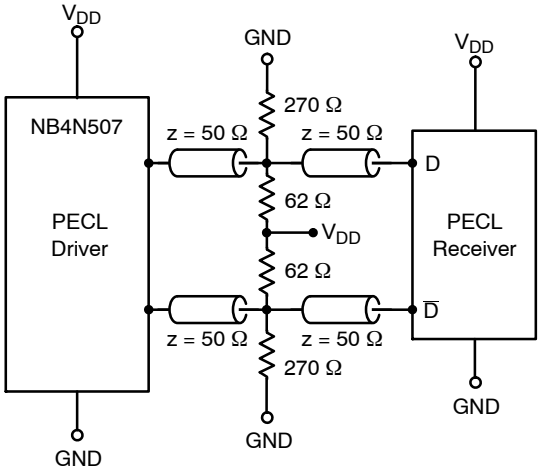

Figure 5. Evaluation Test Load for the NB4N507A

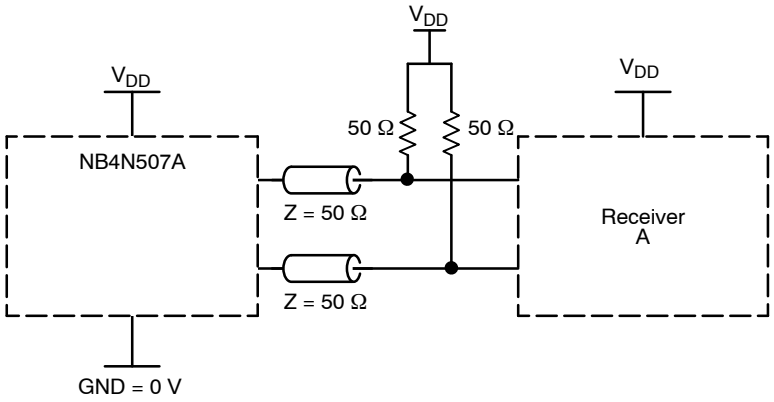

Figure 6. Alternate Termination for Output Driver and Device Evaluation

APPLICATIONS INFORMATION

High Frequency Differential PECL Oscillators: The NB4N507A, along with a low frequency fundamental mode crystal, can build a high frequency differential PECL output oscillator. For example, a 10 MHz crystal connected to the NB4N507A with the 12X output selected (S1 = 0, S0 = 1) produces a 120 MHz PECL output clock.

Crystal Oscillator Input Interface

The NB4N507A features an integrated crystal oscillator to minimize system implementation costs. The oscillator circuit is a parallel resonant circuit and thus, for optimum performance, a parallel resonant crystal should be used.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NB4N507A as possible to avoid any board level parasitics. Surface mount crystals are recommended, but not required.

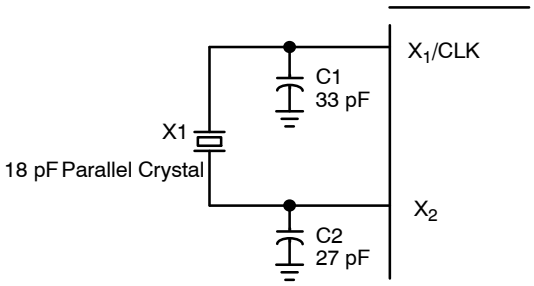

Figure 7. Crystal Input Interface

High Frequency VCXO: The bandwidth of the PLL is guaranteed to be greater than 10 kHz. This means that the PLL will track any modulation on the input with a frequency of less than 10 kHz. By using this property, a low frequency VCXO can be built. The output can then be multiplied by the NB4N507A, thereby producing a high frequency VCXO.

High Frequency TCXO: Extending the previous application, an inexpensive, low frequency TCXO can be built and the output frequency can be multiplied using the NB4N507A. Since the output of the chip is phase−locked to the input, the NB4N507A has no temperature dependence, and the temperature coefficient of the combined system is the same as that of the low frequency TCXO.

Decoupling and External Components

The NB4N507A requires a 0.01 μF decoupling capacitor to be connected between V_{DD} and GND on pins 2 and 5. It must be connected close to the NB4N507A. Other V_{DD} and GND connections should be connected to those pins, or to the V_{DD} and GND planes on the board. Another four resistors are needed for the PECL outputs as shown in Figure 4. Suggested values of these resistors are shown, but they can be varied to change the differential pair output swing, and the DC level.

ORDERING INFORMATION

Device	Package	Shipping†
NB4N507ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 9)

NB4N507ADG	SOIC−16 (Pb−Free)	48 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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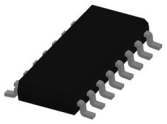
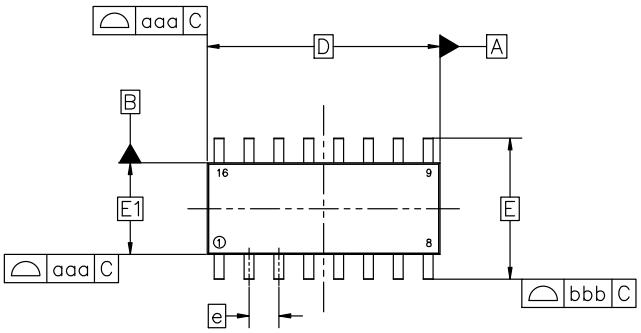
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



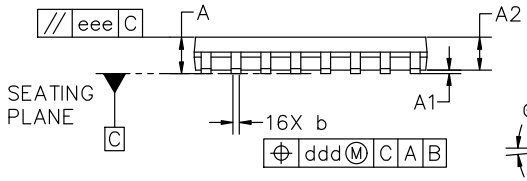
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

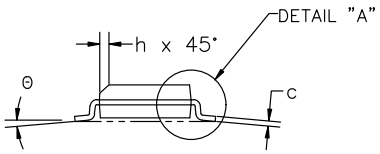
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

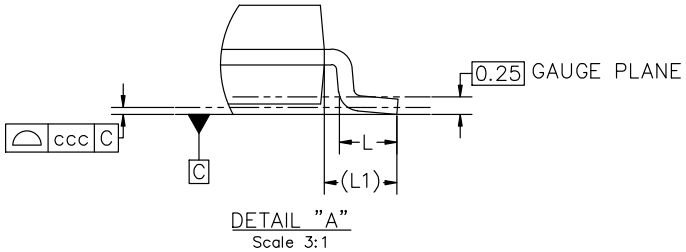


SIDE VIEW

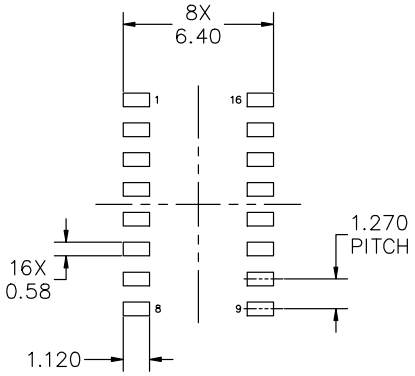


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

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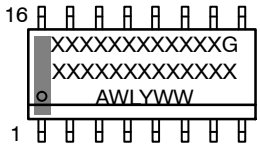
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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