



**THE DATASHEET OF  
N74F164D,602**



# DATA SHEET

**74F164**

**8-bit serial-in parallel-out shift register**

Product specification  
Supersedes data of 1995 Sep 22

2000 Dec 18

# 8-bit serial-in parallel-out shift register

74F164

## FEATURES

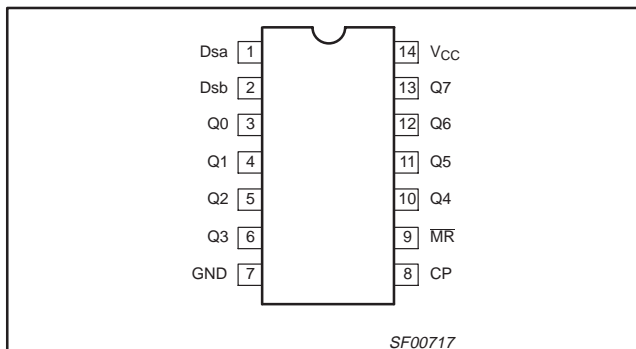
- Gated serial data inputs
- Typical shift frequency of 100MHz
- Asynchronous Master Reset
- Buffered clock and data inputs
- Fully synchronous data transfer
- Industrial temperature range available (-40 to +85 °C)

## DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (Dsa, Dsb); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the clock (CP) input, and enters into Q0 the logical AND of the two data inputs (Dsa, Dsb) that existed one setup time before the rising edge. A Low level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{max}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33 mA

## ORDERING INFORMATION

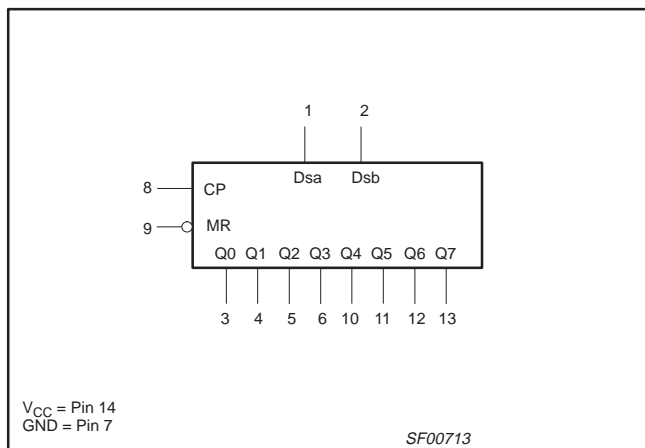
DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5 V \pm 10\%$ , $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$	INDUSTRIAL RANGE $V_{CC} = 5 V \pm 10\%$ , $T_{amb} = -40 \text{ to } +85 \text{ }^\circ\text{C}$	
14-pin plastic DIP	74F164N	I74F164N	SOT27-1
14-pin plastic SO	74F164D	I74F164D	SOT108-1

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

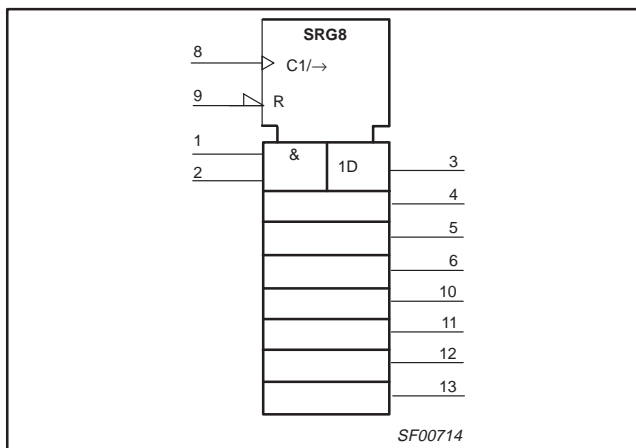
PINS	DESCRIPTION	74F (U.L.) HIGH / LOW	LOAD VALUE HIGH / LOW
Dsa, Dsb	Data inputs	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
CP	Clock pulse input (active rising edge)	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
MR	Master reset input (active-Low)	1.0 / 1.0	20 $\mu\text{A}$ / 0.6 mA
Q0 – Q7	Data outputs	50 / 33	1.0 mA / 20 mA

One (1.0) FAST unit load is defined as: 20  $\mu\text{A}$  in the High state and 0.6 mA in the Low state.

## LOGIC SYMBOL



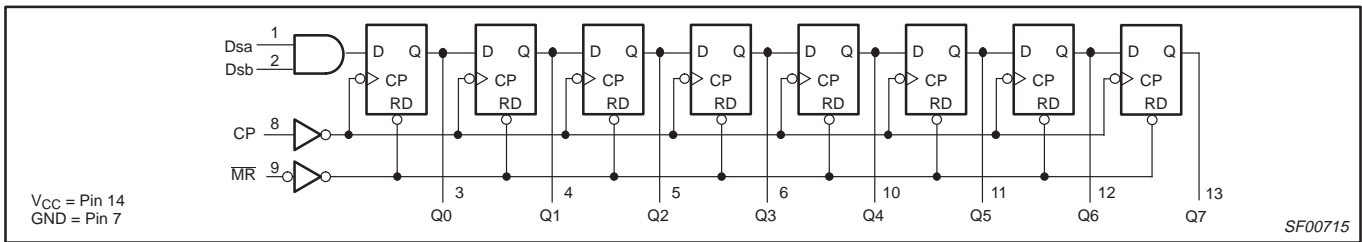
## IEC/IEEE SYMBOL



# 8-bit serial-in parallel-out shift register

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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUTS								OPERATING MODE	
MR	CP	Dsa	Dsb	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7		
L	X	X	X	L	L	L	L	L	L	L	L	L	Reset (Clear)
H	↑	l	l	L	q0	q1	q2	q3	q4	q5	q6	q6	Shift
H	↑	h	l	L	q0	q1	q2	q3	q4	q5	q6	q6	
H	↑	h	h	H	q0	q1	q2	q3	q4	q5	q6	q6	

H = High voltage level  
 h = High voltage level one setup time prior to the Low-to-High clock transition.  
 L = Low voltage level  
 l = Low voltage level one setup time prior to the Low-to-High clock transition.  
 qn = Lower case letter indicate the state of the referenced output one setup time prior to the Low-to-High clock transition.  
 X = Don't care  
 ↑ = Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial Range	0 to +70
		Industrial Range	-40 to +85
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>Ik</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial Range	0	+70	°C
		Industrial Range	-40	+85	

# 8-bit serial-in parallel-out shift register

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## DC ELECTRICAL CHARACTERISTICS

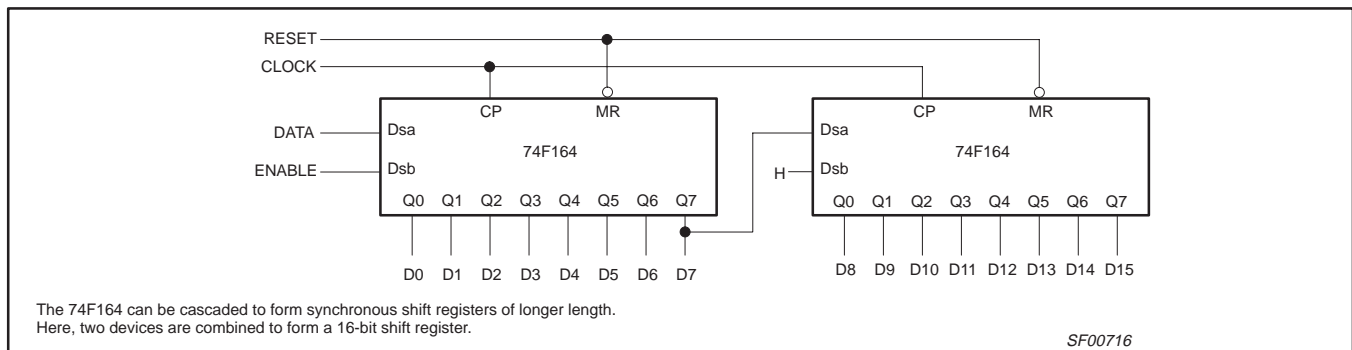
(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
			±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
			±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0 V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20	μA	
I <sub>ILL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-0.6	mA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-60		-150	mA	
I <sub>CC</sub>	Supply current (total) <sup>4</sup>	V <sub>CC</sub> = MAX		33	55	mA	

### Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
3. Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I<sub>OS</sub> tests should be performed last.
4. Measure I<sub>CC</sub> with the serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then applied to Master Reset, and all outputs open.

## APPLICATION



# 8-bit serial-in parallel-out shift register

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = 5\text{ V}$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$			$T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$ $V_{CC} = +5\text{ V}\pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$		$T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$ $V_{CC} = +5\text{ V}\pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$f_{max}$	Maximum clock frequency	Waveform 1	80	100		80		80		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to Qn	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	2.5 5.0	9.0 11.0	ns
$t_{PHL}$	Propagation delay MR to Qn	Waveform 3	5.5	7.5	10.5	5.5	11.5	5.5	11.5	ns

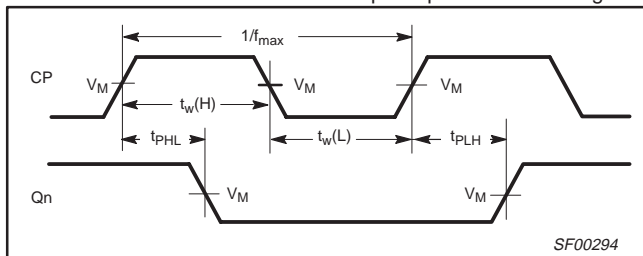
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = 5\text{ V}$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$			$T_{amb} = 0\text{ to }+70\text{ }^{\circ}\text{C}$ $V_{CC} = +5\text{ V}\pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$		$T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$ $V_{CC} = +5\text{ V}\pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\text{ }\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$t_{S(H)}$ $t_{S(L)}$	Setup time, High or Low Dn to CP	Waveform 2	7.0 7.0			7.0 7.0		7.0 7.0		ns
$t_{H(H)}$ $t_{H(L)}$	Hold time, High or Low Dn to CP	Waveform 2	1.0 1.0			2.0 2.0		2.0 2.0		ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		4.0 7.0		ns
$t_{w(L)}$	MR Pulse width Low	Waveform 3	7.0			7.0		7.0		ns
$t_{REC}$	Recovery time MR to CP	Waveform 3	7.0			7.0		7.0		ns

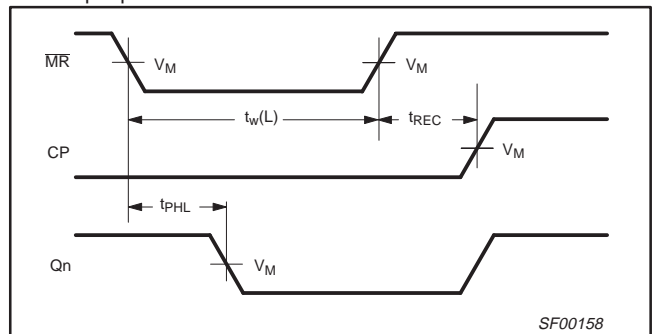
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5\text{ V}$ .

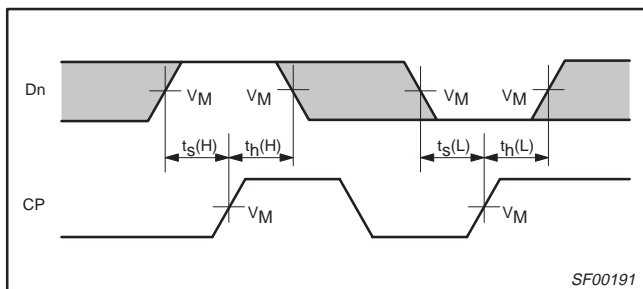
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation delay for Clock input to output, Clock Pulse width, and maximum Clock frequency



Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

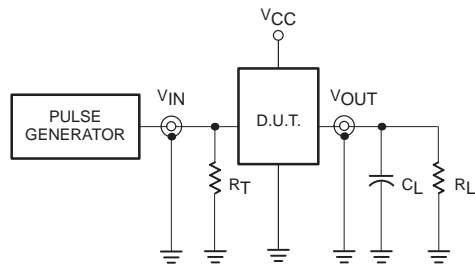


Waveform 2. Data setup and hold times

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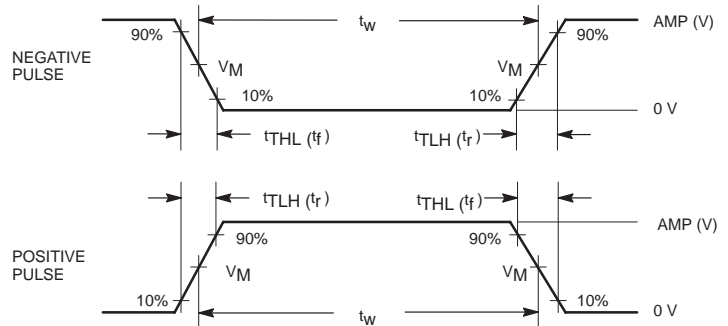
## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

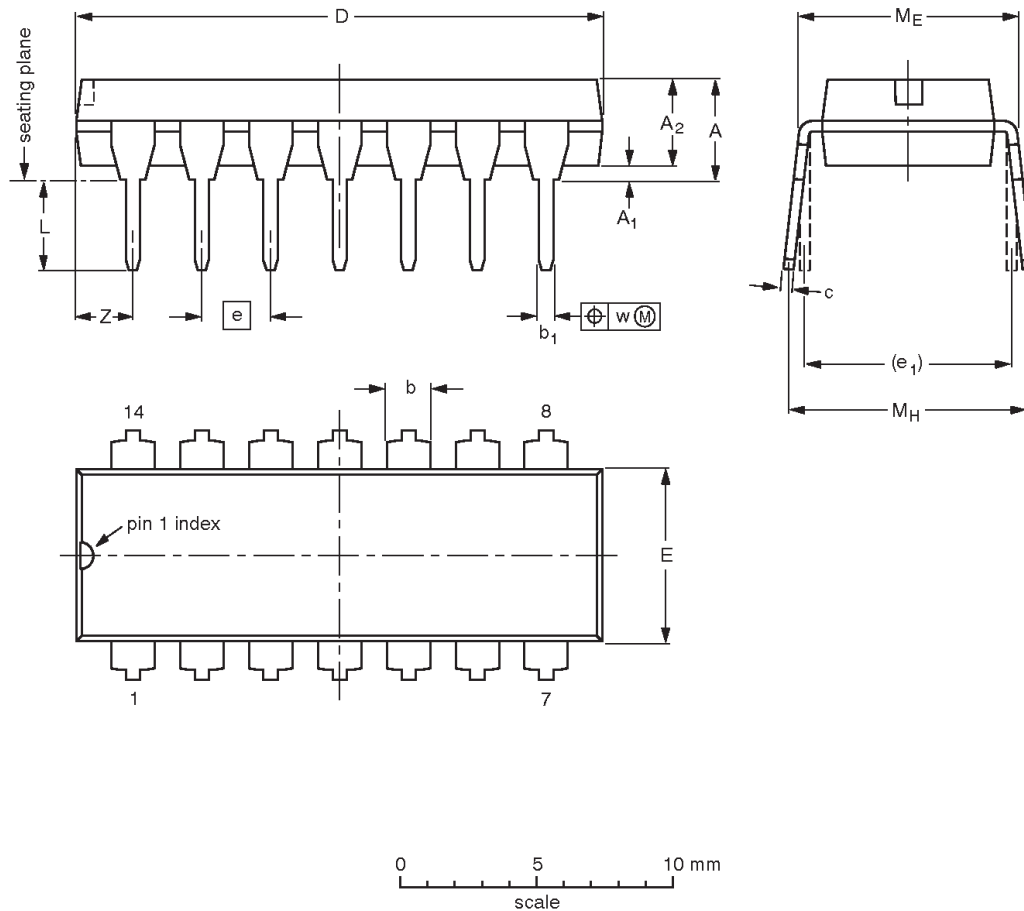
SF00006

# 8-bit serial-in parallel-out shift register

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

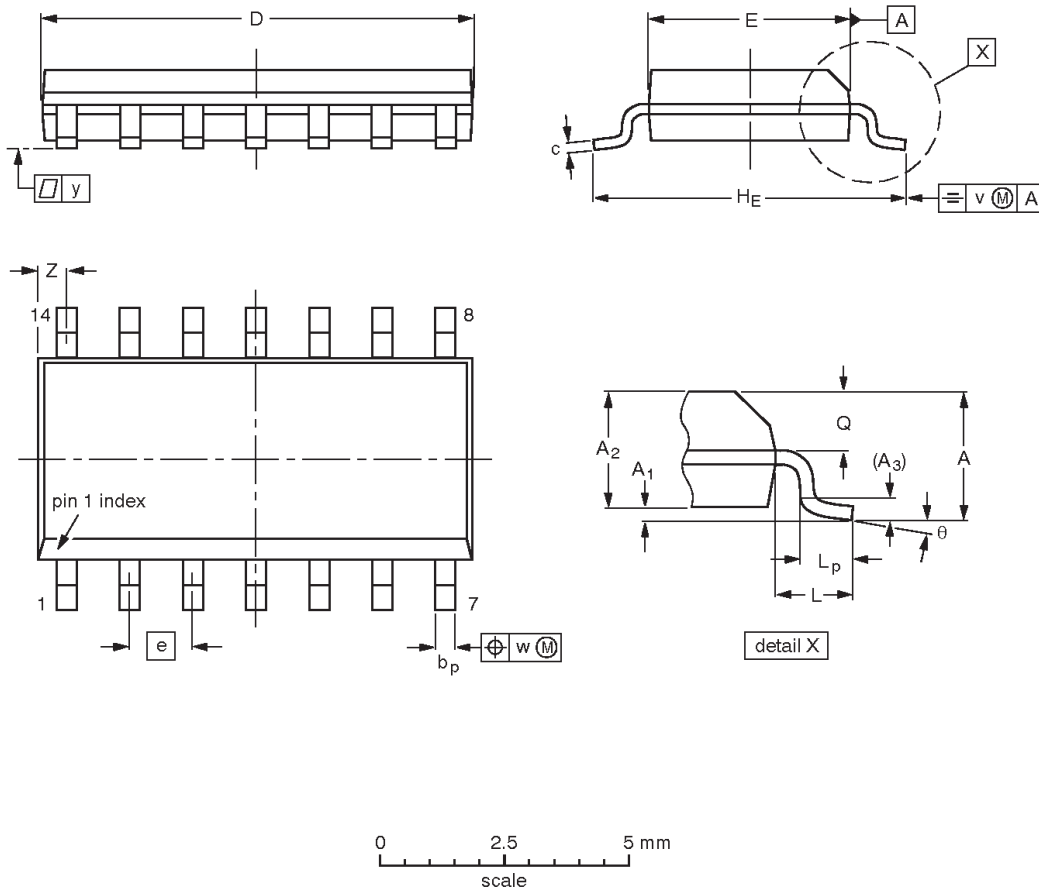
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			95-03-11 99-12-27

# 8-bit serial-in parallel-out shift register

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

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**NOTES**

## 8-bit serial-in parallel-out shift register

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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