WIN SOURCE ELECTRONICS

THE DATASHEET OF

MP2662GC-0000-Z

MP2662

500mA Single-Cell Li-ion Battery Charger with Power Path Management, 1mA Termination and <1μA Battery Leakage

DESCRIPTION

The MP2662 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited portable applications. The MP2662 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The charger function features pre-charge (PRE.C), constant current fast charge(CC) and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. This function features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2662 provides a system short-circuit protection (SCP) function by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to an excessively high current. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below a programmable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I^2C control interface allows the MP2662 to program the charging parameters, such as input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2662 is available in a 9-pin WLCSP (1.75mmx1.75mm) package.

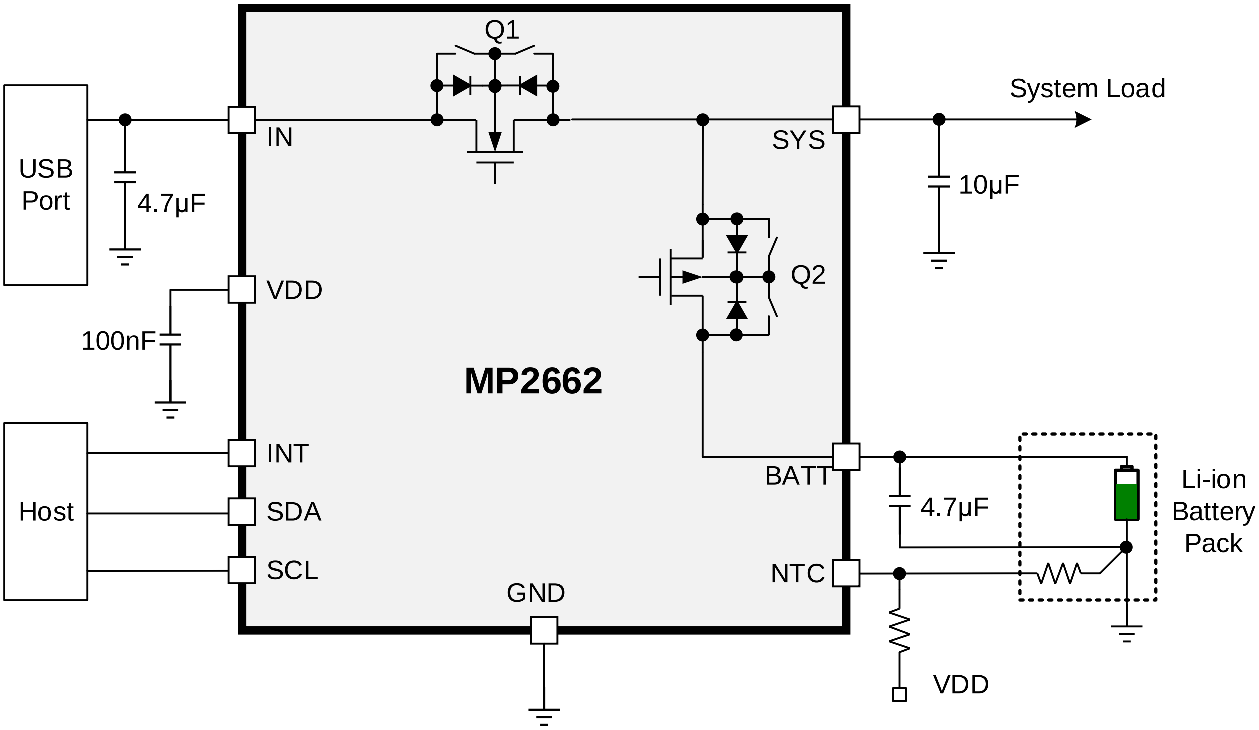
FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion/Polymer Batteries
- 21V Maximum Input Voltage Rating with Over-Voltage Protection (OVP)
- ±0.5% Charging Voltage Accuracy
- I^2C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (PCB_OTP)
- System Reset Function
- Built-In Battery Disconnection Function for Shipping Mode
- Thermal Limiting Regulation On-Chip
- Available in a WLCSP-9 (1.75mmx1.75mm) Package
- Safety-Related Certification:
  - IEC 62368-1 CB Certification

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smartwatches

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2662GC-xxxx**	WLCSP-9 (1.75mmx1.75mm)	*See Below*
EVKT-MP2662	Evaluation Kit	

*For Tape & Reel, add suffix -Z (e.g. MP2662GC-xxxx-Z).
**“xxxx” is the register setting option. The factory default is “0000.” This content can be viewed in the I^2C register map. Please contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING

JAY
LLL

JA: Product code of MP2662GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP2662

EVKT-MP2662 kit contents: (Items below can be ordered separately)

#	Part Number	Item	Quantity
1	EV2662-C-01A	MP2662 evaluation board	1
2	EVKT-USBI2C-02-bag	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order direct from MonolithicPower.com or our distributors.

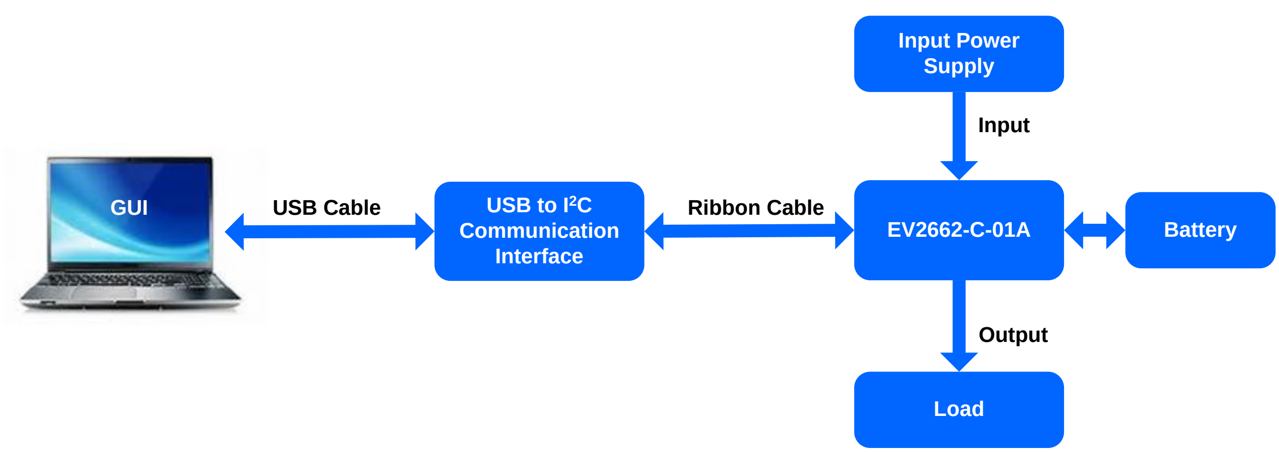
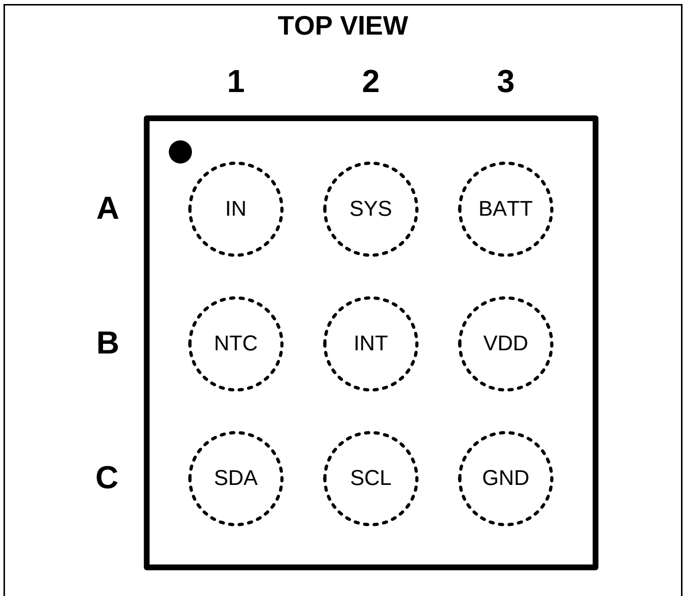


Figure 1: EVKT-MP2662 Evaluation Kit Set-Up

PACKAGE REFERENCE



WLCSP-9 (1.75mmx1.75mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
A1	IN	Power	**Input power pin.** Place a ceramic capacitor from IN to GND, and as close to the IC as possible.
A2	SYS	Power	**System power supply.** Place a ceramic capacitor from SYS to GND, and as close to the IC as possible.
A3	BATT	Power	**Battery pin.** Place a ceramic capacitor from BATT to GND as close to the IC as possible.
B1	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Configure the hot and cold temperature window by placing a resistor divider from VDD to NTC to GND. Charging is suspended when NTC is out of its range. Pull NTC to VDD if the NTC function is not used.
B2	INT	I/O	**Interrupt signal.** INT can send a charging status and fault interrupt signal to the host. INT is also used to disconnect the system from the battery. Pull INT from high to low for longer than t_{RST_DGL} (16s by default). The battery FET turns off and turns on again automatically after t_{RST_DUR} (4s by default), regardless of the INT state. Both t_{RST_DGL} and t_{RST_DUR} can be configured via the I²C interface.
B3	VDD	Power	**Internal control power supply pin.** Connect a 100nF ceramic capacitor from VDD to GND. No external load is allowed.
C1	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
C2	SCL	I	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
C3	GND	Power	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

IN ....-0.3V to +21V
SYS...................-0.3V to +5.3V (5.5V for 500µs)
All other pins to GND ....-0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
.... 0.88W
Junction temperature ....150°C
Lead temperature (solder) ....260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .. 4.35V to 5.5V (USB input)
I_{IN}..Up to 500mA
I_{DSCHG}..Up to 3.2A (5)
I_{CHG}..Up to 456mA
V_{BATT_REG} ....Up to 4.545V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
WLCSP-9 (1.75mmx1.75mm) ...	114 ...	12 .	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input under-voltage lockout threshold	V_{IN_UVLO}	Input falling	3.63	3.73	3.83	V
Input under-voltage lockout threshold hysteresis		Input rising		170		mV
Input over-voltage protection threshold	V_{IN_OVP}	Input rising threshold	5.85	6	6.15	V
Input over-voltage protection threshold hysteresis				350		mV
Input vs. battery voltage headroom threshold	V_{HDRM}	Input rising vs. battery	80	130	170	mV
Input vs. battery voltage headroom threshold hysteresis				90		mV
BATT input voltage (5)	V_{BATT}				4.5	V
Battery under-voltage lockout threshold	V_{BATT_UVLO}	BATT voltage falling, REG01h, bits[2:0] = 000	2.3	2.4	2.5	V
		BATT voltage falling, REG01h, bits[2:0] = 100	2.66	2.76	2.86	
		BATT voltage falling, REG01h, bits[2:0] = 111	2.93	3.03	3.13	
Battery under-voltage threshold hysteresis		V_{BATT_UVLO} = 2.76V		190		mV
Battery over-voltage protection threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		130		mV
Battery over-voltage protection hysteresis				60		
Power Path Management						
Regulated system output voltage accuracy	$V_{SYS\_REG\_ACC}$	V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{CHG} = 0A, REG07h, bits[3:0] = 0000, V_{SYS_REG} = 4.2V	-2		2	%
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{CHG} = 0A, REG07h, bits[3:0] = 1001, V_{SYS_REG} = 4.65V	-2		2	%
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{CHG} = 0A, REG07h, bits[3:0] = 1111, V_{SYS_REG} = 4.95V	-2		2	%
Input current limit	I_{IN_LIM}	REG00h, bits[3:0] = 0000, I_{IN_LIM} = 50mA	30	40	50	mA
		REG00h, bits[3:0] = 0011, I_{IN_LIM} = 140mA	112	126	140	
		REG00h, bits[3:0] = 1001, I_{IN_LIM} = 320mA	275	300	325	
		REG00h, bits[3:0] = 1111, I_{IN_LIM} = 500mA	440	470	500	
Input minimum voltage regulation	V_{IN_MIN}	REG00h, bits[7:4] = 0000, V_{IN_MIN} = 3.88V	3.68	3.88	4.18	V
		REG00h, bits[7:4] = 1001, V_{IN_MIN} = 4.60V	4.40	4.60	4.75	
		REG00h, bits[7:4] = 1111, V_{IN_MIN} = 5.08V	4.88	5.08	5.35	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SYS switch on resistance	R_{ON_Q1}	V_{IN} = 4.5V, I_{SYS} = 100mA		290		mΩ
Input quiescent current	I_{IN_Q}	V_{IN} = 5.5V, EN_HIZ = 0, CEB = 0, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		1.9		mA
		V_{IN} = 5.5V, EN_HIZ = 0, CEB = 1, charge disable		1.7		
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CEB = 0, I_{SYS} = 0A, charge done, V_{BATT} = 4.35V		43		µA
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, disable PCB_OTP function, not including the current from the external NTC resistor		6.5	7.5	
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB_OTP function, not including the current from the external NTC resistor		14.5	21	
		V_{IN} = GND, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB_OTP function, not including the current from the external NTC resistor, enable watchdog		22.5		
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, FET_DIS = 1, shipping mode			350	nA
Battery FET on resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100		mΩ
Battery FET discharge current limit	I_{DSCHG}	REG03h, bits[7:4] = 0001, I_{DSCHG} = 400mA	370	490	585	mA
		REG03h, bits[7:4] = 1001, I_{DSCHG} = 2000mA		2400(5)		
SYS reverse to BATT switch leakage		V_{SYS} = 4.65V, V_{IN} = 5V, V_{BATT} = GND, EN_HIZ = 1, CEB = 1, charge disable			100	nA
Ideal diode forward voltage in supplement mode	V_{FWD}	50mA discharge current		30		mV
Shipping Mode						
Enter shipping mode deglitch time	t_{SMEN_DGL}	REG06h, bit[5] is set from 0 to 1, REG09h, bits[7:6] = 00		1		s
Exit shipping mode by INT or V_{IN} plug-in	t_{SMEX_DGL}	INT is pulled low		2		s
Auto-Reset Mode						
Reset by INT	t_{RST_DGL}	REG01h, bits[7:6] = 00		8		s
		REG01h, bits[7:6] = 10		16		
Battery FET off lasting time	t_{RST_DUR}	REG01h, bit[5] = 0		2		s
		REG01h, bit[5] = 1		4		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery charge voltage regulation	V_{BATT_REG}	REG04h, bits[7:2] = 000000, V_{BATT_REG} = 3.6V	3.582	3.6	3.618	V
		REG04h, bits[7:2] = 101000, V_{BATT_REG} = 4.2V	4.179	4.2	4.221	
		REG04h, bits[7:2] = 110010, V_{BATT_REG} = 4.38V	4.358	4.38	4.4	
		REG04h, bits[7:2] = 111110, V_{BATT_REG} = 4.53V	4.522	4.53	4.568	
Fast charge current	I_{CC}	REG02h, bits[5:0] = 000000, I_{CC} = 8mA	6.9	8	8.5	mA
		REG02h, bits[5:0] = 001011, I_{CC} = 96mA	89	96	103	
		REG02h, bits[5:0] = 100000, I_{CC} = 264mA	251	264	285	
		REG02h, bits[5:0] = 111000, I_{CC} = 456mA	420	456	484	
Junction temperature regulation (5)	T_{J_REG}	Thermal_Limit = 120°C		120		°C
Pre-charge current	I_{PRE}	I_{PRE} = I_{TERM}	1		31	mA
Charge termination current threshold	I_{TERM}	REG03h, bits[3:0] = 0000, I_{TERM} = 1mA	0.8	0.93	1.05	mA
		REG03h, bits[3:0] = 0001, I_{TERM} = 3mA	2.7	3	3.3	
		REG03h, bits[3:0] = 0101, I_{TERM} = 11mA	10	11	12	
		REG03h, bits[3:0] = 0101, I_{TERM} = 31mA	28	31	34	
Termination deglitch time	t_{TERM_DGL}			3.2		s
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, REG04h, bit[1] = 1, V_{BATT_PRE} = 3.0V	2.9	3.0	3.1	V
Pre-charge to fast charge threshold hysteresis				90		mV
Battery auto-recharge voltage threshold	V_{RECH}	Below V_{BATT_REG}, REG04h, bit[0] = 0	60	100	140	mV
		Below V_{BATT_REG}, REG04h, bit[0] = 1	160	200	240	
Battery auto-recharge deglitch time	t_{RECH_DGL}			200		ms
Thermal Protection						
Thermal shutdown threshold (5)	T_{J_SHDN}			150		°C
Thermal shutdown hysteresis (5)				20		°C
NTC output current	I_{NTC}	CEB = 0, NTC = 3V	-1	0	1	µA
NTC cold temp rising threshold	V_{COLD}	As a percentage of V_{DD}	65	66	67	%
NTC cold temp rising threshold hysteresis				60		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{DD}	32.3	33.3	34.3	%
NTC hot temp falling threshold hysteresis				70		mV
NTC hot temp falling threshold for PCB_OTP	V_{HOT_PCB}	As a percentage of V_{DD}	30	32	35	%
NTC hot temp falling threshold hysteresis for PCB_OTP				90		mV
Logic I/O Pin Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I^{2}C Interface (SDA, SCL)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I^{2}C clock frequency	F_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock frequency	F_{CLK}			131		kHz
Watchdog timer	t_{WDT}	REG05h, bits[6:5] = 11		160		s

Note:

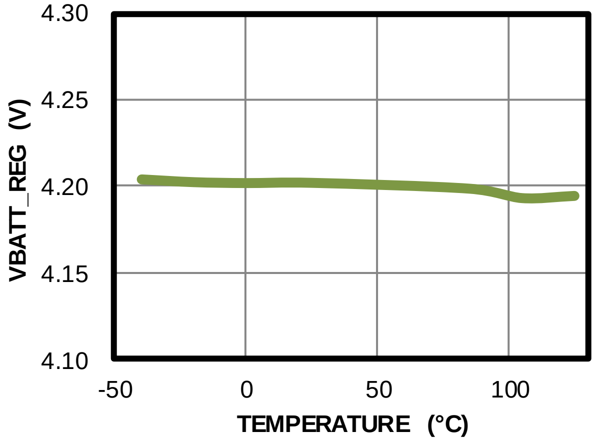
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 500mA, I_{CC} = 128mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

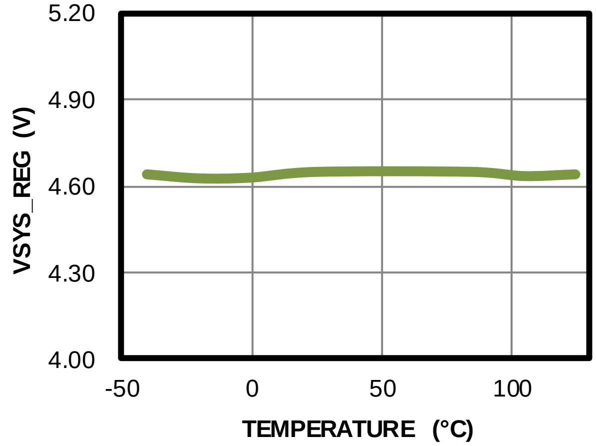
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.2V

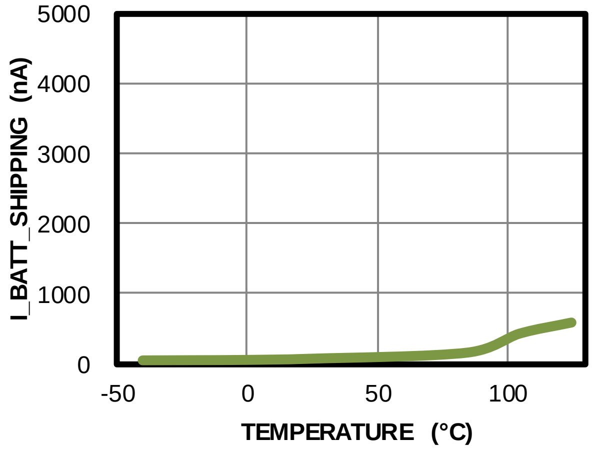


System Regulation Voltage vs. Temperature

V_{SYS_REG} = 4.65V

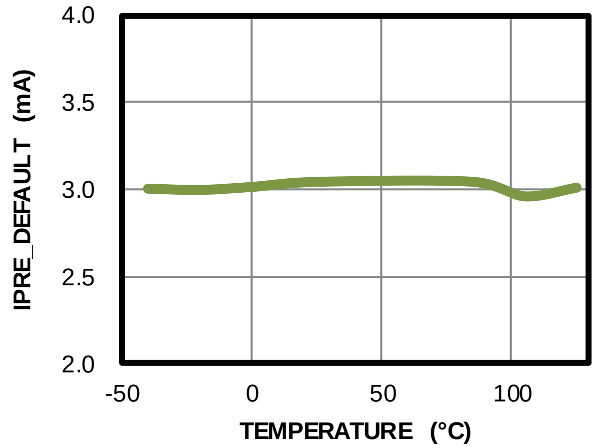


Battery Current under Shipping Mode vs. Temperature



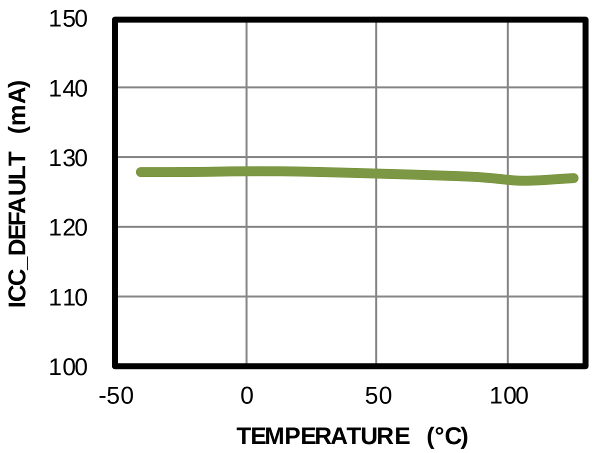
Pre-Charge Current vs. Temperature

I_{PRE} = 3mA



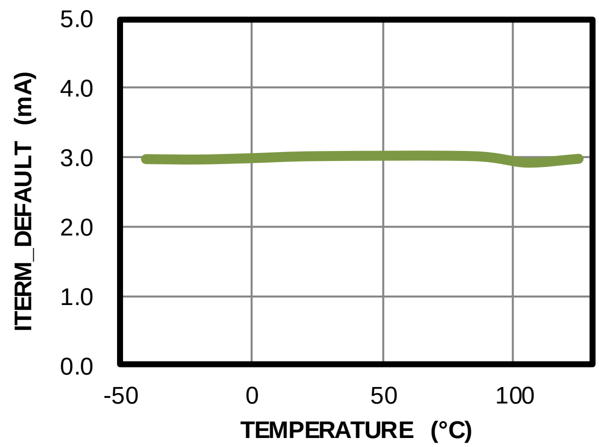
Fast Charge Current vs. Temperature

I_{CC} = 128mA



Battery Termination Current vs. Temperature

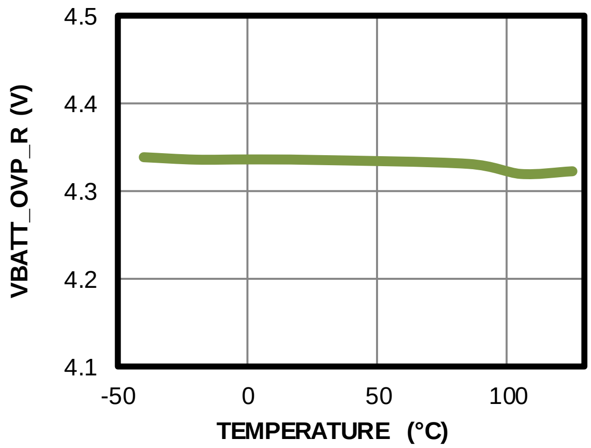
I_{TERM} = 3mA



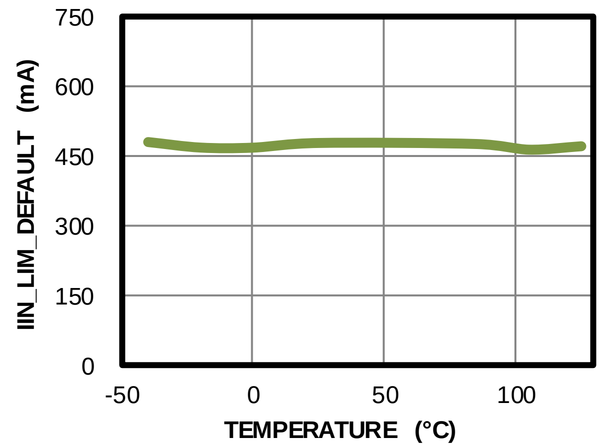
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 500mA, I_{CC} = 128mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

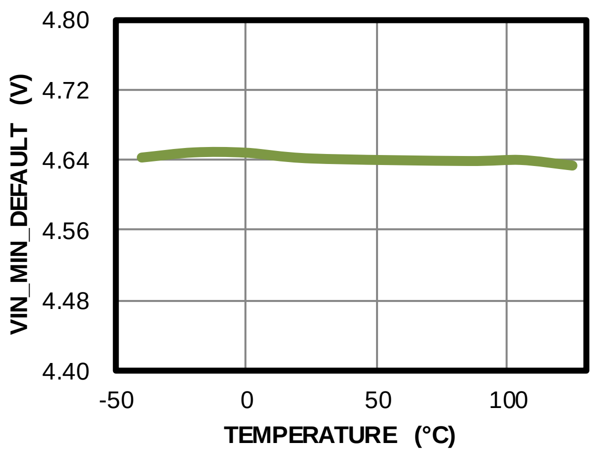
Battery OVP Voltage vs. Temperature
V_{BATT_REG} = 4.2V



Input Current Limit vs. Temperature
I_{IN_LIM} = 500mA



Input Minimum Voltage vs. Temperature
V_{IN_MIN} = 4.60V

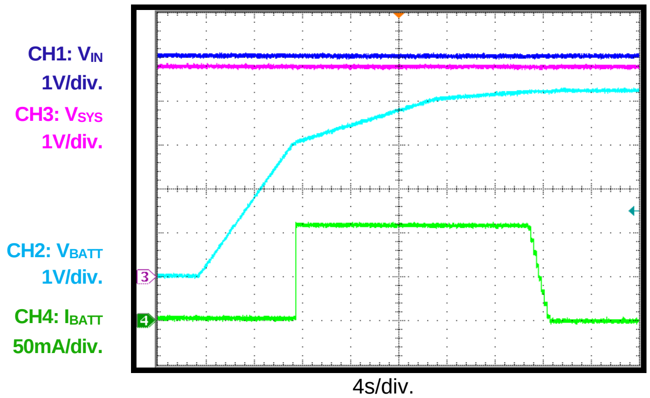


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 500mA, I_{CC} = 128mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

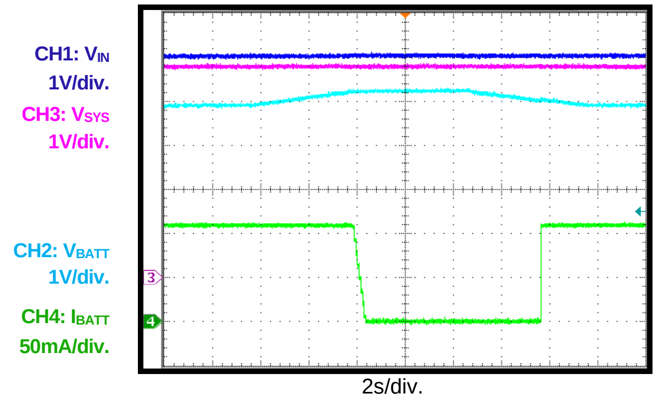
Battery Charge Curve

I_{SYS} = 0A



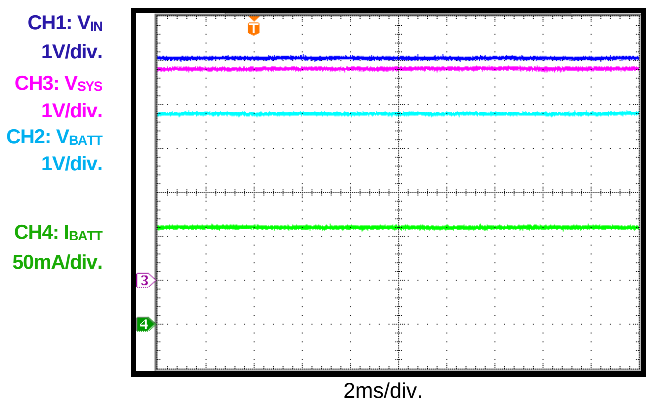
Auto-Recharge

I_{SYS} = 0A



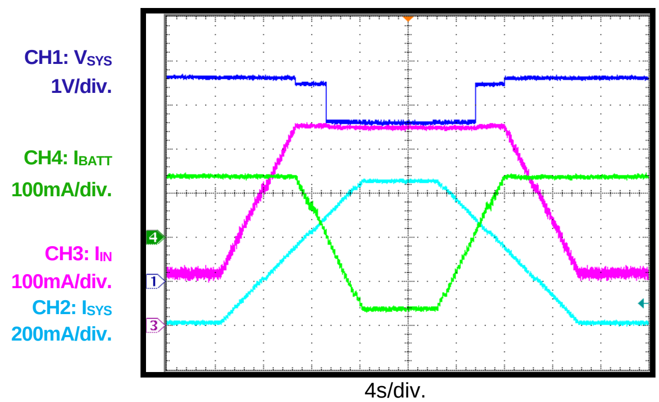
CC Charge Steady State

V_{BATT} = 3.7V, I_{SYS} = 0A



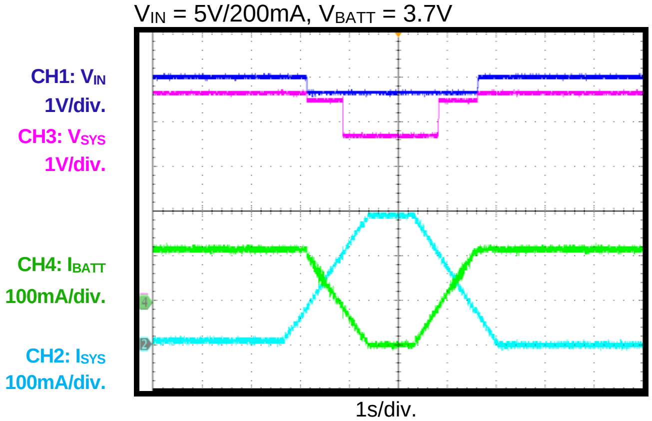
Input Current Limit-Based PPM

V_{BATT} = 3.7V



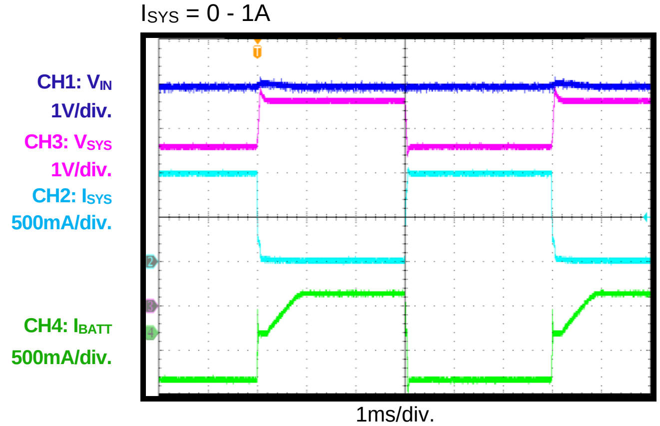
Input Voltage Regulation-Based PPM

V_{IN} = 5V/200mA, V_{BATT} = 3.7V



SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.7V, I_{CC} = 456mA,
I_{SYS} = 0 - 1A

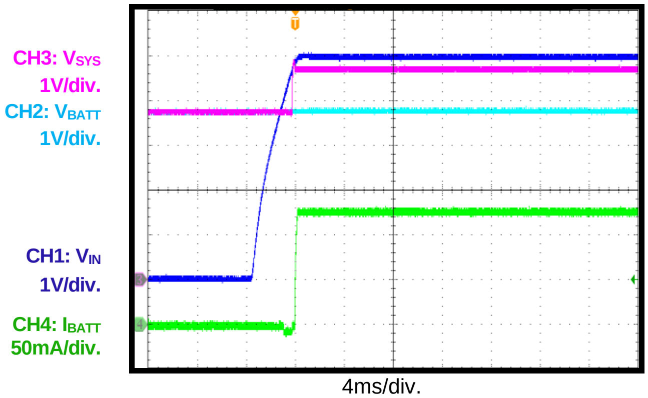


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 500mA, I_{CC} = 128mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

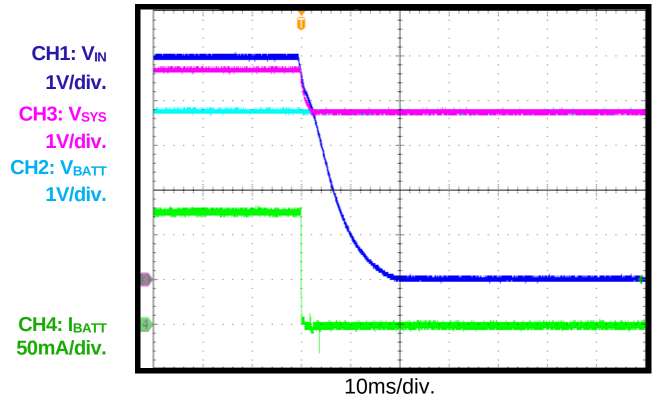
Power On

V_{BATT} = 3.7V, I_{SYS} = 0A



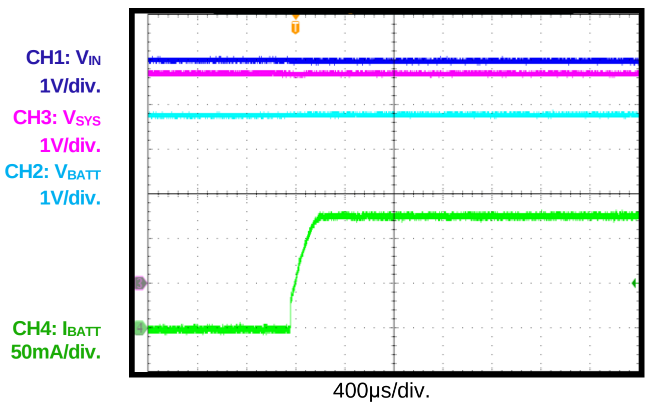
Power Off

V_{BATT} = 3.7V, I_{SYS} = 0A



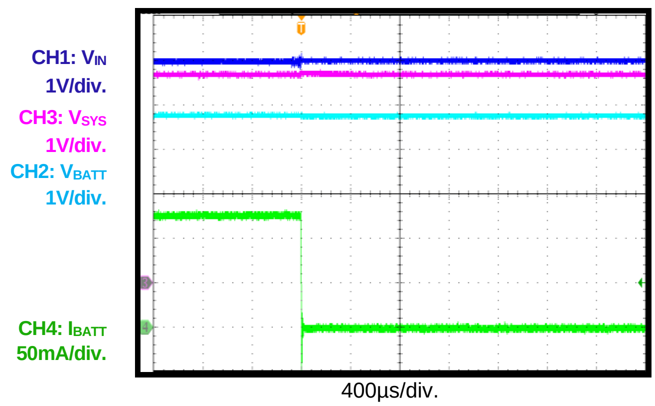
Charge Enable

V_{BATT} = 3.7V, I_{SYS} = 0A



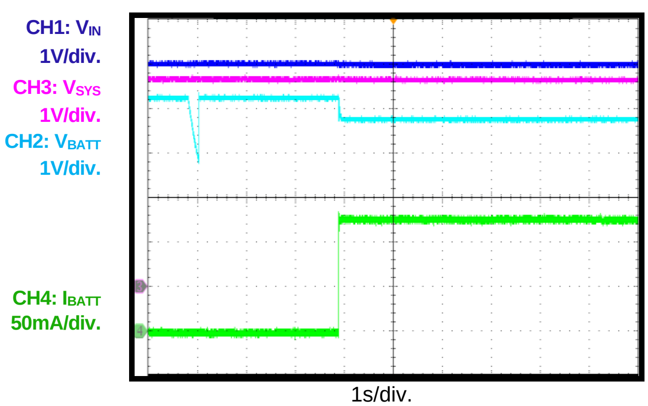
Charge Disable

V_{BATT} = 3.7V, I_{SYS} = 0A



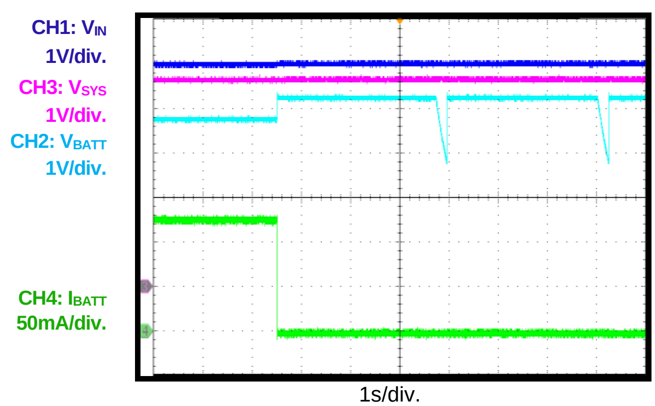
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A

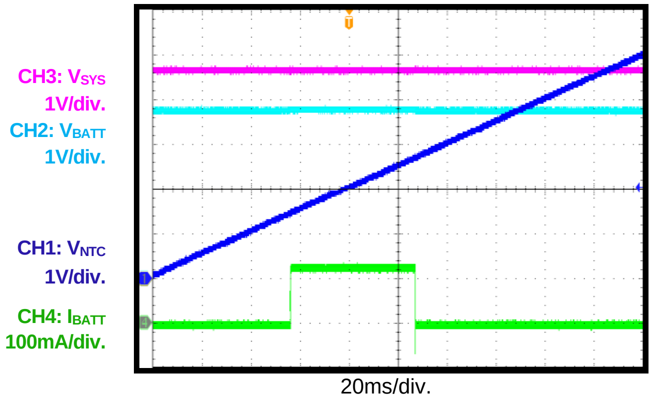


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 500mA, I_{CC} = 128mA, V_{IN_MIN} = 4.6V, unless otherwise noted.

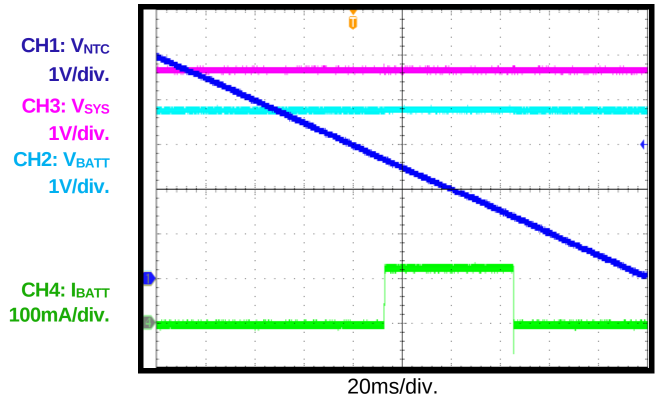
NTC Rising

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB_OTP disable



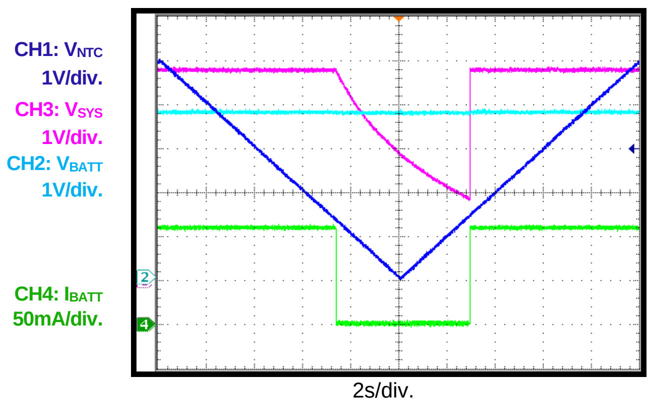
NTC Falling

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB_OTP disable



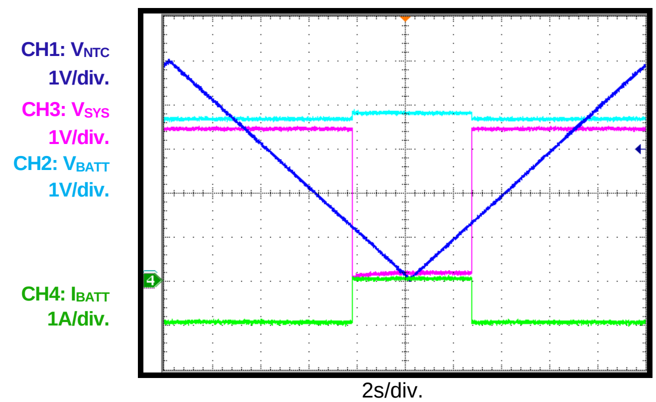
PCB_OTP @ Charge Mode

V_{BATT} = 3.7V, I_{SYS} = 0A



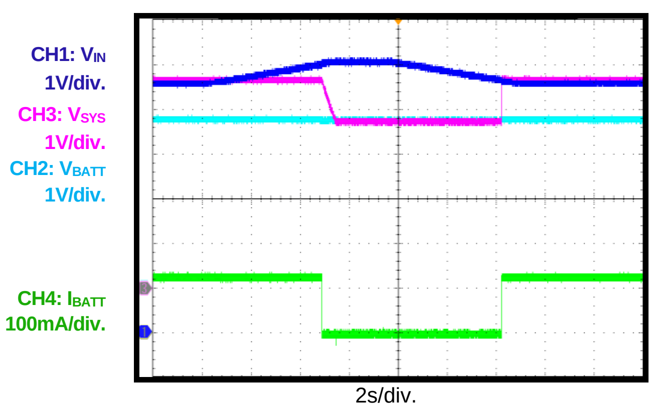
PCB_OTP @ Discharge Mode

V_{IN} = 0V, V_{BATT} = 3.7V, I_{SYS} = 1A



V_{IN} OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



FUNCTIONAL BLOCK DIAGRAM

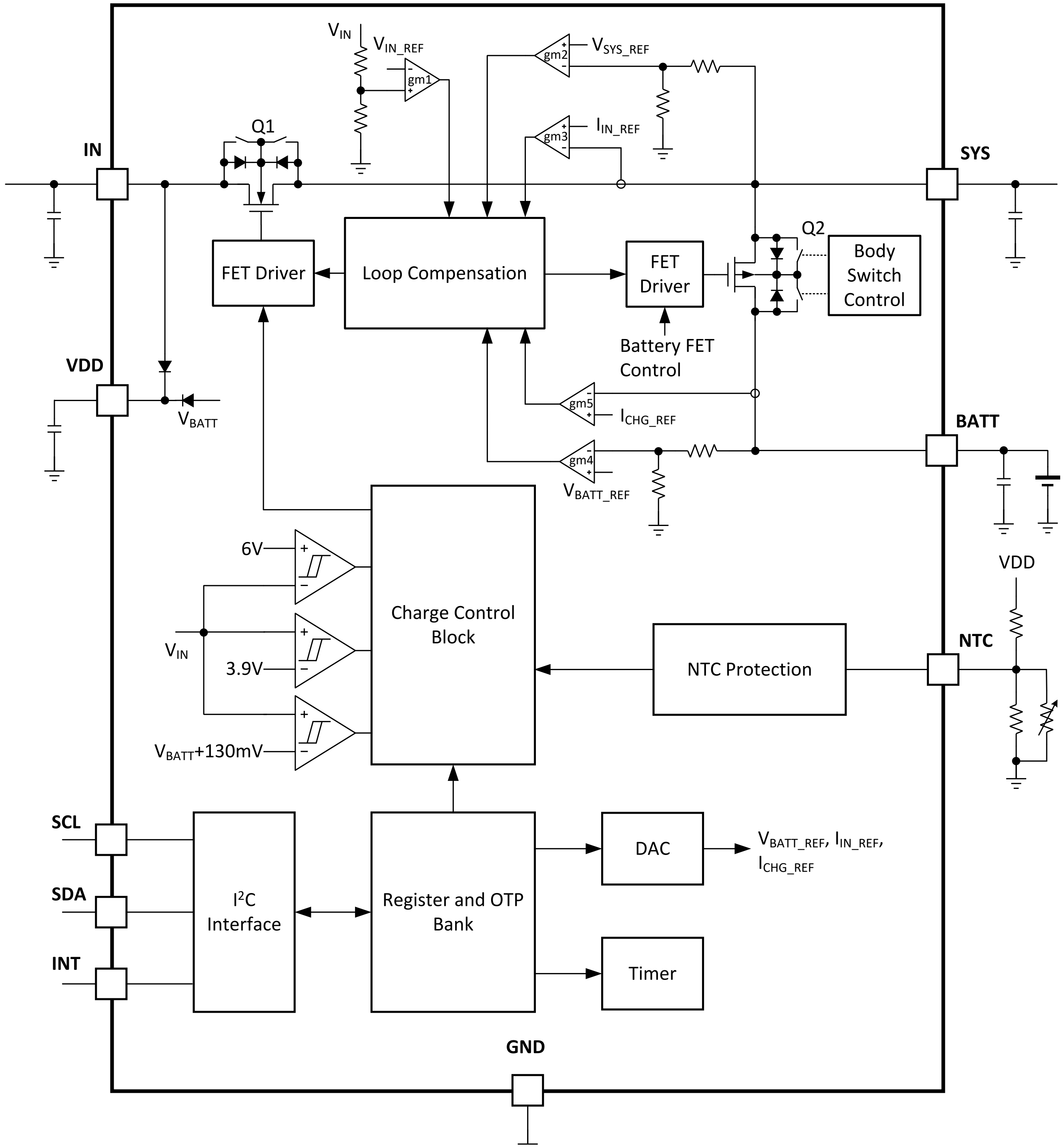


Figure 2: Functional Block Diagram

OPERATION

The MP2662 is an I^{2}C-controlled, single-cell, Li-ion or Li-polymer battery charger with a complete power path management function. The full-charge function includes constant-current pre-charge, constant-current fast charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority to the charge current. When the input power is limited due to an input current limit or input voltage limit, the IC reduces the charge current automatically until the battery supplements the system load.

The IC integrates a 290mΩ LDO FET between IN and SYS and a 100mΩ battery FET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery FET works as a fully featured linear charger with pre-charge, fast charge, constant voltage charge, charge termination, auto-recharge, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I^{2}C interface. The IC adjusts the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 100mΩ battery FET is turned on to connect the battery to the system load when the input power is not sufficient enough to power the system load. When the input is removed, the 100mΩ battery FET is also fully turned on to allow the battery to power up the system.

The system load is satisfied in priority, and the remaining current is used to charge the smart power path management battery. The MP2662 reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 3 shows the power path management structure for the MP2662.

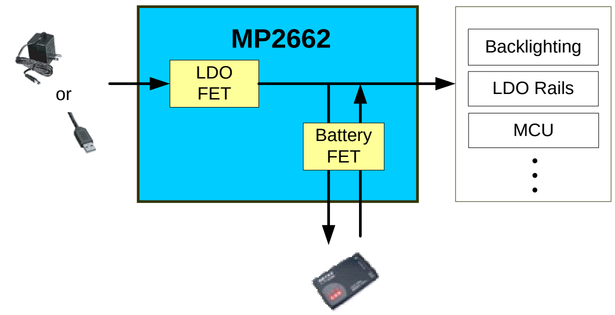


Figure 3: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of either IN or BATT. When IN or BATT rises above its respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and battery FET driver are all active. The I^{2}C interface is ready for communication, and all registers are reset to the default value. The host can access all of the registers.

Input OVP and UVLO

The MP2662 has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage is out of its normal range, the LDO FET (Q1) is turned off immediately.

When the input voltage is identified as a good source, a 200µs immunity timer becomes active. If the input power is normal until the 200µs expires, the system starts up. Otherwise, Q1 remains off (see Figure 4).

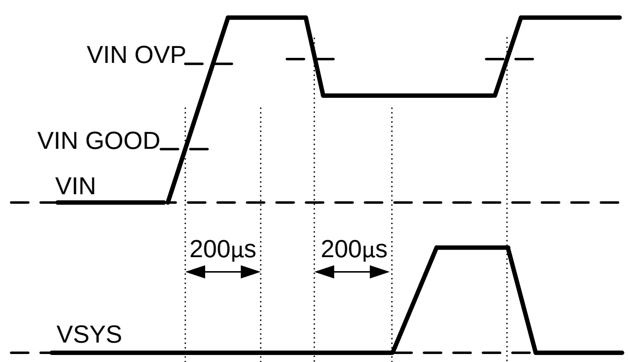


Figure 4: Input Power Detection Operation Profile

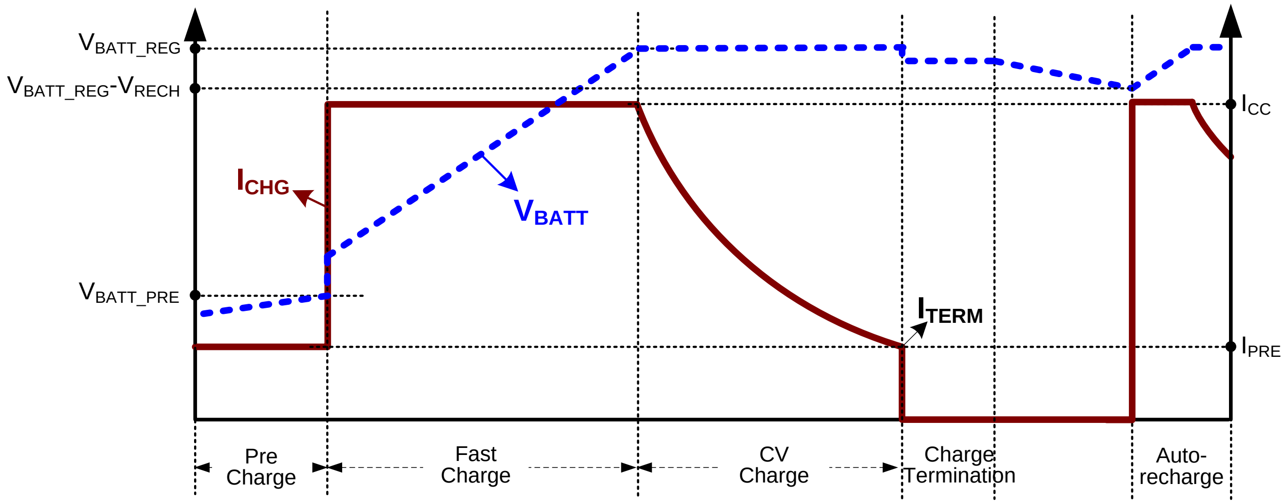


Figure 5: Battery Charge Profile

Power Path Management

The MP2662 employs a pass-through power path structure with the battery FET (Q2) to decouple the system from the battery. This allows for separate control between the system and the battery. The system is given the priority to start up, even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

The direct power structure consists of a front-end LDO FET between IN and SYS and a battery FET between SYS and BATT. The LDO FET and battery FET can be controlled by the I²C.

Table 1: FET Control via I²C

FET On/Off Changed by Control	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 1
LDO FET	OFF	x
Battery FET (charging)	x	OFF
Battery FET (discharging)	x	x

Note: x = Don't care.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO FET is fully on with the input current limit.

V_{SYS_REG} can be programmed through REG07h, bits[3:0].

Battery Charge Profile

The MP2662 provides three main charging phases: pre-charge, fast-current charge, and constant-voltage charge (see Figure 5).

1. Phase 1 (pre-charge): The MP2662 can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast-charge threshold (V_{BATT_PRE}). The pre-charge current is also programmed through REG03h, bits[3:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted.
2. Phase 2 (fast charge): When the battery voltage exceeds V_{BATT_PRE}, the MP2662 enters a fast-charge phase. The fast-charge current can be programmed via REG02h, bits[5:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the battery-full voltage (V_{BATT_REG}) set via REG04h, bits[7:2], the charge mode changes from CC mode to CV mode, and the charge current starts decreasing.

Assuming that the termination function EN_TERM is set via REG05h, bit[4] = 1, the charge cycle is considered to be completed when the charge current (I_{CHG}) reaches the termination current threshold (I_{TERM}) and a 3.2s delay timer is initiated. During this 3.2s delay period, I_{CHG} is always smaller than I_{TERM} + I_{TERM_HYS}.

The charge status is updated to charge done once the 3.2s delay timer expires.

The termination charge current threshold (I_{TERM}) can be programmed via REG03h, bits[3:0].

The charge current can also be terminated when the termination conditions are met if TERM_TMR set via REG05h, bit[0] = 0. Otherwise, the charge current continues to taper off.

If EN_TERM = 0, the termination function is disabled and all of the above actions are invalid (see Table 2).

Table 2: Termination Function Selection Table

EN_ TERM	TERM_ TMR	After I_{BATT} Reaches I_{TERM} in CV Mode	
		Operation	Charge Status
0	x	Keep CV charge	Charge
1	0	Charge done	Charge done
1	1	Keep CV charge	Charge

Note: x = Don't care.

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation.

A new charge cycle starts when any of the following conditions are valid:

- The input power is recycled.
- Battery charging is enabled via the I²C.
- Auto-recharge kicks in.

Under the following conditions:

- No thermistor fault at NTC.
- No safety timer fault.
- No battery over-voltage event.
- Battery FET is not forced off.

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold and V_{IN} is still in the operating range, the MP2662 begins another new charging cycle automatically without having to restart a charging cycle manually.

The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

Battery OVP

The MP2662 is designed with a built-in battery over-voltage limit (about 130mV higher than V_{BATT_REG}). When a battery over-voltage event occurs, the MP2662 suspends charging immediately and asserts a fault.

Input Current- and Input Voltage-Based Power Management

To meet the input source's (typically USB) maximum current limit specification, the MP2662 uses an input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I²C to prevent the input source from being over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage-based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q1 FET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to a minimum value of V_{SYS_REG} - 135mV and V_{IN} - 175mV, the charge current is reduced to prevent the system voltage from dropping further.

The voltage-based DPM regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity.

V_{IN_MIN} set via the I²C should be at least 250mV higher than V_{BATT_REG} to ensure the stable operation of the regulator. The input voltage limit function can be disabled by REG07h, bit[6].

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 37mV below the battery voltage, the MP2662 enters battery supplement mode, and the ideal diode mode is enabled. The battery FET is regulated to keep V_{BATT} - V_{SYS} at 30mV when I_{DSCHG} (supplement current) * R_{ON_BATT} is lower than 30mV. In the case that I_{DSCHG} * R_{ON_BATT} is higher than 30mV, the battery FET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BATT} + 20mV, the ideal diode mode is disabled. Figure 6 shows the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, the MP2662 operates in discharge mode, and the battery FET is always fully on to reduce loss.

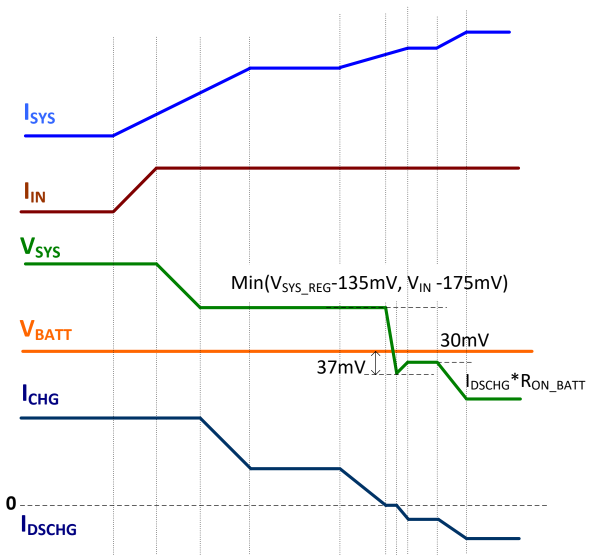


Figure 6: Dynamic Power Management and Battery Supplement Operation Profile

Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG} = 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to 50°C.

Thermal Regulation and Thermal Shutdown

The MP2662 monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of T_{J_REG} (120°C default), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via REG07h, bits[5:4].

When the junction temperature reaches 150°C, both Q1 and Q2 turn off.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the MP2662 to sense the battery temperature using the thermistor (usually available in the battery pack) to ensure a safe operating environment for the battery. Connect appropriately valued resistors from VDD to NTC to ground. The resistor divider works with a thermistor connected from NTC to ground. The NTC voltage is determined by the resistor divider whose divide ratio depends on the temperature. The M2662 sets a pre-determined upper and lower bound of the divide ratio for NTC cold and NTC hot internally.

In the MP2662, the I²C default setting is PCB_OTP. This function can be changed through the I²C (see Table 3).

Table 3: NTC Function Selection Table

I²C Control		Function
EN_NTC	EN_PCB_OTP	
0	x	Disable
1	1	NTC
1	0	PCB_OTP

Note: x = Don't care.

When PCB_OTP is selected and the NTC voltage is lower than the NTC hot threshold, both the LDO FET and battery FET are off. The PCB_OTP fault also sets the NTC_FAULT status (REG09h, bit[1]) to 1 to show the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function works only in charge mode. Once the NTC voltage falls out of this divide ratio, the temperature is outside of the safe operating range, and the MP2662 stops charging and report it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

Safety Timer

The MP2662 provides both a pre-charge and fast-charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when the battery voltage is lower than V_{BATT_PRE}. The fast-charge safety timer starts when the battery enters fast-charge mode. The fast-charge safety timer can be programmed through the I^2C. The safety timer can be disabled via the I^2C.

The following actions can restart the safety timer:

- A new charge cycle is initiated
- Charge enable toggling
- HIZ disable toggling

Host Mode and Default Mode

The MP2662 is a host-controlled device. After the power-on reset, the MP2662 starts up in a watchdog timer expiration state or default mode. All registers are in their default settings.

The watchdog timer works in both charge and discharge mode. When the watchdog timer out, most registers return to the default value (refer to the I^2C Register Map). When the watchdog timer is out in both charge and discharge mode, both the LDO FET and battery FET are turned off. They turn on again automatically after t_{RST_DUR}, which can be programmed by REG01h, bit[5].

To save quiescent current during discharge mode, the watchdog timer can be turned off during by setting REG05h, bit[7] to 0.

Any write to the MP2662 switches it to host mode. All charge parameters are programmable. If the watchdog timer (REG05h, bits[6:5]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG02h, bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the MP2662 goes back to default mode. The watchdog timer limit can also be programmed or disabled by the host control.

When the REG05h, bits[6:5] is set to 00, then the watchdog timer is disabled under both charge mode and discharge mode regardless of the status of REG05h, bit[7].

Operation can also be switched to default mode when one of the following conditions are valid:

- Refresh input without battery.
- Re-insert battery with no V_{IN}.
- Register REG02h, bit[7] is reset.

Battery Discharge Function

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the MP2662 is as low as 6.5µA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The MP2662 has an over-discharge current protection in discharge mode and supplement mode. Once I_{DSCHG} exceeds the programmable discharge current limit (2A default), the battery FET turns off after a 60µs delay. The MP2662 enters hiccup mode as part of the over-current protection (OCP). The discharge current limit can be programmed high to 3.2A through the I^2C. If the discharge current goes high and reaches the internal fixed current limit (about 3.7A), the battery FET turns off and begins hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (2.76V default), the battery FET turns off to prevent an over-discharge.

System Short-Circuit Protection (SCP)

The MP2662 features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, system SCP for both the IN to SYS path and the BATT to SYS path is active. I_{DSCHG} decreases to half of the original value.

For the IN to SYS path, once I_{IN} is over the protection threshold, both the LDO FET and battery FET are turned off immediately, and the MP2662 enters hiccup mode. Otherwise, the maximum current limit is not reached. When V_{SYS} is lower than 1.5V and the setting input current limit is reached, the hiccup mode also starts after a 60µs delay. The hiccup mode interval is 800µs.

For the BATT to SYS path, once I_{BATT} is over the 3.7A protection threshold, both the LDO FET and battery FET are turned off immediately, and the MP2662 enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60µs delay. The hiccup mode interval is 800µs.

For details, please refer to the flow chart shown in Figure 20.

Particularly, if a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths works. The faster one of the two dominates the hiccup operation.

Interrupt to Host (INT)

The MP2662 also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256µs low-state INT pulse. All of the below events can trigger an INT output:

- Good input source detected (PG_STAT)
- Charge completed
- Charging status change
- Faults in REG09h (watchdog timer fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When fault occurs, the MP2662 sends out an INT pulse and latches the fault state in REG09h. After the MP2662 exits the fault state, the fault bit is reset to 0 after the host reads REG09h. The NTC fault bit is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set in REG06h, bits[4:0]. When an INT condition is masked, this means that the INT pin signal (and register bit) will not trigger when the corresponding condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power to be reset during the application. The MP2662 provides both shipping mode (shown in Table 4) and system reset mode for different applications.

Table 4: Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT H to L for 2s	V_{IN} Plug-In
LDO FET	x	x	On
Battery FET (charging)	Off (t_{SMEN_DGL} later)	On	On (2s later)
Battery FET (discharging)	Off (t_{SMEN_DGL} later)	On	On (2s later)

Note: x = Don't care.

The IC has a register bit for battery disconnection control (FET_DIS). If this bit is set to 1, the MP2662 enters shipping mode after a delay time, which can be programmed by REG09h, bits[7:6]. The battery FET turns off, and the FET_DIS bit refreshes to 0 after the battery FET turns off. Pull the INT pin down or plug in the input adapter for 2s to wake the MP2662 up from shipping mode.

The MP2662 can also reuse an INT pin to cut off the path from the battery to the system under the condition needed to reset the system manually. Once the logic at INT is set low for longer than t_{RST_DGL} (which can be programmed by REG01h, bits[7:6]), the battery is disconnected from the system by turning off the battery FET. The off state lasts for t_{RST_DUR}, which can be programmed by REG01h, bit[5]. Then the battery FET is turned on automatically, and the system is powered by the battery again. During the off period, the INT pin is not limited to be high or low.

The MP2662 can reset the system by controlling the INT pin (see Figure 7).

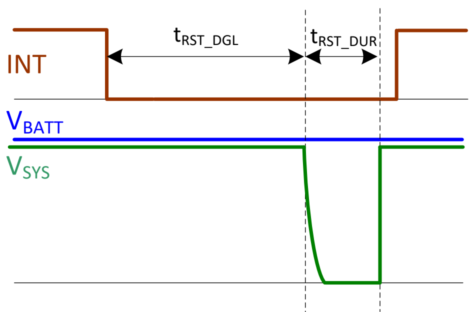


Figure 7: System Reset Function Operation Profile

SERIAL INTERFACE

The IC uses an I²C-compatible interface to set the charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbits/s) and fast mode (up to 400kbits/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. Start and stop conditions are always generated by the master. A start condition is defined as a high-to-low transition on the SDA line while SCL is high. A stop condition is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 8).

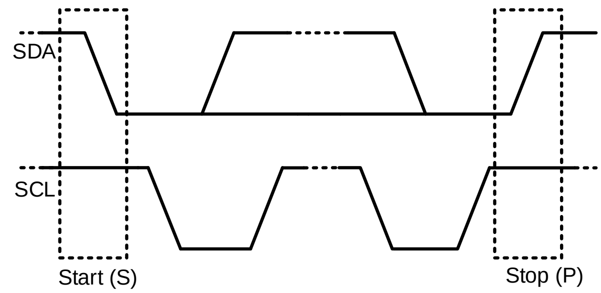


Figure 8: Start and Stop Conditions

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 9). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB).

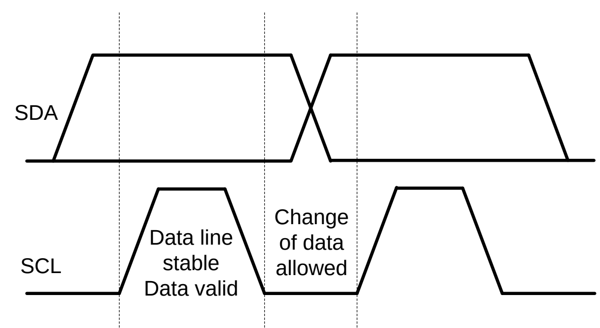


Figure 9: Bit Transfer on the I²C Bus

Each byte has to be followed by an Acknowledge (ACK) bit which is generated by the receiver, to signal the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the ninth clock, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start condition to start a new transfer.

After the start condition, a slave address is sent. This address is 7 bits long, followed by the eighth data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 10 shows the address bit arrangement.

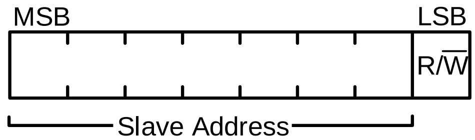


Figure 10: 7-Bit Address

Figures 11–15 show detailed signal sequences.

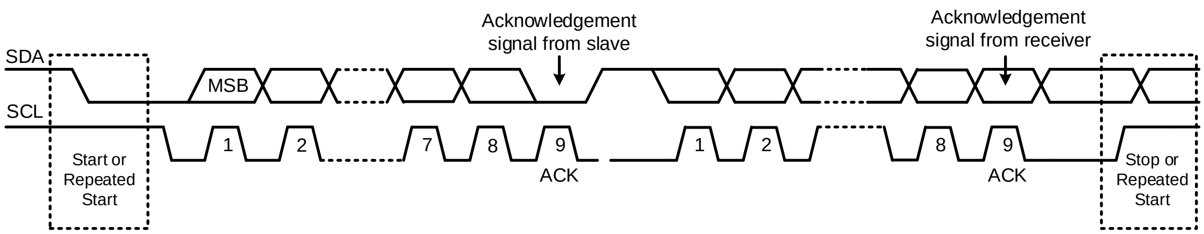


Figure 11: Data Transfer on the I²C Bus

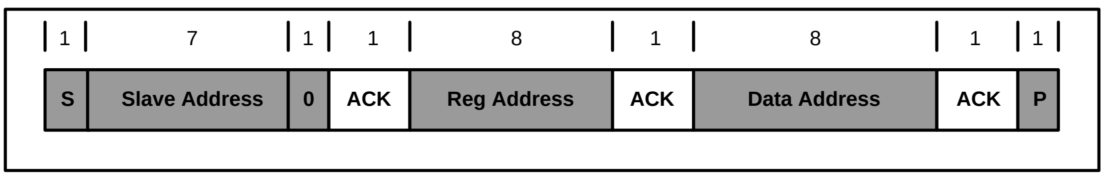


Figure 12: Single Write

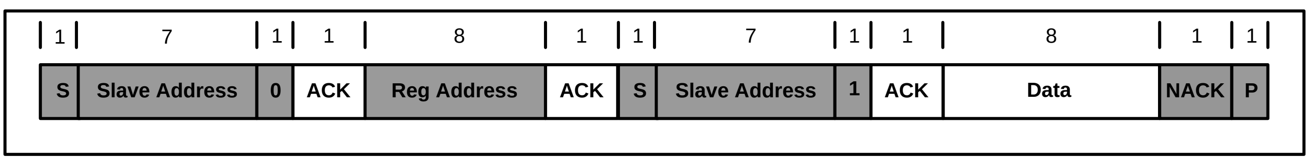


Figure 13: Single Read

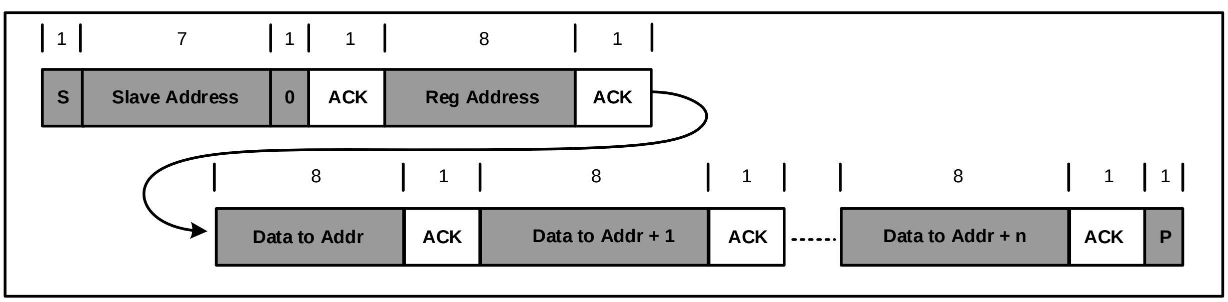


Figure 14: Multi-Write

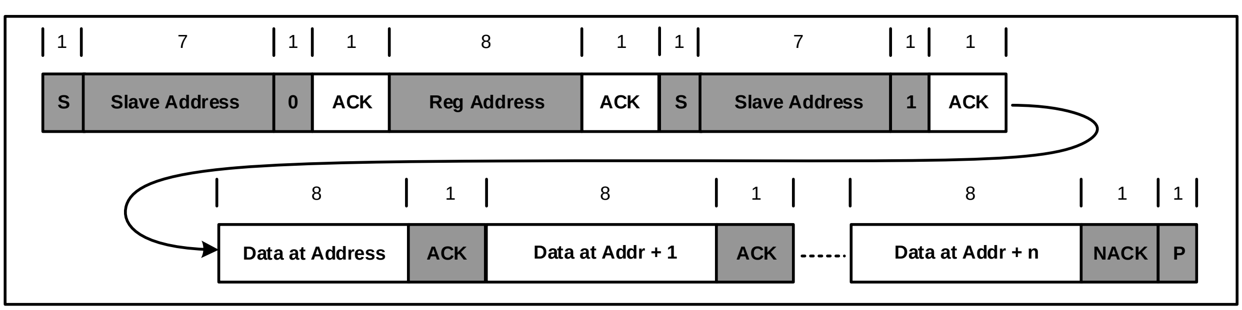


Figure 15: Multi-Read

I2C REGISTER MAP

IC Address: REG07h (reserved some trim options)

Register Name	Address	R/W	Description	Default
REG00h	0x00	r/w	Input source control register	1001 1111
REG01h	0x01	r/w	Power on configuration register	1010 1100
REG02h	0x02	r/w	Charge current control register	0000 1111
REG03h	0x03	r/w	Discharge/termination current	1001 0001
REG04h	0x04	r/w	Charge voltage control register	1010 0011
REG05h	0x05	r/w	Charge termination/timer control register	0011 1010
REG06h	0x06	r/w	Miscellaneous operation control register	1100 0000
REG07h	0x07	r/w	System voltage regulation register	0011 1001
REG08h	0x08	r	System status register	0100 0000
REG09h	0x09	r/w	Fault register	0000 0000
REG0Ah	0x0A	N/A	Address register	1110 0000

REG 00h (Default: 1001 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{IN_MIN} [3]	1	Y	N	r/w	640mV	Offset: 3.88V Range: 3.88V - 5.08V Default: 4.60V (1001)
6	V_{IN_MIN} [2]	0	Y	N	r/w	320mV	
5	V_{IN_MIN} [1]	0	Y	N	r/w	160mV	
4	V_{IN_MIN} [0]	1	Y	N	r/w	80mV	
3	I_{IN_LIM} [3]	1	Y	N	r/w	240mA	Offset: 50mA Range: 50mA - 500mA Default: 500mA (1111)
2	I_{IN_LIM} [2]	1	Y	N	r/w	120mA	
1	I_{IN_LIM} [1]	1	Y	N	r/w	60mA	
0	I_{IN_LIM} [0]	1	Y	N	r/w	30mA	

REG 01h (Default: 1010 1100)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{RST_DGL} [1]	1	Y	Y	r/w	00: 8s 01: 12s 10: 16s 11: 20s	Pull INT low to disconnect the battery. Default: 16s (10)
6	t_{RST_DGL} [0]	0	Y	Y	r/w		
5	t_{RST_DUR}	1	Y	Y	r/w	0: 2s 1: 4s	Battery FET is off for a period of time before auto-on Default: 4s (1)
4	EN_HIZ(6)	0	Y	Y	r/w	0: Disable 1: Enable	Default: Disable (0)
3	CEB	1	Y	Y	r/w	0: Charge enable 1: Charge disable	Charge configuration Default: Charge disable (1)
2	V_{BATT_UVLO} [2]	1	Y	Y	r/w	360mV	Battery UVLO threshold Offset: 2.4V Range: 2.4V - 3.03V Default: 2.76V (100)
1	V_{BATT_UVLO} [1]	0	Y	Y	r/w	180mV	
0	V_{BATT_UVLO} [0]	0	Y	Y	r/w	90mV	

Note:

7) This bit only controls the on and off function of the LDO FET.

REG 02h (Default: 0000 1111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Register Reset	0	Y	N	r/w	0: Keep current setting 1: Reset	Default: Keep current register setting (0)
6	I²C Watchdog Timer Reset	0	Y	Y	r/w	0: Normal 1: Reset	Default: Normal (0)
5	I_{CC} [5]	0	Y	Y	r/w	256mA	Fast charge current setting. Offset: 8mA Range: 8mA (000000) - 456mA (111000) Default: 128mA (001111)
4	I_{CC} [4]	0	Y	Y	r/w	128mA	
3	I_{CC} [3]	1	Y	Y	r/w	64mA	
2	I_{CC} [2]	1	Y	Y	r/w	32mA	
1	I_{CC} [1]	1	Y	Y	r/w	16mA	
0	I_{CC} [0]	1	Y	Y	r/w	8mA	

REG 03h (Default: 1001 0001)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{DSCHG} [3]	1	Y	Y	r/w	1600mA	BATT to SYS discharge current limit. Offset: 200mA Range: 400mA - 3.2A Valid range: 0001 - 1111 Default: 2000mA (1001)
6	I_{DSCHG} [2]	0	Y	Y	r/w	800mA	
5	I_{DSCHG} [1]	0	Y	Y	r/w	400mA	
4	I_{DSCHG} [0]	1	Y	Y	r/w	200mA	
3	I_{TERM} [3]	0	Y	Y	r/w	16mA	Termination current. Offset: 1mA Range: 1mA - 31mA Default: 3mA (0001)
2	I_{TERM} [2]	0	Y	Y	r/w	8mA	
1	I_{TERM} [1]	0	Y	Y	r/w	4mA	
0	I_{TERM} [0]	1	Y	Y	r/w	2mA	

REG 04h (DEFAULT: 1010 0011)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG} [5]	1	Y	Y	r/w	480mV	Battery regulation voltage. Offset: 3.60V Range: 3.60V - 4.545V Default: 4.2V (101000)
6	V_{BATT_REG} [4]	0	Y	Y	r/w	240mV	
5	V_{BATT_REG} [3]	1	Y	Y	r/w	120mV	
4	V_{BATT_REG} [2]	0	Y	Y	r/w	60mV	
3	V_{BATT_REG} [1]	0	Y	Y	r/w	30mV	
2	V_{BATT_REG} [0]	0	Y	Y	r/w	15mV	
1	V_{BATT_PRE}	1	Y	Y	r/w	0: 2.8V 1: 3.0V	Pre-charge to fast charge threshold. Default: 3.0V (1)
0	V_{RECH}	1	Y	Y	r/w	0: 100mV 1: 200mV	Battery recharge threshold (below V_{BATT_REG}). Default: 200mV (1)

REG 05h (Default: 0011 1010)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_WD_DISCHG	0	Y	N	r/w	0: Disable 1: Enable	Watchdog control in discharge mode. Default: Disable (0)
6	WATCHDOG [1]	0	Y	N	r/w	00: Disable timer 01: 40s 10: 80s 11: 160s	I^{2}C watchdog timer limit. Default: 40s (01) If Bit[6:5] = 00, then watchdog timer is disabled regardless of whether bit[7] is set or not.
5	WATCHDOG [0]	1	Y	N	r/w		
4	EN_TERM	1	Y	Y	r/w	0: Disable 1: Enable	Termination setting (controlling the termination is allowed or not). Default: Enable (1)
3	EN_TIMER	1	Y	Y	r/w	0: Disable 1: Enable	Safety timer setting. Default: Enable timer (1)
2	CHG_TMR [1]	0	Y	Y	r/w	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	Fast charge timer. Default: 5hrs (01)
1	CHG_TMR [0]	1	Y	Y	r/w		
0	TERM_TMR	0	Y	Y	r/w	0: Disable 1: Enable	Termination timer control (when TERM_TMR is enabled, the IC will not suspend the charge current after the charge termination). Default: (0)

REG 06h (Default: 1100 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_NTC	1	Y	Y	r/w	0: Disable 1: Enable	Default: Enable (1)
6	TMR2X_EN	1	Y	Y	r/w	0: Disable 2X extended safety timer during PPM 1: Enable 2X extended safety timer during PPM	Default: Enable (1)
5	FET_DIS [7]	0	Y	N	r/w	0: Enable 1: Turn off	Default: Enable (0)
4	PG_INT_Control	0	Y	Y	r/w	0: On 1: Off	Default: On (0)
3	EOC_INT_Control	0	Y	Y	r/w	0: On 1: Off	Charge completed INT mask control Default: On (0)
2	CHG STATUS_ INT_Control	0	Y	Y	r/w	0: On 1: Off	Charging status change INT mask control (charging status contain: not charging, pre charge and charge). Default: On (0)
1	NTC_INT_Control	0	Y	Y	r/w	0: On 1: Off	Default: On (0)
0	BATTOVP_INT_Control	0	Y	Y	r/w	0: On 1: Off	Default: On (0)

Note:

8) This bit only controls the turn off function of the battery FET, including charge and discharge.

REG 07h (Default: 0011 1001)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_PCB_OTP	0	Y	Y	r/w	0: Enable 1: Disable	PCB_OTP enable. Default: Enable (0)
6	EN_VINLOOP	0	Y	Y	r/w	0: Enable 1: Disable	Default: Enable (0)
5	T_{J_REG} [1]	1	Y	Y	r/w	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Thermal regulation threshold. Default: 120°C (11)
4	T_{J_REG} [0]	1	Y	Y	r/w		
3	V_{SYS_REG}(8) [3]	1	Y	N	r/w	400mV	System voltage regulation. Offset: 4.2V Range: 4.2V - 4.95V Default: 4.65V (1001)
2	V_{SYS_REG}(8) [2]	0	Y	N	r/w	200mV	
1	V_{SYS_REG}(8) [1]	0	Y	N	r/w	100mV	
0	V_{SYS_REG}(8) [0]	1	Y	N	r/w	50mV	

Note:

9) It is recommended that V_{SYS_REG} - V_{BATT_REG} > 200mv.

REG 08h (Default: 0100 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_FAULT	0	N/A	N/A	r	0: Normal 1: Watchdog timer expiration	Normal (0)
6	Rev [1]	1	N/A	N/A	r	00: reserved 01: reserved 10: MP2662 11: reserved	Revision number. Default: (10)
5	Rev [0]	0	N/A	N/A	r		
4	CHG_STAT [1]	0	N/A	N/A	r	00: Not charging 01: Pre charge 10: Charge 11: Charge done	Not charging (00)
3	CHG_STAT [0]	0	N/A	N/A	r		
2	PPM_STAT	0	N/A	N/A	r	0: No PPM 1: In PPM	No PPM (0)
1	PG_STAT	0	N/A	N/A	r	0: Power fail 1: Power good	Power fail (0)
0	THERM_STAT	0	N/A	N/A	r	0: No thermal regulation 1: In thermal regulation	No thermal regulation (0)

REG 09h (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_SHIPPING_DGL[1]	0	Y	N	r/w	00: 1s 01: 2s 10: 4s 11: 8s	Enter shipping mode deglitch time Default: 1s (00)
6	EN_SHIPPING_DGL[0]	0	Y	N	r/w		
5	VIN_FAULT	0	N/A	N/A	r	0: Normal 1: Input fault (OVP or bad source)	Normal (0)
4	THEM_SD	0	N/A	N/A	r	0: Normal 1: Thermal shutdown	Normal (0)
3	BAT_FAULT	0	N/A	N/A	r	0: Normal 1: Battery OVP	Normal (0)
2	STMR_FAULT	0	N/A	N/A	r	0: Normal 1: Safety timer expiration	Normal (0)
1	NTC_FAULT [1]	0	N/A	N/A	r	0: Normal 1: NTC hot	Normal (0)
0	NTC_FAULT [0]	0	N/A	N/A	r	0: Normal 1: NTC cold	Normal (0)

REG 0Ah (Default: 1110 0000) (9)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ADDR[2]	1	N/A	N/A	N/A	001: 01h 010: 02h 011: 03h 100: 04h 101: 05h 110: 06h 111: 07h	IC Address. Default: 111 (07h)
6	ADDR[1]	1	N/A	N/A	N/A		
5	ADDR[0]	1	N/A	N/A	N/A		
4	Reserved	0	N/A	N/A	N/A		
3	Reserved	0	N/A	N/A	N/A		
2	Reserved	0	N/A	N/A	N/A		
1	Reserved	0	N/A	N/A	N/A		
0	Reserved	0	N/A	N/A	N/A		

Note:

10) This register is for one-time programming only and is not accessible.

ONE-TIME PROGRAMMING MAP

<table>
<tr><th>#</th><th>Bit7</th><th>Bit6</th><th>Bit5</th><th>Bit4</th><th>Bit3</th><th>Bit2</th><th>Bit1</th><th>Bit0</th></tr>
<tr><td>0x01</td><td colspan="4">N/A</td><td>CEB</td><td colspan="3">N/A</td></tr>
<tr><td>0x02</td><td colspan="2">N/A</td><td colspan="6">I_{CC}: 8mA - 456mA / 8mA step</td></tr>
<tr><td>0x03</td><td colspan="4">N/A</td><td colspan="4">I_{TERM}: 1mA - 31mA/2mA step</td></tr>
<tr><td>0x04</td><td colspan="6">V_{BATT_REG}: 3.6V - 4.545V / 15mV step</td><td colspan="2">N/A</td></tr>
<tr><td>0x05</td><td>N/A</td><td colspan="2">WATCHDOG</td><td colspan="5">N/A</td></tr>
<tr><td>0x07</td><td>N/A</td><td>EN_VINLOOP</td><td colspan="6">N/A</td></tr>
<tr><td>0x0A</td><td colspan="3">Address</td><td colspan="5">N/A</td></tr>
</table>

ONE-TIME PROGRAMMING DEFAULT

One-Time Programmable Items	Default
CEB	Charge disable
I_{CC}	128mA
I_{TERM}	3mA
V_{BATT_REG}	4.2V
WATCHDOG	40s
EN_VINLOOP	Enable
Address	07h

STATE CONVERSION CHART

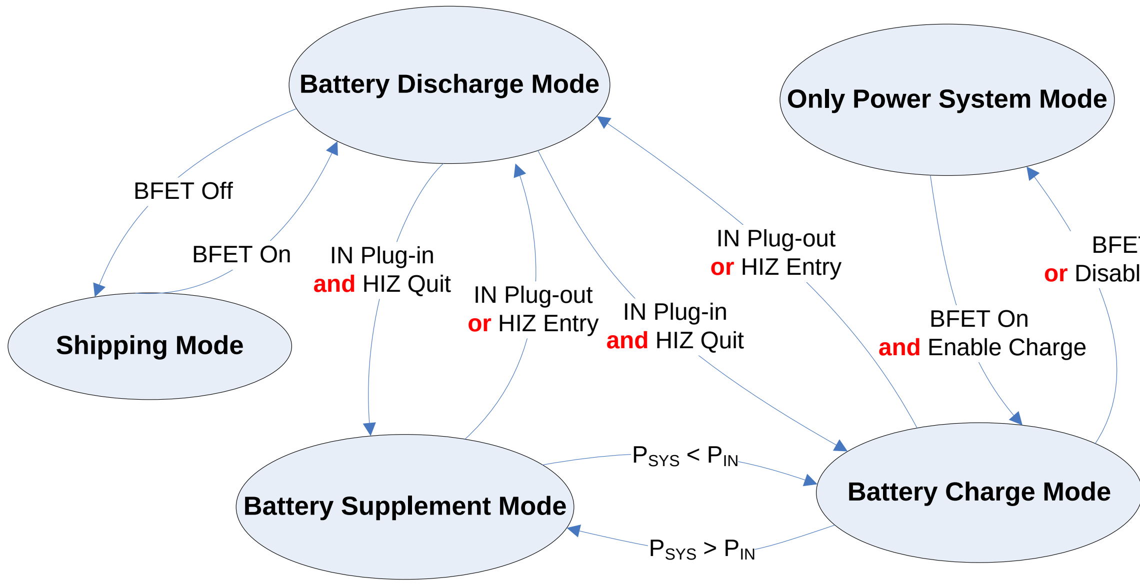


Figure 16: State Machine Conversion

CONTROL FLOWCHART

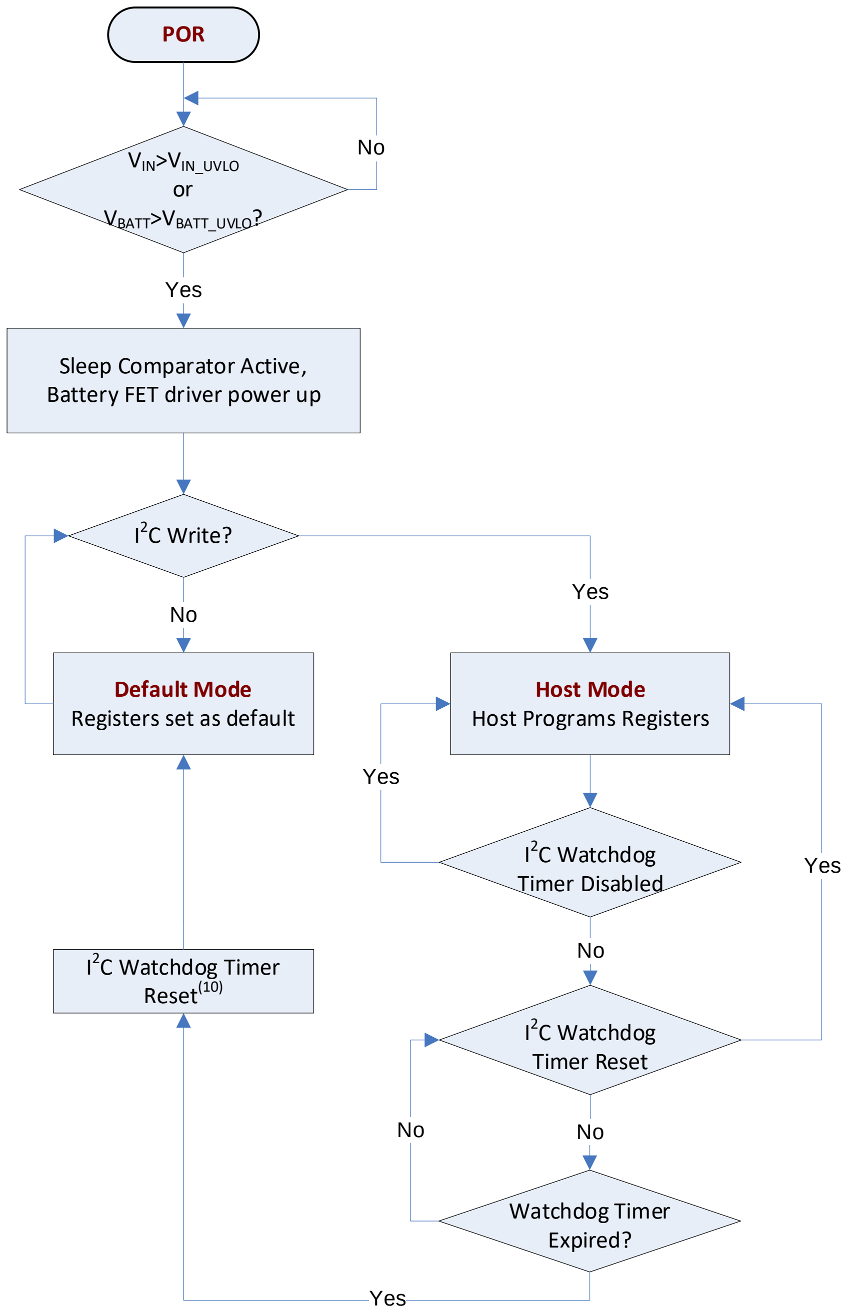


Figure 17: Default Mode and Host Mode Selection

Note:

11) Once the watchdog timer expires, the I²C watchdog timer must be reset or will not be valid in the next cycle.

CONTROL FLOWCHART *(continued)*

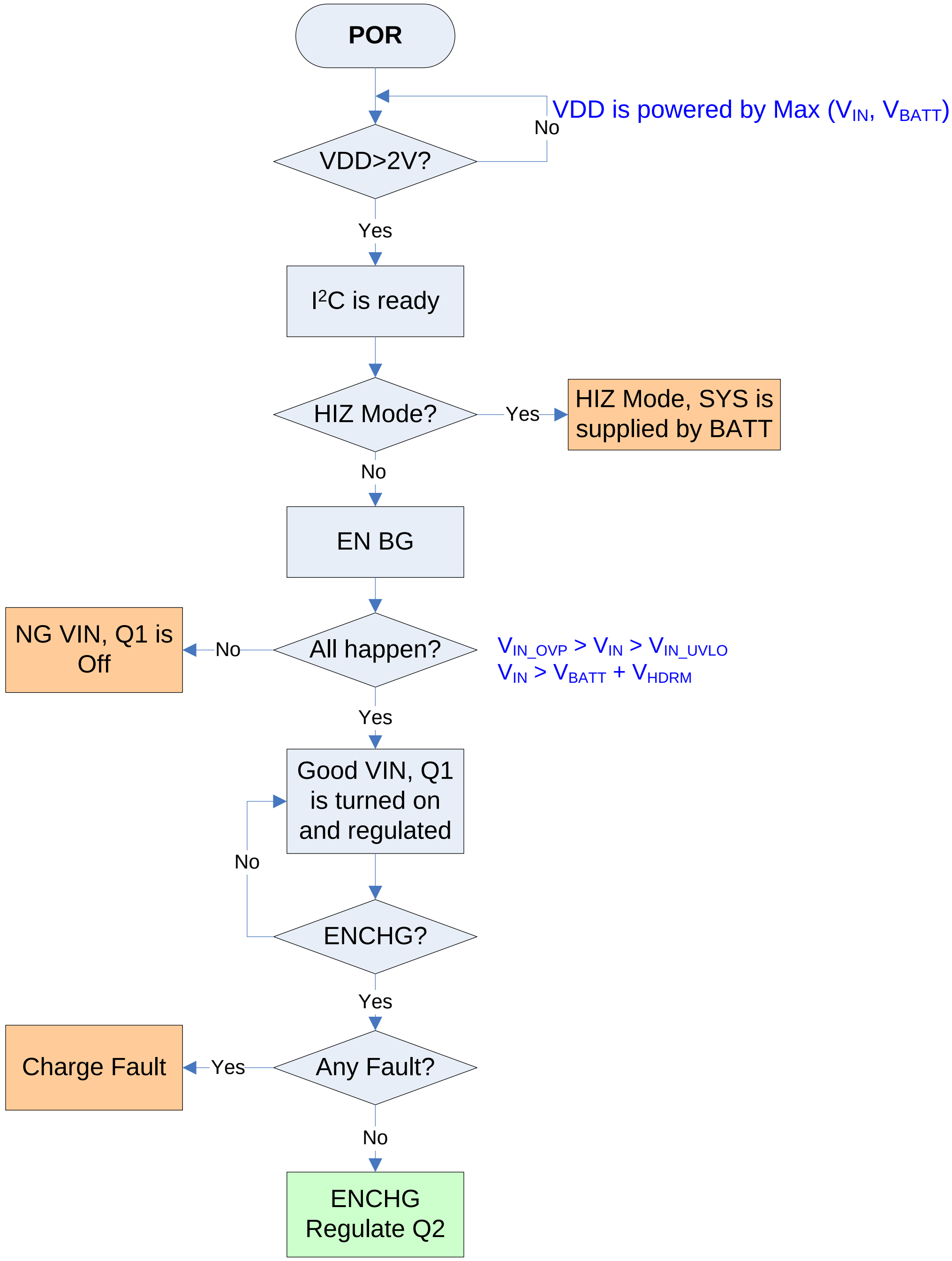


Figure 18: Input Power Start-Up Flow Chart

CONTROL FLOWCHART *(continued)*

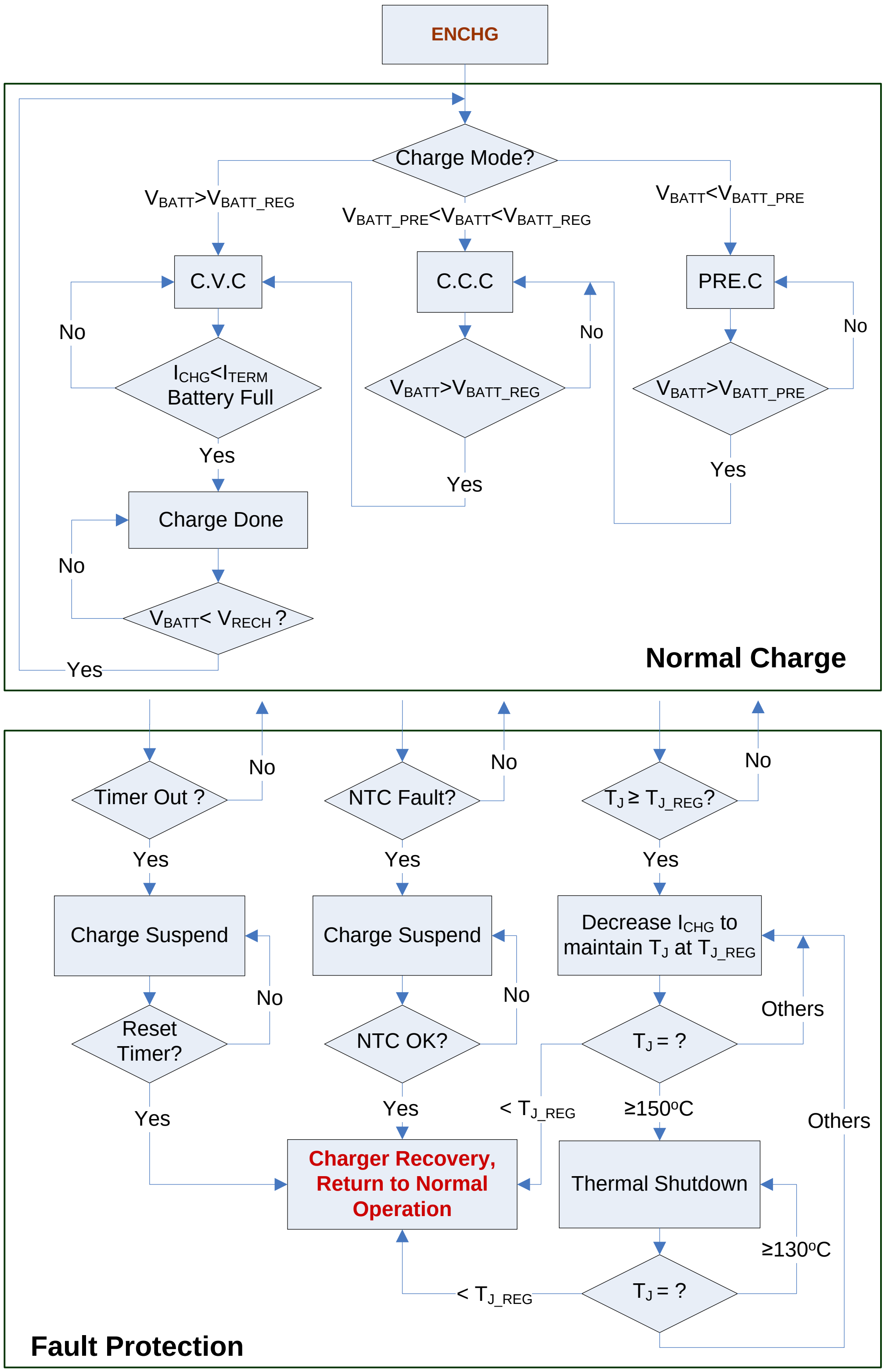


Figure 19: Charging Process

CONTROL FLOWCHART *(continued)*

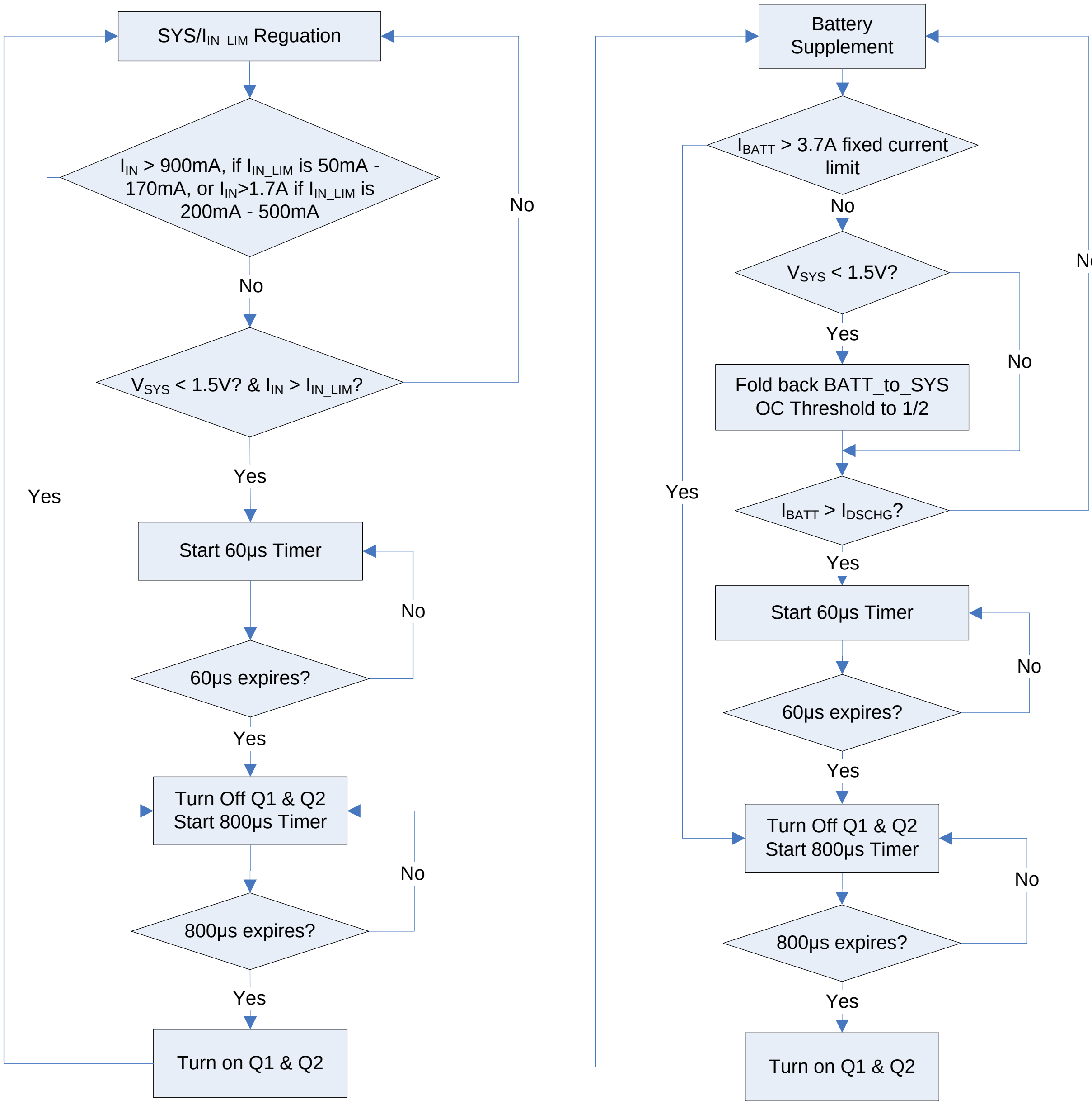


Figure 20: System Short-Circuit Protection

APPLICATION INFORMATION

Selecting a Resistor Divider for the NTC Sensor

The NTC pin uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be programmed independently (see Figure 21). The IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors.

For a given NTC thermistor, the R_{T1} and R_{T2} values depend on the type of NTC resistor used and can be calculated with Equation (1) and Equation (2):

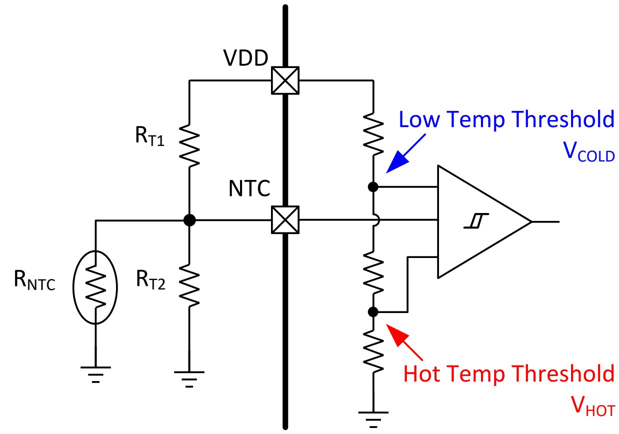


Figure 21: NTC Function Block

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at the high temperature of the required operating temperature range, and R_{NTCL} is the value of the NTC resistor at a low temperature.

For example, for a NCP18XH103 thermistor, R_{NTCL} is 27.219kΩ at 0°C, and R_{NTCH} is 4.161kΩ at 50°C. Using Equation (1) and Equation (2), calculate R_{T1} = 7.33kΩ and R_{T2} = 27.22kΩ, assuming that the NTC window is between 0°C and 50°C and using the V_{COLD} and V_{HOT} values from the EC table.

Selecting the External Capacitor

Like most low dropout regulators, the MP2662 requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimal board space and few components, so these capacitors must be selected correctly for optimal performance.

An input capacitor is required for stability. Connect a at least 4.7µF ceramic capacitor (dielectric types X5R or X7R) between IN to GND for stable operation over the full load current range.

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric types X5R or X7R) at least 10µF is suitable for the application circuit. For the MP2662, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A capacitor from BATT to GND is required. A at least 4.7µF ceramic capacitor (dielectric types X5R or X7R) is suitable for the MP2662 application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND very close to the IC.
3. Keep GND for the I^{2}C wire clean.
4. Place the I^{2}C wire in parallel.

TYPICAL APPLICATION CIRCUIT

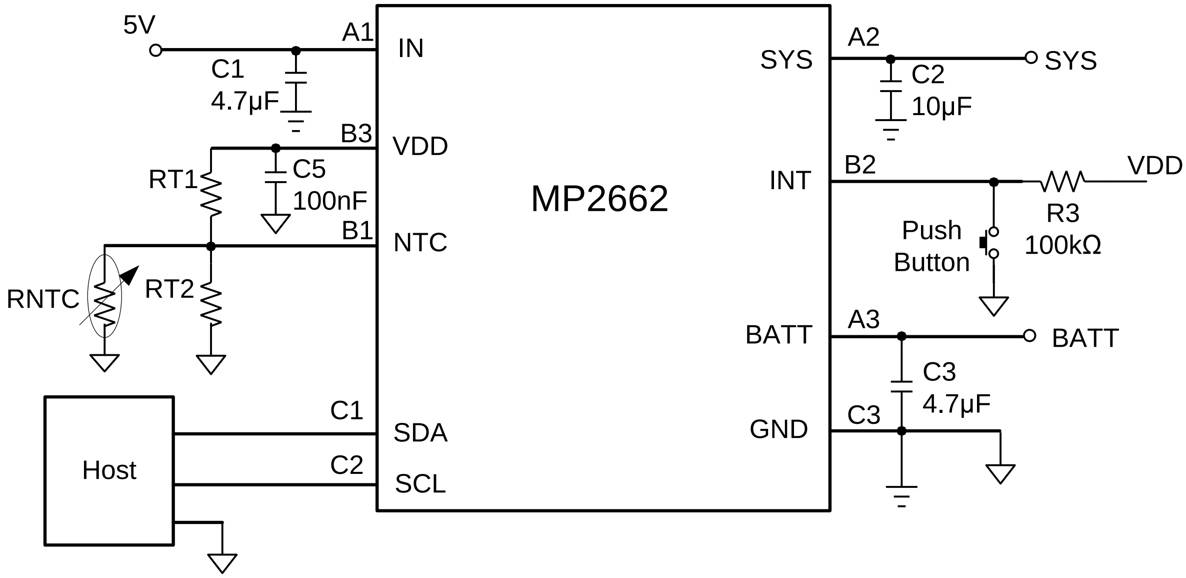


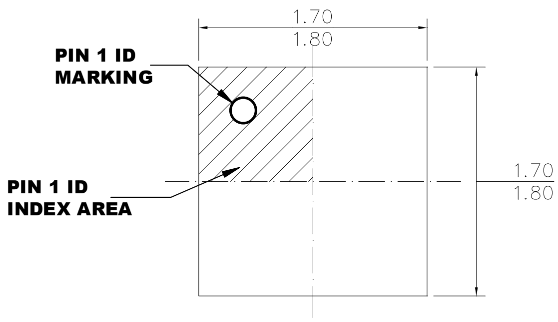
Figure 22: MP2662 Typical Application Circuit with 5V Input

Table 5: Key BOM of Figure 22

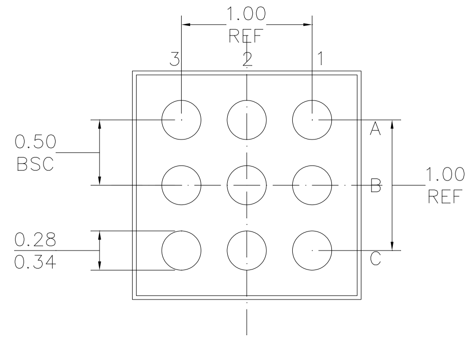
Qty	Ref	Value	Description	Package	Manufacture
1	C1	4.7µF	Ceramic Capacitor, 25V, X5R or X7R	0603	Any
1	C3	4.7µF	Ceramic Capacitor, 16V, X5R or X7R	0603	Any
1	C2	10µF	Ceramic Capacitor, 16V, X5R or X7R	0603	Any
1	C5	100nF	Ceramic Capacitor, 16V, X5R or X7R	0603	Any

PACKAGE INFORMATION

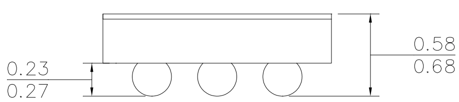
WLCSP-9 (1.75mmx1.75mm)



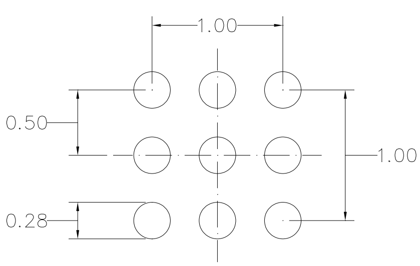
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/31/2019	Initial Release	-
1.01	4/04/2019	Updated NTC pull up/low resistor value in Application section	
		Added SERIES INTERFACE section to describes I2C	
		Changing the VDD cap from 1uF to 100nF in the sections that mentioned VDD cap	
1.02	5/18/2020	Changed “EV2662-C-00A” to EV2662-C-01A	3
		Updated the reset safety timer actions	20
		Removed “UVLO or input over-voltage protection” from the INT section	21
		Added CEB to the OTP map	32
1.1	5/20/2021	Added “Safety-Related Certification” to Features section	1
		Updated pin description	5
		Updated EVKT content: Change “USB dongle” to “communication interface”	3
		Updated I²C interface description	23–24
		Updated register format	7–32
		Improved the description of OPERATION	17–24
1.11	3/17/2023	Added note 9	30
		Updated note numbers	31, 34
		Updated notice in footnote	42
1.2	5/20/2024	Updated formatting in Features section; corrected typo and formatting in Applications section	1
		Updated the NTC cold temp falling threshold from 63/65/67 to 65/66/67	9
		Updated the NTC hot temp falling threshold from 31/33/35 to 32.3/33.3/34.3	10