



THE DATASHEET OF MMA2725W



Xtrinsic MMA27XXW/17XXW DSI3 Inertial Sensor

MMA27XXW/17XXW family, a SafeAssure solution, includes the DSI3 compatible overdamped X-axis or Z-axis satellite accelerometers.

Features

- ± 25 g, ± 125 g, ± 187 g, ± 250 g, ± 375 g, X-axis nominal full-scale range
- ± 250 g, Z-axis nominal full-scale range
- DSI3 compatible
 - Discovery Mode for physical location identification
 - High-side bus switch output driver
 - Command and Response Mode support for device configuration
 - Periodic Data Collection Mode support for acceleration data transfers
 - Background Diagnostic Mode support during Periodic Data Collection Mode
- -40°C to 125°C operating temperature range
- 16 μs internal sample rate, with interpolation to 1 μs
- Six selectable low-pass filter options from 180 Hz to 1200 Hz
- Single-pole, IIR high-pass filter with fast startup and optional output rate limiting
- Pb-Free, 16-pin QFN, 6 x 6 package

Referenced Documents

- DSI3 Standard Revision 1.0, Dated February 16, 2011
- AEC-Q100, Revision G, dated May 14, 2007

ORDERING INFORMATION

| Part Number | Axis | Range | Package | Shipping |
|-------------|------|-------------|---------|-------------|
| MMA2702W | X | ± 25 g | 2086-01 | Rail |
| MMA2712W | X | ± 125 g | 2086-01 | Rail |
| MMA2718W | X | ± 187 g | 2086-01 | Rail |
| MMA2725W | X | ± 250 g | 2086-01 | Rail |
| MMA2737W | X | ± 375 g | 2086-01 | Rail |
| MMA1725W | Z | ± 250 g | 2086-01 | Rail |
| MMA2702WR2 | X | ± 25 g | 2086-01 | Tape & Reel |
| MMA2712WR2 | X | ± 125 g | 2086-01 | Tape & Reel |
| MMA2718WR2 | X | ± 187 g | 2086-01 | Tape & Reel |
| MMA2725WR2 | X | ± 250 g | 2086-01 | Tape & Reel |
| MMA2737WR2 | X | ± 375 g | 2086-01 | Tape & Reel |
| MMA1725WR2 | Z | ± 250 g | 2086-01 | Tape & Reel |

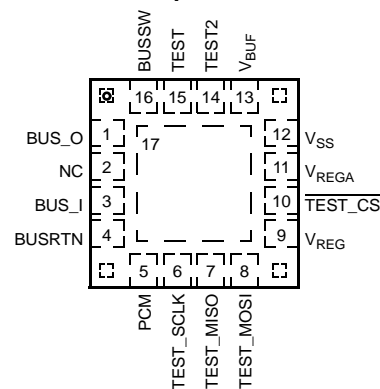
MMA27XXW
MMA17XXW

Bottom View



16-PIN QFN
6 MM X 6 MM X 2 MM
CASE 2086-01

Top View



Pin Connections

This document contains information on a new product. Specifications and information herein are subject to change without notice. Freescale reserves the right to change the detail

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Related Documentation

The MMA27XXW and MMA17XXW devices features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

- Go to the Freescale homepage at:
<http://www.freescale.com/>
- In the Keyword search box at the top of the page, enter the device number MMA27XXW or MMA17XXW.
- In the Refine Your Result pane on the left, click on the Documentation link.

MMA27XXW

1 Block Diagram, Pin Descriptions, Application Diagram, and Device Orientation

1.1 Block diagram

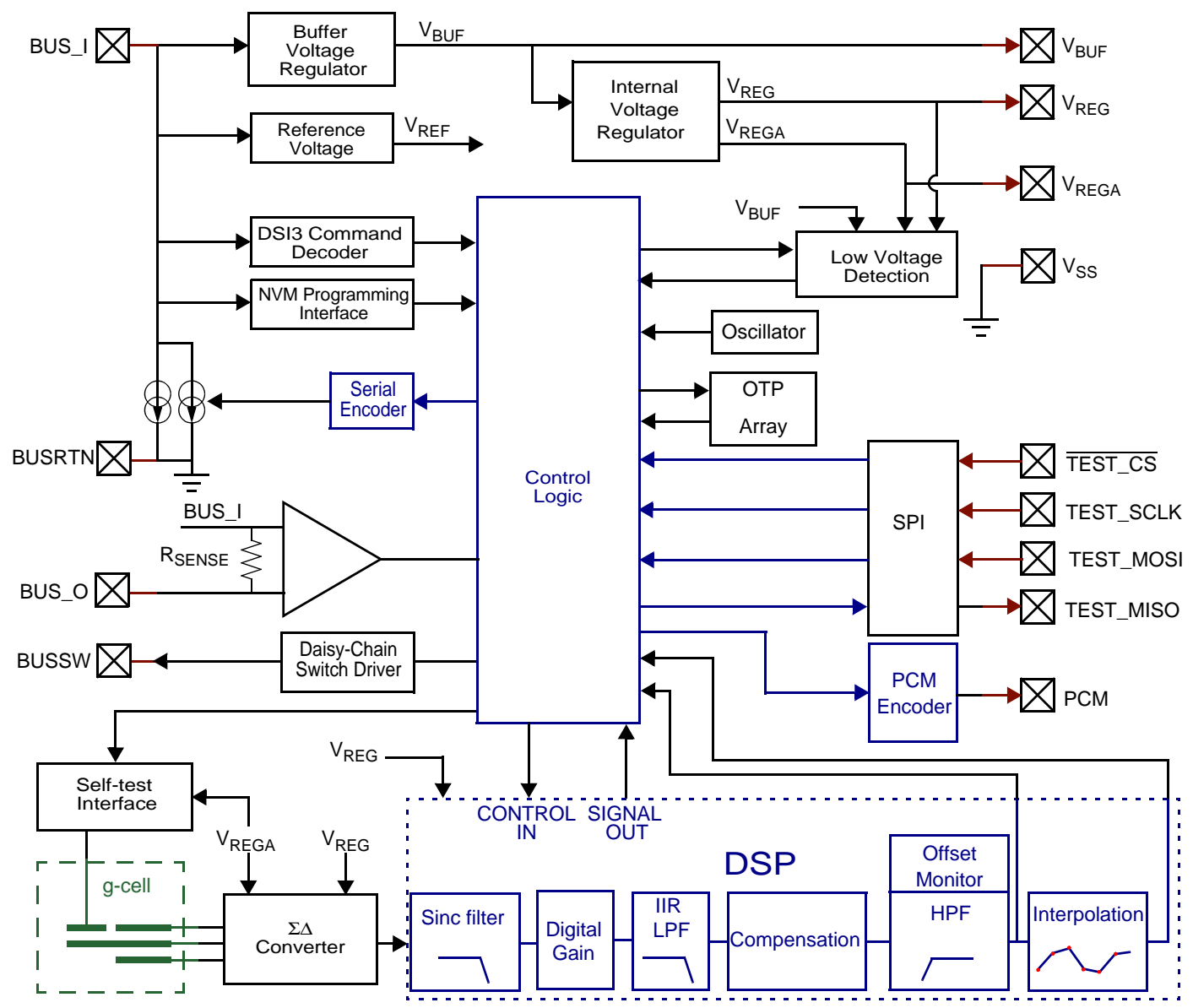


Figure 1. Internal block diagram

1.2 Pin descriptions

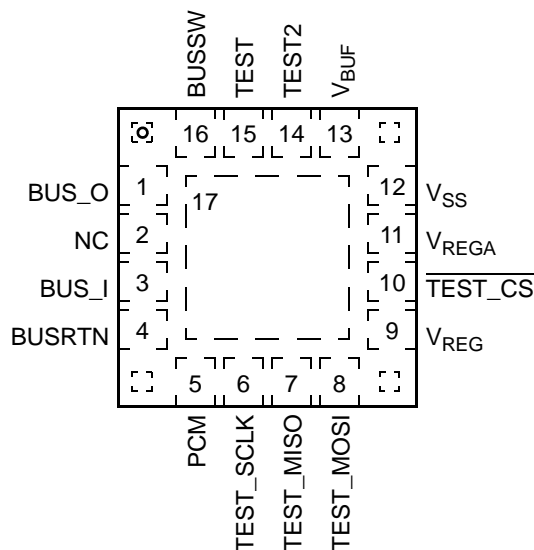


Figure 2. Pin connections

Table 1. Pin descriptions

| Pin | Pin name | Formal name | Definition |
|-----|-----------------------|-----------------------------|--|
| 1 | BUS_O | Supply out | This pin is connected to the BUS_I pin through an internal sense resistor and provides the supply connection to the next slave in a daisy-chain configuration. An external capacitor must be connected between this pin and V_{SS} . Reference Figure 3 . |
| 2 | NC | Not connected | This pin is not internally connected and must be left unconnected or tied to V_{SS} in the application. |
| 3 | BUS_I | Supply and communication | This pin is connected to the DSI supply line and supplies power to the device. An external capacitor must be connected between this pin and BUSRTN. Reference Figure 3 . |
| 4 | BUSRTN | Supply return | This pin is the DSI supply return node. |
| 5 | PCM | Pulse code modulated output | If the PCM output is enabled, this pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. If PCM is unused, this pin must be left unconnected. |
| 6 | TEST_SCLK | SPI clock | This input pin provides the serial clock to the SPI port for test purposes. An internal pull-down device is connected to this pin. This pin must be grounded or left unconnected in the application. |
| 7 | TEST_MISO | SPI data out | This pin functions as the serial data output from the SPI port for test purposes. This pin must be left unconnected in the application. |
| 8 | TEST_MOSI | SPI data in | This pin functions as the serial data input to the SPI port for test purposes. An internal pull-down device is connected to this pin. This pin must be grounded or left unconnected in the application. |
| 9 | V_{REG} | Internal supply | This pin is connected to the power supply for the internal circuitry. An external capacitor must be connected between this pin and V_{SS} . Reference Figure 3 . |
| 10 | $\overline{TEST_CS}$ | Chip select | This input pin provides the chip select to the SPI port for test purposes. An internal pullup device is connected to this pin. This pin must be left unconnected in the application. |
| 11 | V_{REGA} | Internal supply | This pin is connected to the power supply for the internal circuitry. An external capacitor must be connected between this pin and V_{SSA} . Reference Figure 3 . |
| 12 | V_{SS} | Internal supply return | This pin is the power supply return node for the internal power supplies and must be connected to BUSRTN in this application. |
| 13 | V_{BUF} | Power supply | This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies the internal regulators to provide immunity from EMC and supply dropouts. An external capacitor must be connected between this pin and V_{SS} . Reference Figure 3 . |
| 14 | TEST2 | Test pin | This pin is must be connected to V_{SS} in the application. |
| 15 | TEST | Test pin | This pin is must be connected to V_{SS} in the application. |
| 16 | BUSSW | Bus switch gate drive | This pin is the drive for a high-side, daisy-chain switch. When switch is connected, daisy-chain mode is used, this pin is connected to the gate of a p-channel FET which connects BUS_I to the next slave in the daisy chain. An external pullup resistor is required on the gate of the p-channel FET. Reference Section 3.6.4 . If unused, this pin must be left unconnected. |
| 17 | PAD | Die attach pad | This pin is the die attach flag, and is internally connected to V_{SS} . Reference Section 6 for die attach pad connection details. |
| | Corner pads | Corner pads | The corner pads are internally connected to V_{SS} . |

1.3 Application diagram

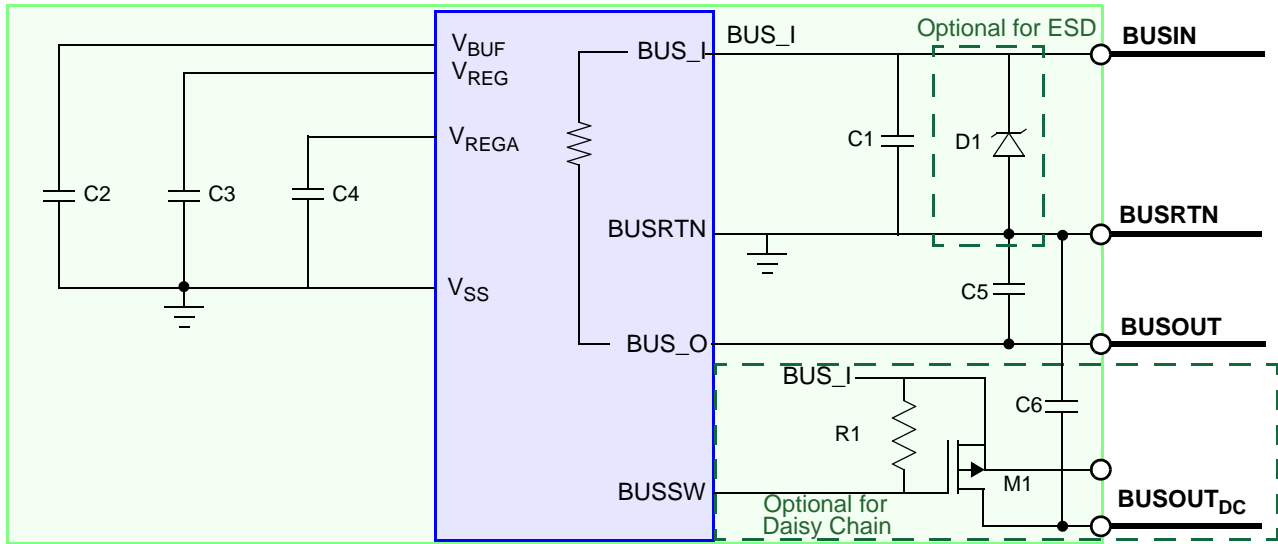


Figure 3. MMA27XXW/17XXW application diagram

Table 2. External component recommendations

| Ref Des | Type | Description | Purpose |
|---------|------------------|-----------------------------------|--|
| C1 | Ceramic | 220 pF, 10%, 50 V minimum, X7R | BUSIN EMC and ESD protection. Capacitor value is dependent on the DSI3 master device and must be chosen by the system implementer. |
| C2 | Ceramic | 1 μ F, 10%, 10 V minimum, X7R | Voltage regulator output capacitor |
| C3 | Ceramic | 1 μ F, 10%, 10 V minimum, X7R | Voltage regulator output capacitor |
| C4 | Ceramic | 1 μ F, 10%, 10 V minimum, X7R | Voltage regulator output capacitor |
| C5 | Ceramic | 100 pF, 10%, 50 V minimum, X7R | BUSOUT EMC and ESD protection |
| C6 | Ceramic | 100 pF, 10%, 50 V minimum, X7R | BUSOUT EMC and ESD protection |
| R1 | General purpose | 100 k Ω , 5%, 200 PPM | Pullup resistor for external high-side, daisy-chain FET |
| M1 | P-channel MOSFET | | High-side, daisy-chain transistor |
| D1 | Zener diode | MMBZ27Vxxxx or equivalent | ESD protection diode |

1.4 Device orientation and device marking

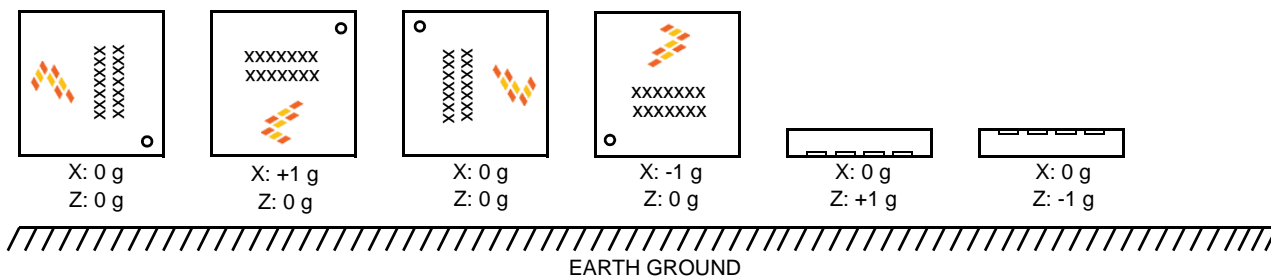


Figure 4. Device orientation diagram

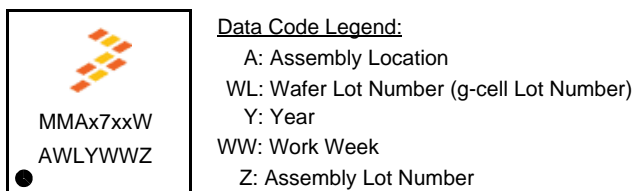


Figure 5. Device marking

2 Electrical Characteristics

2.1 Maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

| # | Rating | Symbol | Value | Unit | |
|----|--|---------------|--------------|----------------|--------|
| 1 | Supply voltage (BUS_I, BUS_O, BUSSW) | | | | |
| 2 | Reverse current ≤ 160 mA, $t \leq 80$ ms | BUS_I_REV | -0.7 | V | (6) |
| 3 | Continuous | BUS_I_MAX | +20.0 | V | (6) |
| 4 | Transient (< 10 us) | BUS_I_TRANS | +25.0 | V | (9) |
| 5 | V_{BUF} | | -0.3 to +4.0 | V | (6) |
| 6 | V_{REG} , V_{REGA} , TEST_SCLK, TEST_CS, TEST_MOSI, TEST_MISO, PCM | | -0.3 to +3.0 | V | (6) |
| 7 | BUS_I, BUS_O and BUSRTN current | | | | |
| 8 | Maximum duration 560 μ s, with 10 ms repetition rate | I_{IN} | 200 | mA | (6) |
| 9 | Continuous | I_{IN} | 150 | mA | (6) |
| 10 | Powered shock (six sides, 0.5 ms duration) | g_{pms} | ± 2000 | g | (5) |
| 11 | Unpowered shock (six sides, 0.5 ms duration) | g_{shock} | ± 2000 | g | (5) |
| 12 | Drop shock (to concrete, tile or steel surface, 10 drops, any orientation) | h_{DROP} | 1.2 | m | (5) |
| 13 | Electrostatic discharge (per AEC-Q100), external pins | | | | |
| 14 | BUS_I, BUS_O, BUSRTN, HBM (100 pF, 1.5 k Ω) | V_{ESD} | ± 4000 | V | (5) |
| 15 | Electrostatic discharge (per AEC-Q100) | | | | |
| 16 | HBM (100 pF, 1.5 k Ω) | V_{ESD} | ± 2000 | V | (5) |
| 17 | CDM (R = 0 Ω) | V_{ESD} | ± 500 | V | (5) |
| 18 | MM (200 pF, 0 Ω) | V_{ESD} | ± 200 | V | (5) |
| 19 | Temperature range | | | | |
| 20 | Storage | T_{stg} | -40 to +125 | $^{\circ}$ C | (5) |
| 21 | Junction | T_J | -40 to +150 | $^{\circ}$ C | (9) |
| 22 | Thermal resistance | θ_{JC} | 2.5 | $^{\circ}$ C/W | (9,11) |

2.2 Operating range

$V_{BUS_I_L} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_I_H}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12^{\circ}$ C/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|--|---------------------------|---------------------|-----|-------------------------|--------------|-------|
| 23 | Supply voltage (measured at BUS_I pin) | | | | | | |
| 24 | V_{HIGH} | * $V_{BUS_I_HIGH_max}$ | — | — | 20.0 | V | (1,6) |
| 25 | V_{LOW} rising | $V_{BUS_I_LOW_Rise}$ | 4.5 | — | — | V | (9) |
| 26 | V_{LOW} falling | * $V_{BUS_I_LOW_Fall}$ | 4.0 | — | — | V | (1) |
| 27 | Supply voltage (undervoltage) | $V_{BUS_I_UV}$ | $V_{BUS_I_UV_F}$ | — | $V_{BUS_I_LOW_Fall}$ | V | (3,6) |
| 28 | Programming voltage ($I_{RD} \leq 85$ mA) Applied to BUS_I | VPP | 14.0 | — | $V_{BUS_I_HIGH_max}$ | V | (6) |
| 29 | ESD operating voltage | | | | | | |
| 30 | (No device reset, $C_{BUS_IN} = 220$ pF, D1 = MMBZ27Vxxxx) | | | | | | |
| 31 | Maximum ± 15 kV air discharge, 330 pF, 2.0 k Ω | $V_{BUS_I_ESD}$ | — | — | 12.0 | V | (9) |
| 32 | Operating temperature range | | T_L | | T_H | | |
| 33 | | T_A | -40 | — | +105 | $^{\circ}$ C | (1) |
| 34 | | T_A | -40 | — | +125 | $^{\circ}$ C | (5,6) |

2.3 Electrical characteristics - supply and I/O

$V_{BUS_LL} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_IH}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12$ °C/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|--|---------------------------------------|-------------------|------------------|-------------------|-------|-------|
| 35 | Quiescent supply current $V_{BUS_I} = 4$ V, $V_{BUS_I} = 20$ V | I_q | 4.0 | — | 8.0 | mA | (1) |
| 36 | Response current Low | I_{RESP} | $I_q + 10.50$ | $I_q + 12.0$ | $I_q + 13.5$ | mA | (1) |
| 37 | High | $2 * I_{RESP}$ | $I_q + 21.0$ | $I_q + 24.0$ | $I_q + 27.0$ | mA | (1) |
| 38 | V_{BUF} current limit | I_{INRUSH_MAX} | — | — | 30 | mA | (6) |
| 39 | Internally regulated voltages V_{BUF} , $V_{BUS_I} = 4$ V, $V_{BUS_I} = 20$ V | V_{BUF} | 3.250 | 3.400 | 3.550 | V | (1) |
| 40 | V_{REG} , $V_{BUS_I} = 4$ V | V_{REG} | 2.400 | 2.500 | 2.600 | V | (1) |
| 41 | V_{REGA} , $V_{BUS_I} = 4$ V, $V_{BUS_I} = 20$ V | V_{REGA} | 2.425 | 2.500 | 2.575 | V | (1) |
| 42 | Low-voltage detection threshold BUS_I falling | $V_{BUS_I_UV_F}$ | 3.60 | 3.75 | 3.90 | V | (3,6) |
| 43 | V_{BUF} falling | $V_{BUF_UV_F}$ | 2.80 | 3.05 | 3.20 | V | (3,6) |
| 44 | V_{REG} falling | $V_{REG_UV_F}$ | 2.15 | 2.25 | 2.35 | V | (3,6) |
| 45 | V_{REGA} falling | $V_{REGA_UV_F}$ | 2.15 | 2.25 | 2.35 | V | (3,6) |
| 46 | Low-voltage detection hysteresis | V_{HYST} | 0.04 | — | — | V | (6) |
| 47 | External capacitor (V_{BUF} , V_{REG} , V_{REGA}) Capacitance | C_{VBUF} , C_{VREG} , C_{VREGA} | 500 | 1000 | 1500 | nF | (9) |
| 48 | ESR (including interconnect resistance) | ESR | 0 | — | 200 | mΩ | (9) |
| 49 | V_{LOW} detection threshold (Section 3.6.1) V_{LOW} detection threshold | V_{DELTA_THRESH} | $V_{HIGH} - 1.25$ | $V_{HIGH} - 1.0$ | $V_{HIGH} - 0.75$ | V | (3,6) |
| 50 | V_{LOW} detection hysteresis | $V_{DELTA_THRESH_Hyst}$ | 40 | 60 | 80 | mV | (6) |
| 51 | Discovery Mode current sense (Section 3.6.3) Sense resistor | R_{SENSE} | 1.3 | 2.15 | 3 | Ω | (6) |
| 52 | I_{RESP} detection threshold ($I_{BUS_O_q} \leq 24$ mA) | I_{RESP_Det} , V_{IRESP_Offset} | 6 | 12 | 18 | mA | (3,6) |
| 53 | Bus switch output low voltage (Section 3.6.4) $I_{Load} = 100$ μA | $V_{BUS_SW_OL}$ | 0.0 | — | 0.45 | V | (3,6) |
| 54 | Bus switch open drain output leakage current (BUSSW) $V_{BUSSW} = 20$ V | $I_{BUS_SW_ODL}$ | — | — | 10 | μA | (3,6) |
| 55 | Output high voltage (PCM) $I_{Load} = -100$ μA | V_{OH} | $V_{REG} - 0.1$ | — | — | V | (3) |
| 56 | Output low voltage (PCM) $I_{Load} = 100$ μA | V_{OL} | — | — | 0.1 | V | (3) |

2.4 Electrical Characteristics - sensor and signal chain

$V_{BUS_I_L} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_I_H}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12$ °C/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|---|---------------------------|--------|--------|--------|-------|---------|
| 57 | Sensitivity ($T_A = 25^\circ\text{C}$, 10-bit output @ 100 Hz, referenced to 0Hz: $\pm 5\%$) ± 25 g range | * SENS ₀₂₅ | 19.456 | 20.480 | 21.504 | LSB/g | (1) |
| 58 | ± 125 g range | * SENS ₁₂₅ | 3.8912 | 4.0960 | 4.3008 | LSB/g | (1) |
| 59 | ± 187 g range | * SENS ₁₈₇ | 2.5944 | 2.7310 | 2.8676 | LSB/g | (1) |
| 60 | ± 250 g range | * SENS ₂₅₀ | 1.9456 | 2.0480 | 2.1504 | LSB/g | (1) |
| 61 | ± 375 g range | * SENS ₃₇₅ | 1.2967 | 1.3650 | 1.4333 | LSB/g | (1) |
| 62 | Sensitivity ($T_L \leq T_A \leq T_H$, $V_{BUS_I_UV_F} \leq V_{BUS_I} \leq V_{LOW}$ 10-bit output @ 100 Hz, referenced to 0 Hz: $\pm 7\%$) ± 25 g range | * SENS ₀₂₅ | 19.046 | 20.480 | 21.914 | LSB/g | (1) |
| 63 | ± 125 g range | * SENS ₁₂₅ | 3.8092 | 4.0960 | 4.3828 | LSB/g | (1) |
| 64 | ± 187 g range | * SENS ₁₈₇ | 2.5398 | 2.7310 | 2.9222 | LSB/g | (1) |
| 65 | ± 250 g range | * SENS ₂₅₀ | 1.9046 | 2.0480 | 2.1914 | LSB/g | (1) |
| 66 | ± 375 g range | * SENS ₃₇₅ | 1.2694 | 1.3650 | 1.4606 | LSB/g | (1) |
| 67 | Digital offset before offset cancellation (10-bit) ± 25 g, ± 125 g, ± 250 g Z-axis | * OFF _{10Bit} | -100 | 0 | +100 | LSB | (1) |
| 68 | $V_{BUS_I_UV_F} \leq V_{BUS_I} \leq V_{LOW}$, ± 25 g, ± 125 g, ± 250 g Z-axis | OFF _{10Bit} | -100 | 0 | +100 | LSB | (6) |
| 69 | ± 187 g, ± 250 g X-axis, ± 375 g | * OFF _{10Bit} | -52 | 0 | +52 | LSB | (1) |
| 70 | $V_{BUS_I_UV_F} \leq V_{BUS_I} \leq V_{LOW}$, ± 187 g, ± 250 g X-axis, ± 375 g | OFF _{10Bit} | -52 | 0 | +52 | LSB | (6) |
| 71 | Digital offset after offset cancellation (10-bit, all filter options) | OFF _{10Bit} | -1 | 0 | +1 | LSB | (6,8,9) |
| 72 | Continuous offset monitor limit 10-bit output, before compensation, ± 25 g | OFF _{MON} | -150 | — | +150 | LSB | (7,8) |
| 73 | 10-bit output, before compensation, ± 125 g, ± 250 g Z-axis | OFF _{MON} | -120 | — | +120 | LSB | (7,8) |
| 74 | 10-bit output, before compensation, ± 187 g, ± 250 g X-axis, ± 375 g | OFF _{MON} | -70 | — | +70 | LSB | (7,8) |
| 75 | Range of output (10-bit mode) Acceleration (signed) | RANGE _{Signed} | -511 | — | +511 | LSB | (7,8) |
| 76 | Acceleration (unsigned) | RANGE _{Unsigned} | 1 | — | 1023 | LSB | (7,9) |
| 77 | Error code (signed) | ERR _{Signed} | — | -512 | — | LSB | (7,8) |
| 78 | Error code (unsigned) | ERR _{Unsigned} | — | 0 | — | LSB | (7,9) |
| 79 | Cross-axis sensitivity Z-axis to X-axis | V _{ZX} | -5 | — | +5 | % | (6) |
| 80 | Y-axis to X-axis | V _{YX} | -5 | — | +5 | % | (6) |
| 81 | X-axis to Z-axis | V _{XZ} | -5 | — | +5 | % | (6) |
| 82 | Y-axis to Z-axis | V _{YZ} | -5 | — | +5 | % | (6) |
| 83 | System output noise peak (peak value of 100 samples @ 2 kHz) 10-bit mode, LPF = 180 Hz, 2-Pole, All Ranges | n _{Peak_180} | -3 | — | +3 | LSB | (1) |
| 84 | 10-bit mode, LPF = 400 Hz, 4-Pole, All Ranges | n _{Peak_400} | -4 | — | +4 | LSB | (6) |
| 85 | System output noise average (average value of 100 samples @ 2 kHz) 10-bit mode, LPF = 180 Hz, 2-pole, all ranges | * n _{RMS_180} | — | — | +1.0 | LSB | (1) |
| 86 | 10-bit mode, LPF = 400 Hz, 4-pole, all ranges | * n _{RMS_400} | — | — | +1.0 | LSB | (6) |
| 87 | Nonlinearity (10-bit output, all ranges) | NL _{OUT} | -2 | — | +2 | % | (6) |

2.5 Electrical characteristics - self-test and overload

$V_{BUS_LL} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_IH}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12^\circ\text{C}/\text{min}$, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|--------------------------|--------------------------|------------------------|--------------------------|-------|-------|
| 88 | 10-bit output during active self-test ±25 g range, X-axis | g_{ST10_25X} | ΔST_{MIN} 124 | ΔST_{NOM} — | ΔST_{MAX} 208 | LSB | (1) |
| 89 | ±125 g range, X-axis | g_{ST10_125X} | 236 | — | 395 | LSB | (1) |
| 90 | ±187 g range, X-axis | g_{ST10_187X} | 156 | — | 263 | LSB | (1) |
| 91 | ±250 g range, X-axis | g_{ST10_250X} | 117 | — | 198 | LSB | (1) |
| 92 | ±375 g range, X-axis | g_{ST10_375X} | 77 | — | 131 | LSB | (1) |
| 93 | ±250 g range, Z-axis | g_{ST10_250Z} | 80 | — | 160 | LSB | (1) |
| 94 | Self-test accuracy: Δ from stored value, including sensitivity error -40°C ≤ T_A ≤ 125°C (Section 3.5.2) | $\Delta STACC$ | -10 | — | +10 | % | (1,5) |
| 95 | Transducer clipping limit ±25 g, X-axis, positive/negative | $g_{g-cell_ClipLowX}$ | 400 | 470 | 500 | g | (9) |
| 96 | ±125 g, ±187 g, ±250 g, ±375 g, X-axis, positive/negative | $g_{g-cell_ClipHiX}$ | 1700 | 2100 | 2300 | g | (9) |
| 97 | ±250 g, Z-axis positive | $g_{g-cell_ClipHiZP}$ | 2200 | 2700 | 3300 | g | (9) |
| 98 | ±250 g, Z-axis negative | $g_{g-cell_ClipHiZN}$ | -3700 | -3200 | -2700 | g | (9) |
| 99 | Sinc filter clipping limit ±25 g, X-axis, positive/negative (MMA2702WR2) | $g_{ADC_Clip_25X_H}$ | 190 | 210 | 240 | g | (9) |
| 100 | ±125 g, X-axis, positive/negative (MMA2712WR2) | $g_{ADC_Clip_125X_H}$ | 920 | 1100 | 1300 | g | (9) |
| 101 | ±187 g, X-axis positive/negative (MMA2718WR2) | $g_{ADC_Clip_187X_H}$ | 1600 | 1900 | 2200 | g | (9) |
| 102 | ±250 g, X-axis positive/negative (MMA2725WR2) | $g_{ADC_Clip_250X_H}$ | 1600 | 1900 | 2200 | g | (9) |
| 103 | ±375 g, X-axis positive/negative (MMA2737WR2) | $g_{ADC_Clip_375X_H}$ | 1600 | 1900 | 2200 | g | (9) |
| 104 | ±250 g, Z-axis, positive (MMA1725WR2) | $g_{ADC_Clip_250ZPH}$ | 1500 | 2000 | 2500 | g | (9) |
| 105 | ±250 g, Z-axis, negative (MMA1725WR2) | $g_{ADC_Clip_250ZNH}$ | -3200 | -2900 | -2500 | g | (9) |

2.6 Dynamic electrical characteristics - DSI3

$V_{BUS_LL} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_IH}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12^\circ\text{C}/\text{min}$, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|---------------------------------|------------------------|---------------------------|---------------------------------|-------------------------|-------|
| 106 | Reset recovery (all modes, excluding V_{BUS_I} voltage ramp time) | | | | | | |
| | POR to 1st command (Section 3.6) | $t_{\text{DSI_POR}}$ | — | 5 | — | ms | (7,8) |
| 107 | POR to acceleration data ready (Section 3.6) | $t_{\text{DSP_POR}}$ | — | $t_{\text{DSI_POR}}$ | — | s | (7,8) |
| | Command reception (general) | | | | | | |
| 108 | V_{HIGH} low-pass filter time constant (Section 3.6.1) | $t_{\text{VHIGH_RC}}$ | 60 | 120 | 180 | μs | (8,9) |
| 109 | V_{HIGH} detection analog delay (Section 3.6.1) | $t_{\text{VHIGH_Delay}}$ | — | — | 600 | ns | (8,9) |
| 110 | i_q low-pass filter time constant (Section 3.6.3) | $t_{\text{IQ_RC}}$ | 200 | 400 | 600 | μs | (8,9) |
| 111 | Command valid time (Section 3.6.1) | $t_{\text{Cmd_Valid}}$ | — | 2 | — | μs | (7,9) |
| | Response transmission (general, Section 4.2.3) | | | | | | |
| 112 | Response slew time: 2.0 mA to 10.0 mA, 10.0 mA to 2.0 mA | $t_{\text{SLEW1_RESP}}$ | 200 | 400 | 600 | ns | (6,8) |
| 113 | Response slew time: 4.0 mA to 20.0 mA, 20.0 mA to 4.0 mA | $t_{\text{SLEW2_RESP}}$ | 200 | 400 | 600 | ns | (6,8) |
| 114 | $t_{\text{SLEW1_RESP}} - t_{\text{SLEW2_RESP}}$ | Δt_{SLEW} | -100 | — | 100 | ns | (8,9) |
| 115 | $t_{\text{SLEW1_RESP_Rise}} - t_{\text{SLEW2_RESP_Fall}}$ | $\Delta t_{\text{SLEW_rf}}$ | -250 | — | 250 | ns | (8,9) |
| 116 | Response current activation time: current activated to 50% | $t_{\text{ACT_RESP}}$ | 200 | — | 400 | ns | (8,9) |
| | Command reception (Discovery Mode) | | | | | | |
| 117 | Command start time (Section 4.1) | $t_{\text{START_DISC}}$ | $t_{\text{DSI_POR}}$ | — | 12 | ms | (7,8) |
| 118 | Command bit time (Section 4.1) | $t_{\text{DISC_BitTime}}$ | — | 16 | — | μs | (7,8) |
| 119 | Command transmission period (Section 4.1) | $t_{\text{PER_DISC}}$ | $1000/f_{\text{OSC}}$ | — | — | s | (7,8) |
| 120 | Command blocking time, Discovery Mode (Section 3.6.1) | $t_{\text{CmdBlock_DISC}}$ | — | 96 | — | μs | (7,8) |
| 121 | I_{CCQ} sample delay time (Section 3.6.3) | $t_{\text{Disc_Dly}}$ | — | 48 | — | μs | (7,9) |
| 122 | I_{CCQ} sample time (Section 3.6.3) | $t_{\text{Disc_Iccqsamp}}$ | — | 15 | — | μs | (7,9) |
| 123 | I_{DISC} sample delay time (Section 3.6.3) | $t_{\text{Discsmp_Dly}}$ | — | 65 | — | μs | (7,9) |
| 124 | I_{DISC} sample time (Section 3.6.3) | t_{Discsmp} | — | 31 | — | μs | (7,9) |
| | Response transmission (Discovery Mode) | | | | | | |
| 125 | Response start delay (Section 4.1) | $t_{\text{START_DISC_RSP}}$ | — | 64 | — | μs | (7,8) |
| 126 | Response ramp time (Section 4.1) | $t_{\text{DISC_Ramp_RSP}}$ | — | 16 | — | μs | (7,8) |
| 127 | Response ramp rate (Section 4.1) | $I_{\text{DISC_Ramp}}$ | — | 1.5 | — | $\text{mA}/\mu\text{s}$ | (6,8) |
| 128 | Response idle time (Section 4.1) | $t_{\text{DISC_Idle_RSP}}$ | — | 16 | — | μs | (7,8) |
| 129 | Response peak current (Section 4.1) | $I_{\text{DISC_Peak}}$ | — | $2 \cdot I_{\text{RESP}}$ | — | mA | (6,8) |
| | Command reception (Command and Response Mode) | | | | | | |
| 130 | Command bit time (Section 4.2) | $t_{\text{Cmd_BitTime}}$ | — | 8 | — | μs | (7,8) |
| 131 | Command transmission period (Section 4.2) | $t_{\text{PER_CRM}}$ | $t_{\text{PER_PDCM}}$ | — | $8 \times t_{\text{PER_PDCM}}$ | s | (7,8) |
| 132 | Command blocking time, CRM (Section 3.6.1) | $t_{\text{CmdBlock_CRM}}$ | — | 456 | — | μs | (7,8) |
| 133 | Command blocking start time, CRM (Section 3.6.1) | $t_{\text{CmdBlock_ST_CRM}}$ | — | 268 | — | μs | (7,8) |
| | Response transmission (Command and Response Mode) | | | | | | |
| 134 | Response chip time | $t_{\text{CHIP_CRM}}$ | — | 5 | — | μs | (7,8) |
| 135 | Response start time (Section 4.2) | $t_{\text{START_CRM}}$ | — | 295 | — | μs | (7,8) |
| | Command reception (Periodic Data Collection Mode) | | | | | | |
| 136 | Command bit time (Section 4.3) | $t_{\text{Cmd_BitTime}}$ | — | 8 | — | μs | (7,8) |
| 137 | Command transmission period (Section 4.3) | $t_{\text{PER_PDCM}}$ | 100 | — | 5000 | μs | (7,8) |
| 138 | Command transmission period resolution | $t_{\text{PER_PDCM_Res}}$ | — | 5 | — | μs | (7,8) |
| 139 | Command blocking time, PDCM (Section 4.3.2) | $t_{\text{CmdBlock_PDCM}}$ | 1 | — | 4095 | μs | (7,8) |
| 140 | Command blocking time resolution, PDCM (Section 4.3.2) | $t_{\text{CmdBlockRes_PDCM}}$ | — | 1 | — | μs | (7,8) |
| 141 | Command blocking start time, PDCM (Section 4.3.2) | $t_{\text{CmdBlock_ST_PDCM}}$ | — | 20 | — | μs | (7,8) |
| 142 | Command blocking start time, BDM command | $t_{\text{CmdBlock_ST_BDM}}$ | — | 44 | — | μs | (7,8) |
| | Response transmission (Periodic Data Collection Mode) | | | | | | |
| 143 | Response chip time typical (Section 3.1.15.3) | $t_{\text{CHIP_PDCM}}$ | 3 | — | 6.5 | μs | (7,8) |
| 144 | Response chip resolution (Section 3.1.15.3) | $t_{\text{CHIPRes_PDCM}}$ | — | 0.5 | — | μs | (7,8) |
| 145 | Response start time typical (Section 4.3) | $t_{\text{START_PDCM}}$ | 20 | — | 4095 | μs | (7,8) |
| 146 | Response start time typical, BDM enabled (Section 4.3) | $t_{\text{START_PDCM_BDM}}$ | 44 | — | 4095 | μs | (7,8) |
| 147 | Response start time resolution | $t_{\text{ST_RES_PDCM}}$ | — | 1 | — | μs | (7,8) |
| | Response transmission (Background Diagnostic Mode) | | | | | | |
| 148 | Response start time (Section 4.3) | $t_{\text{START_BDM}}$ | — | 20 | — | μs | (7,8) |
| 149 | Register write to BUSSW active | t_{BS} | — | 456 | — | μs | (7,8) |
| 150 | DSI data latency | $t_{\text{LAT_DSI}}$ | — | 0.5 | 6.25 | μs | (7,9) |
| 151 | OTP program timing | | | | | | |
| | Time to program the user OTP array | $t_{\text{NVM_WRITE_MAX}}$ | — | — | 60 | ms | (7,8) |

2.7 Dynamic electrical characteristics - signal chain

$V_{BUS_LL} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_IH}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12$ °C/min, unless otherwise specified.

Table 3.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|---|----------------------------|-------|-------|-------|---------|-------|
| 152 | DSP low-pass filter | | | | | | |
| 153 | Cutoff frequency LPF0, 2-pole (referenced to 0 Hz) | f_{C_LPF0} | — | 180 | — | Hz | (6,7) |
| 154 | Cutoff frequency LPF6, 3-pole (referenced to 0 Hz) | f_{C_LPF6} | — | 325 | — | Hz | (6,7) |
| 155 | Cutoff frequency LPF8, 3-pole (referenced to 0 Hz) | f_{C_LPF8} | — | 400 | — | Hz | (7,8) |
| 156 | Cutoff frequency LPF9, 4-pole (referenced to 0 Hz) | f_{C_LPF9} | — | 400 | — | Hz | (7,8) |
| 157 | Cutoff frequency LPF11, 4-pole (referenced to 0 Hz) | f_{C_LPF11} | — | 800 | — | Hz | (7,8) |
| 158 | Cutoff frequency LPF14, 4-pole (referenced to 0 Hz) | f_{C_LPF14} | — | 1200 | — | Hz | (7,8) |
| 159 | DSP offset cancellation low-pass filter | | | | | | |
| 160 | Offset Cancellation low-pass filter Input sample Rate | $t_{OC_SampleRate}$ | — | 256 | — | μ s | (7,9) |
| 161 | Cutoff frequency, startup Phase 1, 1-pole | f_{C_OCPH1} | — | 10.0 | — | Hz | (7,9) |
| 162 | Startup Phase 1 time | t_{OCPH1} | — | 80 | — | ms | (7,9) |
| 163 | Cutoff frequency, startup Phase 2, 1-pole | f_{C_OCPH2} | — | 1.0 | — | Hz | (7,9) |
| 164 | Startup Phase 2 time | t_{OCPH2} | — | 70 | — | ms | (7,9) |
| 165 | Offset cancellation output update rate (10-bit) | $t_{OffRate}$ | — | 2 | — | s | (7,9) |
| 166 | Offset cancellation output step size (10-bit) | OFF_{Step} | — | 0.5 | — | LSB | (7,9) |
| 167 | Offset monitor update rate | $OFFMON_{OSC}$ | — | 500 | — | μ s | (7,8) |
| 168 | Offset monitor count limit | $OFFMON_{CNTLIMIT}$ | — | 4096 | — | 1 | (7,8) |
| 168 | Offset monitor counter size | $OFFMON_{CNTSIZE}$ | — | 8192 | — | 1 | (7,8) |
| 169 | Signal delay excluding LPF group delay and interpolation | t_{SIG_DELAY} | — | — | 100 | μ s | (7,9) |
| 170 | Interpolation latency | t_{LAT_INTERP} | — | 16 | — | μ s | (7,9) |
| 171 | Self-test response time (CS Rising to 90% g_{ST10_xxx}) | | | | | | |
| 172 | Self-test activation time (180 Hz LPF) | $t_{ST_ACT_180}$ | 2.00 | — | 4.00 | ms | (3,6) |
| 173 | Self-test deactivation time (180 Hz LPF) | $t_{ST_DEACT_180}$ | 2.00 | — | 4.00 | ms | (3,6) |
| 174 | Self-test activation time (325 Hz LPF, 3 Pole) | $t_{ST_ACT_325}$ | 1.30 | — | 2.70 | ms | (6) |
| 175 | Self-test deactivation time (325 Hz LPF, 3 Pole) | $t_{ST_DEACT_325}$ | 1.30 | — | 2.70 | ms | (6) |
| 176 | Self-test activation time (400 Hz LPF, 3 or 4 Pole) | $t_{ST_ACT_400}$ | 1.00 | — | 2.50 | ms | (6) |
| 177 | Self-test deactivation time (400 Hz LPF, 3 or 4 Pole) | $t_{ST_DEACT_400}$ | 1.00 | — | 2.50 | ms | (6) |
| 178 | Self-test activation time (800 Hz LPF) | $t_{ST_ACT_800}$ | 0.50 | — | 1.75 | ms | (6) |
| 179 | Self-test deactivation time (800 Hz LPF) | $t_{ST_DEACT_800}$ | 0.50 | — | 1.75 | ms | (6) |
| 180 | Self-test activation time (1200 Hz LPF) | $t_{ST_ACT_800}$ | 0.40 | — | 1.50 | ms | (6) |
| 180 | Self-test deactivation time (1200 Hz LPF) | $t_{ST_DEACT_800}$ | 0.40 | — | 1.50 | ms | (6) |
| 181 | Sensing element rolloff frequency (-3 db) | | | | | | |
| 182 | ± 25 g, X-axis | $f_{gcell_3dB_xlo}$ | 938 | 1600 | 2592 | Hz | (6) |
| 183 | ± 125 g, ± 187 g, ± 250 g, ± 375 g, X-axis | $f_{gcell_3dB_xhi}$ | 3952 | 7200 | 14370 | Hz | (6) |
| 183 | ± 250 g, Z-axis | $f_{gcell_3dB_zhi}$ | 3100 | 4500 | 6500 | Hz | (6) |
| 184 | Sensing element natural frequency | | | | | | |
| 185 | ± 25 g, X-axis | f_{gcell_xlo} | 12651 | 13200 | 13871 | Hz | (9) |
| 186 | ± 125 g, ± 187 g, ± 250 g, ± 375 g, X-axis | f_{gcell_xhi} | 26000 | 27500 | 28700 | Hz | (9) |
| 186 | ± 250 g, Z-axis | f_{gcell_zhi} | 15000 | 17000 | 17500 | Hz | (9) |
| 187 | Sensing element damping ratio | | | | | | |
| 188 | ± 25 g, X-axis | ζ_{gcell_xlo} | 2.76 | 4.20 | 6.77 | | (9) |
| 189 | ± 125 g, ± 187 g, ± 250 g, ± 375 g, X-axis | ζ_{gcell_xhi} | 1.26 | 2.00 | 3.60 | | (9) |
| 189 | ± 250 g, Z-axis | ζ_{gcell_zhi} | 1.40 | 2.00 | 2.90 | | (9) |
| 190 | Sensing element delay (@100 Hz) | | | | | | |
| 191 | ± 25 g, X-axis | $f_{gcell_delay100_xlo}$ | 63 | 100 | 170 | μ s | (9) |
| 192 | ± 125 g, ± 187 g, ± 250 g, ± 375 g, X-axis | $f_{gcell_delay100_xhi}$ | 13 | 24 | 40 | ms | (9) |
| 192 | ± 250 g, Z-axis | $f_{gcell_delay100_zhi}$ | 35 | 40 | 55 | μ s | (9) |
| 193 | Package resonance frequency | $f_{Package}$ | 100 | — | — | kHz | (9) |

2.8 Dynamic electrical characteristics - supply and support circuitry

$V_{BUS_I_L} \leq (V_{BUS_I} - V_{SS}) \leq V_{BUS_I_H}$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 12$ °C/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|------------------------|-------|-------|-------|---------|---------|
| 194 | Internal oscillator period Untrained * | f_{OSC} | 7.600 | 8.000 | 8.400 | MHz | (1) |
| 195 | With oscillator training | f_{OSC} | 7.879 | 8.000 | 8.121 | MHz | (7,8,9) |
| 196 | Oscillator training (Section 3.4.1) Oscillator training time (CRM and PDCM) | $t_{OscTrain}$ | — | 4 | — | ms | (7) |
| 197 | Oscillator training window (CRM and PDCM) | $OscTrain_{WIN}$ | 3.4 | — | 4.6 | ms | (7) |
| 198 | Oscillator training adjustment threshold (CRM and PDCM) | $OscTrain_{ADJ}$ | -60 | — | 60 | μs | (7) |
| 199 | Oscillator training step size (CRM and PDCM) | $OscTrain_{RES}$ | — | 28 | — | μs | (7) |
| 200 | Quiescent current settling time (power applied to $I_q = I_{IDLE} \pm 2$ mA) | t_{SET} | — | — | 4 | ms | (6) |
| 201 | BUS_I microcut Survival time (BUS_I disconnect without reset, $C_{BUF}=C_{REG}=C_{REGA}=700nF$) | $t_{BUS_I_MICROCUT}$ | 30 | — | — | μs | (8) |
| 202 | Reset time (BUS_I disconnect time to reset, $C_{BUF}=C_{REG}=C_{REGA}=1\mu F$) | $t_{BUS_I_RESET}$ | — | — | 1000 | μs | (8) |
| 203 | BUS_I undervoltage detection delay $BUS_I < V_{BUS_I_UV_F}$ to I_{RESP} deactivation | $t_{BUS_I_POR}$ | — | — | 5 | μs | (6) |
| 204 | V_{BUF} undervoltage detection delay $V_{BUF} < V_{BUF_UV_F}$ to I_{RESP} deactivation | $t_{V_{BUF}_POR}$ | — | — | 5 | μs | (6) |
| 205 | V_{REG} , V_{REGA} undervoltage reset delay $V_{REG} < V_{REG_UV_F}$ to POR assertion, $V_{REGA} < V_{REGA_UV_F}$ to \overline{POR} assertion | $t_{V_{REG}_POR}$ | — | — | 50 | μs | (6) |
| 206 | V_{BUF} , V_{REG} , V_{REGA} capacitor monitor POR to capacitor disconnect | $t_{POR_CAPTEST}$ | — | 950 | — | μs | (7,8) |
| 207 | Disconnect time | t_{CAPTST_TIME} | — | 1.5 | — | μs | (7,8) |

NOTES

- Parameter tested 100% at final test. Temperature = -40°C, 25°C and 105°C, $V_{BUS_I} = 8$ V, Unless otherwise stated.
- Not Applicable.
- Parameter verified by pass/fail testing at final test
- Parameter verified by pass/fail testing at final test during safe launch.
- Parameter verified by qualification testing.
- Parameter verified by characterization.
- Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
- Parameter verified by functional evaluation.
- Parameter verified by simulation.
- Not Applicable.
- Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.

* Indicates critical characteristic.

3 Functional Description

3.1 User-accessible data array

A user-accessible data array allows for each device to be customized. The array consists of an OTP factory-programmable block, an OTP user-programmable block, and read-only registers for data and device status. The OTP blocks incorporate independent data verification (reference [Section 3.2](#)). Portions of the factory-programmable array are reserved for factory-programmed trim values.

Table 4. User-accessible data

| Byte Addr | Register | Bit Function | | | | Bit Function | | | | Type |
|-------------|--------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| \$00 | ICTYPEID | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | R |
| \$01 | ICMFGID | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | R |
| \$02 | ICREVID | 0 | 0 | 1 | ICREVID[4] | 0 | 0 | 0 | 0 | R |
| \$03 | MODTYPE | 0 | 0 | 0 | 0 | 0 | MODTYPE[2] | MODTYPE[1] | MODTYPE[0] | U,R |
| \$04 | MODMFGID | 0 | 0 | 0 | 0 | 0 | MODMFGID[2] | MODMFGID[1] | MODMFGID[0] | U,R |
| \$05 | MODREV | 0 | 0 | 0 | 0 | 0 | MODREV[2] | MODREV[1] | MODREV[0] | U,R |
| \$06 | USERID1 | USERID1[7] | USERID1[6] | USERID1[5] | USERID1[4] | USERID1[3] | USERID1[2] | USERID1[1] | USERID1[0] | U,R |
| \$07 - \$08 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | R |
| \$09 | PN | PN[7] | PN[6] | PN[5] | PN[4] | PN[3] | PN[2] | PN[1] | PN[0] | F,R |
| \$0A | SN0 | SN[7] | SN[6] | SN[5] | SN[4] | SN[3] | SN[2] | SN[1] | SN[0] | F,R |
| \$0B | SN1 | SN[15] | SN[14] | SN[13] | SN[12] | SN[11] | SN[10] | SN[9] | SN[8] | F,R |
| \$0C | SN2 | SN[23] | SN[22] | SN[21] | SN[20] | SN[19] | SN[18] | SN[17] | SN[16] | F,R |
| \$0D | SN3 | SN[31] | SN[30] | SN[29] | SN[28] | SN[27] | SN[26] | SN[25] | SN[24] | F,R |
| \$0E - \$0F | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | R |
| \$10 | DSIREV | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | R |
| \$11 | PHYSADDR | 0 | 0 | 0 | 0 | PADDR[3] | PADDR[2] | PADDR[1] | PADDR[0] | U,R/W |
| \$12 | BDM_CFG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BDM_EN | R/W |
| \$13 | CRM_CFG | 0 | 0 | 0 | CK_CAL_RST | CRM_PER[1] | CRM_PER[0] | CK_CAL_EN | SS_EN | R/W |
| \$14 | PDCM_CFG | 0 | 0 | 0 | 0 | 0 | 0 | DATALENGTH | STATLENGTH | R/W |
| \$15 | PDCM_EN | PDCM_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R/W |
| \$16 | CHIPTIME | 0 | 0 | 0 | 0 | 0 | CHIPTIME[2] | CHIPTIME[1] | CHIPTIME[0] | R/W |
| \$17 | PDCM_PER | 0 | 0 | 0 | 0 | 0 | PDCM_PER[2] | PDCM_PER[1] | PDCM_PER[0] | R/W |
| \$18 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | R/W |
| \$19 | PDCM_RSPST_L | PDCM_RSPST[7] | PDCM_RSPST[6] | PDCM_RSPST[5] | PDCM_RSPST[4] | PDCM_RSPST[3] | PDCM_RSPST[2] | PDCM_RSPST[1] | PDCM_RSPST[0] | R/W |
| \$1A | PDCM_RSPST_H | 0 | 0 | 0 | 0 | PDCM_RSPST[11] | PDCM_RSPST[10] | PDCM_RSPST[9] | PDCM_RSPST[8] | R/W |
| \$1B | PDCM_CMD_B_L | PDCM_CMD_B[7] | PDCM_CMD_B[6] | PDCM_CMD_B[5] | PDCM_CMD_B[4] | PDCM_CMD_B[3] | PDCM_CMD_B[2] | PDCM_CMD_B[1] | PDCM_CMD_B[0] | R/W |
| \$1C | PDCM_CMD_B_H | 0 | 0 | 0 | 0 | PDCM_CMD_B[11] | PDCM_CMD_B[10] | PDCM_CMD_B[9] | PDCM_CMD_B[8] | R/W |
| \$1D | SOURCEID | 0 | 0 | 0 | 0 | SOURCEID[3] | SOURCEID[2] | SOURCEID[1] | SOURCEID[0] | R/W |
| \$1E | BUSSW_CTRL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BUSSW_CTRL | R/W |
| \$1F | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | R |
| \$20 | DEVLOCK | LOCK_U | 0 | 0 | 0 | 0 | 0 | 0 | 0 | U,R |
| \$21 | DEVSTAT | RESERVED | DEVRES | OSCTRAIN_ERR | BUSSW | TESTMODE | ST_ACTIVE | OFFSET_ERR | OC_INIT | R |
| \$22 | DEVSTAT2 | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_UNLOCKED | RESERVED | ST_INCMPLT | VBUF_UV_ERR | BUSI_UV_ERR | R |
| \$23 | ST_CONTROL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | ST_5_PTRN | ST_A_PTRN | SELFTEST | R/W |
| \$24 | WRITE_NVM_EN | 0 | 0 | 0 | 0 | 0 | 0 | WR_NVM_EN[1] | WR_NVM_EN[0] | R/W |
| \$25 | C_CRMCRCPLY | C_CRMCRCPLY[7] | C_CRMCRCPLY[6] | C_CRMCRCPLY[5] | C_CRMCRCPLY[4] | C_CRMCRCPLY[3] | C_CRMCRCPLY[2] | C_CRMCRCPLY[1] | C_CRMCRCPLY[0] | R/W |
| \$26 | R_CRMCRCPLY | R_CRMCRCPLY[7] | R_CRMCRCPLY[6] | R_CRMCRCPLY[5] | R_CRMCRCPLY[4] | R_CRMCRCPLY[3] | R_CRMCRCPLY[2] | R_CRMCRCPLY[1] | R_CRMCRCPLY[0] | R/W |
| \$27 | PDCMCRCPLY | PDCMCRCPLY[7] | PDCMCRCPLY[6] | PDCMCRCPLY[5] | PDCMCRCPLY[4] | PDCMCRCPLY[3] | PDCMCRCPLY[2] | PDCMCRCPLY[1] | PDCMCRCPLY[0] | R/W |
| \$28 - \$2F | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | R |
| \$30 | ACC_FCTCFG | 0 | PCM | AXIS | RNG[4] | RNG[3] | RNG[2] | RNG[1] | RNG[0] | F,R |
| \$31 | ACC_STDATA | ACC_ST[7] | ACC_ST[6] | ACC_ST[5] | ACC_ST[4] | ACC_ST[3] | ACC_ST[2] | ACC_ST[1] | ACC_ST[0] | F,R |
| \$32 | ACC_CFG | LPF[3] | LPF[2] | LPF[1] | LPF[0] | SD | OC_FILTER[2] | OC_FILTER[1] | OC_FILTER[0] | R/W |
| \$33 | ACC_DATA1 | ACC_D[7] | ACC_D[6] | ACC_D[5] | ACC_D[4] | ACC_D[3] | ACC_D[2] | ACC_D[1] | ACC_D[0] | R |
| \$34 | ACC_DATAH | ACC_D[15] | ACC_D[14] | ACC_D[13] | ACC_D[12] | ACC_D[11] | ACC_D[10] | ACC_D[9] | ACC_D[8] | R |
| \$35 | ACC_STAT | 0 | 0 | 0 | 0 | 0 | ST_ACTIVE | OFFSET_ERR | OC_INIT | R |

Type codes:

F: Freescale programmed OTP location.

U: User programmable OTP location.

R: Readable register.

R/W: User writable register.

3.1.1 IC Type register

The IC Type register is a read-only register which contains the IC type as defined in the DSI3 standard.

Table 5. IC Type register

| Location | | Bit | | | | | | | |
|----------|----------|-----|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$00 | ICTYPEID | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

3.1.2 IC Manufacturer Identification register

The IC Manufacturer Identification register is a read-only register which contains the IC manufacturer ID as defined in the DSI3 standard.

Table 6. IC Manufacturer Identification register

| Location | | Bit | | | | | | | |
|----------|----------|-----|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$01 | ICMFGID | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

3.1.3 IC Manufacturer Revision register

The IC revision register is a read-only register which contains the IC revision as defined in the DSI3 standard. ICREVID[4] is set to '0' for the MMAx7xxJWR2 part numbers and set to '1' for the MMAx7xxWR2 part numbers.

Table 7. IC Manufacturer Revision register

| Location | | Bit | | | | | | | |
|----------|----------|-----|---|---|------------|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$02 | ICREVID | 0 | 0 | 1 | ICREVID[4] | 0 | 0 | 0 | 0 |

3.1.4 Module Type register (MODTYPE)

The module type register is a user programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in [Section 3.2](#).

Table 8. Module Type register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|---|------------|------------|------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$03 | MODTYPE | 0 | 0 | 0 | 0 | 0 | MODTYPE[2] | MODTYPE[1] | MODTYPE[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.5 Module Manufacturer ID register (MODMFGID)

The module manufacturer identification register is a user-programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in [Section 3.2](#).

Table 9. Module Manufacturer ID register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|---|-------------|-------------|-------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$04 | MODMFGID | 0 | 0 | 0 | 0 | 0 | MODMFGID[2] | MODMFGID[1] | MODMFGID[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.6 Module Revision register (MODREV)

The Module Revision register is a user programmed OTP register which contains user specific module identification information as defined in the DSI3 Standard. The register is included in the user programmed OTP verification described in [Section 3.2](#).

Table 10. Module Revision register (MODREV)

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|---|-----------|-----------|-----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$05 | MODREV | 0 | 0 | 0 | 0 | 0 | MODREV[2] | MODREV[1] | MODREV[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.7 User ID 1 registers (USERID1)

User ID registers 1 is a user programmable OTP register which contains user specific information. The bits have no impact on the device performance. The register is included in the user programmed OTP verification described in [Section 3.2](#).

Table 11. User ID 1 registers

| Location | | Bit | | | | | | | |
|-----------------|----------|------------|------------|------------|------------|------------|------------|------------|------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$06 | USERID1 | USERID1[7] | USERID1[6] | USERID1[5] | USERID1[4] | USERID1[3] | USERID1[2] | USERID1[1] | USERID1[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.8 Part Number register

The Part Number register is a factory-programmed OTP register which includes the numeric portion of the device part number. The register is included in the factory-programmed OTP verification described in [Section 3.2](#). Beyond this, the contents of the part number register have no impact on device operation or performance.

Table 12. Part Number register

| Location | | Bit | | | | | | | |
|-----------------|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$09 | PN | PN[7] | PN[6] | PN[5] | PN[4] | PN[3] | PN[2] | PN[1] | PN[0] |
| Factory Default | | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| PN Register Value | | Range (g) | Transducer |
|-------------------|------|-----------|----------------------------------|
| Decimal | HEX | | |
| 2 | 0x02 | 25 | Medium-g Lateral |
| 12 | 0x0C | 125 | High-g Lateral |
| 18 | 0x12 | 187 | High g Lateral |
| 25 | 0x19 | 250 | High-g Lateral / High-g Vertical |
| 37 | 0x25 | 375 | High-g Lateral |

3.1.9 Device Serial Number registers

The serial number registers are factory-programmed OTP registers which include a unique serial number and lot number combination for each device, regardless of range or axis of sensitivity. Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned. The serial number registers are included in the factory-programmed OTP verification described in [Section 3.2](#). Beyond this, the contents of the serial number registers have no impact on device operation or performance.

Table 13. Device Serial Number registers

| Location | | Bit | | | | | | | |
|-----------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$0A | SN0 | SN[7] | SN[6] | SN[5] | SN[4] | SN[3] | SN[2] | SN[1] | SN[0] |
| \$0B | SN1 | SN[15] | SN[14] | SN[13] | SN[12] | SN[11] | SN[10] | SN[9] | SN[8] |
| \$0C | SN2 | SN[23] | SN[22] | SN[21] | SN[20] | SN[19] | SN[18] | SN[17] | SN[16] |
| \$0D | SN3 | SN[31] | SN[30] | SN[29] | SN[28] | SN[27] | SN[26] | SN[25] | SN[24] |
| Factory Default | | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

The serial number is composed of the following information:

| Bit range | Content |
|-----------|---------------|
| SN[12:0] | Serial Number |
| SN[31:13] | Lot Number |

3.1.10 DSI Protocol Revision register (DSI_REV)

The factory-configuration register is a read-only register which contains the DSI revision supported, as specified in the DSI3 standard. The protocol revision value for DSI3 is \$01.

Table 14. DSI Protocol Revision register

| Location | | Bit | | | | | | | |
|----------|----------|-----|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$10 | DSIREV | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

3.1.11 Physical Address register (PHYSADDR)

The physical address register is a user programmed OTP register which contains the physical address of the slave.

If the physical address is zero, the address is assigned either during Discovery Mode as described in [Section 4.1.3](#) or during Command and Response Mode as described in [Section 4.1.2](#).

If the physical address is non-zero, the device ignores Discovery Mode and uses the programmed physical address for Command and Response Mode, as described in [Section 4.2](#). The physical address register value can be changed by a Command and Response Mode register write command. However, if the LOCK_U bit is set, the value will always be reset to the OTP array value after a reset.

The OTP register value is included in the user programmed OTP verification described in [Section 3.2](#). The value is also stored in a secondary register that can be written as described above. This secondary register is included in the read/write array verification described in [Section 3.2](#).

Table 15. Physical Address register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|----------|----------|----------|----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$11 | PHYSADDR | 0 | 0 | 0 | 0 | PADDR[3] | PADDR[2] | PADDR[1] | PADDR[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.12 DSI3 Background Diagnostic Mode Configuration register (BDM_CFG)

The DSI3 Background Diagnostic Mode configuration register is a user programmed read/write register which contains user specific configuration information for DSI3 Background Diagnostic Mode. The register is included in the read/write array verification described in [Section 3.2](#). Reference [Section 4.3](#) for details regarding Background Diagnostic Mode.

Table 16. DSI3 Background Diagnostic Mode Configuration register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|---|---|---|--------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$12 | BDM_CFG | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BDM_EN |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.12.1 Background Diagnostic Mode Enable (BDM_EN)

The Background Diagnostic Mode enable bit enables Background Diagnostic Mode as described below and in [Section 3.1.14](#). Reference [Section 4.3](#) for details regarding Background Diagnostic Mode.

| BDM_EN | BDM command fragment length |
|--------|-----------------------------|
| 0 | Disabled |
| 1 | 4 |

3.1.13 DSI3 Command and Response Mode Configuration register (CRM_CFG)

The DSI3 Command and Response Mode configuration register is a user programmed read/write register which contains user specific configuration information for DSI3 Command and Response Mode. The register is included in the read/write array verification described in [Section 3.2](#).

Table 17. DSI3 Command and Response Mode Configuration register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|------------|------------|------------|-----------|-------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$13 | CRM_CFG | 0 | 0 | 0 | CK_CAL_RST | CRM_PER[1] | CRM_PER[0] | CK_CAL_EN | SS_EN |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.13.1 Clock Calibration Value Reset (CK_CAL_RST)

The clock calibration reset bit controls the state of the oscillator training when the CK_CAL_EN bit is cleared as described in the table in [Section 3.1.13.3](#). Reference [Section 3.4.1](#) for details regarding oscillator training.

3.1.13.2 Command and Response Mode Period (CRM_PER[1:0])

The Command and Response Mode Period bits set the period for Command and Response Mode commands in increments of the Periodic Data Collection Mode Period (PDCM_PER). This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the CRM_CFG register. Command and Response Mode commands will be decoded and responded to regardless of the value of this register as long as the general Command and Response Mode timing parameters specified in [Section 2.6](#) are met. Reference [Section 3.4.1](#) for details regarding oscillator training.

| CRM_PER[1] | CRM_PER[0] | Command and Response Mode period (Multiples of the Periodic Data Collection Mode period) |
|------------|------------|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

3.1.13.3 Clock Calibration Enable (CK_CAL_EN)

The clock calibration enable bit enables oscillator training over the DSI communication interface. Reference [Section 3.4.1](#) for details regarding oscillator training.

| CK_CAL_EN | CK_CAL_RST | Oscillator training |
|-----------|------------|--|
| 0 | 0 | The oscillator value is maintained at the last trained value prior to clearing the CK_CAL_RST bit. |
| 0 | 1 | The oscillator value is reset to the untrained value with a tolerance specified in Section 2.8 . |
| 1 | x | Oscillator is trained as specified in Section 3.4.1 |

3.1.13.4 Simultaneous Sampling Enable (SS_EN)

The simultaneous sampling enable bit selects between one of two data latency methods. Reference [Section 3.7](#) for details regarding sample timing.

| SS_EN | Data latency |
|-------|---|
| 0 | Synchronous Sampling Mode: Latency relative to transmission start time (PDCM_RSPST) |
| 1 | Simultaneous Sampling Mode: Latency relative to the start of the Periodic Data Collection Mode command (falling edge) |

3.1.14 Periodic Data Collection Mode Enable register (PDCM_EN)

The Periodic Data Collection Mode register is a read/write register which contains the Periodic Data Collection Mode Enable bit. The register is included in the read/write array verification described in [Section 3.2](#).

Table 18. Periodic Data Collection Mode Enable register

| Location | | Bit | | | | | | | |
|-----------------|----------|---------|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$15 | PDCM_EN | PDCM_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Periodic Data Collection Mode Enable bit enables Periodic Data Collection Mode as described in [Section 4.3](#). The PDCM_EN bit can be set by receiving the Enter PDCM command in Command and Response Mode, or by a Command and Response Mode register write command. Once Periodic Data Collection Mode is enabled, the registers listed in [Section 3.2.3](#) are locked and the user array read/write register array verification is enabled.

Once set, the PDCM_EN bit can only be cleared by a device reset.

| PDCM_EN | BDM_EN | Command and Response Mode | Periodic Data Collection Mode | Background Diagnostic Mode |
|---------|--------|---------------------------|-------------------------------|----------------------------|
| 0 | 0 | Enabled | Disabled | Disabled |
| 0 | 1 | Enabled | Disabled | Disabled |
| 1 | 0 | Disabled | Enabled | Disabled |
| 1 | 1 | Disabled | Enabled | Enabled |

3.1.15 DSI3 Periodic Data Collection Mode Configuration registers (PDCM_CFG1, PDCM_CFG2)

The DSI3 Periodic Data Collection Mode configuration registers are user programmed read/write registers which contain user specific configuration information for DSI3 Periodic Data Collection Mode. The registers are included in the read/write array verification described in [Section 3.2](#).

| Location | | Bit | | | | | | | |
|-----------------|--------------|---------------|---------------|---------------|---------------|----------------|----------------|---------------|---------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$14 | PDCM_CFG | 0 | 0 | 0 | 0 | 0 | 0 | DATALENGTH | STATLENGTH |
| \$16 | CHIPTIME | 0 | 0 | 0 | 0 | 0 | CHIPTIME[2] | CHIPTIME[1] | CHIPTIME[0] |
| \$17 | PDCM_PER | 0 | 0 | 0 | 0 | 0 | PDCM_PER[2] | PDCM_PER[1] | PDCM_PER[0] |
| \$18 | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| \$19 | PDCM_RSPST_L | PDCM_RSPST[7] | PDCM_RSPST[6] | PDCM_RSPST[5] | PDCM_RSPST[4] | PDCM_RSPST[3] | PDCM_RSPST[2] | PDCM_RSPST[1] | PDCM_RSPST[0] |
| \$1A | PDCM_RSPST_H | 0 | 0 | 0 | 0 | PDCM_RSPST[11] | PDCM_RSPST[10] | PDCM_RSPST[9] | PDCM_RSPST[8] |
| \$1B | PDCM_CMD_B_L | PDCM_CMD_B[7] | PDCM_CMD_B[6] | PDCM_CMD_B[5] | PDCM_CMD_B[4] | PDCM_CMD_B[3] | PDCM_CMD_B[2] | PDCM_CMD_B[1] | PDCM_CMD_B[0] |
| \$1C | PDCM_CMD_B_H | 0 | 0 | 0 | 0 | PDCM_CMD_B[11] | PDCM_CMD_B[10] | PDCM_CMD_B[9] | PDCM_CMD_B[8] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.15.1 Data Field Length (DATALENGTH)

The data field length bits set the data field length in the Periodic Data Collection Mode response as described below. The sensitivity of the data is the same for both the 10-bit and 14-bit data lengths. If the 14-bit data length is selected, four additional bits of range are transmitted. These additional four bits of range are intended for test use only and are not covered by the specifications listed in [Section 2](#).

| DATALENGTH | Data Length |
|------------|-------------|
| 0 | 10 Bits |
| 1 | 14 Bits |

3.1.15.2 Status Field Length (STATLENGTH)

The status field length bits set the status field length in the Periodic Data Collection Mode response as described below. Reference [Section 4.3.2.2](#) for details regarding the Periodic Data Collection Mode status field.

| STATLEN | Status Field Length (Bits) | Data Transmitted |
|---------|----------------------------|---|
| 0 | 4 | Reference Section 4.3.2.2 |
| 1 | 0 | N/A |

3.1.15.3 Chip time (CHIPTIME)

The DSI3 Periodic Data Collection Mode configuration chip time bits set the chip time for Periodic Data Collection Mode as described below.

| CHIPTIME[2] | CHIPTIME[1] | CHIPTIME[0] | Chip time |
|-------------|-------------|-------------|-------------|
| 0 | 0 | 0 | 3.0 μ s |
| 0 | 0 | 1 | 3.5 μ s |
| 0 | 1 | 0 | 4.0 μ s |
| 0 | 1 | 1 | 4.5 μ s |
| 1 | 0 | 0 | 5.0 μ s |
| 1 | 0 | 1 | 5.5 μ s |
| 1 | 1 | 0 | 6.0 μ s |
| 1 | 1 | 1 | 6.5 μ s |

3.1.15.4 Periodic Data Collection Mode Period (PDCM_PER[3:0])

The Periodic Data Collection Mode period selection bits set the period data collection mode period to be used by the DSI master as shown in the table below. This value is only necessary for oscillator training and is only used if the CK_CAL_EN bit is set in the CRM_CFG register. Periodic Data Collection Mode and Background Diagnostic Mode commands will be decoded and responded to regardless of the value of this register as long as the general Periodic Data Collection Mode timing parameters specified in Section 2.6 are met. Reference Section 3.4.1 for details regarding oscillator training.

| PDCM_PER[2] | PDCM_PER[1] | PDCM_PER[0] | Periodic Data Collection Mode Period |
|-------------|-------------|-------------|--------------------------------------|
| 0 | 0 | 0 | 500 μ s |
| 0 | 0 | 1 | 125 μ s |
| 0 | 1 | 0 | 250 μ s |
| 0 | 1 | 1 | 333 μ s |
| 1 | 0 | 0 | 500 μ s |
| 1 | 0 | 1 | 1000 μ s |
| 1 | 1 | 0 | 2000 μ s |
| 1 | 1 | 1 | 4000 μ s |

3.1.15.5 Periodic Data Collection Mode Response Start Time (PDCM_RSPST[11:0])

The DSI3 Periodic Data Collection Mode Response Start Time bits set the Periodic Data Collection Mode response start time. The value is stored in 1 μ s increments, with zero as the default value of 20 μ s.

Care must be taken to prevent from programming response start times which cause data contention in the system.

| PDCM_RSPST[11:0] | Periodic Data Collection Mode Response Start Time |
|------------------|---|
| 0 - 20 | 20 μ s |
| 21 - 4095 | PDCM response start = PDCM_RSPST x 1 μ s |

3.1.15.6 Periodic Data Collection Mode Command Blocking time (PDCM_CMD_B[11:0])

The DSI3 Periodic Data Collection Mode command blocking time bits set the Periodic Data Collection Mode command blocking time. in 1 μ s increments, with zero as the default value of 450 μ s. Reference Section 3.6.1 for details regarding the command receiver and command blocking.

Care must be taken to prevent from programming command blocking times which prevent proper command decoding in the system and to ensure proper sampling of the V_{HIGH} voltage. As shown in Section 3.6.1, Figure 29, The V_{HIGH} voltage is initially captured at the end of the command blocking time and then filtered. The user must ensure that the command blocking end time is set for a time when no command or response transmissions are occurring to provide the most stable BUS_I voltage.

| PDCM_CMD_B[11:0] | Periodic Data Collection Mode Command blocking time |
|------------------|---|
| 0 | 450 μ s |
| Non-Zero | PDCM Command blocking time = PDCM_CMD_B x 1 μ s |

3.1.16 Source Identification register (SOURCEID)

The source identification register is a user programmed read/write register which contains the source identification which will be used for Periodic Data Collection Mode as described in Section 4.3.2.2. The register is included in the read/write array verification described in Section 3.2. SOURCEID[3:0] is initialized to the values stored in PADDR[3:0] after reset.

Table 19. Source Identification register

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|-------------|-------------|-------------|-------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$1D | SOURCEID | 0 | 0 | 0 | 0 | SOURCEID[3] | SOURCEID[2] | SOURCEID[1] | SOURCEID[0] |
| Factory Default | | 0 | 0 | 0 | 0 | PADDR[3] | PADDR[2] | PADDR[1] | PADDR[0] |

3.1.17 Bus Switch Control register (BUSSW_CTRL)

The bus switch control register is a user programmed read/write register which controls the state of the bus switch output driver. The register is included in the read/write array verification describe in [Section 3.2](#).

Table 20. Bus Switch Control register

| Location | | Bit | | | | | | | |
|-----------------|------------|-----|---|---|---|---|---|---|------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$1E | BUSSW_CTRL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BUSSW_CTRL |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The BUSSW_CTRL bit controls the state of the BUSSW pin.

| BUSSW_CTRL | BUSSW Pin Sate |
|------------|---|
| 0 | High impedance An External Pullup is required if an external switch is connected |
| 1 | Output Actively Driven Low |

3.1.18 Device Lock register (DEVLOCK)

The device lock register is a user programmed OTP register which contains the LOCK_U bit. The register is included in the user programmed OTP verification describe in [Section 3.2](#). The LOCK_U bit allows the user to prevent writes to the user configuration array once OTP programming is complete. If the LOCK_U bit is written to '1' when an "Execute Programming of NVM" command is executed, the LOCK_U OTP bit will be programmed. Upon completion of the OTP programming, future OTP writes to both the OTP array and the mirror registers for the array are prevented and the User Programmable OTP Array Verification is activated. The exception to this is the PADDR[3:0] bits. Once the LOCK_U bit is set, the PADDR[3:0] OTP bits cannot be written. However, the mirror register bits for PADDR[3:0] can be written to allow changes to the physical address through Command and Response Mode.

Table 21. Device Lock register

| Location | | Bit | | | | | | | |
|-----------------|----------|--------|---|---|---|---|---|---|---|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$20 | DEVLOCK | LOCK_U | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.19 Device Status registers (DEVSTAT, DEVSTAT2)

The device status registers are read-only registers which contain device status information.

Table 22. Device Status registers

| Location | | Bit | | | | | | | |
|----------|----------|-----------|-----------|-------------|------------|----------|------------|-------------|--------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$21 | DEVSTAT | RESERVED | DEVRES | OSCTRIN_ERR | BUSSW | TESTMODE | ST_ACTIVE | OFFSET_ERR | OC_INIT |
| \$22 | DEVSTAT2 | F_OTP_ERR | U_OTP_ERR | U_RW_ERR | U_UNLOCKED | RESERVED | ST_INCMPLT | VBUF_UV_ERR | BUSIN_UV_ERR |

3.1.19.1 Device Reset (DEVRES)

The device reset bit is set following a device reset. The device reset bit is cleared only by a read of the DEVSTAT register.

| DEVRES | Error Condition |
|--------|-----------------------|
| 0 | Normal operation |
| 1 | Device reset occurred |

3.1.19.2 Oscillator Training Error (OSCTRAIN_ERR)

The oscillator training error bit is set if an error detected in either the oscillator training settings, or the master communication timing. Reference [Section 3.4.2](#).

| OSCTRAIN_ERR | Error Condition |
|--------------|--|
| 0 | No error detected |
| 1 | Oscillator Training Error. Reference Section 3.4.2 |

3.1.19.3 Bus Switch Status (BUSSW)

The Bus Switch status bit is set if the bus switch output pin is activated.

| BUSSW | BUSSW Pin State |
|-------|-----------------------|
| 0 | BUSSW pin is inactive |
| 1 | BUSSW pin is active |

3.1.19.4 Test Mode (TESTMODE)

The test mode bit is set if the device is in test mode.

| TESTMODE | Operating Mode |
|----------|-------------------------|
| 0 | Test Mode is not active |
| 1 | Test Mode is active |

3.1.19.5 Self-Test Active (ST_ACTIVE)

The self-test active bit is set if any of the self-test bits in the ST_CONTROL register are set.

| ST_ACTIVE | Condition |
|-----------|--------------------------------------|
| 0 | ST_5_PTRN & ST_A_PTRN & SELFTEST = 0 |
| 1 | ST_5_PTRN ST_A_PTRN SELFTEST = 1 |

3.1.19.6 Offset Error Flag (OFFSET_ERR)

The offset error flag is set if the acceleration signal reaches the offset limit.

| OFFSET_ERR | Error Condition |
|------------|-----------------------|
| 0 | No error detected |
| 1 | Offset error detected |

3.1.19.7 Offset Cancellation Init Status Flag (OC_INIT)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

| OC_INIT | Error Condition |
|---------|---|
| 0 | Offset Cancellation in initialization |
| 1 | Offset Cancellation initialization complete |

3.1.19.8 Freescale OTP Array Error (F_OTP_ERR)

The factory OTP array error bit is set if a register data fault is detected in the factory OTP array. A device reset is required to clear the error.

| F_OTP_ERR | Error Condition |
|-----------|---|
| 0 | No error detected |
| 1 | Error Detected in the Factory OTP Array |

3.1.19.9 User OTP Array Error (U_OTP_ERR)

The user OTP array error bit is set if a register data fault is detected in the user OTP array. A device reset is required to clear the error.

| U_OTP_ERR | Error Condition |
|-----------|--------------------------------------|
| 0 | No error detected |
| 1 | Error Detected in the User OTP Array |

3.1.19.10 User Read/Write Array Error (U_RW_ERR)

The user read/write array error bit is set if a register data fault is detected in the user read/write array. A device reset is required to clear the error.

| U_RW_ERR | Error Condition |
|----------|---|
| 0 | No error detected |
| 1 | Error Detected in the User Read/Write Array |

3.1.19.11 User OTP Array Unlocked (U_UNLOCKED)

The user OTP array unlocked bit is set if LOCK_U bit in the DEVLOCK register is not set, indicating that the user array is not locked.

| U_UNLOCKED | Condition |
|------------|--------------------------|
| 0 | User Array is Locked |
| 1 | User Array is not Locked |

3.1.19.12 Self-Test Incomplete (ST_INCMPLT)

The self-test incomplete bit is set after a device reset and is only cleared when the SELFTTEST bit is written to a '1' through Command and Response Mode.

| ST_INCMPLT | Condition |
|------------|---|
| 0 | Self-test has been activated since the last Reset |
| 1 | Self-test has not been activated since the last Reset |

3.1.19.13 V_{BUF} Undervoltage Error (VBUF_UV_ERR)

The V_{BUF} undervoltage error bit is set if the V_{BUF} voltage falls below the voltage specified in [Section 2.3](#). Reference [Section 3.3](#) for details on the V_{BUF} undervoltage monitor. The VBUF_UV_ERR bit is cleared on a read of the DEVSTAT2 register.

| VBUF_UV_ERR | Error Condition |
|-------------|-------------------|
| 0 | No error detected |
| 1 | VBUF Voltage Low |

3.1.19.14 BUS IN Undervoltage Error (BUSI_UV_ERR)

The BUS IN undervoltage error bit is set if the BUS_I voltage falls below the voltage specified in [Section 2.3](#). Reference [Section 3.3](#) for details on the BUS IN undervoltage monitor. The BUSI_UV_ERR bit is cleared on a read of the DEVSTAT2 register.

| BUSI_UV_ERR | Error Condition |
|-------------|-------------------|
| 0 | No error detected |
| 1 | BUS_I Voltage Low |

3.1.20 Self-Test Control register (ST)

The self-test control register is a user programmed read/write register which contains user specific device configuration information. The register is included in the read/write array verification described in [Section 3.2](#).

Table 23. Self-Test Control register

| Location | | Bit | | | | | | | |
|-----------------|------------|----------|----------|----------|----------|----------|-----------|-----------|----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$23 | ST_CONTROL | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | ST_PTRN_5 | ST_PTRN_A | SELFTEST |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.20.1 Self-Test Pattern Write Bits (ST_PTRN_5, ST_PTRN_A)

The self-test pattern write bits inhibit DSP writes to the ACC_DATAH and ACC_DATAH registers and forces a write of specific values to the registers when set. When cleared, DSP writes to the ACC_DATAH and ACC_DATAH registers resume as specified. These bits are automatically cleared when the PDCM bit is set.

| ST_PTRN_A | ST_PTRN_5 | Function |
|-----------|-----------|--|
| 0 | 0 | DSP writes to the ACC_DATAH and ACC_DATAH registers as specified |
| 0 | 1 | 0x5555 written to ACC_DATAH and ACC_DATAH. DSP write to registers inhibited. |
| 1 | 0 | 0xAAAA written to ACC_DATAH and ACC_DATAH. DSP write to registers inhibited. |
| 1 | 1 | 0xFFFF written to ACC_DATAH and ACC_DATAH. DSP write to registers inhibited. |

3.1.20.2 Self-Test Control (SELFTEST)

The self-test control bit activates and deactivates self-test as described below. Reference [Section 3.5.2](#) for details regarding self-test. This bit is automatically cleared when the PDCM bit is set.

| Self-test | Function |
|-----------|-----------------------|
| 0 | Self-test deactivated |
| 1 | Self-test activated |

After a device reset, the ST_INCMPLT bit is set in the DEVSTAT2 register and the device status defaults to Self-test Activation Incomplete as defined in [Section 4.3.2.2](#). The ST_INCMPLT bit will only be cleared by writing the SELFTEST bits to '1' through Command and Response Mode. If PDCM is entered without activating self-test, the status bits will include the Self-test Activation Incomplete" status until a device reset.

If both the SELFTEST bit and one of the Self-test Pattern Write bits are set, the self-test pattern data will be written to the ACC_DATAH and ACC_DATAH registers. However, the transducer self-test will still be activated as described in [Section 3.5.2](#).

3.1.21 Write NVM Enable register

The write NVM enable register is a user programmed read/write register that allows the user to write the contents of the user programmed OTP array mirror registers to the OTP registers. The register is included in the read/write array verification described in [Section 3.2](#).

Table 24. Write NVM Enable register

| Location | | Bit | | | | | | | |
|-----------------|--------------|-----|-----|-----|-----|-----|-----|--------------|--------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$24 | WRITE_NVM_EN | 0 | 0 | 0 | 0 | 0 | 0 | WR_NVM_EN[1] | WR_NVM_EN[0] |
| Factory Default | | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

DSI3 Register Writes executed by the user to the user programmed OTP array only update the mirror register contents for the OTP array, not the actual OTP registers. To copy the values to the actual OTP registers, a series of three consecutive DSI3 Register Write operations to the Write NVM Enable register must be completed. The register write operations must be consecutive and in the order shown below to enable the write to NVM. If any commands are transmitted in between the listed commands, or if the data does not match as shown, the sequence will be reset and no OTP write will be initiated.

Depending upon the operating mode used, the user will need to write the NVM values to OTP either with or without the PHYSADDR register being written to OTP. If Discovery Mode or switch connected daisy-chain mode will be used, the PHYSADDR register must remain unprogrammed (0x0000). If a preprogrammed bus mode will be used, the PHYSADDR register must be programmed to a non-zero value. To support these two user modes, two NVM Write sequences are necessary: one that allocates the PHYSADDR register to OTP and one that does not.

All user array programming, including locking the user array by setting the LOCK_U bit, must be completed with one NVM Write command sequence in order to prevent inadvertent user array ECC errors. The procedure for writing to the user OTP array is listed below:

1. Write the desired values to the user array registers using Command and Response Mode.
2. Set the LOCK_U bit in the DEVLOCK registers using Command and Response Mode.

NOTE

This procedure must only be executed once and the LOCK_U bit must be set to prevent inadvertent ECC errors.

3. Execute the appropriate NVM Write Sequence using Command and Response Mode to copy the register data to the OTP array with or without the PHYSADDR register.

Table 25. NVM Write Sequence: PHYSADDR register conditionally included

| Register Write to WRITE_NVM_EN | WRITE_NVM_EN[7:2] | WRITE_NVM_EN[1] | WRITE_NVM_EN[0] | Effect |
|--------------------------------|-------------------|-----------------|-----------------|---|
| DSI3 Register Write 1 | 0 0 0 0 0 0 | 1 | 0 | No Effect |
| DSI3 Register Write 2 | 0 0 0 0 0 0 | 1 | 1 | No Effect |
| DSI3 Register Write 3 | 0 0 0 0 0 0 | 0 | 1 | Write to OTP initiated PHYSADDR Register included if and only if assigned by CRM |

Table 26. NVM Write Sequence: PHYSADDR register excluded

| Register Write to WRITE_NVM_EN | WRITE_NVM_EN[7:2] | WRITE_NVM_EN[1] | WRITE_NVM_EN[0] | Effect |
|--------------------------------|-------------------|-----------------|-----------------|---|
| DSI3 Register Write 1 | 0 0 0 0 0 0 | 0 | 1 | No Effect |
| DSI3 Register Write 2 | 0 0 0 0 0 0 | 1 | 1 | No Effect |
| DSI3 Register Write 3 | 0 0 0 0 0 0 | 1 | 0 | Write to OTP initiated PHYSADDR Register is excluded |

4. Delay $t_{NVM_WRITE_MAX}$ to allow the device to complete the writes to OTP.
5. Verify that the OTP write has successfully completed by completing a read back of all of the OTP registers using Command and Response Mode Register Read commands.

3.1.22 DSI3 Communication CRC Polynomial registers

The DSI3 communication CRC polynomial registers are user programmed read/write registers which contain the CRC polynomials used for communication. The register is included in the read/write array verification described in [Section 3.2](#).

Table 27. DSI3 Communication CRC Polynomial registers

| Location | | Bit | | | | | | | |
|-----------------|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$25 | C_CRMCRCPLY | C_CRMCRCPLY[7] | C_CRMCRCPLY[6] | C_CRMCRCPLY[5] | C_CRMCRCPLY[4] | C_CRMCRCPLY[3] | C_CRMCRCPLY[2] | C_CRMCRCPLY[1] | C_CRMCRCPLY[0] |
| \$26 | R_CRMCRCPLY | R_CRMCRCPLY[7] | R_CRMCRCPLY[6] | R_CRMCRCPLY[5] | R_CRMCRCPLY[4] | R_CRMCRCPLY[3] | R_CRMCRCPLY[2] | R_CRMCRCPLY[1] | R_CRMCRCPLY[0] |
| \$27 | PDCMCRCPY | PDCMCRCPY[7] | PDCMCRCPY[6] | PDCMCRCPY[5] | PDCMCRCPY[4] | PDCMCRCPY[3] | PDCMCRCPY[2] | PDCMCRCPY[1] | PDCMCRCPY[0] |
| Factory Default | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

The C_CRMCRCPLY register contains the 8-bit CRC polynomial used for the Command and Response Mode command as well as the Background Diagnostic Mode command. The default polynomial is $x^8 + x^5 + x^3 + x^2 + x + 1$. When this register value is changed using a Command and Response Mode Register Write command, the new polynomial value is enabled for the next Command and Response Mode command received.

The R_CRMCRCPLY register contains the 8-bit CRC polynomial used for the Command and Response Mode response as well as the Background Diagnostic Mode response. The default polynomial is $x^8 + x^5 + x^3 + x^2 + x + 1$. When this register value is changed using a Command and Response Mode Register Write command, the new polynomial value is enabled for the response to the next Command and Response Mode command received. The response to the Register Write command uses the original polynomial value.

The PDCMCRCPY register contains the 8-bit CRC polynomial used for the Periodic Data Collection Mode response. The default polynomial is $x^8 + x^5 + x^3 + x^2 + x + 1$. This polynomial is enabled once the device enters Periodic Data Collection Mode as described in [Section 4.3](#).

3.1.23 Acceleration Factory Configuration register (ACC_FCTCFG)

The Acceleration Factory Configuration register is a factory-programmable OTP register which contains acceleration data specific configuration information. The register is included in the factory-programmed OTP verification. Reference [Section 3.2](#) for details regarding the OTP verification.

Table 28. Acceleration Factory Configuration register (ACC_FCTCFG)

| Location | | Bit | | | | | | | |
|-----------------|------------|-----|-----|------|--------|--------|--------|--------|--------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$30 | ACC_FCTCFG | 0 | PCM | AXIS | RNG[4] | RNG[3] | RNG[2] | RNG[1] | RNG[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.23.1 PCM Enable Bit (PCM)

The PCM bit enables the PCM output pin. When the PCM bit is set, the PCM output pin is active and outputs a pulse code modulated signal proportional to the acceleration response. Reference [Section 3.5.4.10](#) for more information regarding the PCM output. When the PCM bit is cleared, the PCM output pin is actively pulled low.

| PCM | PCM Output |
|-----|---------------------|
| 0 | Actively pulled low |
| 1 | PCM signal enabled |

3.1.23.2 Axis Indication Bit (AXIS)

The axis indication bit indicates the axes of sensitivity as shown below.

| AXIS | Axis |
|------|------|
| 0 | X |
| 1 | Z |

3.1.23.3 Range Indication Bits (RNG[4:0])

The range indication bits indicate the full-scale range of the device as shown below.

| RNG[4] | RNG[3] | RNG[2] | RNG[1] | RNG[0] | Full-Scale Acceleration Range |
|--------|--------|--------|--------|--------|-------------------------------|
| 0 | 0 | 1 | 1 | 0 | ±25 g |
| 1 | 0 | 1 | 0 | 0 | ±125 g |
| 1 | 0 | 1 | 1 | 0 | ±187 g |
| 1 | 1 | 0 | 0 | 1 | ±250 g |
| 1 | 1 | 1 | 0 | 0 | ±375 g |

3.1.24 Self-Test Deflection register (ACC_STDATA)

The self-test deflection register is a factory-programmable OTP register which contains the nominal self-test deflection value at 25°C. The register is included in the factory-programmed OTP verification described in [Section 3.2](#).

Table 29. Self-Test Deflection register

| Location | | Bit | | | | | | | |
|----------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$31 | ACC_STDATA | ACC_ST[7] | ACC_ST[6] | ACC_ST[5] | ACC_ST[4] | ACC_ST[3] | ACC_ST[2] | ACC_ST[1] | ACC_ST[0] |

The self-test value is a positive deflection value, measured at the factory, and factory-programmed for each device. The stored value is equal to the difference between the factory measured value at nominal temperature and the minimum self-test limit at 25°C ($ACC_STDATA = ST_{MEASURED} - \Delta ST_{MIN}$). When self-test is activated, the acceleration reading is compared to the value in this register. The difference from the measured deflection value, and the nominal deflection value stored in the register shall not fall outside the self-test accuracy limits specified in [Section 2.5](#) (ΔST_{ACC}). Reference [Section 3.5.2](#) for more details on calculating the self-test limits.

3.1.25 Acceleration Configuration register (ACC_CFG)

The acceleration configuration register is a user programmable read/write register which contains acceleration data specific configuration information. The register is included in the read/write array verification described in [Section 3.2](#).

Table 30. Acceleration Configuration register (ACC_CFG)

| Location | | Bit | | | | | | | |
|-----------------|----------|--------|--------|--------|--------|----|------------|------------|------------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$32 | ACC_CFG | LPF[3] | LPF[2] | LPF[1] | LPF[0] | SD | OC_FILT[2] | OC_FILT[1] | OC_FILT[0] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.25.1 Low-pass filter selection bits (LPF[3:0])

The low-pass filter selection bits select the low-pass filter for the acceleration signal. Reference [Section 3.5.4.3](#) for details regarding the low-pass filter.

| LPF[3] | LPF[2] | LPF[1] | LPF[0] | Low-pass filter selected |
|--------|--------|--------|--------|--------------------------|
| 0 | 0 | 0 | 0 | 180 Hz, 2 Pole |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | Reserved |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | 325 Hz, 3 Pole |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | 400 Hz, 3 Pole |
| 1 | 0 | 0 | 1 | 400 Hz, 4 Pole |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 800 Hz, 4 Pole |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | 1200 Hz, 4 Pole |
| 1 | 1 | 1 | 1 | Reserved |

3.1.25.2 \overline{SD} Bit

The \overline{SD} bit determines the format of acceleration data. If the \overline{SD} bit is set to a logic '1', unsigned results are transmitted. If the \overline{SD} bit is cleared, signed results are transmitted. Reference [Section 3.5.4.9](#) for details on signed and unsigned data.

| SD | Operating mode |
|----|----------------------|
| 1 | Unsigned Data Output |
| 0 | Signed Data Output |

3.1.25.3 Offset cancellation filter selection bits (OC_FILT[2:0])

The offset cancellation filter selection bits select the high-pass filter and rate limiting used for normal operation. Reference [Section 3.5.4.5](#) for details regarding offset cancellation.

| OC_FILT[2] | OC_FILT[1] | OC_FILT[0] | High-pass filter | Rate limiting |
|------------|------------|------------|----------------------|---------------|
| 0 | 0 | 0 | 0.10 Hz, Single Pole | Enabled |
| 0 | 0 | 1 | 0.10 Hz, Single Pole | Bypassed |
| 0 | 1 | 0 | Reserved | Reserved |
| 0 | 1 | 1 | Reserved | Reserved |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | None | NA |
| 1 | 1 | 1 | None | NA |

3.1.26 Acceleration Data registers (ACC_DATAL, ACC_DATAH)

The Acceleration Data registers are read-only registers which contain the 16-bit output acceleration data. A read of the ACC_DATAL register responds with the data from both the ACC_DATAH and ACC_DATAL registers. If all 16-bits of data are desired, it is recommended to read the ACC_DATAL register and to use all 16-bits of the response data.

A read of the either register does not freeze the value of the other register. Thus, subsequent register reads will result in invalid data when re-assembled into a 16-bit value.

Reference [Section 3.5.4.8](#) for details regarding the 16-bit acceleration data.

Table 31. Acceleration Data registers (ACC_DATAL, ACC_DATAH)

| Location | | Bit | | | | | | | |
|-----------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$33 | ACC_DATAL | ACC_D[7] | ACC_D[6] | ACC_D[5] | ACC_D[4] | ACC_D[3] | ACC_D[2] | ACC_D[1] | ACC_D[0] |
| \$34 | ACC_DATAH | ACC_D[15] | ACC_D[14] | ACC_D[13] | ACC_D[12] | ACC_D[11] | ACC_D[10] | ACC_D[9] | ACC_D[8] |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.27 Acceleration Status register (ACC_STAT)

The acceleration status register is a read-only register which contains acceleration data specific status information.

Table 32. Acceleration Status register (ACC_STAT)

| Location | | Bit | | | | | | | |
|-----------------|----------|-----|---|---|---|---|-----------|------------|---------|
| Address | Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| \$35 | ACC_STAT | 0 | 0 | 0 | 0 | 0 | ST_ACTIVE | OFFSET_ERR | OC_INIT |
| Factory Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

3.1.27.1 Self-Test Active Flag (ST_ACTIVE)

The self-test active bit is set if any of the self-test bits in the ST_CONTROL register are set.

| ST_ACTIVE | Condition |
|-----------|---------------------------------------|
| 0 | ST_5_PTRN & ST_A_PTRN & SELFTTEST = 0 |
| 1 | ST_5_PTRN ST_A_PTRN SELFTTEST = 1 |

3.1.27.2 Offset Error Flag (OFFSET_ERR)

The offset error flag is set if the acceleration signal reaches the offset limit.

| OFFSET_ERR | Error Condition |
|------------|-----------------------|
| 0 | No error detected |
| 1 | Offset error detected |

3.1.27.3 Offset Cancellation Init Status Flag (OC_INIT)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

| OC_INIT | Error Condition |
|---------|---|
| 0 | Offset Cancellation in initialization |
| 1 | Offset Cancellation initialization complete |

3.1.28 Reserved Registers

A register read command to a reserved register or a register with reserved bits will result in a valid response. The data for reserved bits may be '0' or '1'.

A register write command to a reserved register or a register with reserved bits will execute and result in a valid response. The data for the reserved bits may be '0' or '1'. A write to the reserved bits must always be '0' for normal device operation and performance.

3.1.29 Invalid Register Addresses

A register read command to a register address outside of the addresses listed in [Table 4](#) will result in a valid response. The data for the registers will be '0x00'.

A register write command to a register address outside of the addresses listed in [Table 4](#) will not execute, but will result in a valid response. The data for the registers will be '0x00'.

A register write command to a read-only register will not execute, but will result in a valid response. The data for the registers will be the current contents of the register.

3.2 OTP and Read/Write register array CRC verification

3.2.1 Factory-programmed OTP array lock and verification

The factory-programmed OTP array is verified for errors with an error detection algorithm. The error verification is enabled only when the factory-programmed array is locked.

Once enabled, the verification is continuously calculated on all bits in the registers listed below as well as on the factory-programmable device configuration bits with the exception of the factory lock bit. If an error is detected in the OTP array, the F_OTP_ERR is set in the DEVSTAT2 register.

| Register Address | Register Name |
|------------------|--------------------|
| \$09 | PN |
| \$0A - \$0D | SN0, SN1, SN2, SN3 |
| \$30 | ACC_FCTCFG |
| \$31 | ACC_STDATA |

The verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.2 User Programmable OTP Array Lock and Error Verification

The User Programmable OTP array is independently verified for errors with an error detection algorithm. The verification is enabled only when the User Programmable OTP array is locked.

Once the LOCK_U bit is active, the verification is continuously calculated on the user programmable OTP Array, which includes the registers listed below. If an error is detected in the OTP array, the U_OTP_ERR is set in the DEVSTAT2 register.

| Register Address | Register Name | Number of Bits |
|------------------|--|----------------|
| \$03 - \$05 | MODTYPE[2:0], MODMFGID[2:0], MODREV[2:0] | 9 |
| \$06 | USERID[7:0] | 8 |
| \$11 | PHYSADDR[3:0] | 4 |
| \$20 | DEVLOCK[7] | 1 |

The verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.3 User Programmable Read/Write Array Lock and CRC Verification

The User Programmable read/write array is independently verified for errors with an error detection algorithm. The verification is enabled only when the PDCM_EN bit is set in the PDCM_EN register.

Once the PDCM_EN bit is set, register writes are ignored and the verification is continuously calculated on the user programmable read/write array, which includes the registers listed below. If an error is detected in the array, the U_RW_ERR is set in the DEVSTAT2 register.

| Register Address | Register Name |
|------------------|---|
| \$11 | PHYSADDR[3:0] - Secondary Register written during Discovery Mode and/or CRM |
| \$12 - \$1E | BDM_CFG, CRM_CFG, PDCM_CFG, PDCM_EN, CHIPTIME, PDCM_PER_L, PDCM_PER_H, PDCM_RSPST_L, PDCM_RSPST_H, PDCM_CMD_B_L, PDCM_CMD_B_H, SOURCEID, BUSSW_CTRL |
| \$23 | ST_CONTROL |
| \$24 | WRITE_NVM_EN |
| \$25 - \$27 | C_CRMCRCPLY, R_CRMCRCPLY, PDCMCRCPLY |
| \$32 | ACC_CFG |

3.3 Voltage regulators

The device derives its internal supply voltage from the BUS_I and V_{SS} pins. The internal regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC and supply dropouts on BUS_I. External filter capacitors are required, as shown in Figure 3 on page 5.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the undervoltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the undervoltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

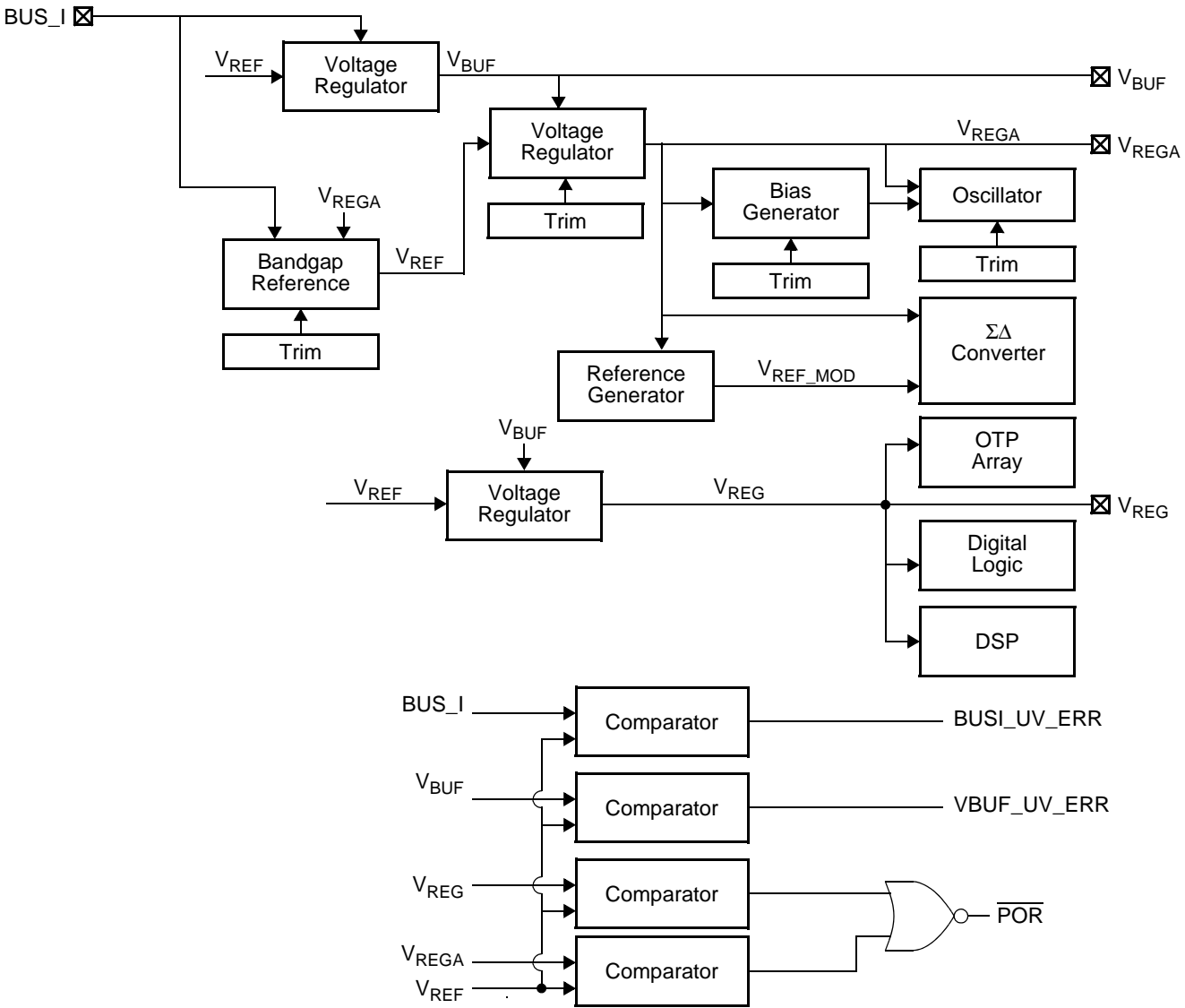


Figure 6. Voltage regulation and monitoring

3.3.1 V_{BUF}, V_{REG} and V_{REGA} regulator capacitor

The internal regulators require an external capacitor between the V_{BUF} pin and the V_{SS} pin, the V_{REG} pin and the V_{SS} pin and the V_{REGA} pin and the V_{SSA} pin for stability. Figure 3 on page 5 shows the recommended types and values for each of these capacitors.

3.3.2 BUS_I, V_{BUF}, V_{REG}, V_{REGA}, undervoltage monitor

A circuit is incorporated to monitor the BUS_I supply voltage and the internally regulated voltages, V_{BUF}, V_{REG} and V_{REGA}. If any of the voltages fall below the specified undervoltage thresholds in [Section 2.3](#), the device will react as listed below.

- BUS_I
 - If BUS_I falls below the specified threshold at any time, the BUSI_UV_ERR bit is set in the DEVSTAT2 register. The BUS_I_UV_ERR bit will be cleared once the supply returns above the threshold and either one Periodic Data Collection Mode status is transmitted with the VBUF_ERR bit set, or a response to a Command and Response Mode Register Read of the DEVSTAT2 register is transmitted.
 - If BUS_I falls below the specified threshold during a command transmission in Command and Response Mode, the command is ignored, and no DSI3 response transmission occurs. Once the supply returns above the threshold, the device will resume decoding commands.
 - If BUS_I falls below the specified threshold during a response transmission in Command and Response Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume decoding commands.
 - If BUS_I falls below the specified threshold during a command transmission in Periodic Data Collection Mode, the command is ignored and no periodic response occurs during that period. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands. The device will resume decoding Background Diagnostic Mode commands after the Start Condition is met.
 - If BUS_I falls below the specified threshold during a periodic response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands. The device will resume decoding Background Diagnostic Mode commands after the Start Condition is met.
 - If BUS_I falls below the specified threshold during a Background Diagnostic Mode response transmission in Periodic Data Collection Mode, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume periodic transmissions in response to commands. The device will resume decoding Background Diagnostic Mode commands after the Start Condition is met.
- V_{BUF}
 - If V_{BUF} falls below the specified threshold at any time, the VBUF_UV_ERR bit is set in the DEVSTAT2 register. If a response transmission is in process, the response is terminated. No attempt is made to resend the response. Once the supply returns above the threshold, the device will resume decoding commands and transmission of responses. The VBUF_UV_ERR bit will be cleared once the supply returns above the threshold and one Periodic Data Collection Mode status is transmitted with the VBUF_UV_ERR bit set.
- V_{REG} or V_{REGA}
 - If V_{REG} or V_{REGA} falls below the specified threshold at any time, the device is reset.

Reference [Figure 7](#) for an example of a supply line interruption during a response in Periodic Data Collection Mode.

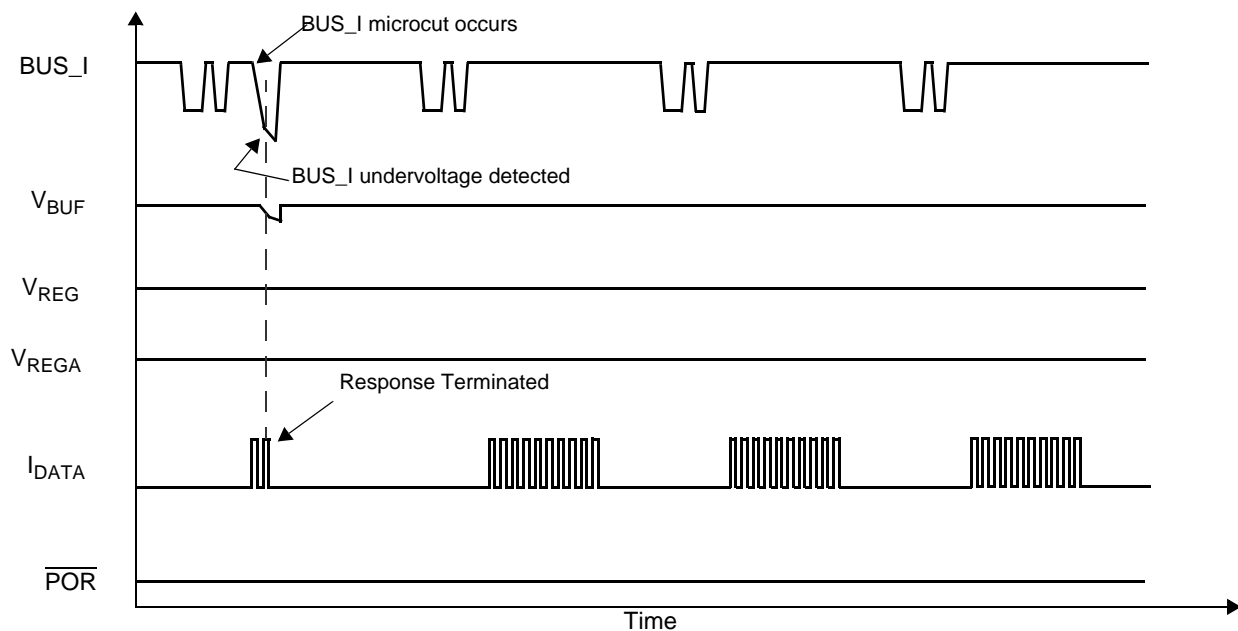


Figure 7. BUS_I Microcut response

3.3.3 V_{BUF} Capacitance monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF} capacitor becomes open. The V_{BUF} regulator is disabled t_{POR_CAPTEST} seconds after POR for a duration of t_{V_{BUF}CAPTST_TIME} seconds. If the external capacitor is not present, the regulator voltage will fall below the threshold specified in Section 2.3 causing the V_{BUF_ERR} bit to be set in the DEVSTAT2 register.

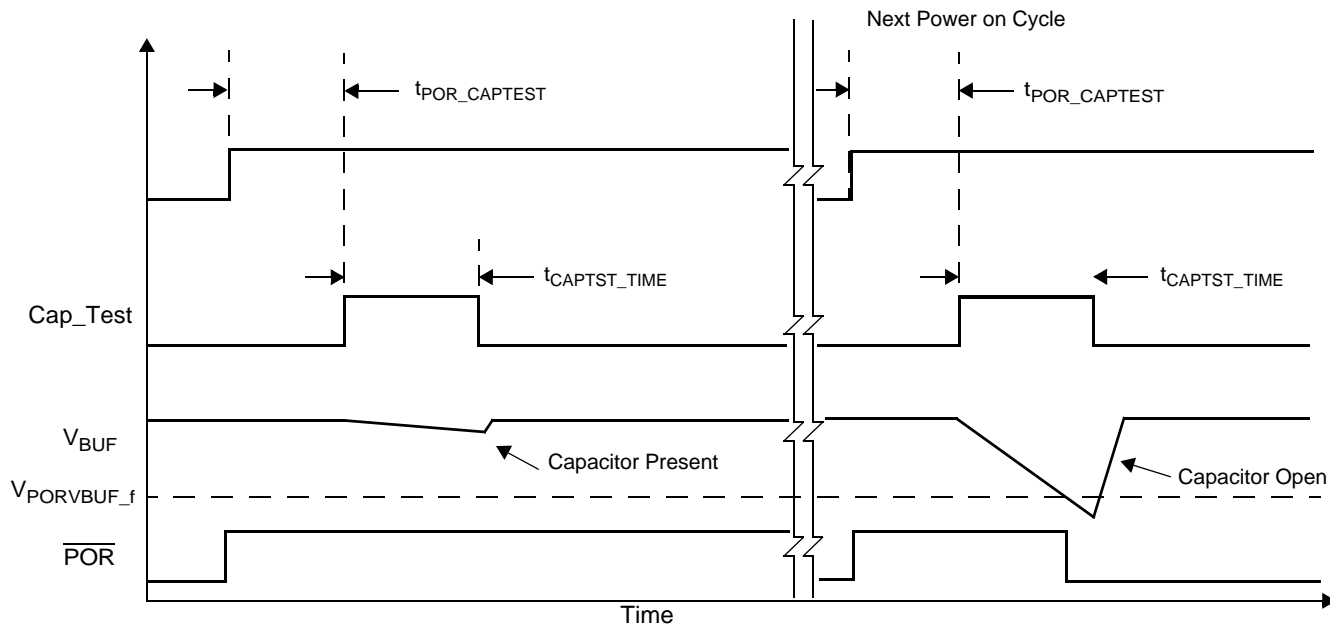


Figure 8. V_{BUF} Capacitor monitor

3.3.4 V_{REG} capacitance monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{REG} capacitor becomes open. The V_{REG} regulator is disabled $t_{POR_CAPTEST}$ seconds after POR for a duration of $t_{VREGCAPTST_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

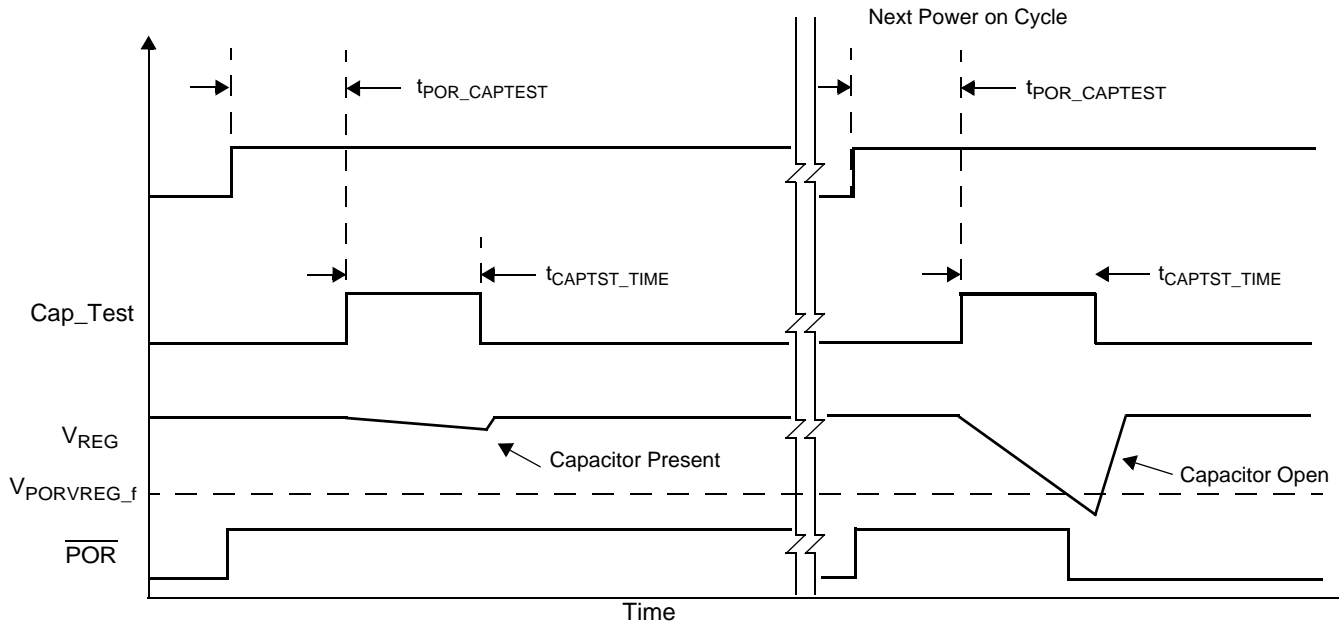


Figure 9. V_{REG} Capacitor Monitor

3.3.5 V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{REGA} capacitor becomes open. The V_{REGA} regulator is disabled $t_{POR_CAPTEST}$ seconds after POR for a duration of $t_{VREGCAPTST_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

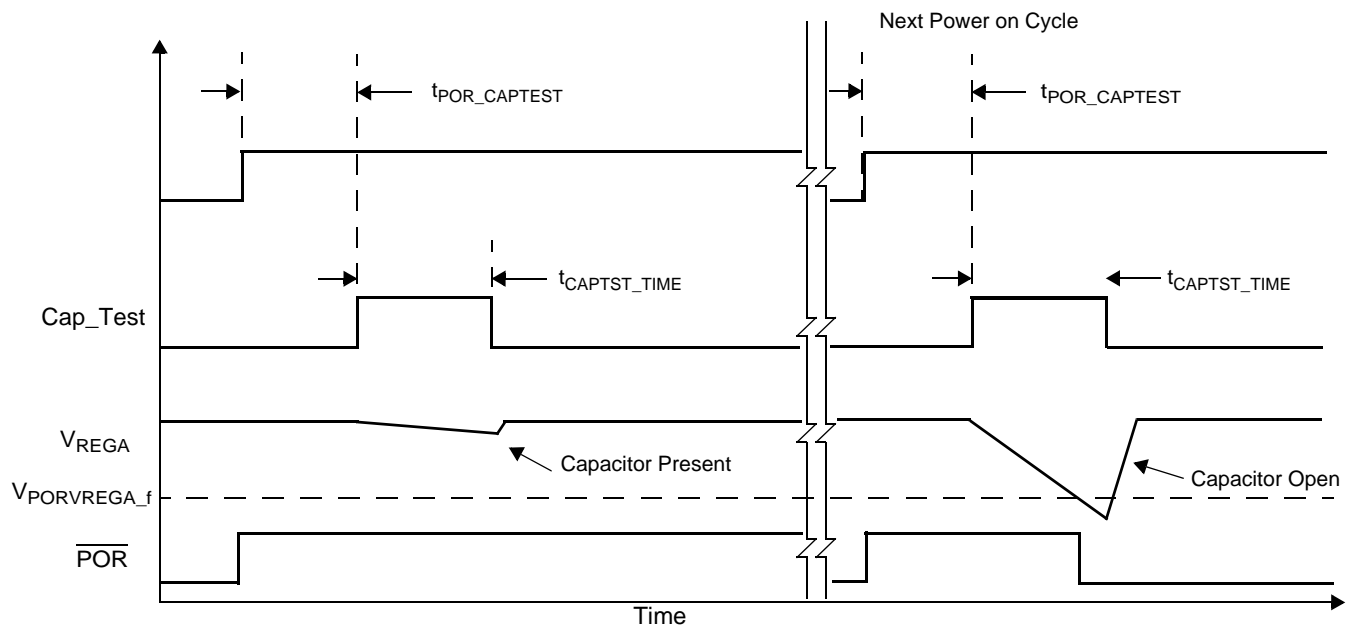


Figure 10. V_{REGA} capacitor monitor

3.4 Internal oscillator

The device includes a factory-trimmed oscillator as specified in [Section 2.8](#).

3.4.1 Oscillator training

The device includes a feature to train the oscillator to a tighter accuracy than the factory-trimmed capability assuming the system master has a tighter oscillator accuracy than the slave factory trimmed capability. Oscillator training is enabled if the CK_CAL_EN bit is set in the CRM_CFG register and is accomplished by verifying the timing of periodic transmissions from the master against the values stored in the CRM_PER[1:0] and PDCM_PER[2:0] bits of the user read/write register array. The master programs the intended Periodic Data Collection Mode command period into the PDCM_PER[2:0] bits and the intended Command and Response Mode command period into the CRM_PER[1:0] bits. The device then calculates the number of transmission periods for every 4 ms ($n_{CRM_PER_4ms_TYP}$ and $n_{PDCM_PER_4ms_TYP}$).

In Command and Response Mode, oscillator training is completed over 4 ms periods if and only if the CK_CAL_EN bit is set and the Command and Response Mode period is between 500 μ s and 4 ms, inclusive. The following procedure is used to train the oscillator ([Figure 11](#)):

1. The device counts the number of oscillator cycles in $n_{CRM_PER_4ms_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC_4ms_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in [Section 2.8](#), an oscillator adjustment is made. Otherwise, no adjustment is made.
 - a) If n_{OSC_4ms} is greater than $n_{OSC_4ms_TYP} + OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
 - b) If n_{OSC_4ms} is less than $n_{OSC_4ms_TYP} - OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
 - c) The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{CRM_PER_OSC}$ calculation.

If the CK_CAL_EN bit is cleared after oscillator training has already been initiated, the state of the oscillator is determined by the state of the CK_CAL_RST bit in the CRM_CFG register. If the CK_CAL_RST bit is cleared, the last adjustment value for the oscillator is maintained. If the CK_CAL_RST bit is set, the oscillator is reset to its untrained value with the untrained tolerance specified in [Section 2.8](#).

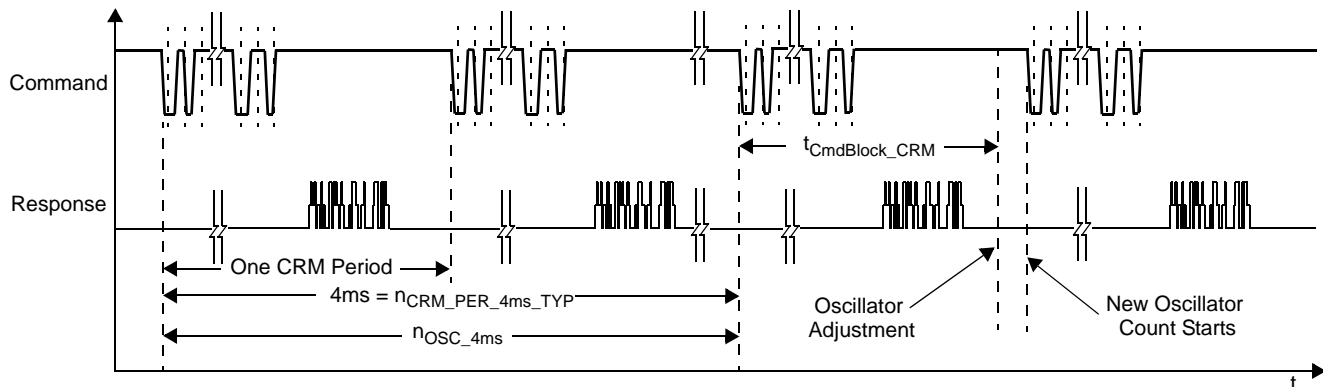


Figure 11. Command and Response Mode oscillator training timing diagram

In Periodic Data Collection Mode, oscillator training is completed over 4 ms periods if the CK_CAL_EN bit is set. The following procedure is used to train the oscillator (reference [Figure 12](#)):

1. The device counts the number of oscillator cycles in $n_{PDCM_PER_4ms_TYP}$ periods (n_{OSC_4ms}).
2. n_{OSC_4ms} is compared to $n_{OSC_4ms_TYP}$. If the value is within the acceptable training window ($OscTrain_{WIN}$) specified in [Section 2.8](#), an oscillator adjustment is made. Otherwise, no adjustment is made.
 - a) If n_{OSC_4ms} is greater than $n_{OSC_4ms_TYP} + OscTrain_{ADJ}$, the oscillator frequency target is decreased by $OscTrain_{RES}$.
 - b) If n_{OSC_4ms} is less than $n_{OSC_4ms_TYP} - OscTrain_{ADJ}$, the oscillator frequency target is increased by $OscTrain_{RES}$.
 - c) The oscillator frequency target value is changed at the end of the command blocking time for the command ending the $n_{PDCM_PER_OSC}$ calculation.

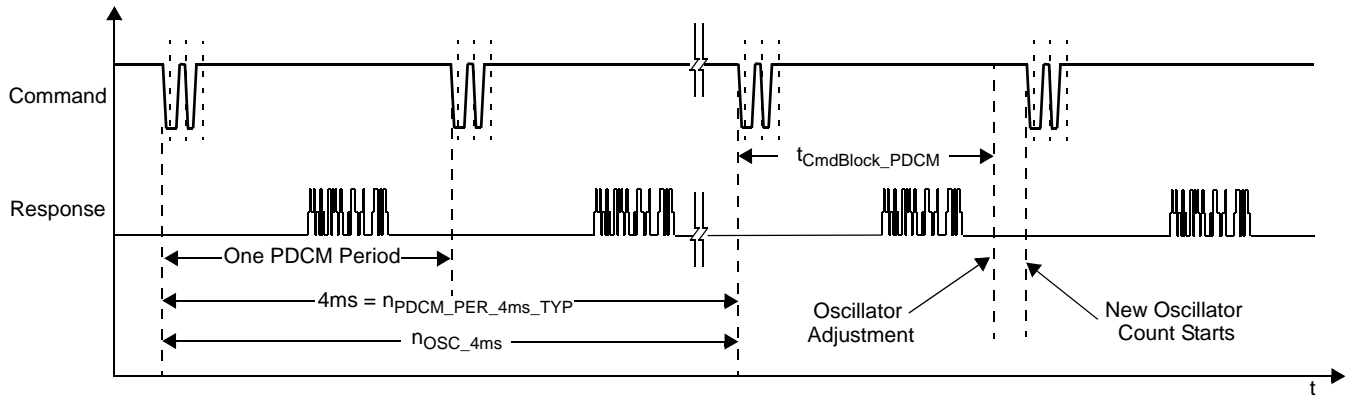


Figure 12. Periodic Data Collection Mode oscillator training timing diagram

3.4.2 Oscillator training error handling

If oscillator training is enabled by the user, but the conditions are not correct to complete oscillator training, the OSC_TRAIN bit is set in the DEVSTAT register. The following conditions will result in the OSCTRAIN_ERR bit being set.

- The CLK_CAL_EN bit in the CRM_CFG register is set, the device is in Command and Response Mode and Command and Response Mode period is not set to 500 μ s, 666 μ s, 1000 μ s, 1333 μ s, 2000 μ s or 4000 μ s.
- The CLK_CAL_EN bit in the CRM_CFG register is set and the measured period (n_{OSC_4ms}) for either Command and Response Mode or Periodic Data Collection Mode is outside of the Oscillator Training Window (OscTrain_{WIN}).
 - The result of the comparison is filtered with an up and down counter.
 - If n_{OSC_4ms} is outside the oscillator training window, the counter is incremented.
 - If n_{OSC_4ms} is inside the oscillator training window, the counter is decremented.
 - If the counter reaches 64 counts, the OSCTRAIN_ERR bit is set.
 - The up and down counter has a maximum value of 127 and a minimum value of 0.

3.5 Acceleration signal path

3.5.1 Transducer

The device transducer is an overdamped mass-spring-damper system defined by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2} \quad \text{Eqn. 1}$$

where:

- ζ = Damping Ratio
- ω_n = Natural Frequency = $2 \cdot \pi \cdot f_n$

Reference [Section 2.7](#) for transducer parameters.

3.5.2 Self-test interface

The self-test interface applies a voltage to the g-cell, causing deflection of the proof mass. The resulting acceleration readings can be compared against the values stored in the Self-Test Deflection registers (Reference [Section 3.1.24](#)). The self-test interface is controlled through SPI write operations to the ST_CONTROL register described in [Section 3.1.20](#). The PDCM_EN bit in the PDCM_EN register must also be low to enable self-test (Periodic Data Collection Mode not enabled). A diagram of the self-test interface is shown in [Figure 13](#).

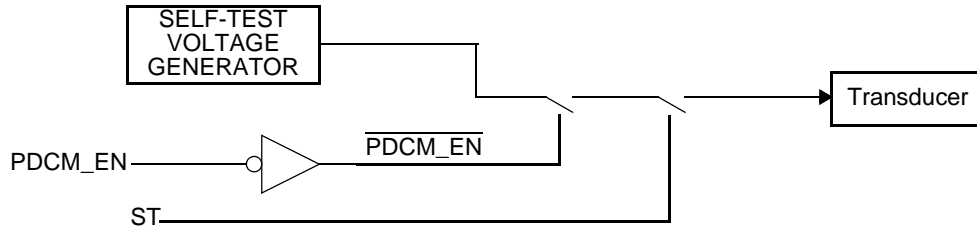


Figure 13. Self-test interface

Self-test can be verified via two methods:

3.5.2.1 Raw self-test deflection verification

The raw self-test deflection can be verified against raw self-test limits in [Section 2.5](#).

3.5.2.2 Delta self-test deflection verification

The raw self-test deflection can be verified against the nominal temperature self-test deflection value recorded at the time the device was produced. The production self-test deflection is stored in the ACC_STDATA register such that the minimum stored value (0x00) is equivalent to ΔST_{MIN} , and the maximum stored value (0xFF) is equivalent to ΔST_{MAX} . The Delta Self-test Deflection limits can then be determined by the following equations:

$$\Delta ST_{ACCMINLIMIT} = \text{FLOOR} \cdot [(\Delta ST_{MIN} + \text{ACCSTDATA}) \times (1 - \Delta ST_{ACC})] \quad \text{Eqn. 2}$$

$$\Delta ST_{ACCMAXLIMIT} = \text{CEIL} \cdot [(\Delta ST_{MIN} + \text{ACCSTDATA}) \times (1 + \Delta ST_{ACC})] \quad \text{Eqn. 3}$$

where:

ΔST_{ACC} = The accuracy of the self-test deflection relative to the stored deflection as specified in [Section 2.5](#).

ACCSTDATA = The value stored in the ACC_STDATA register.

ΔST_{MIN} = The minimum self-test deflection at 25°C as specified in [Section 2.5](#).

ΔST_{MAX} = The maximum self-test deflection at 25°C as specified in [Section 2.5](#).

3.5.3 Analog front-end and $\Sigma\Delta$ converter

A sigma delta modulator converts the differential capacitance of the transducer to a data stream that is input to the DSP.

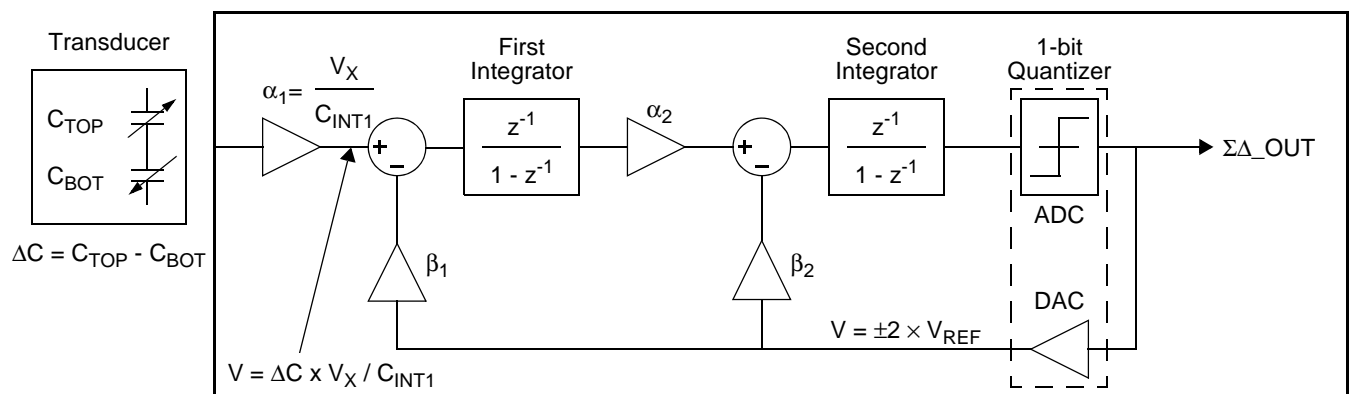


Figure 14. $\Sigma\Delta$ Converter block diagram

3.5.4 Digital-signal processor

A digital-signal processor (DSP) is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP is shown in [Figure 15](#).

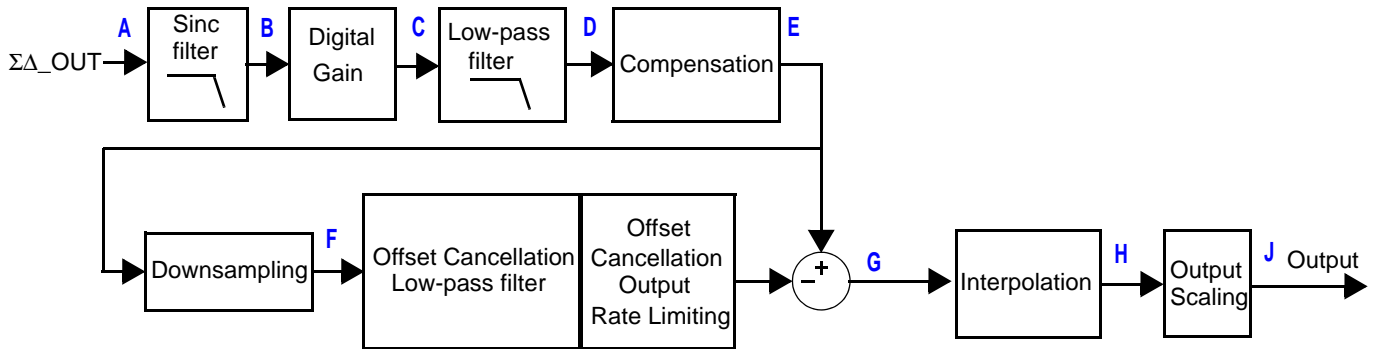


Figure 15. Signal-chain diagram

Table 33. Signal-chain characteristics

| | Description | Sample time (μs) | Data Width (Bits) | Overrange (Bits) | Signal Width (Bits) | Signal Noise (Bits) | Signal Margin (Bits) | Typical Block Latency | Reference |
|---|--------------------------------|------------------|-------------------|------------------|---------------------|---------------------|----------------------|---------------------------------|---------------------------------|
| A | SD | 1 | 1 | | 1 | | | 51 μs | Section 3.5.3 |
| B | SINC filter | 16 | 20 | | 14 | | | | Section 3.5.4.1 |
| C | Digital gain | 16 | 20 | | 14 | | | | Section 3.5.4.2 |
| D | Low-pass filter | 16 | 26 | 4 | 10 | 3 | 9 | Section 3.5.4.3 | Section 3.5.4.3 |
| E | Compensation | 16 | 26 | 4 | 10 | 3 | 9 | 17 μs | Section 3.5.4.4 |
| F | Down sampling | 256 | 26 | 4 | 10 | 3 | 9 | | |
| G | Offset cancellation | 256 | 26 | 4 | 10 | 3 | 9 | Section 3.5.4.5 | Section 3.5.4.5 |
| H | DSP sampling and interpolation | 8 | | | 10 | | | 8 μs | Section 3.5.4.7 |
| J | 10-bit output scaling | 1 | | | 10 | | | 1 μs | Section 3.5.4.8 |

3.5.4.1 Decimation Sinc filter

The serial data stream produced by the $\Sigma\Delta$ converter is decimated and converted to parallel values by a 3rd order sinc filter with a decimation factor of 16.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})} \right]^3 \quad \text{Eqn. 4}$$

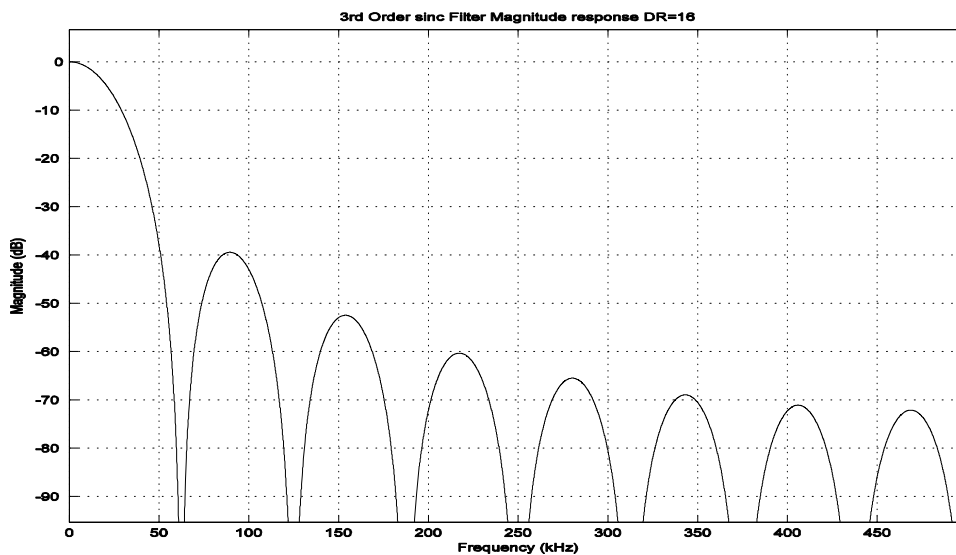


Figure 16. Sinc-filter response

3.5.4.2 Digital gain

The DSP applies a selectable one or two times digital gain to the output of the sinc filter. The gain applied is dependent on the output range of the device.

3.5.4.3 Low-pass filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{21} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})} \quad \text{Eqn. 5}$$

The device provides the option for one of six low-pass filters. The filter is selected with the LPF[3:0] bits in the ACC_CFG register. The filter selection options are listed in [Section 3.1.25.1](#). Response parameters for the low-pass filter are specified in [Section 2.7](#). Filter characteristics are illustrated in the following figures.

Table 34. Low-pass filter coefficients

| Filter Number | Description -3dB Frequency (±5%) | Filter order | Filter Coefficients | | | | Group Delay | Attenuation @ 1000 Hz (dB) | | |
|---------------|---|--------------|---------------------|------------------------|-----------------|-------------------------|-------------|----------------------------|------|------|
| | | | | | | | | Min | Typ | Max |
| | 180 Hz | 2 | a ₀ | 0.000534069200512 | | | 1190 μs | 24.8 | 25.6 | 26.5 |
| | | | n ₁₁ | 0.25 | d ₁₁ | 1 | | | | |
| | | | n ₁₂ | 0.499999985098839 | d ₁₂ | -1.959839582443237 | | | | |
| | | | n ₁₃ | 0.25 | d ₁₃ | 0.960373640060425 | | | | |
| | | | n ₂₁ | 1 | d ₂₁ | 1 | | | | |
| | | | n ₂₂ | 0 | d ₂₂ | 0 | | | | |
| | | | n ₂₃ | 0 | d ₂₃ | 0 | | | | |
| | 325Hz | 3 | a ₀ | 0.04247547499835491180 | | | 856 μs | 20.2 | 21.4 | 22.6 |
| | | | n ₁₁ | 0.00109037756919860840 | d ₁₁ | 1 | | | | |
| | | | n ₁₂ | 0.00108939409255981445 | d ₁₂ | -0.95752453804016113281 | | | | |
| | | | n ₁₃ | 0 | d ₁₃ | 0 | | | | |
| | | | n ₂₁ | 0.24988752603530883789 | d ₂₁ | 1 | | | | |
| | | | n ₂₂ | 0.49999989569187164307 | d ₂₂ | -1.93140876293182373047 | | | | |
| | | | n ₂₃ | 0.25011256337165832520 | d ₂₃ | 0.93358850479125976562 | | | | |
| | 400 Hz | 3 | a ₀ | 0.05189235225042199 | | | 697 μs | 15.5 | 16.7 | 17.8 |
| | | | n ₁₁ | 0.001629077582099646 | d ₁₁ | 1 | | | | |
| | | | n ₁₂ | 0.001630351547919014 | d ₁₂ | -0.9481076477495780 | | | | |
| | | | n ₁₃ | 0 | d ₁₃ | 0 | | | | |
| | | | n ₂₁ | 0.2500977520825902 | d ₂₁ | 1 | | | | |
| | | | n ₂₂ | 0.4999999235890745 | d ₂₂ | -1.915847097557409 | | | | |
| | | | n ₂₃ | 0.2499023243303036 | d ₂₃ | 0.9191065266874253 | | | | |
| | 400 Hz | 4 | a ₀ | 0.003135988372378 | | | 841 μs | 18.1 | 19.5 | 21.0 |
| | | | n ₁₁ | 0.000999420881271 | d ₁₁ | 1.0 | | | | |
| | | | n ₁₂ | 0.001998946070671 | d ₁₂ | -1.892452478408814 | | | | |
| | | | n ₁₃ | 0.000999405980110 | d ₁₃ | 0.89558845758438 | | | | |
| | | | n ₂₁ | 0.250004753470421 | d ₂₁ | 1.0 | | | | |
| | | | n ₂₂ | 0.499986037611961 | d ₂₂ | -1.919075012207031 | | | | |
| | | | n ₂₃ | 0.250009194016457 | d ₂₃ | 0.923072755336761 | | | | |
| | 800 Hz | 4 | a ₀ | 0.011904109735042 | | | 420 μs | 4.42 | 4.94 | 5.54 |
| | | | n ₁₁ | 0.003841564059258 | d ₁₁ | 1.0 | | | | |
| | | | n ₁₂ | 0.007683292031288 | d ₁₂ | -1.790004611015320 | | | | |
| | | | n ₁₃ | 0.003841534256935 | d ₁₃ | 0.801908731460571 | | | | |
| | | | n ₂₁ | 0.250001862645149 | d ₂₁ | 1.0 | | | | |
| | | | n ₂₂ | 0.499994158744812 | d ₂₂ | -1.836849451065064 | | | | |
| | | | n ₂₃ | 0.250003993511200 | d ₂₃ | 0.852215826511383 | | | | |
| | 1200 Hz | 4 | a ₀ | 0.025461918674409 | | | 280 μs | 1.83 | 2.03 | 2.27 |
| | | | n ₁₁ | 0.008307680487633 | d ₁₁ | 1.0 | | | | |
| | | | n ₁₂ | 0.016615495085716 | d ₁₂ | -1.692260980606079 | | | | |
| | | | n ₁₃ | 0.008307650685310 | d ₁₃ | 0.717722892761230 | | | | |
| | | | n ₂₁ | 0.250000774860382 | d ₂₁ | 1.0 | | | | |
| | | | n ₂₂ | 0.499997481703758 | d ₂₂ | -1.753850817680359 | | | | |
| | | | n ₂₃ | 0.250001743435860 | d ₂₃ | 0.787081658840179 | | | | |

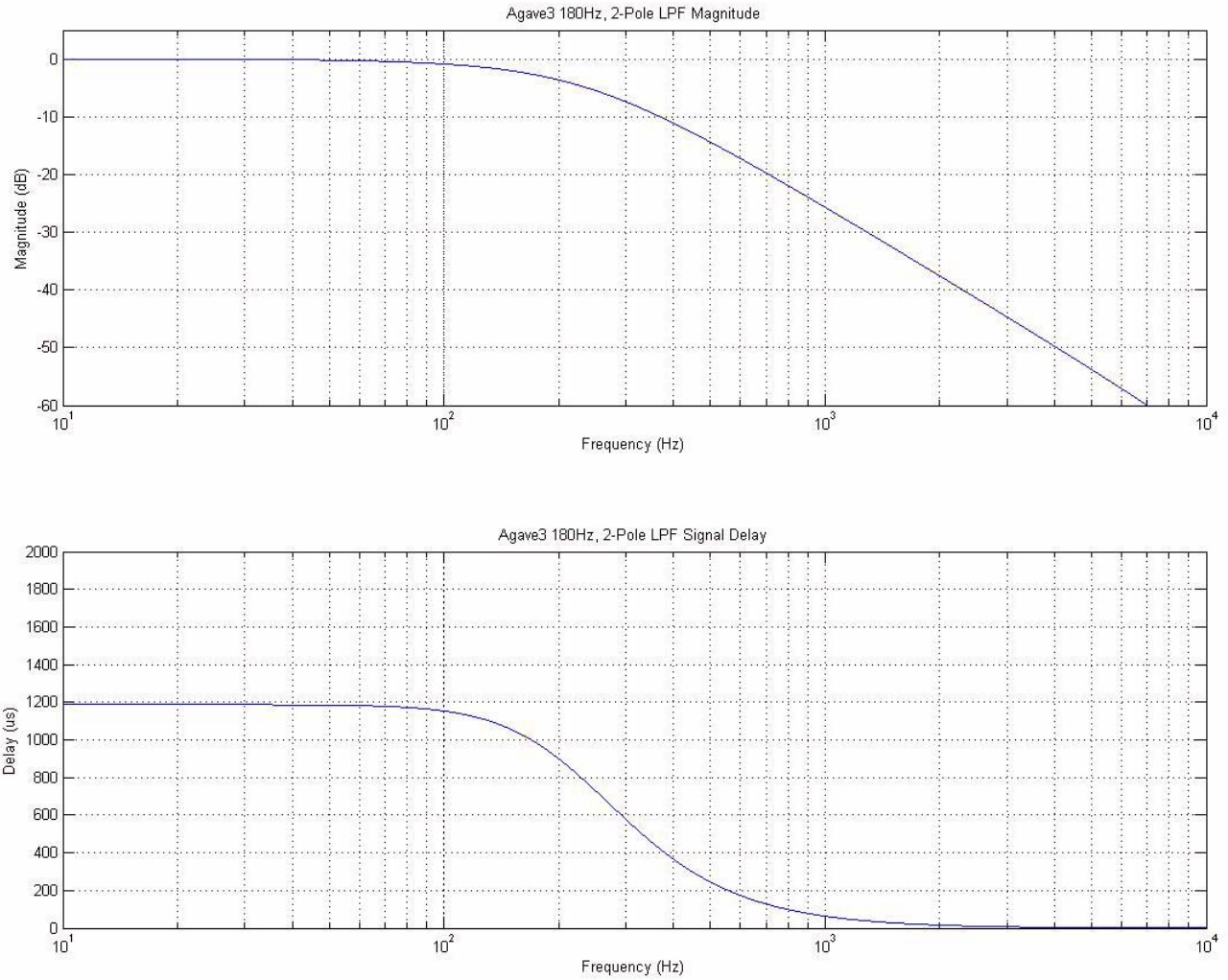


Figure 17. Low-pass filter characteristics: $f_C = 180$ Hz, 2-Pole, $t_S = 16 \mu\text{s}$

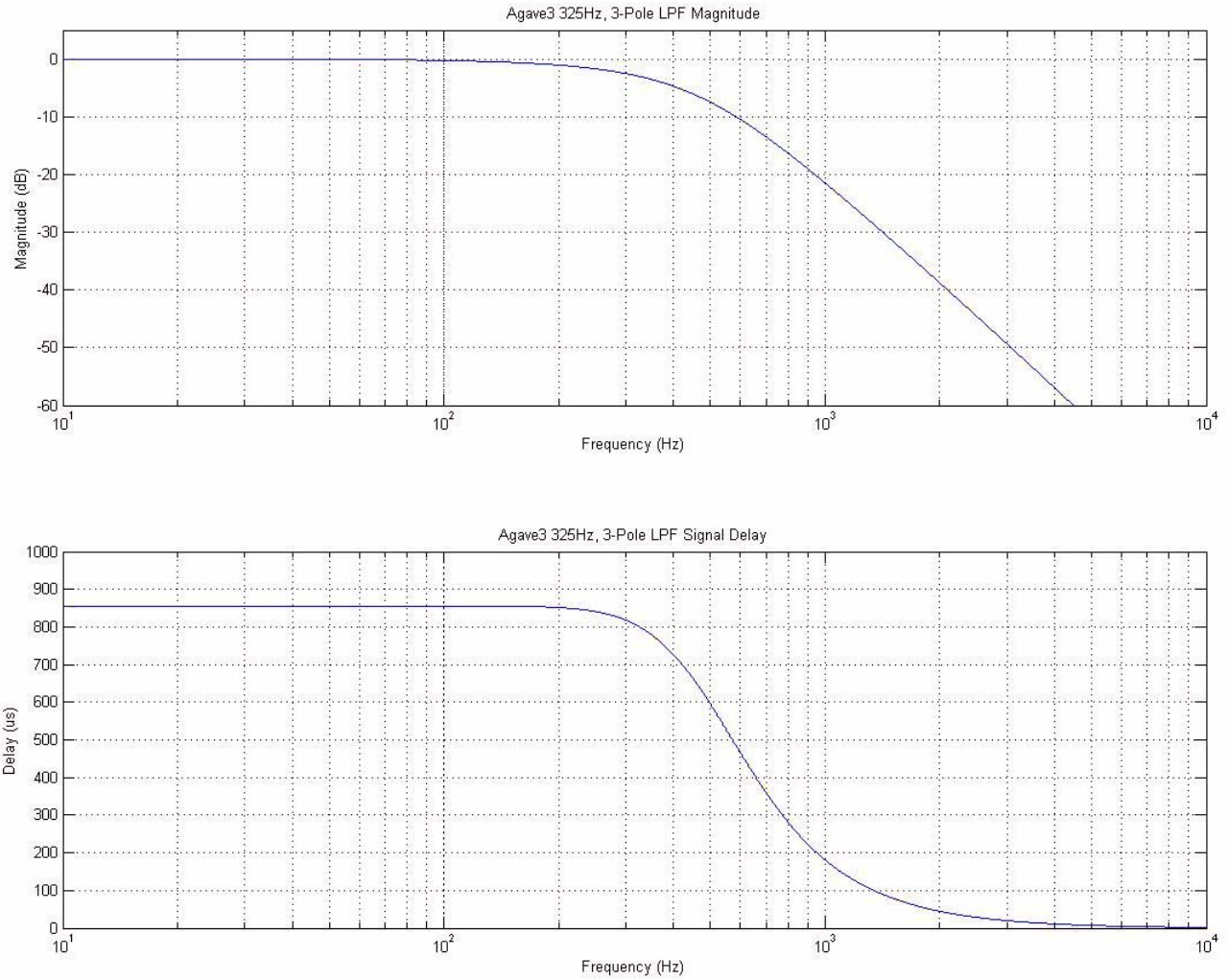


Figure 18. Low-pass filter characteristics: $f_C = 325$ Hz, 3-Pole, $t_S = 16$ μ s

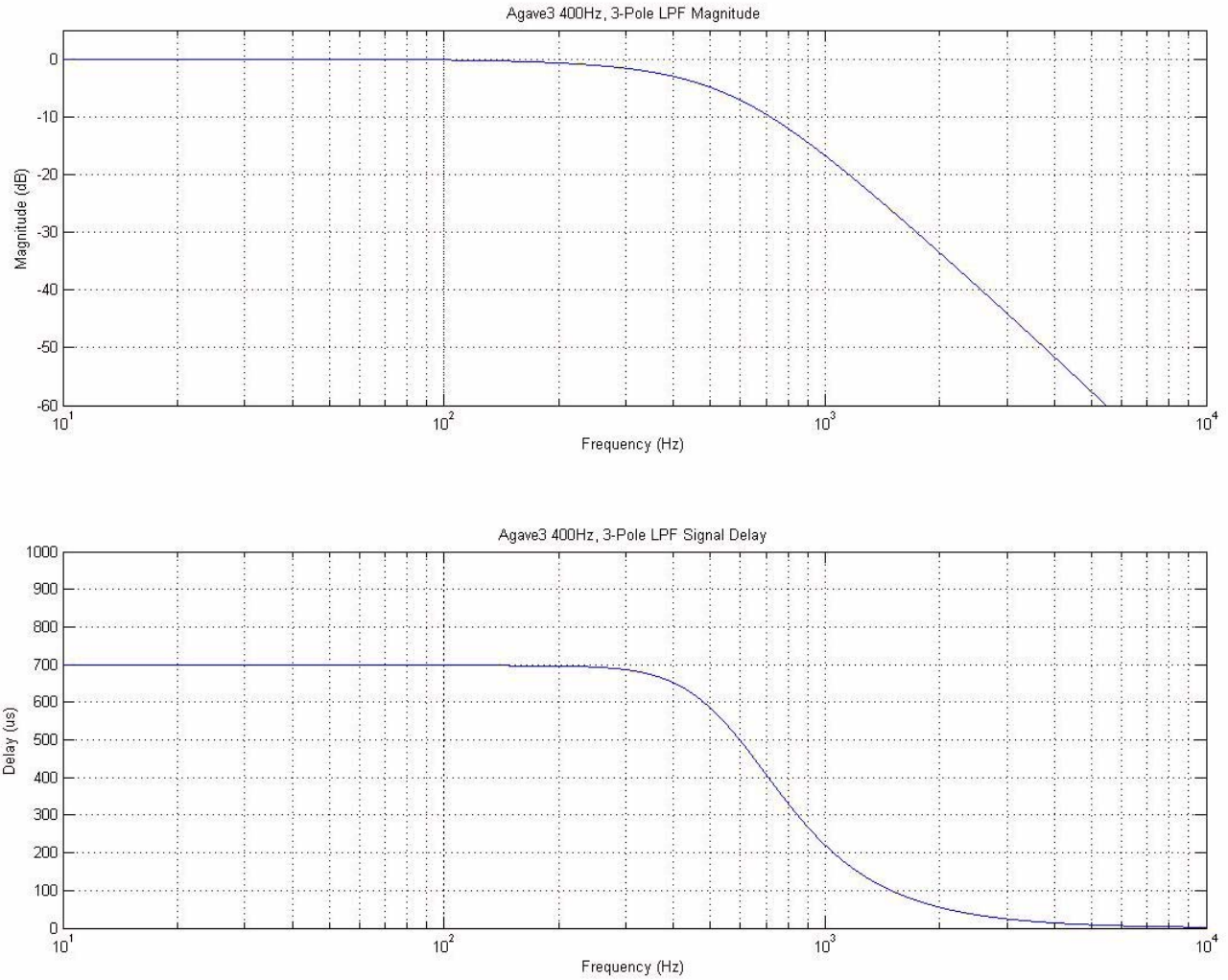


Figure 19. Low-pass filter characteristics: $f_C = 400$ Hz, 3-Pole, $t_S = 16 \mu\text{s}$

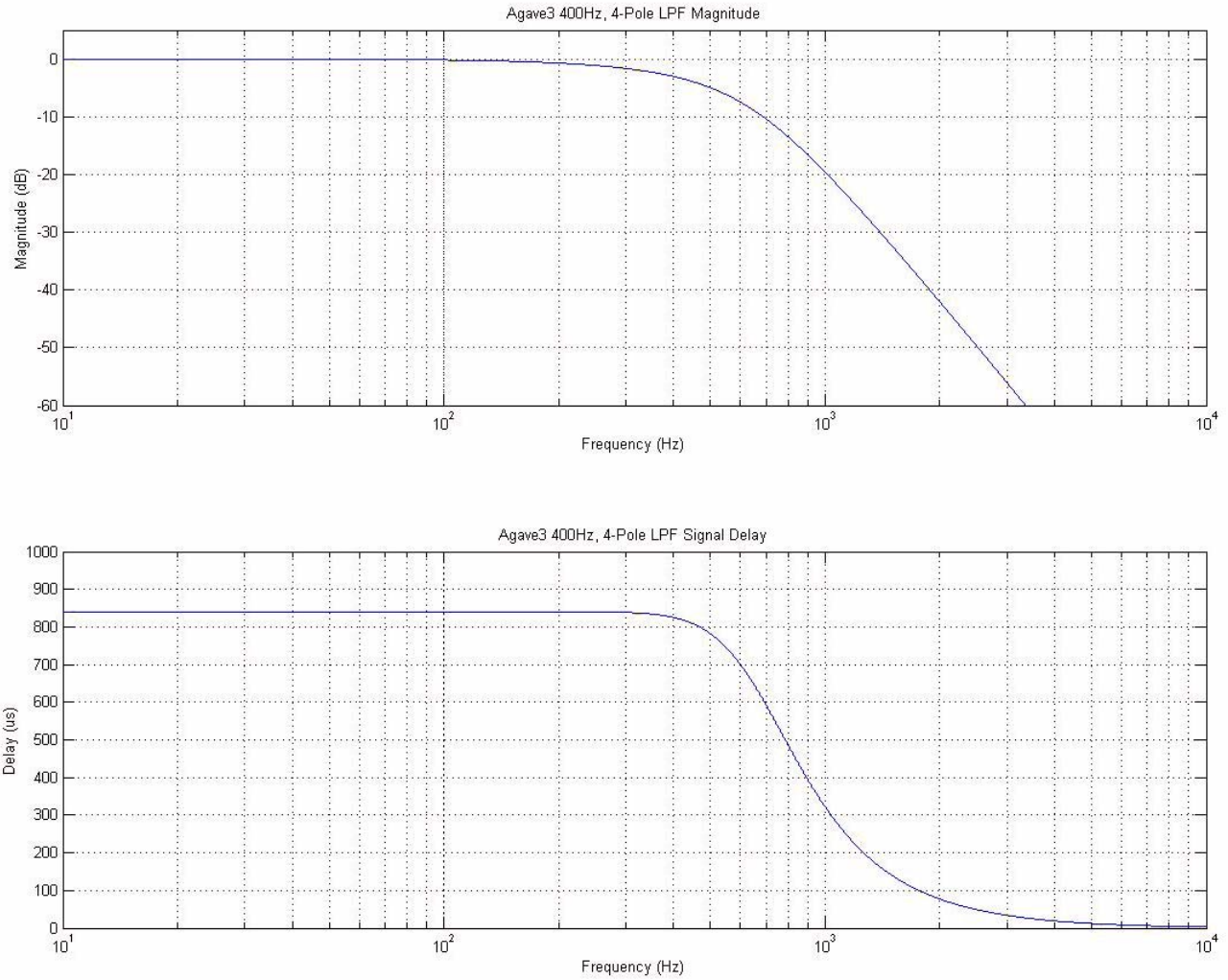


Figure 20. Low-pass filter characteristics: $f_C = 400$ Hz, 4-Pole, $t_S = 16 \mu s$

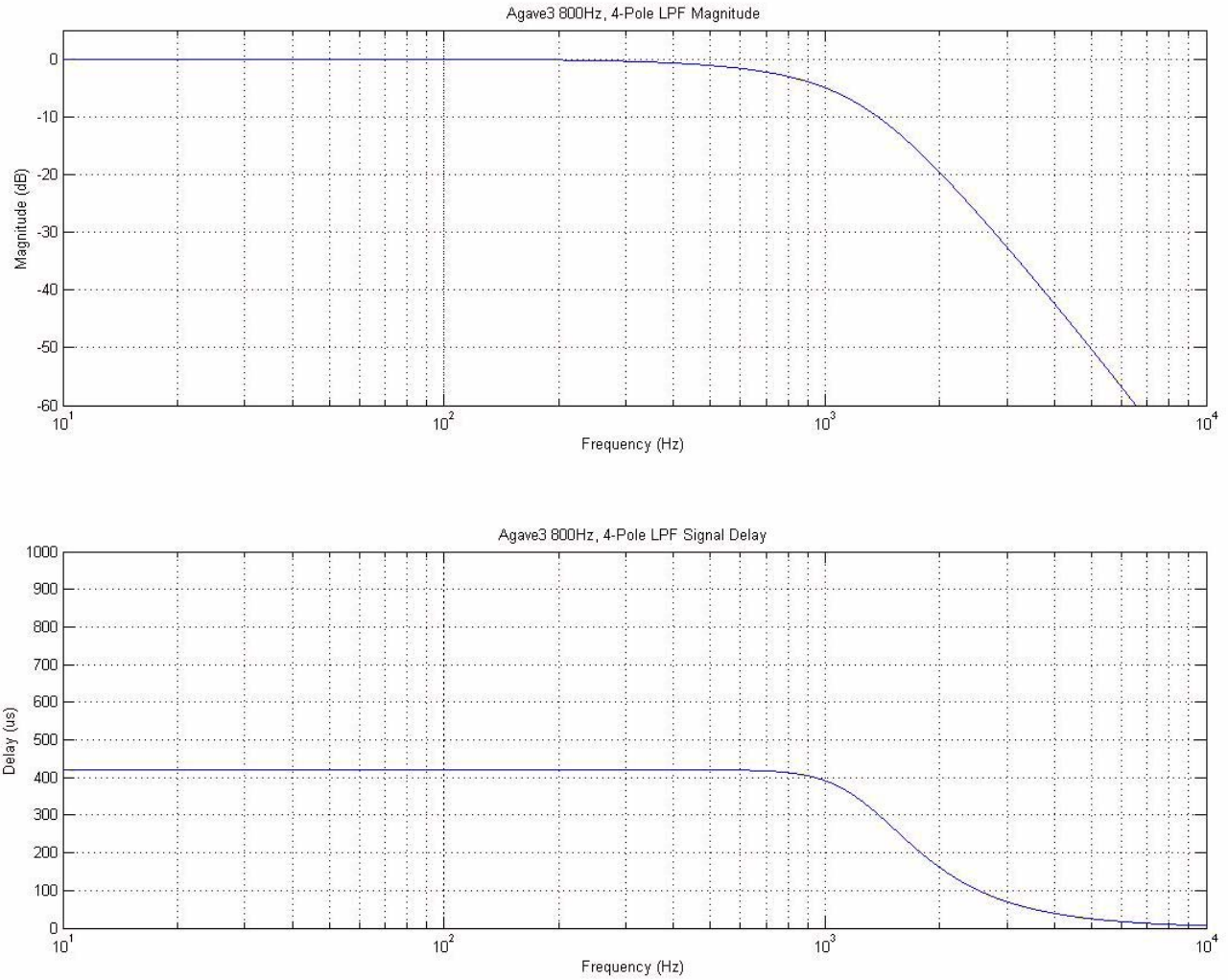


Figure 21. Low-pass filter characteristics: $f_C = 800$ Hz, 4-Pole, $t_S = 16 \mu$ s

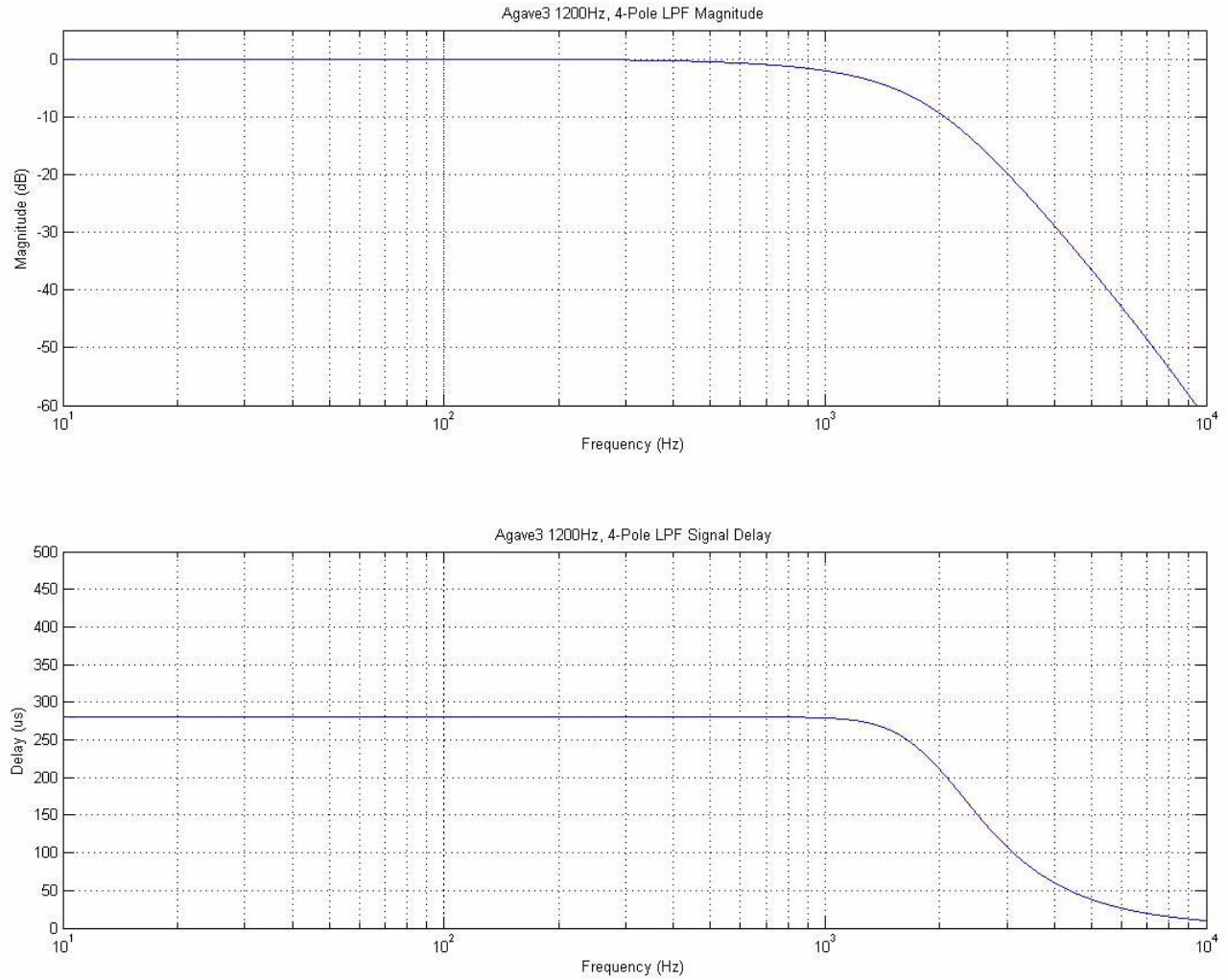


Figure 22. Low-pass filter characteristics: $f_C = 1200$ Hz, 4-Pole, $t_S = 16 \mu$ s

3.5.4.4 Signal compensation

The device includes internal gain and compensation circuitry to compensate for sensor offset, sensitivity and non-linearity.

3.5.4.5 Offset cancellation

The device provides an optional offset cancellation circuit to remove internal offset error. A block diagram of the offset cancellation is shown in Figure 23.

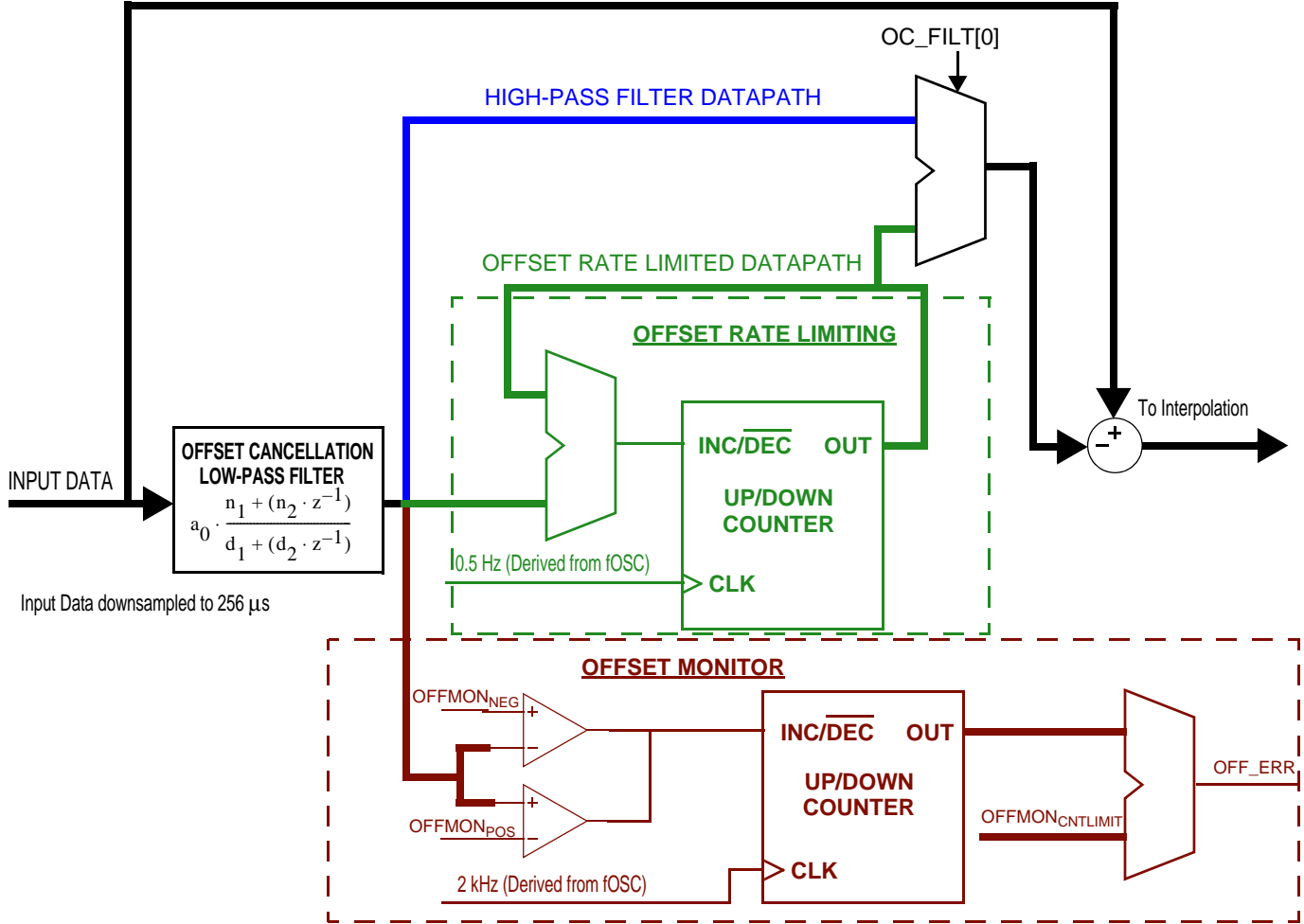


Figure 23. Offset cancellation block diagram

The transfer function for the offset LPF is:

$$H(z) = a_0 \cdot \frac{n_0 + (n_1 \cdot z^{-1})}{d_0 + (d_1 \cdot z^{-1})} \quad \text{Eqn. 6}$$

Response parameters are specified in Section 2 and the offset LPF coefficients are specified in Table 36.

During start up, two phases of the offset LPF are used to allow for fast convergence of the internal offset error during initialization. The timing for the startup phases is shown in Table 35.

The offset low-pass filter used in normal operation is selected by the OC_FILT[2:0] bits in the ACC_CFG register. Output rate limiting can be applied to the output of the offset low-pass filter. Rate limiting is also enabled by the OC_FILT[2:0] bits. If rate limiting is enabled, the offset cancellation output is updated by OFF_{Step} LSB every t_{OffRate} seconds.

The offset cancellation circuit output value is frozen when self-test is active, even if the offset cancellation circuit is in a startup phase. The timers controlling the startup phase times listed in Table 35 are not frozen. To ensure proper offset cancellation startup, prior to activating self-test, the user should verify that the offset cancellation initialization is complete by monitoring the OC_INIT bit in the DEVSTAT register.

Table 35. Offset cancellation startup characteristics and timing

| Offset cancellation startup phase | Offset LPF | Output rate limiting | Total time for phase |
|-----------------------------------|---|--------------------------|----------------------|
| 1 | 10 Hz | Bypassed | 80 ms |
| 2 | 1.0 Hz | Bypassed | 70 ms |
| Self-test | Offset Cancellation Updates are Suspended | | User Enabled |
| Complete | Selected by OC_FILT[2:0] | Selected by OC_FILT[2:0] | N/A |

Table 36. Offset low-pass filter coefficients

| Description -3 dB frequency (±5%) | Coefficients | | | | Latency/Group delay |
|---|-----------------|------------------------|-----------------|-------------------------|---------------------|
| 10 Hz | ao ₀ | 0.015956938266754 | | | 15.91 ms |
| | no ₁ | 0.499998132328277 | do ₁ | 1.0 | |
| | no ₂ | 0.499998132328277 | do ₂ | -0.984043061733246 | |
| 1.0 Hz | ao ₀ | 0.00160720286658033729 | | | 159.1ms |
| | no ₁ | 0.5 | do ₁ | 1.0 | |
| | no ₂ | 0.5 | do ₂ | -0.99839282035827636719 | |
| 0.1 Hz | ao ₀ | 0.0001608133316040 | | | 1591 ms |
| | no ₁ | 0.4999999403953552 | do ₁ | 1.0 | |
| | no ₂ | 0.4999999403953552 | do ₂ | -0.9998391270637512 | |

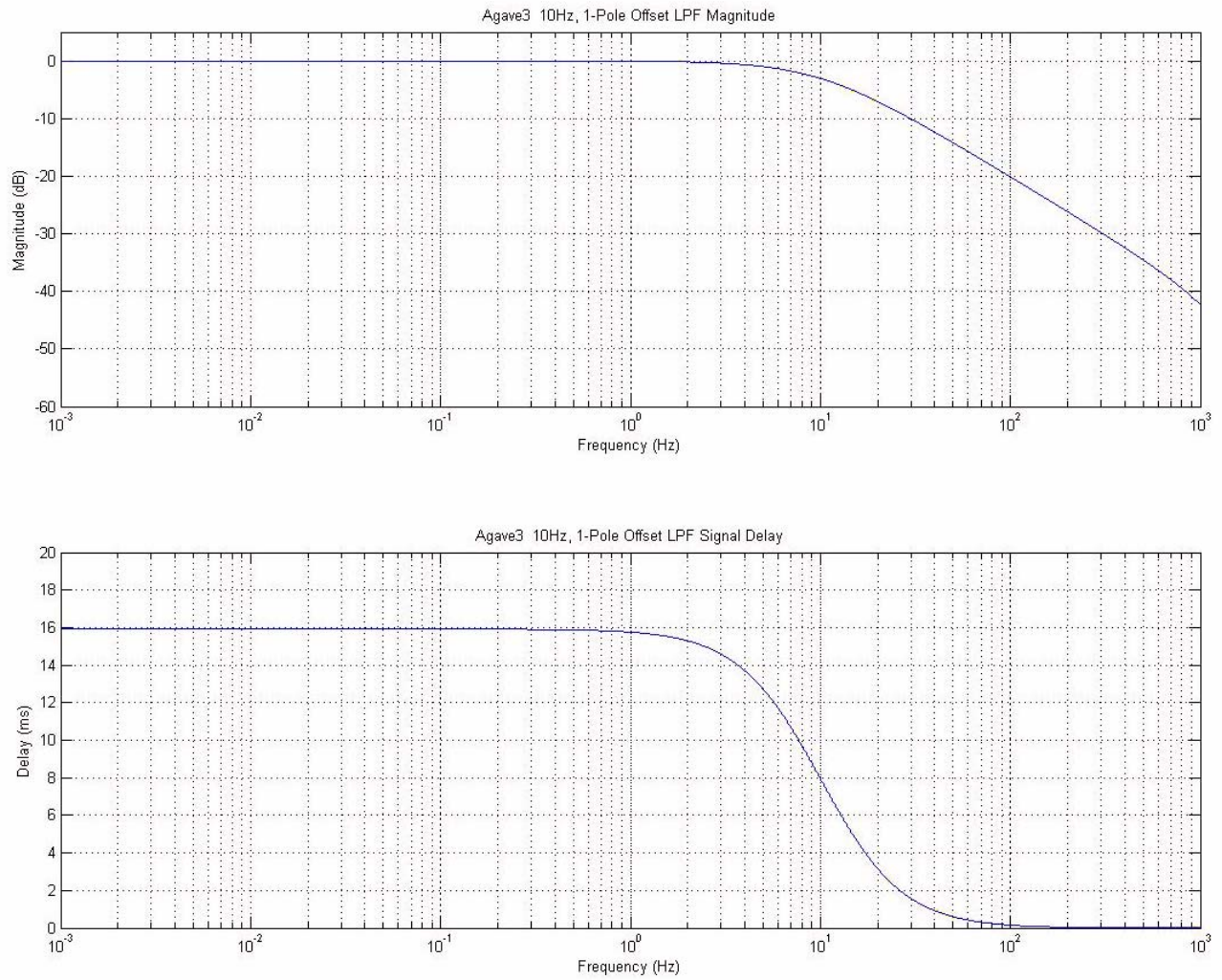


Figure 24. 10 Hz offset cancellation low-pass filter characteristics

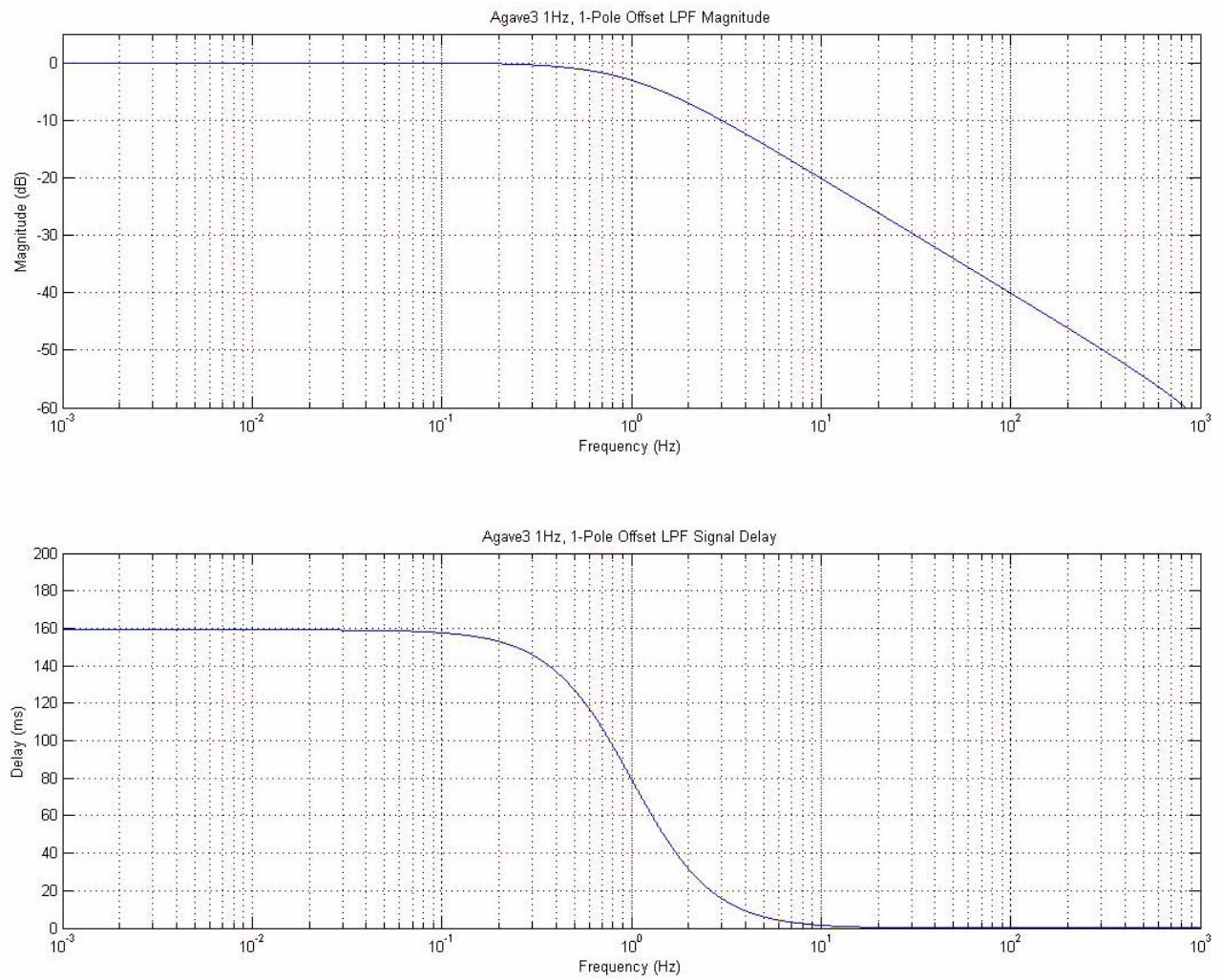


Figure 25. 1.0 Hz offset cancellation low-pass filter characteristics

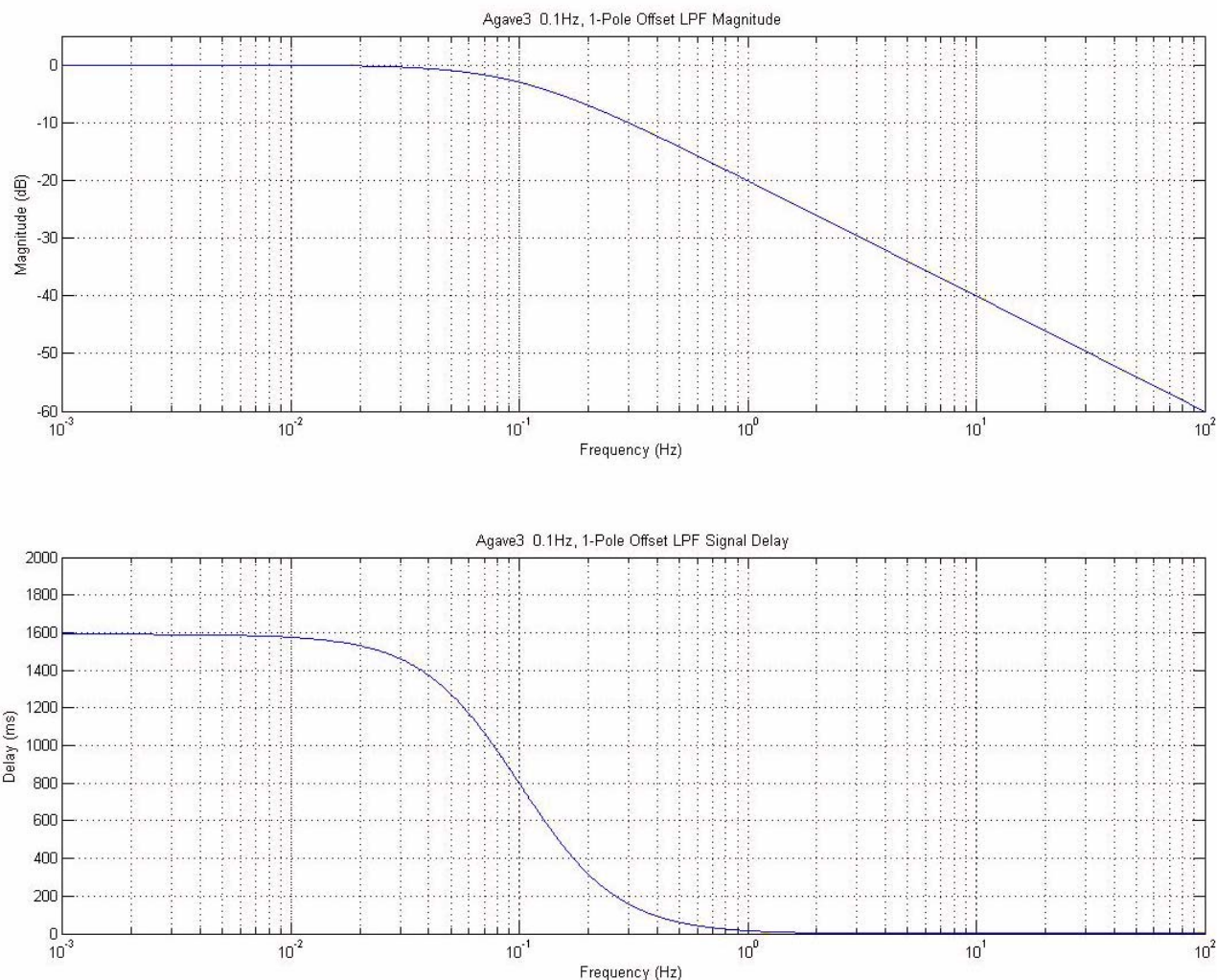


Figure 26. 0.1 Hz offset cancellation low-pass filter characteristics

3.5.4.6 Offset monitor

The device includes an offset monitor circuit. The offset monitor is enabled 2.1 seconds following reset regardless of the state of the OC_FILT bits in the ACC_CFG register. The output of the single pole, low-pass filter in the offset cancellation block is continuously monitored against the offset limits specified in Section 2.4. An up/down counter is employed to count up if the output exceeds the limits, and to count down if the output is within the limits. The output of the counter is compared against the count limit OFFMON_{CNTLIMIT}. If the counter exceeds the limit, the OFFSET_ERR bit in the ACC_STAT register and in the DEVSTAT register is set. The counter rails once the max counter value is reached (OFFMON_{CNTSIZE}).

3.5.4.7 Data interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. On detection of a Periodic Data Collection Mode command, the transmitted data is interpolated from the one previous samples, resulting in a latency of one sample time, and a maximum signal jitter of 1 μ s.

3.5.4.8 Output scaling

The 26-bit digital output from the DSP is clipped and scaled to a 10-bit, 14-bit, or 16-bit data word. The 10-bit and 14-bit data words are used for Periodic Data Collection Mode and the 16-bit range is stored in the ACC_DATAH and ACC_DATA_L registers for access during Command and Response Mode.

The sensitivity of the data is the same for all ranges. If the 14-bit data length is selected, four additional bits of range are transmitted. If the ACC_DATAH and ACC_DATA_L registers are accessed, six additional bits of range are available. These additional bits of range are intended for test use only and are not covered by the specifications listed in Section 2.4. Reference Table 37 for the acceleration data values for all ranges.

3.5.4.9 Output data values

Table 37. Nominal acceleration data values

| 16-bit data | | | | 10-bit data | | | | Nominal acceleration (g) | | | | |
|------------------------|------------------|----------------------|------------------|------------------------|-------|----------------------|-------|--------------------------|-------------|-------------|-------------|-------------|
| Unsigned digital value | | Signed digital value | | Unsigned digital value | | Signed digital value | | 25 g range | 125 g range | 187 g range | 250 g range | 375 g range |
| Decimal | Hex | Decimal | Hex | Decimal | Hex | Decimal | Hex | | | | | |
| 33280 to 65535 | 0x8200 to 0xFFFF | 512 to 32767 | 0x200 to 0x7FFF | NA | NA | NA | NA | Overrange data | | | | |
| 33279 | 0x81FF | 511 | 0x1FF | 1023 | 0x3FF | 511 | 0x1FF | 24.9512 | 124.756 | 186.633 | 249.512 | 374.277 |
| 33278 | 0x81FE | 510 | 0x1FE | 1022 | 0x3FE | 510 | 0x1FE | 24.9023 | 124.512 | 186.267 | 249.023 | 373.544 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 32770 | 0x8002 | 2 | 0x0002 | 514 | 0x202 | 2 | 0x002 | 0.976563 | 0.488281 | 0.730460 | 0.976563 | 1.46488 |
| 32769 | 0x8001 | 1 | 0x0001 | 513 | 0x201 | 1 | 0x001 | 0.048828 | 0.244141 | 0.365230 | 0.488281 | 0.732440 |
| 32768 | 0x8000 | 0 | 0x0000 | 512 | 0x200 | 0 | 0x000 | 0 | 0 | 0 | 0 | 0 |
| 32767 | 0x7FFF | -1 | 0xFFFF | 511 | 0x1FF | -1 | 0x3FF | -0.048828 | -0.244141 | -0.365230 | -0.488281 | -0.732440 |
| 32766 | 0x7FFE | -2 | 0xFFFE | 510 | 0x1FE | -2 | 0x3FE | -0.976563 | -0.488281 | -0.730460 | -0.976563 | -1.46488 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 32258 | 0x7E02 | -510 | 0xFE02 | 2 | 0x002 | -510 | 0x202 | -24.9023 | -124.512 | -186.267 | -249.023 | -373.544 |
| 32257 | 0x7E01 | -511 | 0xFE01 | 1 | 0x001 | -511 | 0x201 | -24.9512 | -124.756 | -186.633 | -249.512 | -374.277 |
| 1 to 32256 | 0x0001 to 0x7E00 | -32767 to -512 | 0x8001 to 0xFE00 | NA | NA | NA | NA | Overrange Data | | | | |
| 0 | 0x0000 | -32768 | 0x8000 | 0 | 0x000 | -512 | 0x200 | Fault | | | | |

3.5.4.10 PCM output function

The device provides the option for a PCM output function. The PCM output is enabled if the PCM bit is set in the ACC_FCTCFG register. Selecting the PCM output enables the following functions:

- The acceleration value output from the offset cancellation block is saturated to 9-bits and converted to an unsigned value.
- The 9-bit acceleration value is input into a summer clocked at 8MHz.
- The carry from the summer circuit is output to the PCM pin.

A block diagram of the PCM output is shown in [Figure 27](#).

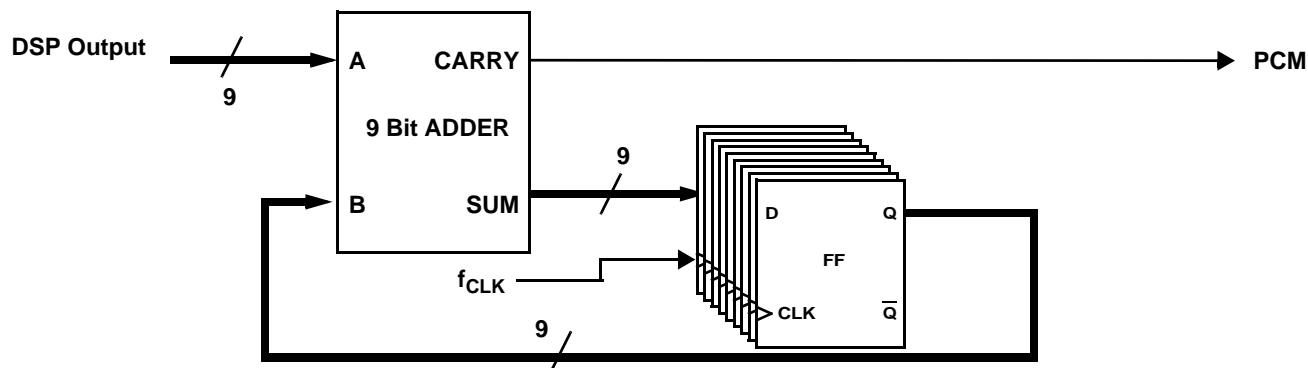


Figure 27. PCM output function block diagram

3.6 DSI3 physical layer

3.6.1 Command receiver

The command receive block converts voltage transitions on the BUS_I pin to a digital pulse train for decoding by the DSI data link layer.

The supply voltage can vary throughout the specified range, so the communication high voltage (V_{HIGH}) must be sampled and averaged with a low-pass filter. The communication low voltage is then determined by comparing the supply voltage to the sampled and averaged V_{HIGH} voltage. Figure 28 shows a block diagram of the command receiver physical layer.

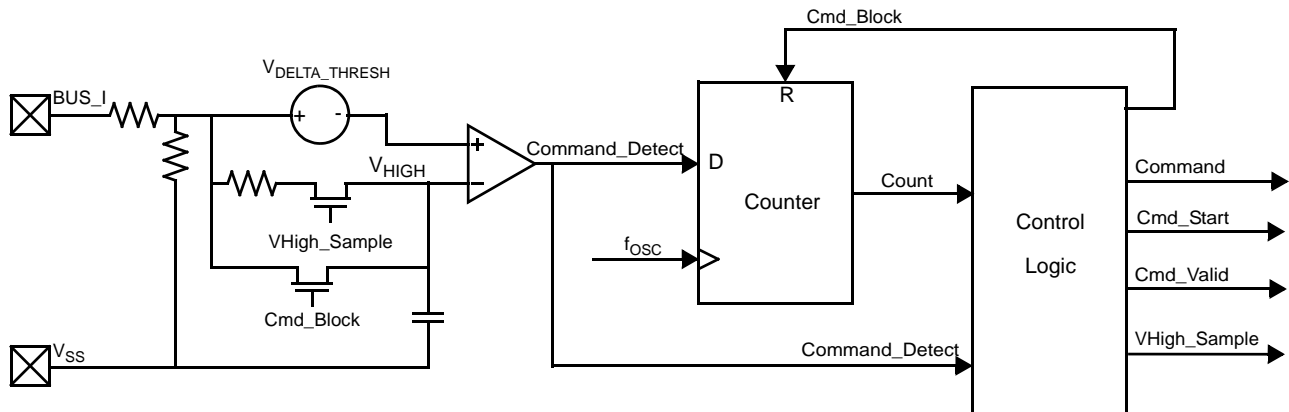


Figure 28. Command receiver physical layer

The start of a command is detected when the comparator output (Command_Detect) is low. The comparator output is input to a counter that is updated at the internal oscillator frequency. Control logic monitors the counter output and generates the following signals:

1. Cmd_Start
 - a) Asserted when the counter reaches a value of one.
 - b) Deasserted at POR, if the counter does not reach Cmd_Valid_Count (t_{Cmd_Valid}) within $t_{Cmd_BitTime}$ of Cmd_Start assertion, or at the end of the command blocking time for the operating mode ($t_{CmdBlock_DISC}$, $t_{CmdBlock_CRM}$, $t_{CmdBlock_PDCM}$, $t_{CmdBlock_BDM}$).
2. Cmd_Valid
 - a) Asserted if the counter reaches Cmd_Valid_Count within $t_{CMD_BitTime}$ of Cmd_Start assertion (t_{Cmd_Valid}).
 - b) Deasserted at POR and when Cmd_Start is deasserted.
3. VHigh_Sample
 - a) Asserted $t_{DSI_DISC_POR}$ after POR and when Cmd_Start is deasserted.
 - b) Deasserted when Cmd_Start is asserted.
4. Cmd_Block:
 - a) Asserted based on the operating mode:
 - Discovery Mode: A complete command is received as defined in Section 4.1.3 and Section 2.6.
 - Command and Response Mode: A complete command is received as defined in Section 4.2 and Section 2.6.
 - Periodic Data Collection Mode: A complete command is received as defined in Section 4.3 and Section 2.6.
 - b) Deasserted at POR and when Cmd_Start is deasserted.

Once a full command is received, based on the operating mode, the command is transferred to the DSI data link layer for decoding.

Figure 29 shows a timing diagram of the command receiver when a valid command is received, and Figure 30 shows a timing diagram of the command receiver when a microcut is received during the command window. Voltage values and timing parameters are specified in Section 2.3 and Section 2.7.

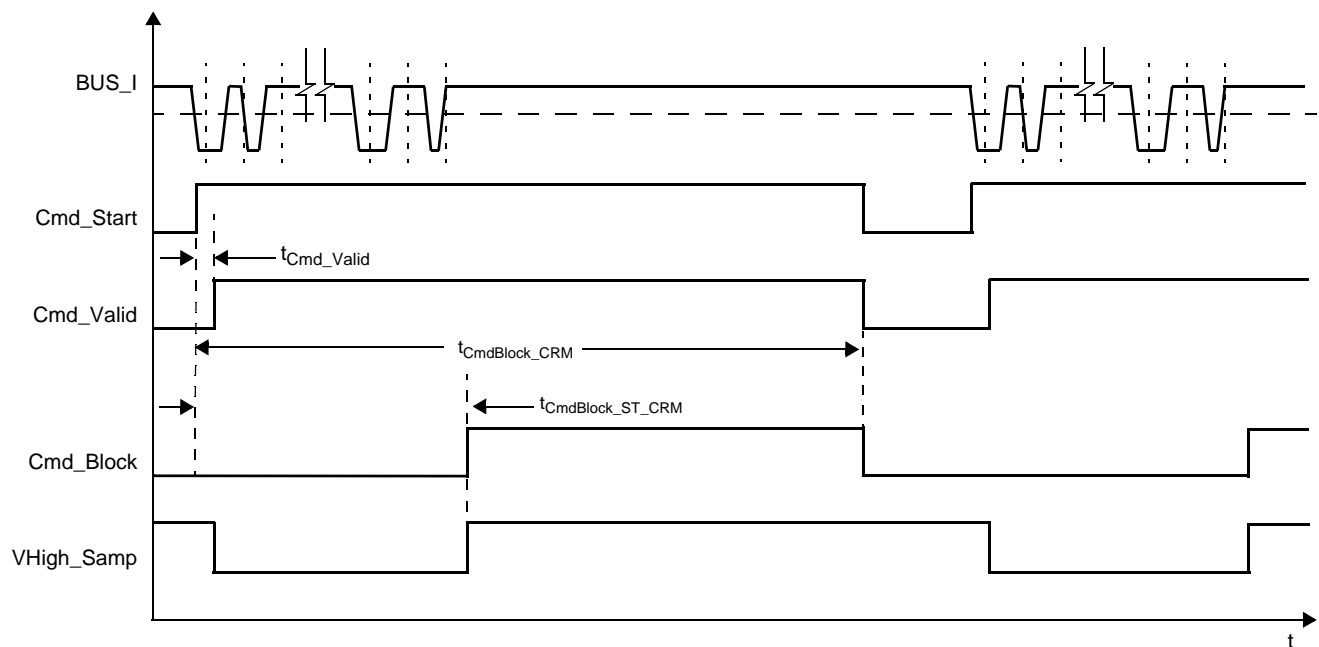


Figure 29. DSI3 Command receiver timing diagram: Valid command

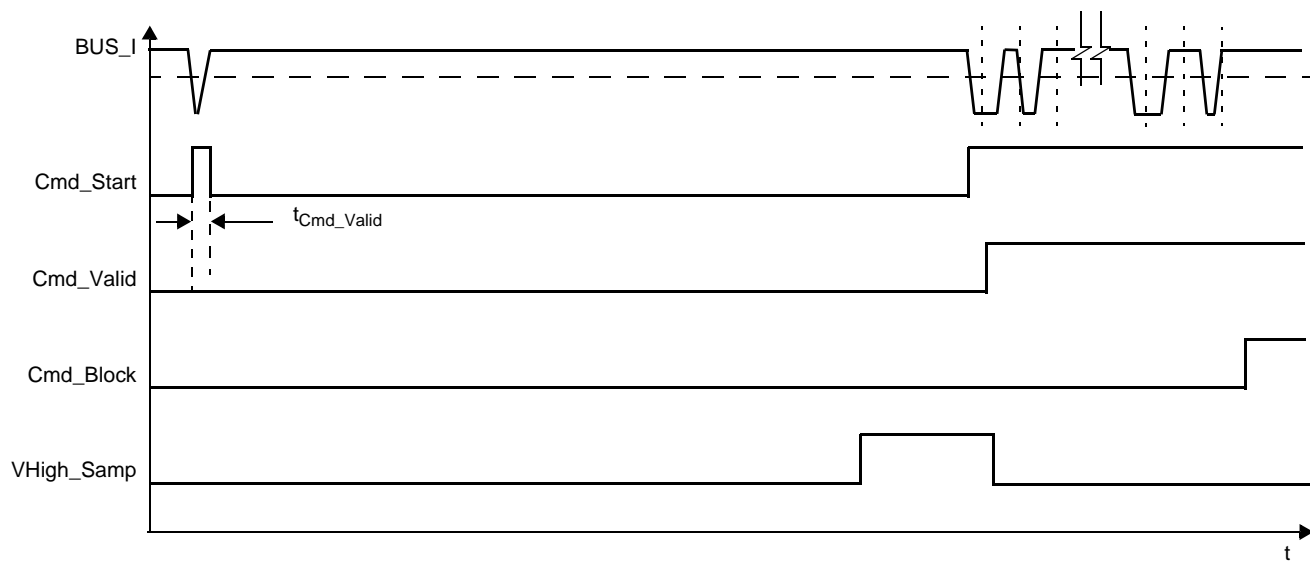


Figure 30. DSI3 Command receiver timing diagram: Microcut

3.6.2 Response transmitter

The response transmitter block converts two digital signals into two supply modulation currents. The response currents are generated such that the rise and fall times are the same whether the I_{RESP} current is being transmitted or the $2 \times I_{RESP}$ current is being transmitted. A diagram of the response transmitter is shown in Figure 29. Current values and timing parameters are specified in Section 2.3 and Section 2.7.

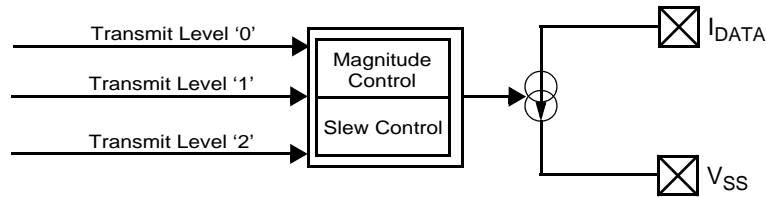


Figure 31. DSI3 transmitter block diagram

3.6.3 Discovery Mode current sense

The current sense circuit is used during Discovery Mode to determine if any additional slaves are connected to the BUS_O pin of the device. A diagram of the current sense circuit is shown in Figure 32. Current values and timing parameters are specified in Section 2.3 and Section 2.7. Details regarding Discovery Mode are included in Section 4.1.3.

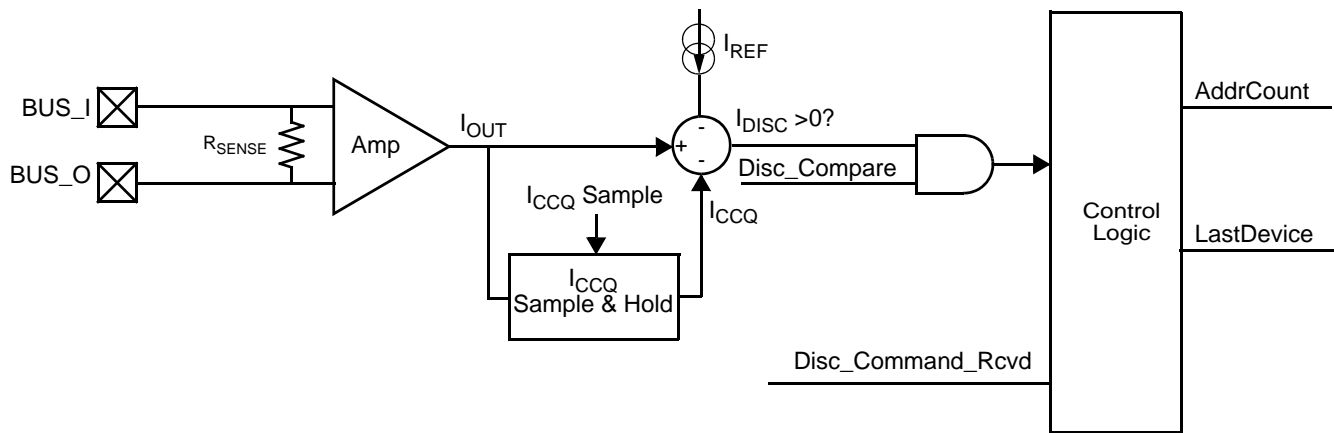


Figure 32. Discovery Mode current sense circuit block diagram

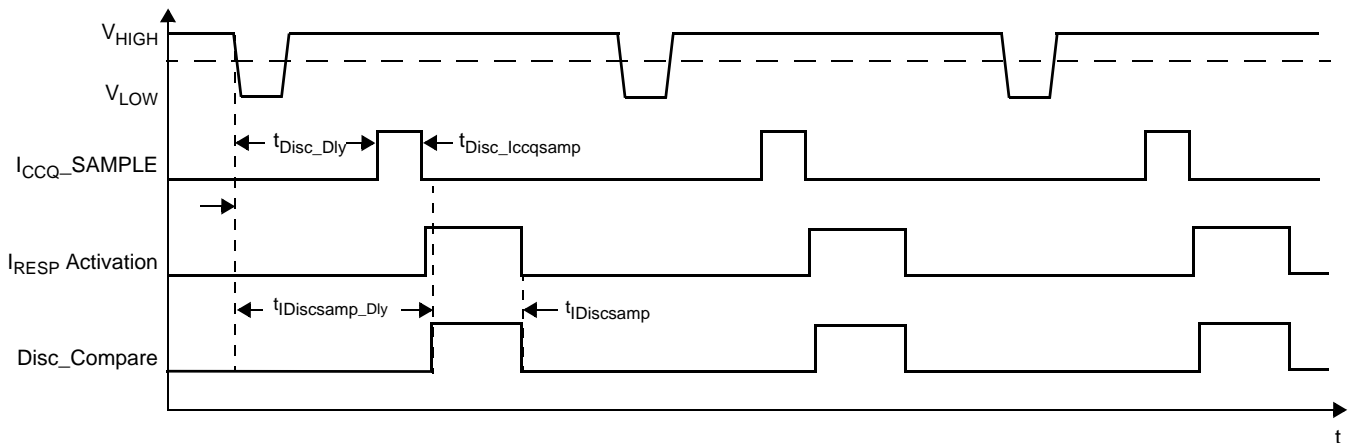


Figure 33. DSI3 Discovery Mode sensing timing diagram

3.6.4 Bus-switch control

The bus-switch output pin is the driver for a high-side, daisy-chain switch. When switch connected daisy-chain mode is used, as described in [Section 4.1.2](#), the BUSSW pin is connected to the gate of an external p-channel FET which connects BUS_I to the next slave in the daisy chain. If used, an external pullup resistor is required on the gate of the p-channel FET. Reference [Figure 3 on page 5](#) for details on the recommended external circuitry.

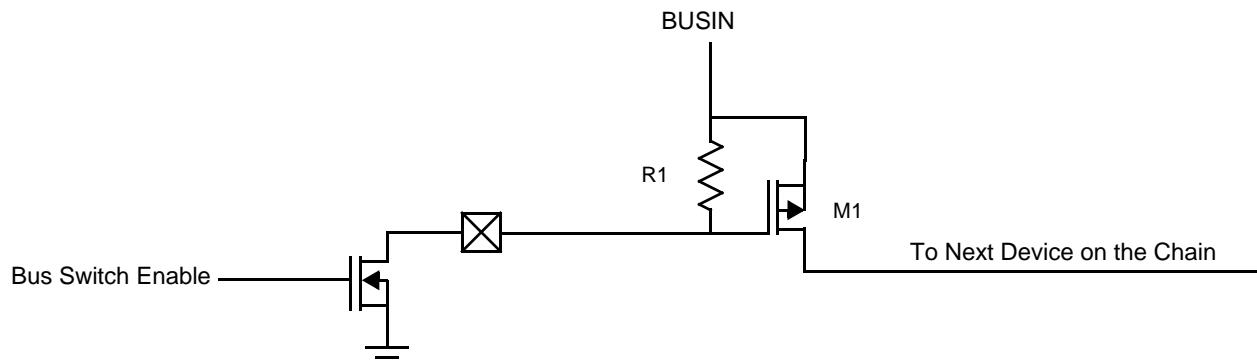


Figure 34. Daisy-chain bus switch driver block diagram

3.7 Data transmission modes

3.7.1 Simultaneous Sampling mode

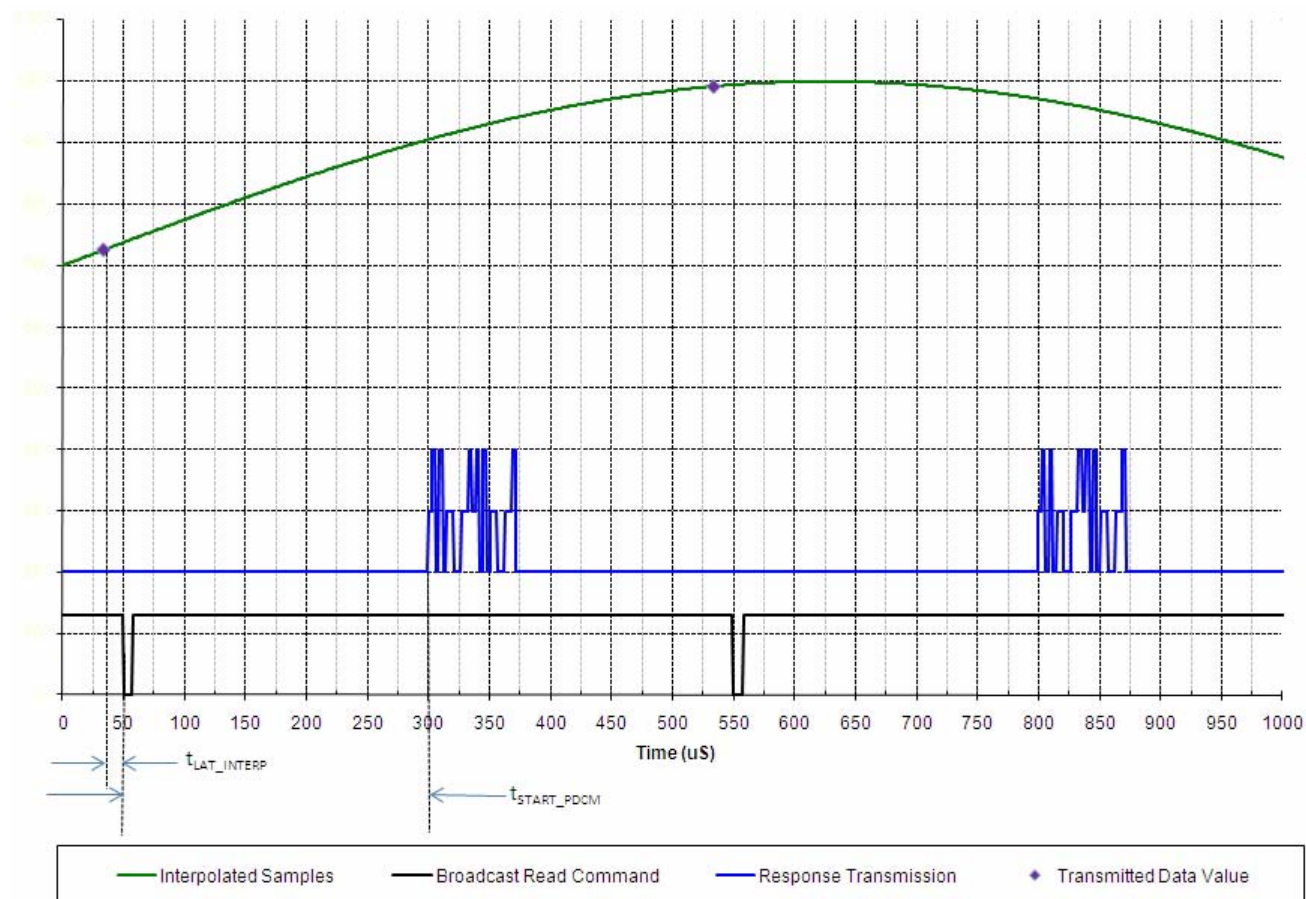


Figure 35. Simultaneous Sampling mode

3.7.2 Synchronous Sampling mode with minimum latency

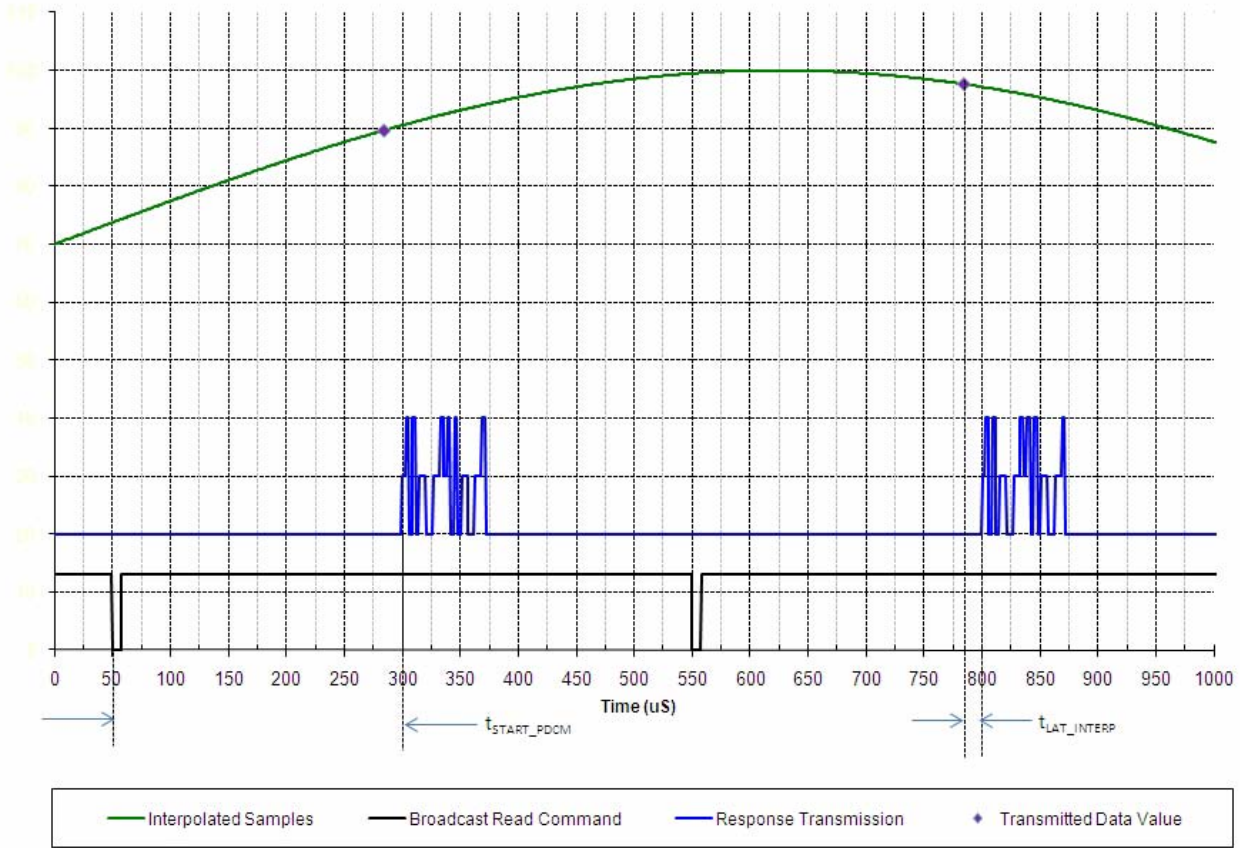


Figure 36. Synchronous sampling mode with minimum latency

3.8 Initialization timing

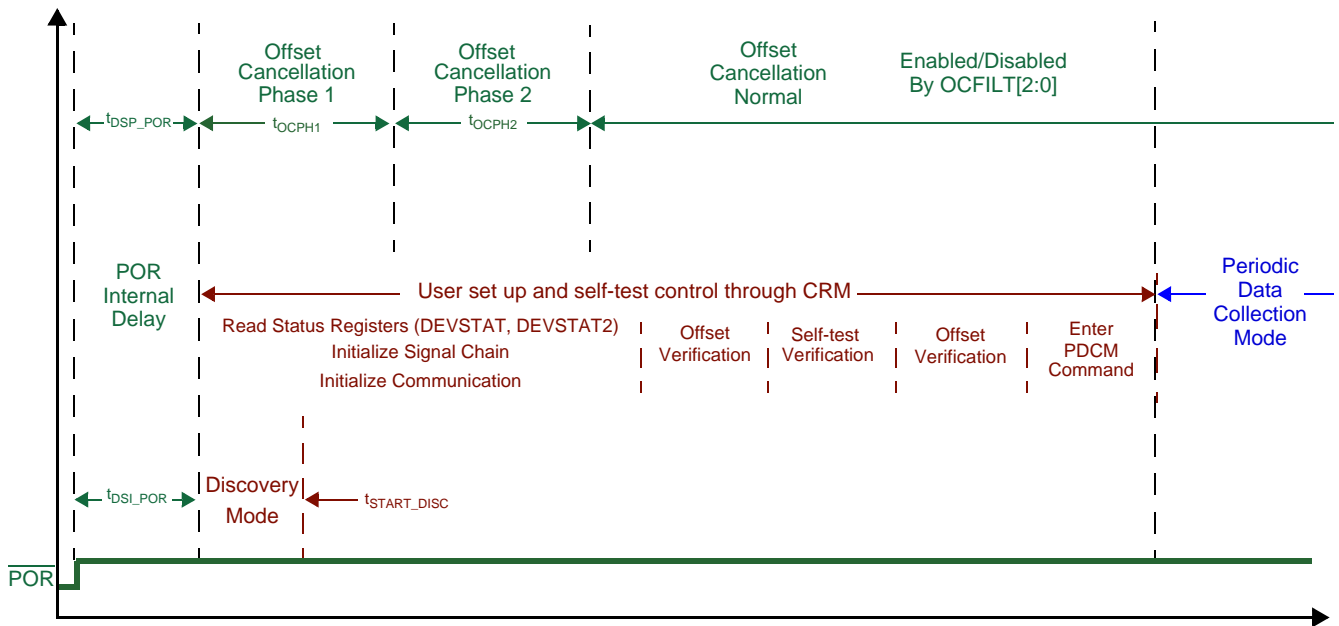


Figure 37. Initialization timing

3.9 Overload response

3.9.1 Overload performance

The device is designed to operate within a specified range. Acceleration beyond that range (overload) impacts the output of the sensor. Acceleration beyond the range of the device can generate a DC shift at the output of the device that is dependent upon the overload frequency and amplitude. The g-cell is overdamped, providing the optimal design for overload performance. However, the performance of the device during an overload condition is affected by many other parameters, including:

- g-cell damping
- Non-linearity
- Clipping limits
- Symmetry

Figure 38 shows the g-cell, ADC and output clipping of the device over frequency. The relevant parameters are specified in Section 2.

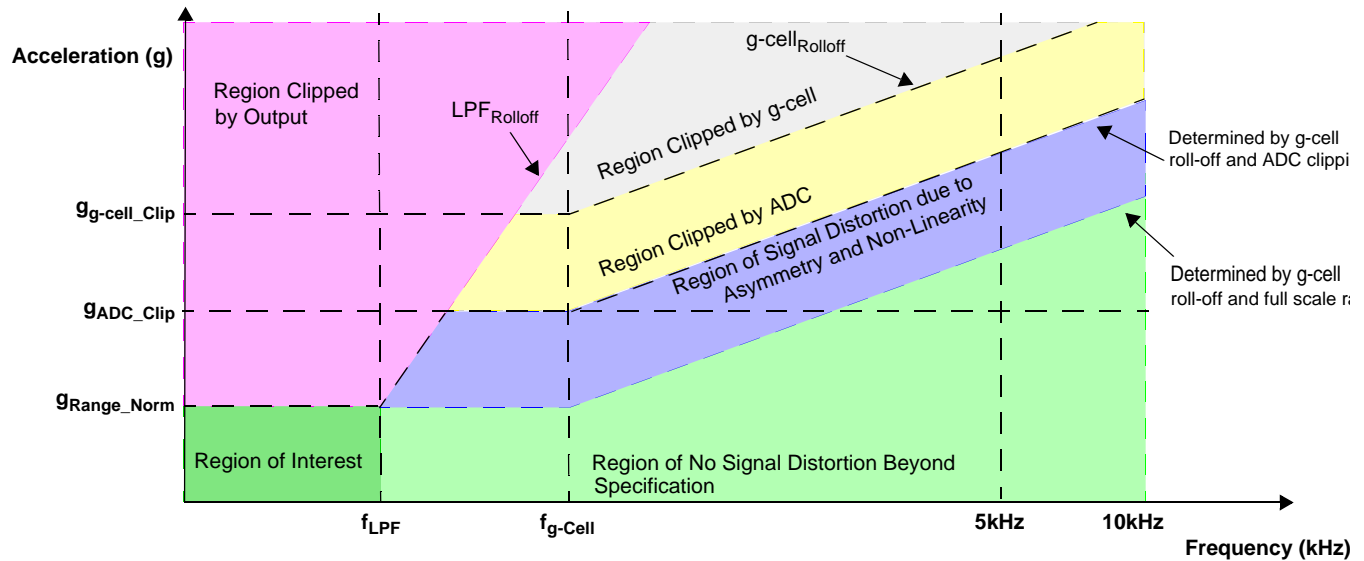


Figure 38. Output clipping vs. frequency

3.9.2 Sigma Delta modulator overrange response

Overrange conditions exist when the signal level is beyond the full-scale range of the device but within the computational limits of the DSP. The $\Sigma\Delta$ converter can saturate at levels above those specified in Section 2 (G_{ADC_CLIP}). The DSP operates predictably under all cases of overrange, although the signal may include residual high-frequency components for some time after returning to the normal range of operation due to non-linear effects of the sensor.

4 DSI3 Protocol

The DSI3 standard describes two function classes: Signal Function Class and Power Function Class. This device is a slave conforming to the Signal Function Class requirements. The device does not support Power Function Class. The following sections describe the DSI3 Signal Function Class features supported by the device.

4.1 Address assignment

The device supports all three address assignment methods described in the DSI3 standard as described below.

4.1.1 Address assignment method for parallel connected slaves

Devices connected in parallel must have preprogrammed addresses by storing a non-zero value into the PADDR[3:0] bits of the PHYSADDR NVM register. If a non-zero value is stored in this NVM register, The device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration. Reference [Section 4.2](#) for details regarding Command and Response Mode.

4.1.2 Address assignment method for bus switch connected daisy-chain devices

A device connected in daisy chain by a bus switch may have either a preprogrammed address as described in [Section 4.1.1](#), or an un-programmed address.

If the address is preprogrammed, the device does not participate in any other address assignment method and waits for Command and Response Mode for further configuration information, including activating the bus switch to connect the next device on the bus. Reference [Section 4.2](#) for details regarding Command and Response Mode.

If the address is un-programmed, once power is applied, the device is the only device on the segment which requires an address assignment. The device will accept a Command and Response Mode register write command addressed to Address \$0 (global command), which writes the PADDR[3:0] bits to a non-zero value. Once a physical address is assigned to the device, Command and Response Mode is used with the assigned physical address for further configuration. This includes closing the bus switch to connect the next device and/or bus segment to the master.

On power up, the device bus switch output defaults to de-activated.

4.1.3 DSI3 Discovery Mode: Address assignment method for resistor connected daisy-chain devices

A device connected via in daisy chain via a resistor has an un-programmed address and uses Discovery Mode to obtain it's physical address (PADDR[3:0]).

The Master device must initiate Discovery Mode automatically after power is applied to the bus segment by sending a sequence of Discovery commands. The Discovery Command is shown in [Figure 39](#) and the timing is defined in [Section 2.6](#). The device will detect a Discovery Command t_{START_DISC} after a power on reset and for intervals of t_{PER_DISC} until Discovery Mode has ended (the maximum value of t_{START_DISC}).

The Discovery Mode follows the sequence listed below. [Figure 39](#) shows a timing diagram of the Discover Protocol for a four device segment.

1. The master powers up the bus segment to a known state.
2. The master transmits the Discovery Command.
3. After a predetermined delay ($t_{START_DISC_RSP}$), all devices without a physical address activate a current ramp to the 2x response current at a ramp rate of i_{DISC_RAMP} .
4. Each device monitors the current through its sense resistor (Δi_{SENSE}).
 - a) If the current is above i_{RESP} , the device disables its response current, increments its physical address counter and waits for the next Discovery Command.
 - b) If the current is low (Δi_{SENSE} less than i_{RESP}), the device continues to ramp its response current to $2 * i_{RESP}$ in time $t_{DISC_RAMP_RSP}$ and maintains the current at $2 * i_{RESP}$ for time $t_{DISC_IDLE_RSP}$.
 - c) After time $t_{DISC_IDLE_RSP}$ if a device has not detected a current through its current sense resistor of i_{RESP} the device accepts physical address '1' and disables its response current.
5. After a predefined period (t_{PER_DISC}), the master transmits another Discovery Command.
6. Steps 3 and 4 are repeated, with the device accepting the address in its address assignment counter if the sense current is low.
7. The master repeats step 5 until it has transmitted Discovery Commands for all the devices it expects on the bus.
8. Device initialization can now begin using Command and Response Mode.

Once the Discovery Mode is complete, a physical address is assigned to the device, and Command and Response Mode is used with the assigned physical address for further configuration.

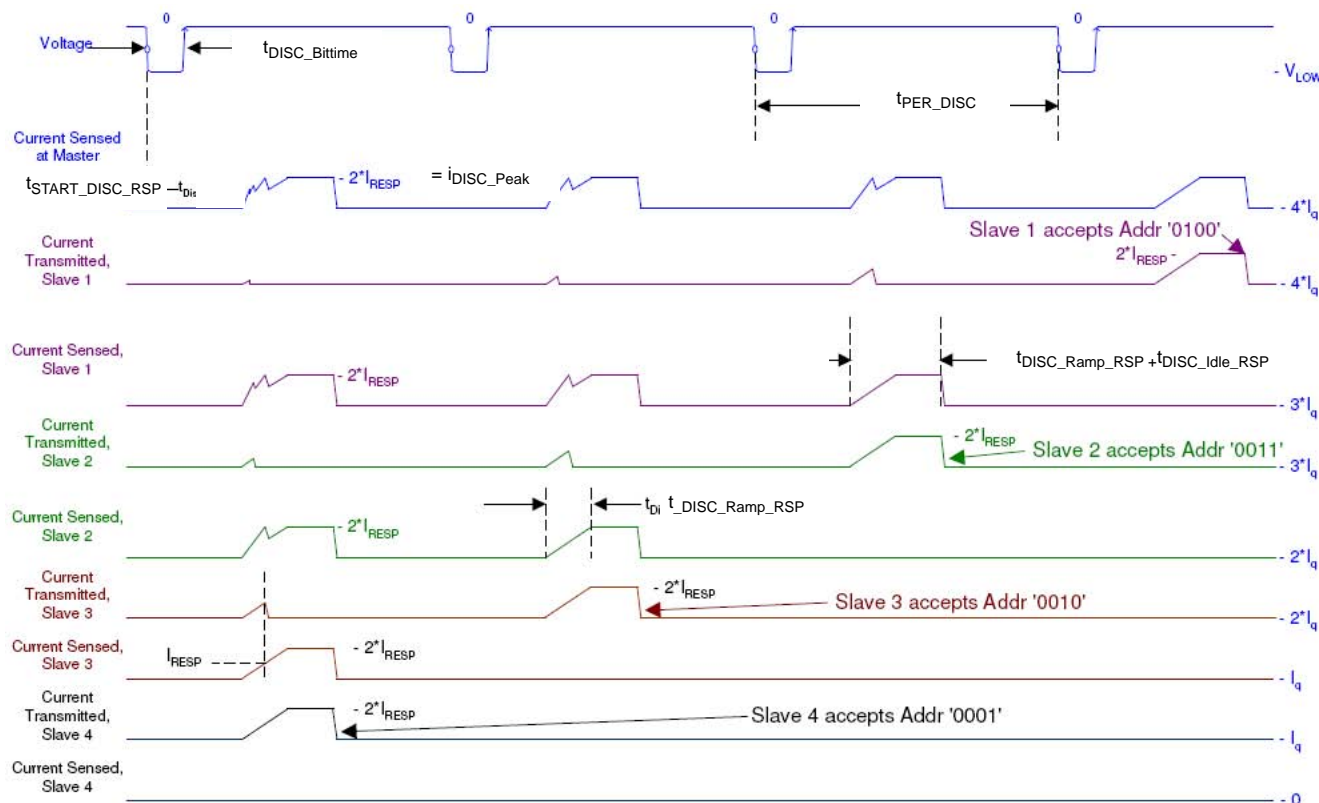


Figure 39. DSI3 Discovery Mode timing diagram

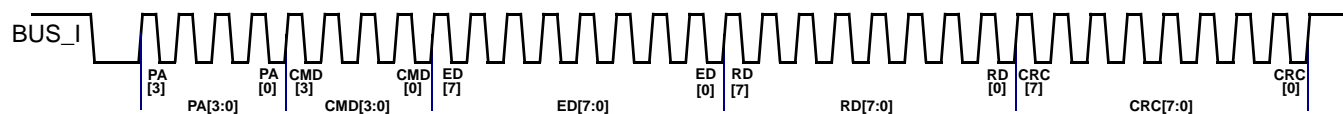
4.2 DSI3 Command and Response Mode

DSI3 Command and Response Mode is the main communication method used for initialization of the device.

4.2.1 DSI3 Command and Response Mode Command reception

Command and Response Mode data packets are exchanged between a single master and a single slave. The primary purpose of command and response transactions are to read from and write to registers within the device memory.

An example Command and Response Mode Command is shown in Figure 40. The command consists of 32 bits of data broken up into multiple fields as described in Section 4.2.1.2.



| Physical Address | | | | Command | | | | Extended Data | | | | | | | | Register Data | | | | | | | | Error Checking | | | | | | | |
|------------------|-----|-----|-----|---------|----|----|----|---------------|-----|-----|-----|-----|-----|----|----|---------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

Figure 40. Command and Response Mode example command

4.2.1.1 Bit encoding

Figure 41 shows the bit encoding used for Command and Response Mode commands from the master device.

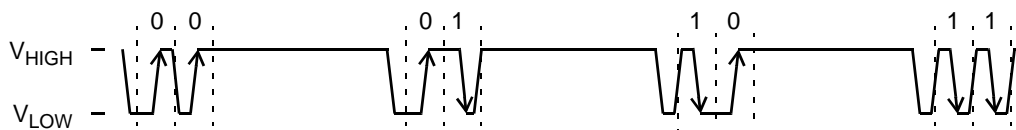


Figure 41. Command and Response Mode Command bit encoding

4.2.1.2 Command message format

The Command and Response Mode Command format is shown in Table 38.

Table 38. Command and Response Mode - Command Format

| Physical address | Command | Extended Data | Register Data | CRC |
|------------------|----------|---------------|---------------|----------|
| PA[3:0] | CMD[3:0] | ED[7:0] | RD[7:0] | CRC[7:0] |

Table 39. Command and Response Mode - Field Definitions

| Field | Length (bits) | Definition |
|----------|---------------|---|
| PA[3:0] | 4 | Physical Address Must match the value in the PADDR[3:0] of the PHYSADDR register |
| CMD[3:0] | 4 | Command (reference Section 4.2.4) |
| ED[7:0] | 8 | Extended Data (reference Section 4.2.4) |
| RD[7:0] | 8 | Register Data (reference Section 4.2.4) |
| CRC[7:0] | 8 | Error Checking (reference Section 4.2.1.3) |

4.2.1.3 Error checking

The device calculates a 8-bit CRC on the entire 32-bits of each command. Data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC decoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
4. If the shift register contains all zeros, the CRC is correct.
5. If the shift register contains a value other than zero, the CRC is incorrect.

The CRC polynomial is specified in the C_CRMCRCPLY register. The CRC default polynomial and Seed for Command and Response Mode are shown in [Table 40](#).

Table 40. Command and Response Mode Command CRC

| Mode | Default Polynomial | Seed |
|---------------------------|---------------------------------|-----------|
| Command and Response Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |

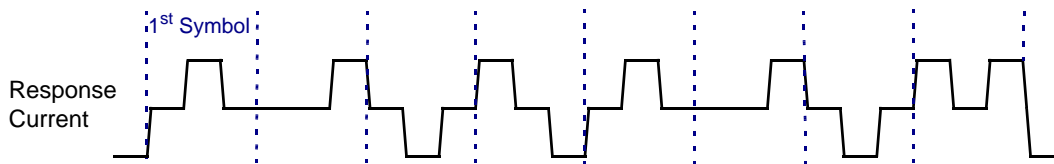
Some example CRC calculations are shown in [Table 41](#).

Table 41. Command and Response Mode - CRC Calculation Examples

| Physical Address | Command | Extended Data | Register Data | 8 Bit CRC |
|------------------|---------|---------------|---------------|-----------|
| 0x01 | 0x08 | 0x11 | 0x86 | 0xB0 |
| 0x02 | 0x01 | 0x25 | 0xFF | 0x38 |
| 0x03 | 0x0F | 0x1A | 0x41 | 0x2C |
| 0x04 | 0x01 | 0x01 | 0x01 | 0xD4 |

4.2.2 DSI3 Command and Response Mode Response Transmission

An example Command and Response Mode Response is shown in [Figure 42](#). The response consists of 32 bits of data broken up into multiple fields as described in [Section 4.2.2.2](#).

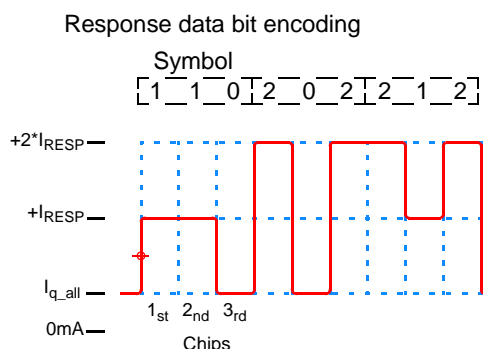


| Physical Address | | | | Command | | | | Extended Data | | | | | | | | Register Data | | | | | | | | Error Checking | | | | | | | |
|------------------|-----|-----|-----|---------|----|----|----|---------------|-----|-----|-----|-----|-----|----|----|---------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

Figure 42. Command and Response Mode Response example

4.2.2.1 Symbol Encoding

The device response to a Command and Response Mode Command uses multi-level source coding where data nibbles are first encoded into symbols and then the symbols are encoded into current levels. The symbols are assembled from three consecutive three-level current pulses called chips. Within a symbol there are three consecutive chips that can assume one of three discrete current levels: i_q , $i_q + i_{RESP}$ and $i_q + 2 \times i_{RESP}$. Figure 43 shows the chip transmissions and an example of a three symbol (nine chip), 12-bit data packet.



Each symbol encodes four data bits

Figure 43. Response symbol encoding

Of the 27 possible combinations for three consecutive tri-level chips, the combinations that begin with the null current level (i_q) are discarded. Of the remaining 18 symbols, the two symbols that contain the same value for all three chips are also discarded. The remaining 16 symbols all begin with a non-null current level and have at least one transition. These characteristics guarantee that any response packet has a transition at the beginning of a packet and at least one transition in every symbol. Each 3-chip symbol encodes the information of 4-bits. Table 42 shows the symbol encoding used by the device.

Table 42. Symbol mapping

| Encoded Data (4 Bits) | | Symbol Transmitted | | |
|-----------------------|-----|--------------------|----------|----------|
| Binary | HEX | 1st Chip | 2nd Chip | 3rd Chip |
| 0000 | 0 | 1 | 1 | 0 |
| 0001 | 1 | 2 | 1 | 1 |
| 0010 | 2 | 1 | 0 | 2 |
| 0011 | 3 | 2 | 0 | 2 |
| 0100 | 4 | 1 | 0 | 0 |
| 0101 | 5 | 2 | 1 | 2 |
| 0110 | 6 | 1 | 1 | 2 |
| 0111 | 7 | 2 | 0 | 1 |
| 1000 | 8 | 2 | 2 | 0 |
| 1001 | 9 | 2 | 1 | 0 |
| 1010 | A | 1 | 2 | 2 |
| 1011 | B | 2 | 2 | 1 |
| 1100 | C | 1 | 2 | 0 |
| 1101 | D | 2 | 0 | 0 |
| 1110 | E | 1 | 0 | 1 |
| 1111 | F | 1 | 2 | 1 |

where:
 0 = i_q
 1 = i_{RESP}
 2 = $2 \times i_{RESP}$

4.2.2.2 Response Message Format

The Command and Response Mode response format is shown in [Table 43](#).

Table 43. Command and Response Mode response format

| Physical Address | Command | Register + 1 Data | Register Data | CRC |
|------------------|----------|-------------------|---------------|----------|
| PA[3:0] | CMD[3:0] | RD1[7:0] | RD[7:0] | CRC[7:0] |

Table 44. Command and Response Mode field definitions

| Field | Length (Bits) | Definition |
|----------|---------------|---|
| PA[3:0] | 4 | Physical Address Matches the value in the PADDR[3:0] of the PHYSADDR register |
| CMD[3:0] | 4 | An echo of the received command |
| ED[7:0] | 8 | The data contained in the register addressed by RA[7:0] +1 (reference Section 4.2.4) |
| RD[7:0] | 8 | The data contained in the register addressed by RA[7:0] (reference Section 4.2.4) |
| CRC[7:0] | 8 | Error Checking (reference Section 4.2.2.3) |

4.2.2.3 Error Checking

The device calculates a CRC on the entire 32-bits of each response. Data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial is specified in the R_CRMCRCPLY register. The CRC default polynomial and Seed for Command and Response Mode are shown in [Table 45](#).

Table 45. Command and Response Mode Response CRC

| Mode | Default Polynomial | Seed |
|---------------------------|---------------------------------|-----------|
| Command and Response Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | 1111 1111 |

Some example CRC calculations are shown in [Table 41](#).

4.2.3 DSI3 Command and Response Mode timing

A timing diagram for Command and Response Mode is shown in Figure 44. Timing parameters are specified in Section 2.7.

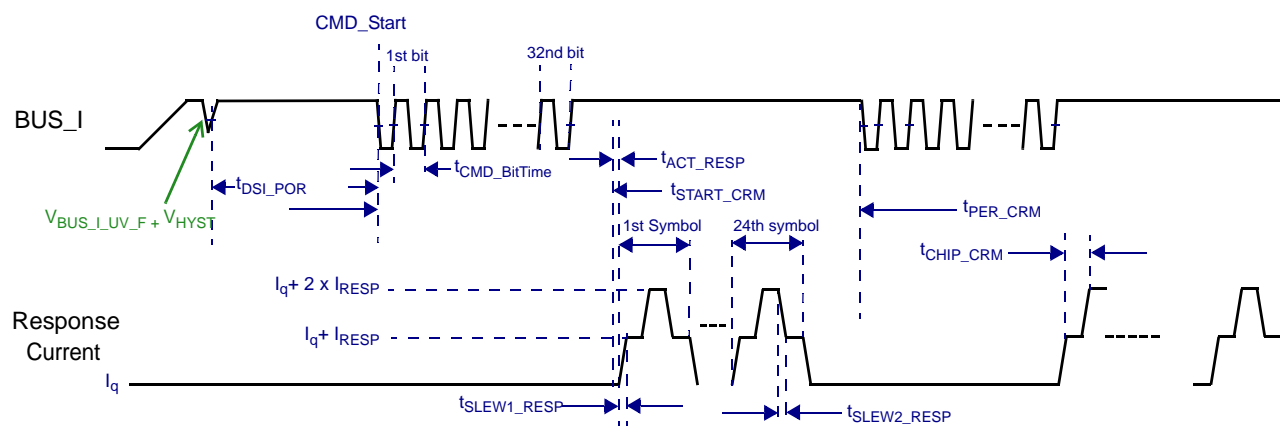


Figure 44. Command and Response Mode timing diagram

4.2.4 DSI3 Command and Response Mode command summary

Table 46. DSI bus command summary

| Command | | | | | | Data | | | | | | | | | | | | | | | |
|---------|----|----|----|-----|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| C3 | C2 | C1 | C0 | Hex | Description | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | \$0 | Register Read | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | \$1 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | \$2 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | \$3 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | \$4 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | \$5 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | \$6 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | \$7 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | \$8 | Register Write | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] |
| 1 | 0 | 0 | 1 | \$9 | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | \$A | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | \$B | Enter PDCM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | \$C | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | \$D | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | \$E | Not Implemented | N/A | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | \$F | Not Implemented | N/A | | | | | | | | | | | | | | | |

4.2.4.1 Register Read Command

The device supports the Register Read Command as a device address specific command only. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device responds to the command.

The device ignores the Register Read Command if the command is sent to any other physical address, including the DSI Global Device Address of '0000'.

The Register Read Command uses the byte address definitions shown in Table 4. Readable registers along with their Byte addresses are shown in Table 4. If an attempt is made to read a register that is not readable, the device will respond with all zero data.

Table 47. Register Read Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---------|-------|-------|-------|---------|----|----|----|-------|-------|-------|-------|-------|-------|-------|-------|----|----|----|----|----|----|----|----|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | 0 | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

Table 48. Register Read Command bit definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored. |
| C[3:0] | Register Read Command = '0000' |
| RA[7:0] | RA[7:0] contains the byte address of the register to be read. |

Table 49. Response - Register Read Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---------|-------|-------|-------|---------|----|----|----|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

Table 50. Register Read Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Read Command = '0000' |
| RD[15:8] | The data contained in the register addressed by RA[7:0] +1 |
| RD[7:0] | The data contained in the register addressed by RA[7:0] |

4.2.4.2 Register Write Command

The device supports the Register Write Command as a device address specific command. If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will execute the register write and respond to the command.

The device ignores the Register Write Command if the command is sent to any other physical address, including the DSI Global Device Address of '0000', with one exception as explained in [Section 4.2.4.3](#).

The Register Write Command uses the byte address definitions shown in [Table 4](#). Writable registers along with their Byte addresses are shown in [Table 4](#). If an attempt is made to write to a register that is not writable, the device will respond with all zero data.

Table 51. Register Write Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---------|-------|-------|-------|---------|----|----|----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RA[7] | RA[6] | RA[5] | RA[4] | RA[3] | RA[2] | RA[1] | RA[0] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

Table 52. Register Write Command bit definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register. Otherwise, the command is ignored. |
| C[3:0] | Register Write Command = '1000' |
| RA[7:0] | RA[7:0] contains the byte address of the register to be read. |
| RD[7:0] | RD[7:0] contains the data to be written to the register addressed by RA[7:0]. |

Table 53. Response - Register Write Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---------|-------|-------|-------|---------|----|----|----|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

Table 54. Register Write Response bit definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Write Command = '1000' |
| RD[15:8] | The data contained in the register addressed by RA[7:0] +1 |
| RD[7:0] | The data contained in the register addressed by RA[7:0] (after the register write is executed) |

4.2.4.3 Global Register Write Command to the PHYSADDR register

The device supports the Register Write Command as a global address under the following conditions:

1. The Register Write Command is written to the PHYSADDR register (\$11).
2. The PADDR[3:0] bits of the PHYSADDR register are equal to '0000' prior to the register write being executed.

If these conditions are met, the device will execute the register write and respond to the command.

Table 55. Global Register Write Command to the PHYSADDR register

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC | |
|---------|-----|-----|-----|---------|----|----|----|------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|-------|-------|-------|-------|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

Table 56. Register Write Command bit definitions

| Bit Field | Definition |
|-----------|---|
| PA[3:0] | The DSI Global address of '0000'. |
| C[3:0] | Register Write Command = 1000' |
| RA[7:0] | RA[7:0] must be set to the PHYSADDR register address (\$11) |
| RD[3:0] | RD[3:0] contains the new physical address for the device. |

Table 57. Response - Global Register Write Command to the PHYSADDR register

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | | | CRC |
|---------|-------|-------|-------|---------|----|----|----|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 0 | 0 | RD[15] | RD[14] | RD[13] | RD[12] | RD[11] | RD[10] | RD[9] | RD[8] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 8 bits |

Table 58. Register Write Response bit definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | The new DSI physical address programmed to the PADDR[3:0] bits in the PHYSADDR register. |
| C[3:0] | Register Write Command = 1000' |
| RD[15:8] | The data contained in register by \$12 |
| RD[7:0] | The data contained in the PHYSADDR register after the register write is executed. |

4.2.4.4 Enter Periodic Data Collection Mode Command

The device supports an Enter PDCM Command as a device address specific command and as a Global Command.

If the PA[3:0] field in the command matches the value in the PADDR[3:0] bits of the PHYSADDR register, the device will set the PDCM_EN bit in the PDCM_EN register, enter Periodic Data Collection Mode and respond to the command as shown below. If the PA[3:0] field in the command matches the Global address of '0000', the device will set the PDCM_EN bit in the PDCM_EN register and enter Periodic Data Collection Mode. No response is transmitted for a global command. The device ignores the Enter PDCM command if the command is sent to any other physical address.

Table 59. Enter Periodic Data Collection Mode Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | CRC | | | |
|---------|-------|-------|-------|---------|----|----|----|------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|-----|----|----|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

Table 60. Enter Periodic Data Collection Mode Command bit definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | DSI physical address. This field contains the physical address. This field must match the PADDR[3:0] bits in the PHYSADDR register or the Global Address of '0000'. Otherwise, the command is ignored. |
| C[3:0] | Enter PDCM Command = '1011' |

Table 61. Response - Enter Periodic Data Collection Mode Command

| Address | | | | Command | | | | Data | | | | | | | | | | | | | | CRC | | | |
|---------|-------|-------|-------|---------|----|----|----|------|-----|-----|-----|-----|-----|-------|-------|-------|----|----|----|----|----|-----|----|----|--------|
| PA3 | PA2 | PA1 | PA0 | C3 | C2 | C1 | C0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | | D1 | D0 | |
| PA[3] | PA[2] | PA[1] | PA[0] | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Ch[2] | Ch[1] | Ch[0] | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 bits |

Table 62. Enter Periodic Data Collection Mode Response bit definitions

| Bit Field | Definition |
|-----------|---|
| PA[3:0] | DSI physical address. This field contains the PADDR[3:0] bits in the PHYSADDR register. |
| Ch[2:0] | CHIPTIME[2:0] in the CHIPTIME register |
| C[3:0] | Register Write Command = '1000' |

4.3 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode

When the PDCM_EN bit in the PDCM_EN register is set, Periodic Data Collection Mode is enabled. If the BDM_EN bit in the BDM_CFG register is also set, the optional Background Diagnostic Mode is also enabled.

4.3.1 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode Command Reception

When Periodic Data Collection Mode is enabled, the device will decode the DSI3 Broadcast Read command as well as Background Diagnostic Mode command fragments as described below.

4.3.1.1 Bit Encoding

The Command Bit encoding for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the bit encoding for Command and Response Mode, as described in [Section 4.2.1.1](#).

4.3.1.2 Command Message Format

The command message format for Periodic Data Collection Mode and Background Diagnostic Mode is the same as the command message format for Command and Response Mode, as described in [Section 4.2.1.2](#).

If Background Diagnostic Mode is disabled, then the device responds with the Periodic Data Collection Mode response only if the command is the single bit Broadcast Read Command. A Broadcast Read Command may be either a '1' or a '0'.

If Background Diagnostic Mode is enabled:

- Background Diagnostic Mode commands are transmitted and decoded in 4-bit fragments.
- The device responds with the Periodic Data Collection Mode response if and only if the command is a Broadcast Read Command or a 4-bit command fragment.
- A Broadcast Read Command or any command length other than four bits resets the Background Diagnostic Mode command decode.
- The device responds with a Background Diagnostic Mode response only when eight consecutive 4-bit command fragments are received and the decoded command is a valid Command and Response Mode command.

Refer to [Section 4.3.4](#) for additional details on Background Diagnostic Mode timing.

4.3.1.3 Error checking

The error checking for Background Diagnostic Mode commands is the same as the error checking for Command and Response Mode, and described in [Section 4.2.1.3](#).

No error checking is employed for the Broadcast Read commands.

4.3.2 DSI3 Periodic Data Collection Mode response transmission

When Periodic Data Collection Mode is enabled and the device receives either a Broadcast Read or Background Diagnostic Mode command, the device will respond with periodic data as shown in Figure 45 and described in the following sections.

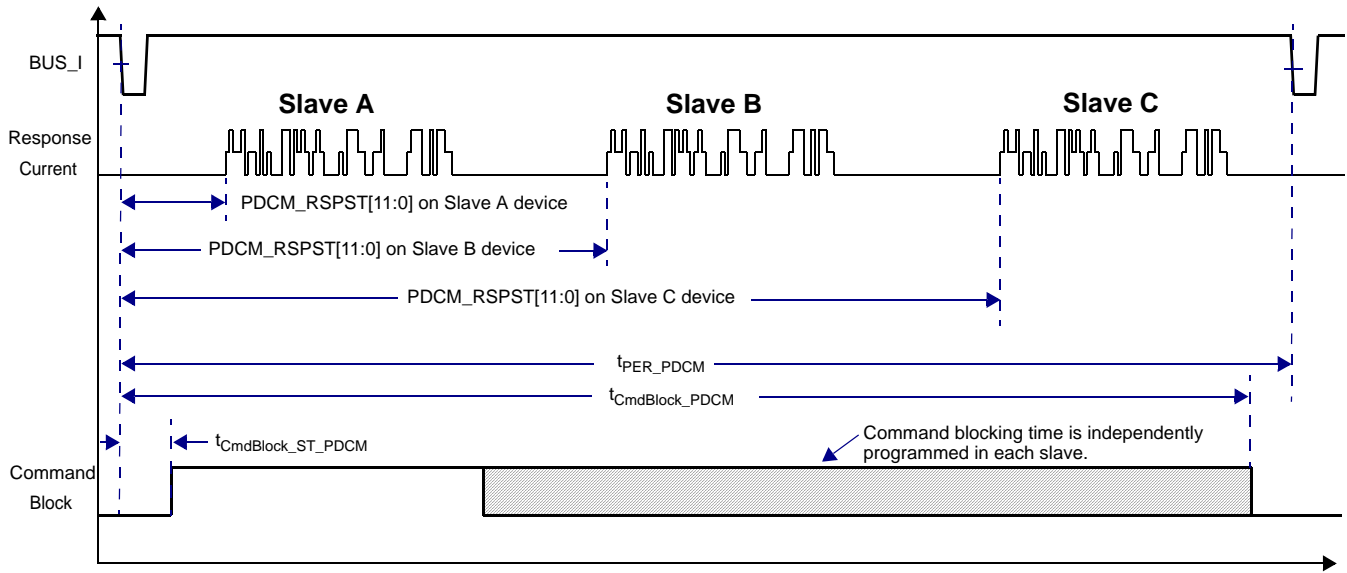


Figure 45. Periodic Data Collection Mode response transmission

4.3.2.1 Symbol encoding

The symbol encoding used for Periodic Data Collection Mode responses is the same as for Command and Response Mode responses, and described in Section 4.2.2.1.

4.3.2.2 Response message format

The Periodic Data Collection Mode response format is shown in Table 63.

Table 63. Periodic Data Collection Mode - response format

| Source ID | Keep Alive Counter | Status | Acceleration Data | CRC |
|--------------|--------------------|--------|-------------------|----------|
| SOURCID[3:0] | KAC[1:0] | S[x:0] | D[x:0] | CRC[7:0] |

Table 64. Periodic Data Collection Mode Response field definitions

| Field | Length (Bits) | Definition |
|--------------|------------------------------------|---|
| SOURCID[3:0] | 4 | Transmits the least significant 4 bits of the SOURCEID register |
| KAC[1:0] | 2 | Transmits the value of a 2-bit rolling counter. The counter is incremented each time a valid Broadcast Read Command is received or a valid Background Diagnostic Mode command is received. The counter does not increment for Command and Response Mode commands or for invalid commands. |
| S[3:0] | STATLEN = 0: 4 STATLEN = 1: 0 | Reference Table 65. |
| D[x:0] | DATALEN = 0: 10 DATALEN = 1, 14 | Transmits the value in the ACC1_D[15:0] registers as defined in Section 3.1.15.1. |
| CRC[7:0] | 8 | Transmits an 8-bit CRC as defined in Section 4.3.2.3 |

The status bit messages and message priority are listed in [Table 65](#). Reference [Section 5](#) for details on exception handling.

Table 65. Periodic Data Collection Mode Status field definitions

| s[3:0] | | | | Description | DEVSTAT State | Error Priority | Acceleration Data Field Value |
|--------|---|---|---|---------------------------------|------------------|----------------|-------------------------------|
| 0 | 0 | 0 | 0 | Normal mode | N/A | NA | Acceleration Data |
| 0 | 0 | 0 | 1 | Offset Error | OFFSET_ERR set | 4 | Acceleration Data |
| 0 | 0 | 1 | 0 | Freescale OTP Array Error | F_OTP_ERR set | 1 | Error Code |
| 0 | 0 | 1 | 1 | User OTP Array Error | U_OTP_ERR set | 2 | Error Code |
| 0 | 1 | 0 | 0 | User Read/Write Array Error | U_RW_ERR set | 3 | Error Code |
| 0 | 1 | 0 | 1 | Reserved | N/A | 8 | Acceleration Data |
| 0 | 1 | 1 | 0 | Reserved | N/A | 9 | Acceleration Data |
| 0 | 1 | 1 | 1 | Oscillator Training Error | OSCTRAIN_ERR set | 6 | Acceleration Data |
| 1 | 0 | 0 | 0 | Self-test Activation Incomplete | ST_INCMPLT set | 5 | Acceleration Data |
| 1 | 0 | 0 | 1 | Reserved | N/A | 7 | Acceleration Data |
| 1 | 0 | 1 | 0 | Reserved | N/A | 10 | Acceleration Data |
| 1 | 0 | 1 | 1 | Reserved | N/A | 11 | Acceleration Data |
| 1 | 1 | 0 | 0 | Reserved | N/A | 12 | Acceleration Data |
| 1 | 1 | 0 | 1 | Reserved | N/A | 13 | Acceleration Data |
| 1 | 1 | 1 | 0 | Reserved | N/A | 14 | Acceleration Data |
| 1 | 1 | 1 | 1 | Test mode active | TESTMODE set | 15 | Error Code |

4.3.2.3 Error checking

The device calculates a CRC on the entire response. Data is entered into the CRC calculator MSB first, consistent with the transmission order of the message.

The CRC Encoding procedure is:

1. A seed value is preset into the least significant bits of the shift register.
2. Using a serial CRC calculation method, the transmitter rotates the transmitted message into the least significant bits of the shift register, MSB first.
3. Following the transmitted message, the transmitter feeds eight zeros into the shift register, to match the length of the CRC.
4. When the last zero is fed into the input adder, the shift register contains the CRC.
5. The CRC is transmitted.

The CRC polynomial is specified in the PDCMCRPLY register. The CRC default polynomial and Seed for Command and Response Mode are shown in [Table 66](#).

Table 66. Periodic Data Collection Mode Response CRC

| Mode | Default Polynomial | Seed |
|-------------------------------|---------------------------------|---------------|
| Periodic Data Collection Mode | $x^8 + x^5 + x^3 + x^2 + x + 1$ | SOURCEID[7:0] |

Some example CRC calculations are shown in [Table 67](#).

Table 67. Periodic Data Collection Mode - CRC Calculation Examples

| Source Identification (4 Bits) | Keep Alive Counter (2 Bits) | Status (4 Bits) | Acceleration Data (10 Bits) | 8-bit CRC |
|--------------------------------|-----------------------------|-----------------|-----------------------------|-----------|
| 0x1 | 0x3 | 0x0 | 0x1FF | 0xD6 |
| 0x2 | 0x2 | 0x0 | 0x1FE | 0x70 |
| 0x3 | 0x1 | 0x0 | 0x20D | 0xB0 |
| 0x4 | 0x0 | 0x0 | 0x1EA | 0x5F |

4.3.3 DSI3 Periodic Data Collection Mode timing

A timing diagram for Periodic Data Collection Mode is shown in [Figure 46](#). Timing parameters are specified in [Section 2.7](#).

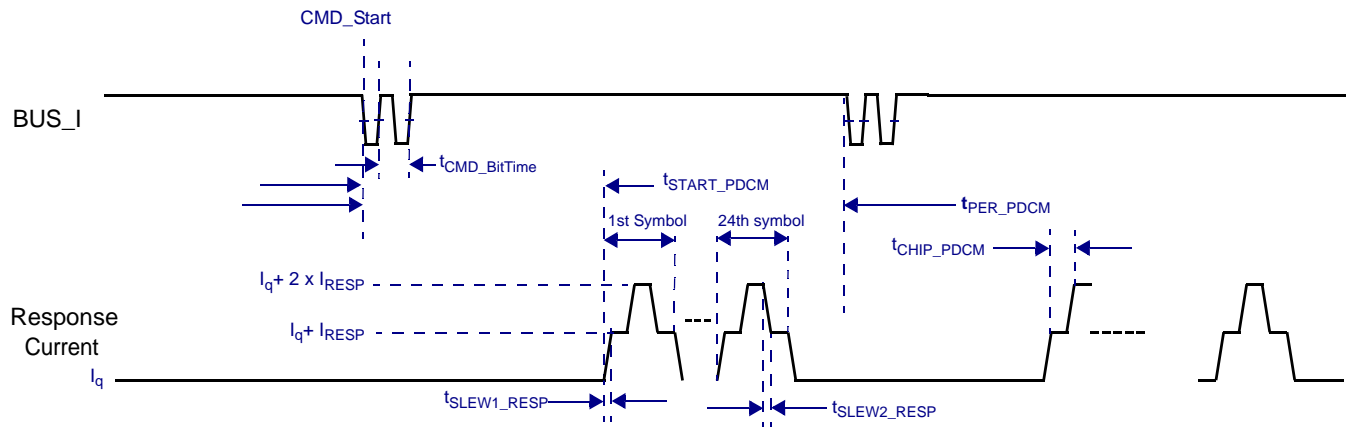


Figure 46. Periodic Data Collection Mode Timing Diagram

4.3.4 Background Diagnostic Mode Response Transmission

4.3.4.1 Symbol Encoding

The Background Diagnostic Mode response symbol encoding is the same as the symbol encoding used for Command and Response Mode responses and is described in [Section 4.2.2.1](#).

4.3.4.2 Response Message Format

The Background Diagnostic Mode response message format is the same as the format used for Command and Response Mode responses and is described in [Section 4.2.2.1](#).

- If a complete 32-bit command is received and decoded to a valid Command and Response Mode command the device provides a Background Diagnostic Mode response.
- Responses are initiated by the master transmitting 1 bit Broadcast Read Commands following a completed Background Diagnostic Mode command transmission.
- Responses are transmitted in one symbol fragments following the 1-bit Broadcast Read Command, using the same timing window within the frame that the Background Diagnostic Mode Command used.
- Responses are transmitted if and only if Broadcast Read Commands are received.
- Eight consecutive Broadcast Read Commands are required following a valid Background Diagnostic Mode command to complete a response transmission.
- If any command other than the Broadcast Read Command is received, no response is transmitted and the remainder of the Broadcast Read Command response is terminated.
- The data to be transmitted in the response is latched just before the first symbol of the Background Diagnostic Mode response.

Reference [Figure 47](#) for Background Diagnostic Mode timing.

4.3.4.3 Error Checking

The error checking for Background Diagnostic Mode responses is the same as used for Command and Response Mode, and described in [Section 4.2.1.3](#).

4.3.5 DSI3 Background Diagnostic Mode Timing

A timing diagram for Background Diagnostic Mode is shown in [Figure 47](#). Timing parameters are specified in [Section 2.7](#).

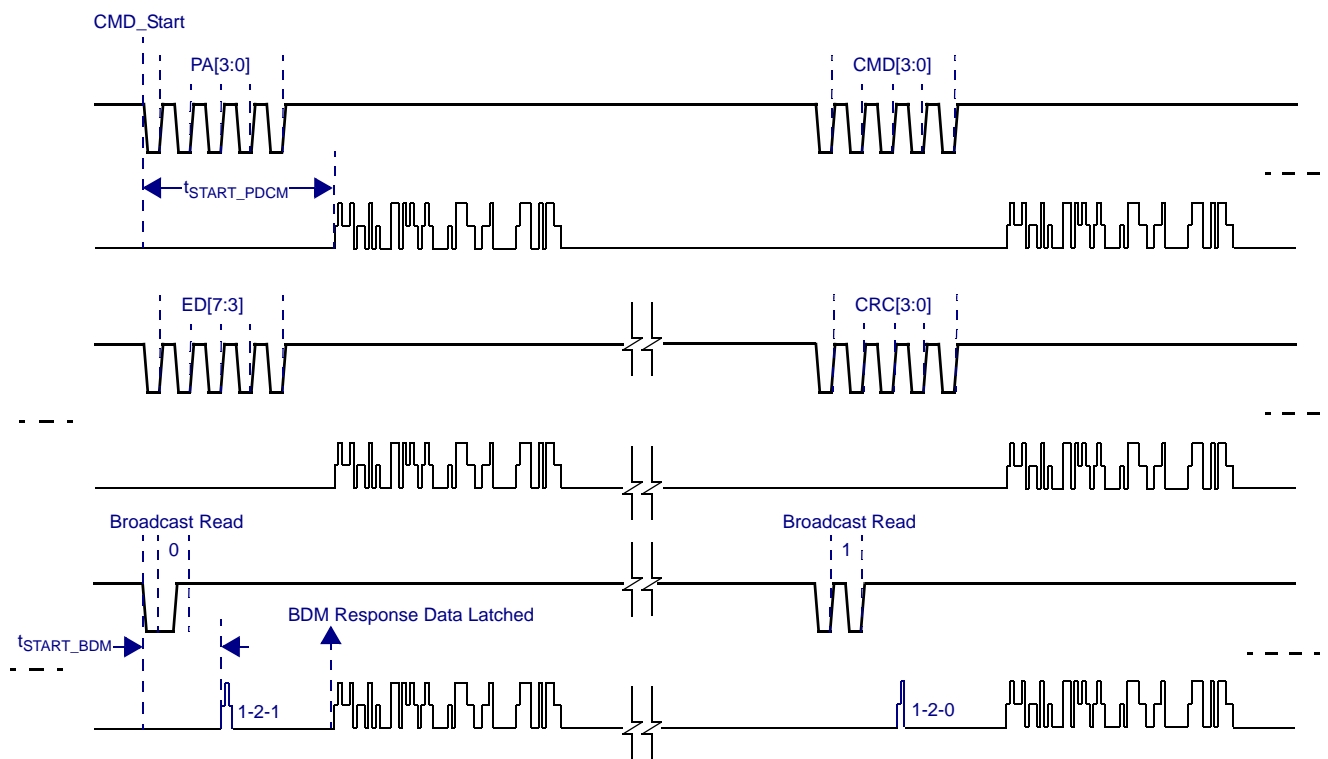


Figure 47. Background Diagnostic Mode Timing Diagram

4.3.6 DSI3 Periodic Data Collection Mode and Background Diagnostic Mode Command Summary

When Periodic Data Collection Mode is enabled, the Background Diagnostic Mode supports the Register Read command as described in the Command and Response Mode command summary, [Section 4.2.4.1](#). The Register Write command is not supported in Background Diagnostic Mode.

4.4 Maximum number of devices on a network

The theoretical maximum number of devices on a DSI3 network is 16: 1 master and 15 slaves. The practical limit for the number of devices on a bus is dependent on the minimum common capability of the devices on the bus. The capability of the device is different depending on the bus configuration and operating mode. The impact of the device capability on the practical limit for the number of devices on the network is described in this section.

4.4.1 Preconfigured, Parallel Connected Network

The number of devices in a preconfigured, parallel connected network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
 - The bus operating voltage
 - The bus supply current
 - The bus current limit
 - The bit rate
 - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.

4.4.2 Bus switch connected daisy-chain network

The number of devices in a bus switch connected daisy-chain network is not directly limited by the capability of the device. The practical limit is determined by a combination of the following:

- The capability of the master device, including, but not limited to:
 - The bus operating voltage
 - The bus supply current
 - The bus current limit
 - The bit rate
 - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The current handling capability and resulting voltage drop of the external bus switches in the network.

4.4.3 Resistor connected daisy-chain network using Discovery Mode

The number of devices in a resistor connected daisy-chain network is limited by the capability of the device. The maximum number of equivalent devices connected to the BUS_O pin of the device is three. This is limited by the total quiescent current drawn from the BUS_O pin during Discovery Mode ($I_{BUS_O_q}$).

The practical limit is determined by a combination of the above restriction and the following:

- The capability of the master device, including, but not limited to:
 - The bus operating voltage
 - The bus supply current
 - The bus current limit
 - The bit rate
 - The response current detection capability (distinguishing response current from quiescent current)
- The total quiescent current of all slaves on the network.
- The maximum allowed quiescent current drawn from the BUS_O pin of other slaves in the system.
- The resulting voltage drop of the Discovery Mode resistors in all slaves in the network.

5 Exception Handling

Table 68 summarizes the exception conditions detected by the device and the response for each exception.

Table 68. Exception handling

| Condition | | Description | Device Response |
|-------------------------------------|---------|---|--|
| Exception | PDCM_EN | | |
| Power On Reset | N/A | Power Applied | <ul style="list-style-type: none"> Reference Section 3.8. ST_INCMPLT Bit Set, PDCM S[3:0] = '1000'. |
| V_{BUS_I} Undervoltage | N/A | $V_{BUS_I} < V_{BUS_I_UV_F}$ | <ul style="list-style-type: none"> Response Current Deactivated. BUSI_UV_ERR set. The device reacts to all DSI commands but no response current is activated. |
| V_{BUF} Undervoltage | N/A | $V_{BUF} < V_{BUF_UV_F}$ | <ul style="list-style-type: none"> Response Current Deactivated. VBUF_UV_ERR set. The device reacts to all DSI commands but no response current is activated. |
| V_{REG} Undervoltage | N/A | $V_{REG} < V_{REG_UV_F}$ | <ul style="list-style-type: none"> The device is held in Reset. No response to DSI commands. If activated, BUSSW is deactivated within t_{BS_OFF}. The device must be re-initialized when V_{REG} returns above $V_{PORCREG_r}$. |
| V_{REGA} Undervoltage | N/A | $V_{REGA} < V_{REGA_UV_F}$ | <ul style="list-style-type: none"> The device is held in Reset. No response to DSI commands. If activated, BUSSW is deactivated within t_{BS_OFF}. The device must be re-initialized when V_{REGA} returns above $V_{PORCREGA_r}$. |
| V_{BUF} Capacitor Test Failure | N/A | | <ul style="list-style-type: none"> The device is reset and will continue to be reset every $t_{POR_CAPTEST}$ until the capacitor failure is removed. No response to DSI commands. If activated, BUSSW is deactivated within t_{BS_OFF}. The device must be re-initialized when the capacitor failure is removed. |
| V_{REG} Capacitor Test Failure | N/A | | <ul style="list-style-type: none"> The device is reset and will continue to be reset every $t_{POR_CAPTEST}$ until the capacitor failure is removed. No response to DSI commands. If activated, BUSSW is deactivated within t_{BS_OFF}. The device must be re-initialized when the capacitor failure is removed. |
| V_{REGA} Capacitor Test Failure | N/A | | <ul style="list-style-type: none"> The device is reset and will continue to be reset every $t_{POR_CAPTEST}$ until the capacitor failure is removed. No response to DSI commands. If activated, BUSSW is deactivated within t_{BS_OFF}. The device must be re-initialized when the capacitor failure is removed. |
| OTP CRC Fault (Factory Array) | N/A | Error detected in factory-programmed OTP array. | <ul style="list-style-type: none"> Periodic Data Collection Mode response data set to error response. PDCM S[3:0] = '0010'. |
| OTP CRC Fault (User Array) | N/A | Error detected in User programmed OTP array and the LOCK_U bit is set. | <ul style="list-style-type: none"> Periodic Data Collection Mode response data set to error response. PDCM S[3:0] = '0011'. |
| User R/W Array CRC Fault | 0 | N/A | N/A |
| | 1 | Error detected in user read write registers and the PDCM_EN bit is set. | <ul style="list-style-type: none"> Periodic Data Collection Mode response data set to error response. PDCM S[3:0] = '0100'. |
| Self-test Activated | 0 | ST activated during initialization | <ul style="list-style-type: none"> Internal self-test circuitry enabled. Self-test Activation Incomplete status cleared. Acceleration Data Registers (ACC_DATAAL, ACC_DATAH) contain self-test active data. |
| | 1 | ST activated in Periodic Data Collection Mode | <ul style="list-style-type: none"> Periodic Data Collection Mode acceleration response data normal. Self-test Activation ignored. |
| Self-test Never Activated after POR | 0 | In initialization, before Self-test | <ul style="list-style-type: none"> Normal Responses to Command and Response Mode. |
| | 1 | In PDCM, Self-test incomplete | <ul style="list-style-type: none"> Periodic Data Collection Mode acceleration response data normal. ST_INCMPLT bit set, PDCM S[3:0] = '1000'. |

6 Recommended Footprint

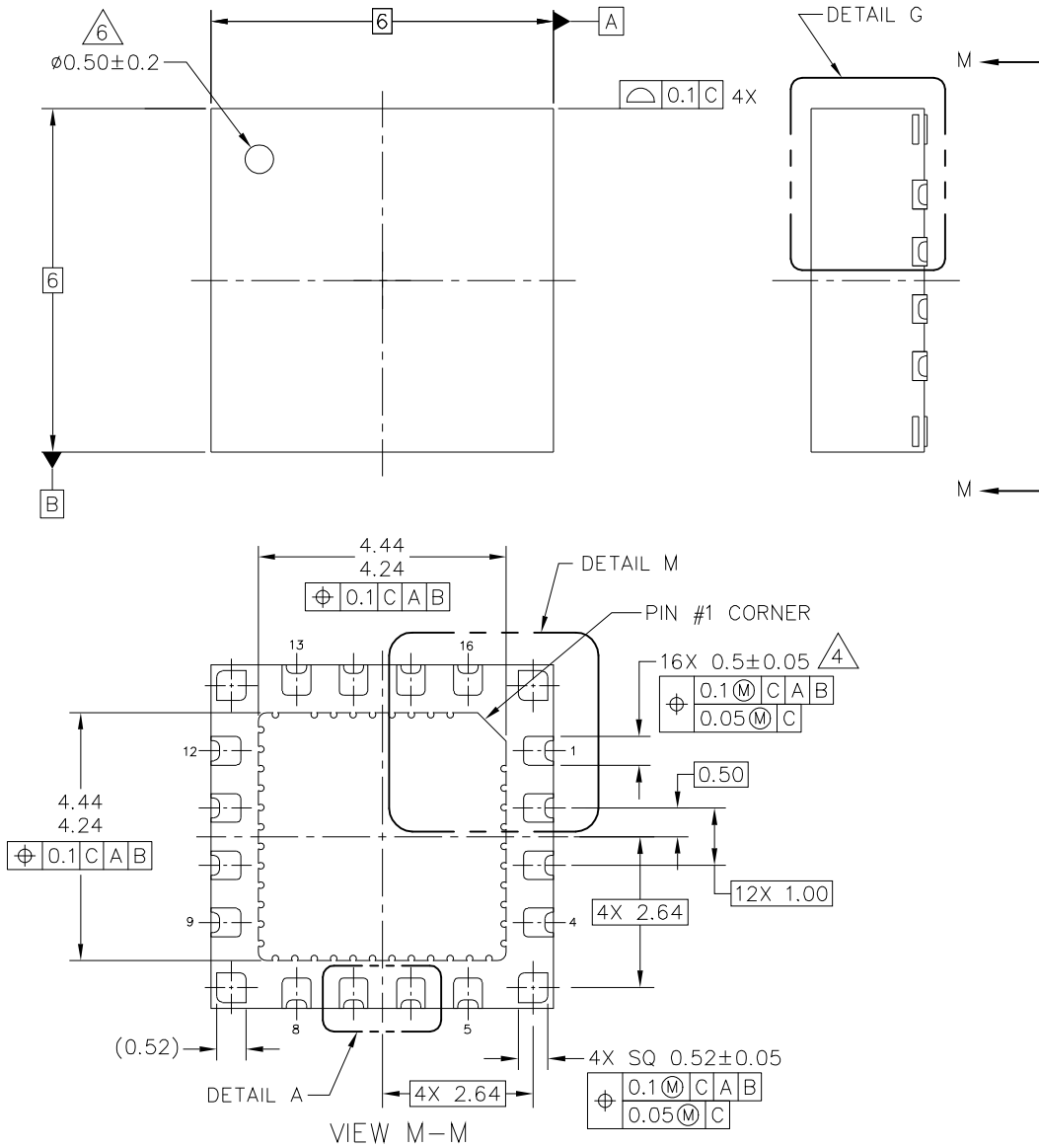
Reference Freescale Application Note AN3111, latest revision:

http://www.freescale.com/files/sensors/doc/app_note/AN3111.pdf

Reference Freescale Application Note AN4530, latest revision:

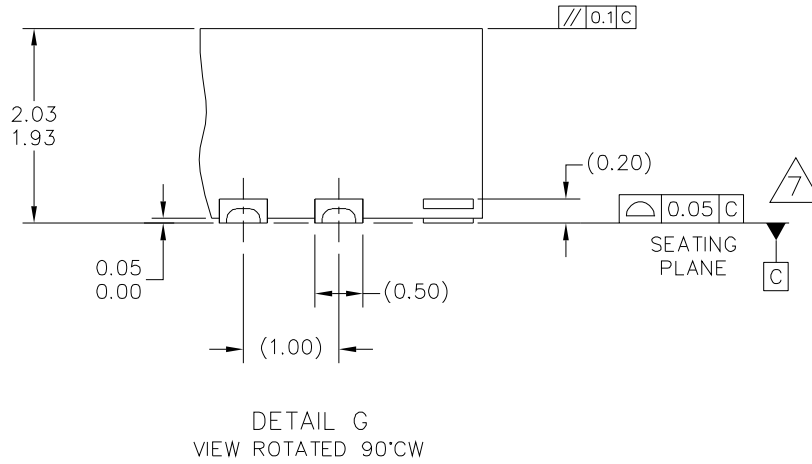
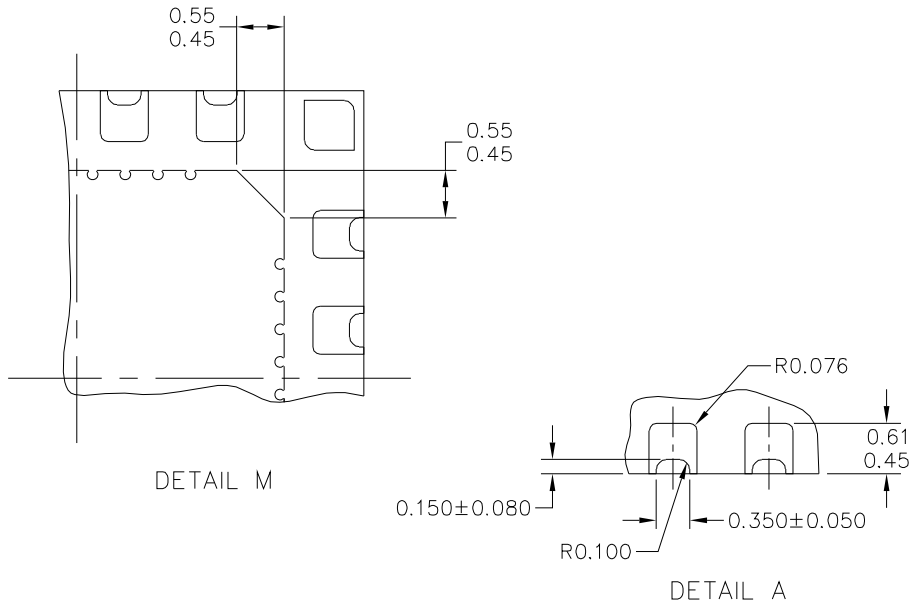
http://www.freescale.com/files/sensors/doc/app_note/AN4530.pdf

7 Package Dimensions



| | | | |
|---|---------------------------|----------------------------|--|
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| | CASE NUMBER: 2086-01 | 26 MAY 2011 | |
| | STANDARD: NON-JEDEC | | |

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NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M. – 1994.
4. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION *b* SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. MAX. PACKAGE WARPAGE IS 0.05 MM.
6. PIN #1 ID ON TOP WILL BE LASER MARKED.
7. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. THIS IS NON JEDEC REGISTERED PACKAGE.
10. MIN. METAL GAP SHOULD BE 0.2 MM

| | | | |
|---|---------------------------|----------------------------|--|
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| | CASE NUMBER: 2086-01 | 26 MAY 2011 | |
| | STANDARD: NON-JEDEC | | |

**CASE 2086-01
ISSUE C
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8 Revision History

Table 69. Revision history

| Revision number | Revision date | Description of changes |
|-----------------|---------------|--|
| 0 | 10/2012 | <ul style="list-style-type: none"> Initial release. |
| 0.5 | 04/2013 | <ul style="list-style-type: none"> Deleted "J" versions of devices and Silicon rev. column on ordering information table. Added Rail options to table. Figure 3: Added C6 capacitor between BUSRTN and BUSOUT_{DC}. Table 2: Added additional information for description of C1. Added C6 capacitor description. Added additional information for description of C1. Figure 5: Deleted (J) from the marking diagram. Section 2.4: Electrical characteristics - Sensor and Signal Chain table: Deleted "trimmed with a..." sentence from lines 57-66. Section 2.5: Electrical characteristics - Self-test and Overload table: Deleted lines 99 and 100 characteristics for "J" versions of device. Section 2.6: Dynamic electrical characteristics - DSI3: Updated Typ values for lines 106, 111, 118, 120-126, 128, 130, 132-136, 140-142, 144, and 147-150. Updated Min and Max values for lines 139, 143, 145, 146, and 150. Section 2.7: Dynamic electrical characteristics - signal chain: Added x-pole description to Cutoff frequency lines. Deleted lines for "Filter order LPFx" and "Filter order, startup Phase x". Updated Typ values for lines 161, 163, 166, 168, and 178. Section 2.7: Dynamic electrical characteristics - supply and support circuitry: Deleted line Oscillator cycles in training time row, Updated Min, Typ and Max values for lines 199-201 and Min values for lines 208 and 209. Deleted Section 2.9. Table 33: Updated Typical Block Latency column values. Table 34: Updated Group Delay column values. Replaced paragraph for Section 4.3. |

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