





Analog, Mixed-Signal and Power Management

# MC33903/4/5 System Basis Chip Gen2 with High Speed CAN and LIN Interface

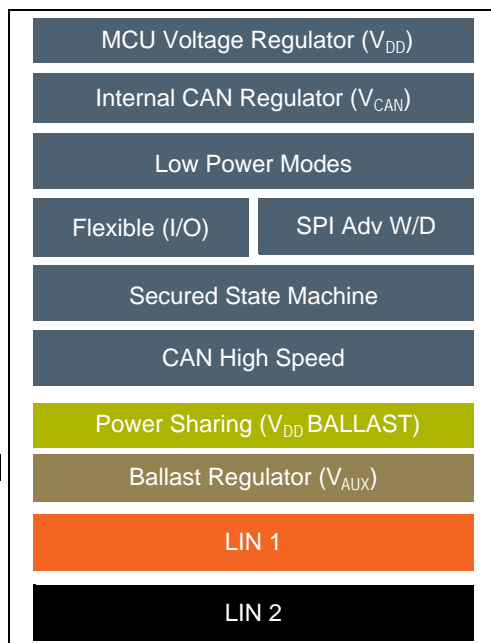
## Overview

The MC33903/4/5 is the second generation family of System Basis Chips, which combine several features and enhance present module designs. The device works as an advanced power management unit for the MCU and additional integrated circuits such as sensors and CAN transceivers. It has a built-in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostics, protection, and fail safe operation mode. The SBC may include one or two LIN 2.1/J2602-2 interfaces with LIN master terminal outputs. It includes wake-up input pins that can also be configured as output drivers for flexibility.

This device implements multiple Low Power modes with very low-current consumption. In addition, the device is part of a family concept where pin compatibility, among the various devices with and without LIN interfaces, adds versatility to module design.

The MC33903/4/5 also implements an innovative and advanced fail-safe state machine and concept solution. This family of devices are supported by an enablement ecosystem that includes an evaluation board, software interface, EMC/ESD conformance reports and training material that allows a faster time to market and eases your designs.

MC33903/4/5 Block Diagram



### Legend

- 33903
- 33903S
- 33903D
- 33904
- 33905S
- 33905D

### Power Management Scalability

- MCU power supply ( $V_{DD}$ ): 5.0 or 3.3 V / 150 mA (power split option for scalable needs - up to 300 mA)
- 5.0 or 3.3 V voltage regulator ( $V_{AUX}$ ) for auxiliary loads
- Dedicated 5.0 V voltage regulator (5 V CAN) for High Speed CAN

### Functional Safety

- Innovative cranking pulse management during  $V_{DD}$  low
- Fail safe & configurable state machine
- Enhanced protections and diagnostics

### Energy Savings

- Ultra low power modes (typ 15  $\mu$ A with  $V_{DD}$  off)
- Innovative Wake-up management and cyclic sense capability

### Robust Physical Layers

- Certification to LIN 2.1, J2602-2, and ISO11898-2-5 standards
- Successfully certified for stringent EMC, ISO, and ESD standards

### Easy to Use

- Ecosystem to lower development time and simplify access
- Debug mode to save time during application development

### Flexibility & Compatibility:

- Selectable parameters (RST time, W/D type,  $V_{DD}$  under-voltage threshold,  $V_{AUX}$  3.3 or 5.0 V)
- 1 or 2 LIN options (33903S, 33905S and 33903D, 33905D)
- Scalable (I/O pins configurable as wake-up inputs or output LIN master terminations)

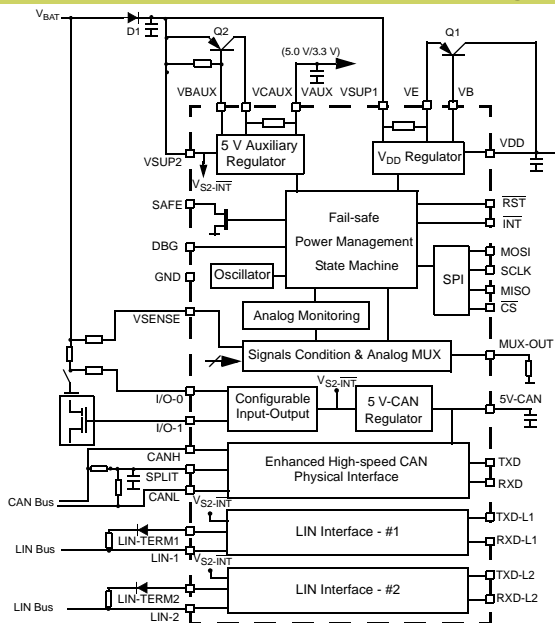
## IDEAL COMPANION CHIP FOR MCU IN BODY, SAFETY, AND POWERTRAIN APPLICATIONS

| Segment          | Applications              | Proposed FSL MCU    |
|------------------|---------------------------|---------------------|
| Body             |                           |                     |
|                  | Body Controller           | S12x, MPC560x       |
|                  | Gateway                   |                     |
|                  | Seat Module               | S12x, MPC560x, S08x |
|                  | Door Module               |                     |
|                  | Lighting Control Module   |                     |
|                  | Column Module             |                     |
|                  | HVAC                      |                     |
|                  | Cluster                   |                     |
| Safety & Chassis |                           |                     |
|                  | Seat Belt Pre-tensioner   | S12x, MPC560x       |
|                  | Electric Parking Brake    |                     |
|                  | Steering                  |                     |
| Power Train      |                           |                     |
|                  | Fuel Pump                 | S12x, S08x          |
|                  | Water Pump                |                     |
|                  | Glow Plug                 | S12x, MPC563x       |
|                  | Engine Management Low End |                     |

### Key Characteristics

| Parameter                                   | Characterization   |
|---|--|
| MCU Linear $V_{REG}$ (LDO)                  | 5.0 / 3.3 V  |
| Output Current                              | (300 mA for 33903D/S, 33904, 33905D/S with optional external PNP implementation) |
| Bus Output                                  | CAN  |
| 33903D/S, 33905D/S only                     | LIN  |
| Data Rate                                   |  |
| CAN   | 40 kB/s – 1.0 MB/s   |
| LIN   | 10.4 kB/s – 20 kB/s (100 kB/s in fast mode)                                      |
| Low Power $V_{DD}$ OFF/ $V_{DD}$ ON Current | 15/25 $\mu$ A  |
| ESD - Module Level (CAN and LIN)            | $\pm$ 8000 V   |
| Operating Voltage                           | 5.5 - 28 V   |
| Maximum Input Voltage                       | 27 VDC, 40 V (Load Dump)   |
| Operating Temperature                       | -40 °C < $T_A$ < 125 °C  |

## MC33905D Simplified Application Drawing

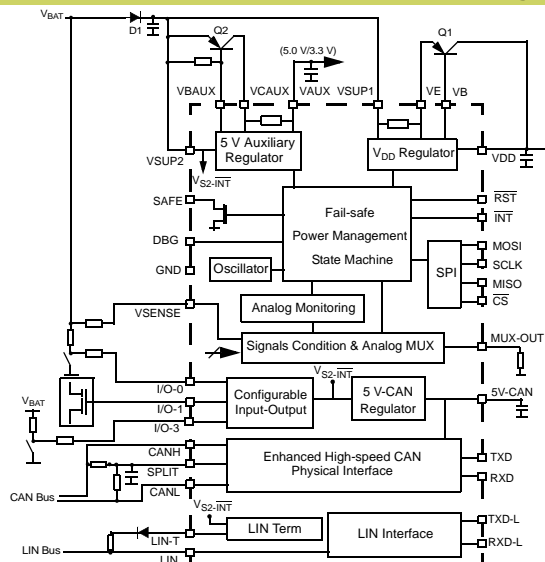


### Features

- LDO Linear Power Supply 5.0 or 3.3 V, up to 300 mA with an optional external ballast transistor
- LDO Auxiliary Regulator with ballast transistor (5.0 / 3.3 V configurable)
- Under-voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- High precision  $V_{SUP}$  sense monitoring
- Multiple Analog sensing to 1 MUX output
- Dual configurable I/O with W/U feature
- "B" versions are recommended for new designs. Changes implemented on "B" versions: resolved  $V_{SUP}$  slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN, ISO11898-2 and 11898-5 compliant**
- **2 LIN transceivers - 2.0, 2.1, and SAE J2602-2 compliant**

| Freescale Part Number        | $V_{DD}$ output voltage | CAN interface | LIN interface(s) | I/O Wake-up Capability   | $V_{AUX}$ | $V_{SENSE}$ | MUX | Package                  |
|------------------------------|-------------------------|---------------|------------------|--|-----------|-------------|-----|--------------------------|
| <b>MC33905D (Dual LIN)</b>   |                         |               |                  |  |           |             |     |                          |
| MCZ33905BD3EK/R2             | 3.3 V                   | 1             | 2                | 2 wake-up + 2 LIN terms<br>or<br>3 wake-up + 1 LIN terms<br>or<br>4 wake-up + no LIN terms | Yes       | Yes         | Yes | SOIC 54 pins exposed pad |
| MCZ33905CD3EK/R2             |                         |               |                  |  |           |             |     |                          |
| MCZ33905D5EK/R2              | 5.0 V                   | 1             | 2                | 2 wake-up + 2 LIN terms<br>or<br>3 wake-up + 1 LIN terms<br>or<br>4 wake-up + no LIN terms | Yes       | Yes         | Yes | SOIC 54 pins exposed pad |
| MCZ33905BD5EK/R2             |                         |               |                  |  |           |             |     |                          |
| MCZ33905CD5EK/R2             |                         |               |                  |  |           |             |     |                          |
| <b>MC33905S (Single LIN)</b> |                         |               |                  |  |           |             |     |                          |
| MCZ33905BS3EK/R2             | 3.3 V                   | 1             | 1                | 3 Wake-up + 1 LIN terms<br>or<br>4 Wake-up + no LIN terms                                  | Yes       | Yes         | Yes | SOIC 32 pin exposed pad  |
| MCZ33905CS3EK/R2             |                         |               |                  |  |           |             |     |                          |
| MCZ33905S5EK/R2              | 5.0 V                   | 1             | 1                | 3 Wake-up + 1 LIN terms<br>or<br>4 Wake-up + no LIN terms                                  | Yes       | Yes         | Yes | SOIC 32 pin exposed pad  |
| MCZ33905BS5EK/R2             |                         |               |                  |  |           |             |     |                          |
| MCZ33905CS5EK/R2             |                         |               |                  |  |           |             |     |                          |

## MC33905S Simplified Application Drawing



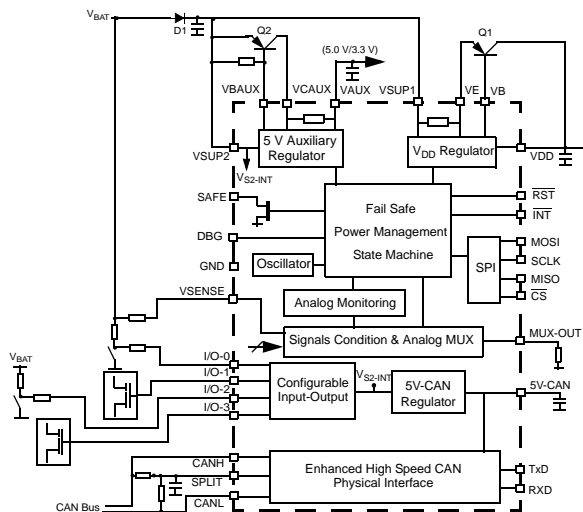
### Features

- LDO Linear Power Supply 5.0 or 3.3 V, up to 300 mA with an optional external ballast transistor
- LDO Auxiliary Regulator with ballast transistor (5.0 / 3.3 V configurable)
- Under voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- High precision  $V_{SUP}$  sense monitoring
- Multiple Analog sensing to 1 MUX output
- Triple configurable I/O with W/U feature
- "B" versions are recommended for new designs. Changes implemented on "B" versions: resolved  $V_{SUP}$  slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN, ISO11898-2 and 11898-5 compliant**
- **1 LIN transceiver - 2.0, 2.1, and SAE J2602-2 compliant**

## MC33904 Simplified Application Drawing

### Features

- LDO Linear Power Supply 5.0 or 3.3 V, up to 300 mA with an optional external ballast transistor
- LDO Auxiliary Regulator with ballast transistor (5.0 / 3.3 V configurable)
- Under-voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- High precision  $V_{SUP}$  sense monitoring
- Multiple Analog sensing to 1 MUX output
- Quad configurable I/O with W/U feature
- “B” versions are recommended for new designs. Changes implemented on “B” versions: resolved  $V_{SUP}$  slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN transceiver: ISO11898-2 and 11898-5 compliant**

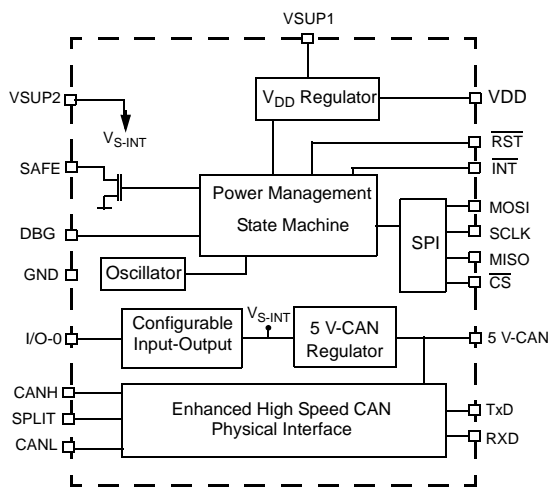


| Freescale Part Number | V <sub>DD</sub> output voltage | CAN interface | LIN interface(s) | I/O Wake-up Capability | V <sub>AUX</sub> | V <sub>SENSE</sub> | MUX | Package                  |
|-----------------------|--------------------------------|---------------|------------------|------------------------|------------------|--------------------|-----|--------------------------|
| <b>MC33904</b>        |                                |               |                  |                        |                  |                    |     |                          |
| MCZ33904B3EK/R2       | 3.3 V                          | 1             | 0                | 4 Wake-up              | Yes              | Yes                | Yes | SOIC 32 pins exposed pad |
| MCZ33904C3EK/R2       |                                |               |                  |                        |                  |                    |     |                          |
| MCZ33904A5EK/R2       |                                |               |                  |                        |                  |                    |     |                          |
| MCZ33904B5EK/R2       | 5.0 V                          |               |                  |                        |                  |                    |     |                          |
| MCZ33904C5EK/R2       |                                |               |                  |                        |                  |                    |     |                          |

## MC33903 Simplified Application Drawing

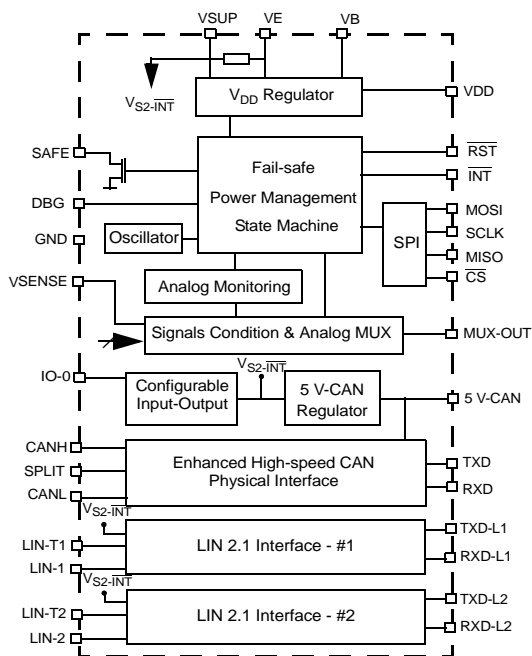
### Features

- LDO Linear Power Supply 5.0 or 3.3 V
- V<sub>DD</sub> does not allow usage of an external PNP on the 33903. Output current limited to 150 mA
- Under-voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- Configurable I/O with W/U feature
- “B” versions are recommended for new designs. Changes implemented on “B” versions: resolved  $V_{SUP}$  slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN transceiver: ISO11898-2 and 11898-5 compliant**



| Freescale Part Number | V <sub>DD</sub> output voltage | CAN interface | LIN interface(s) | I/O Wake-up Capability | V <sub>AUX</sub> | V <sub>SENSE</sub> | MUX | Package                  |
|-----------------------|--------------------------------|---------------|------------------|------------------------|------------------|--------------------|-----|--------------------------|
| <b>MC33903</b>        |                                |               |                  |                        |                  |                    |     |                          |
| MCZ33903B3EK/R2       | 3.3 V                          | 1             | 0                | 1 Wake-up              | No               | No                 | No  | SOIC 32 pins exposed pad |
| MCZ33903C3EK/R2       |                                |               |                  |                        |                  |                    |     |                          |
| MCZ33903B5EK/R2       | 5.0 V                          |               |                  |                        |                  |                    |     |                          |
| MCZ33903C5EK/R2       |                                |               |                  |                        |                  |                    |     |                          |

### MC33903D Simplified Application Drawing

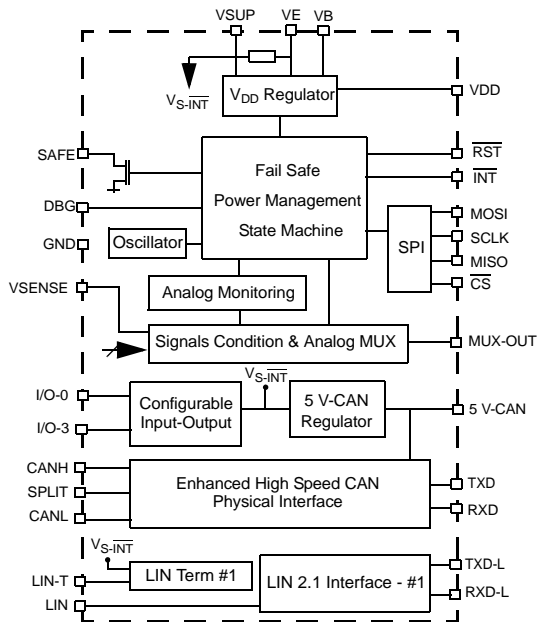


### Features

- LDO Linear Power Supply 5.0 or 3.3 V, up to 300 mA with an optional external ballast transistor
- Under-voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- High precision V<sub>SUP</sub> sense monitoring
- Multiple Analog sensing to 1 MUX output
- Configurable I/O with W/U feature
- “B” versions are recommended for new designs. Changes implemented on “B” versions: resolved V<sub>SUP</sub> slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN, ISO11898-2 and 11898-5 compliant**
- **2 LIN transceivers - 2.0, 2.1, and SAE J2602-2 compliant**

| Freescle Part Number       | V <sub>DD</sub> output voltage | CAN interface | LIN interface(s) | I/O Wake-up Capability   | V <sub>AUX</sub> | V <sub>SENSE</sub> | MUX | Package                  |
|----------------------------|--------------------------------|---------------|------------------|--------------------------|------------------|--------------------|-----|--------------------------|
| <b>MC33903D (Dual LIN)</b> |                                |               |                  |                          |                  |                    |     |                          |
| MCZ33903BD3EK/R2           | 3.3 V                          | 1             | 2                | 1 wake-up + 2 LIN terms  | No               | Yes                | Yes | SOIC 32 pins exposed pad |
| MCZ33903CD3EK/R2           |                                |               |                  | 2 wake-up + 1 LIN terms  |                  |                    |     |                          |
| MCZ33903BD5EK/R2           | 5.0 V                          | 1             | 2                | 3 wake-up + no LIN terms | No               | Yes                | Yes | SOIC 32 pins exposed pad |
| MCZ33903CD5EK/R2           |                                |               |                  | 3 wake-up + no LIN terms |                  |                    |     |                          |

### MC33903S Simplified Application Drawing



### Features

- LDO Linear Power Supply 5.0 or 3.3 V, up to 300 mA with an optional external ballast transistor
- Under-voltage management for cranking
- Internal 5.0 V regulator for CAN driver supply
- Low current consumption in sleep mode
- Fail safe state machine linked with SAFE pin
- Secured SPI with Watchdog capability
- High precision V<sub>SUP</sub> sense monitoring
- Multiple Analog sensing to 1 MUX output
- Configurable I/O with W/U feature
- “B” versions are recommended for new designs. Changes implemented on “B” versions: resolved V<sub>SUP</sub> slow ramp up behavior, enhanced device current consumption, and improved oscillator
- **CAN, ISO11898-2 and 11898-5 compliant**
- **1 LIN transceiver - 2.0, 2.1, and SAE J2602-2 compliant**

| Freescale Part Number        | V <sub>DD</sub> output voltage | CAN interface | LIN interface(s) | I/O Wake-up Capability                                    | V <sub>AUX</sub>              | V <sub>SENSE</sub> | MUX | Package |
|------------------------------|--------------------------------|---------------|------------------|---|-------------------------------|--------------------|-----|---------|
| <b>MC33903S (Single LIN)</b> |                                |               |                  |   |                               |                    |     |         |
| MCZ33903BS3EK/R2             | B                              | 3.3 V         | 1                | 2 Wake-up + 1 LIN terms<br>or<br>3 Wake-up + no LIN terms | SOIC<br>32 pin<br>exposed pad | No                 | Yes | Yes     |
| MCZ33903CS3EK/R2             | C                              |               |                  |   |                               |                    |     |         |
| MCZ33903BS5EK/R2             | B                              | 5.0 V         |                  |   |                               |                    |     |         |
| MCZ33903CS5EK/R2             | C                              |               |                  |   |                               |                    |     |         |
| <b>MC33903P</b>              |                                |               |                  |   |                               |                    |     |         |
| MCZ33903CP5EK/R2             | C                              | 5.0 V         | 0                | 3 Wake-up   | SOIC<br>32 pin<br>exposed pad | No                 | Yes | Yes     |
| MCZ33903CP3EK/R2             |                                | 3.3 V         |                  |   |                               |                    |     |         |

## MC33903, MC33904, AND MC33905 KEY FEATURES AND BENEFITS

| Features                                   | Benefits   |
|--|--|
| <b>Ecosystem</b>                           |  |
| Easy-to-Use Ecosystem                      | <ul style="list-style-type: none"> <li>• Faster time to market.</li> <li>• EVB + SW interface to ease SBC usage &amp; programming.</li> <li>• Electrical and EMC/ESD conformance reports.</li> <li>• Training material.</li> </ul>                 |
| <b>Energy Management</b>                   |  |
| Ultra Low Power Modes                      | <ul style="list-style-type: none"> <li>• Best-in-class quiescent current down to 15 <math>\mu</math>A including LIN and CAN wake-up active.</li> <li>• Reduces contribution of active blocks during stand-by mode.</li> </ul>                      |
| Innovative Wake-up Event                   | <ul style="list-style-type: none"> <li>• Save time during cyclic check by reducing the number of state machine transitions. This contributes in reducing overall ECU energy consumption (Energy = Current x Time).</li> </ul>                      |
| Scalable Power Supply                      | <ul style="list-style-type: none"> <li>• Enables platform solution (150 mA internal supply, or up to 300 mA with an optional ballast transistor).</li> </ul>   |
| <b>System Management</b>                   |  |
| Flexible Fail Safe Modes                   | <ul style="list-style-type: none"> <li>• Flexibility to address the ECU functional safety assessment and program the default fail safe behavior via hardware implementation.</li> </ul>  |
| Secured SPI                                | <ul style="list-style-type: none"> <li>• Fast SPI access – higher frequency combined with new register addressing methodology to save time.</li> <li>• Parity checks.</li> </ul>   |
| Innovative Cranking Pulse Management       | <ul style="list-style-type: none"> <li>• System alternative to save customer cost (PCB space, cost of capacitor) while keeping some degraded functionalities during cranking mode.</li> </ul>  |
| Advanced Watchdog                          | <ul style="list-style-type: none"> <li>• Improved, safer and optional Watchdog (in addition to time-out and window watchdog) implemented to avoid unpredictable Watchdog recognition, so that closed loop MCU activity can be detected.</li> </ul> |
| Ease Customer Debug Mode                   | <ul style="list-style-type: none"> <li>• The DBG pin is used to inhibit the watchdog during debug mode. This helps hardware and software designers save time during application development.</li> </ul>  |
| <b>Robust Physical Layers</b>              |  |
| Certification and Car OEM Approval Process | <ul style="list-style-type: none"> <li>• LIN and CAN HS P/L meets conformance tests and EMC/ESD standard requirements to secure the customer design</li> </ul>   |

## Development Tools

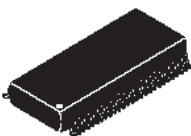
| Part Number      | Description   |
|------------------|---|
| KIT33903BD3EVBE  | Evaluation board to demonstrate the key features of the MC33903     |
| KIT33903BD5EVBE  | Evaluation board to demonstrate the key features of the MC33903     |
| KIT33905BD3EVBE  | Evaluation board to demonstrate the key features of the MC33903/4/5 |
| KIT33905D5EKEVBE | Evaluation board to demonstrate the key features of the MC33903/4/5 |

## Documentation

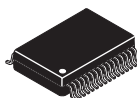
| Document Number | Title          | Description                                   |
|-----------------|----------------|---|
| MC33903_4_5     | Data Sheet     | Presents the specifications for the product   |
| SG1002          | Selector Guide | Analog and power management device comparison |
| SG187           | Selector Guide | Automotive device comparison                  |

## Questions

- Are you looking for an automotive certified High Speed CAN and LIN Physical Layer integrated on a single chip SBC?
- What is the maximum current capability of your MCU?
- Do you need to implement very low application quiescent current?
- How many wake-up sources are required by your system?
- Do you need to monitor bus failures during network communications?
- What battery voltage range is required by your system? What is the application behavior expected during cranking pulse?
- Do you need continuous system monitoring (temperature, battery voltage, inputs signals,...)?
- What are the safety level requirements of your application? Do you need external components to monitor your MCU (watchdog,...)?
- How many regulator outputs, and what logic voltage levels are required by your system (3.3 or 5.0 V)?



EK SUFFIX (PB-FREE)  
54-PIN SOICW-EP  
98ASA10506D



EK SUFFIX (PB-FREE)  
32-PIN SOICW-EP  
98ASA10556D

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