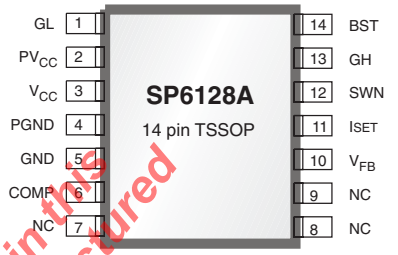
THE DATASHEET OF

MCP4231-503E/P

Low Voltage, Synchronous Step Down PWM Controller

Ideal for 2A to 10A, Small Footprint, DC-DC Power Converters

- Optimized for Single Supply, 3V - 5.5V Applications
- High Efficiency: Greater Than 95% Possible
- Discontinuous Startup for Precharged Output
- Accurate Fixed 300kHz Frequency Operation
- Fast Transient Response
- Internal Soft Start Circuit
- Accurate 0.8V Reference Allows Low Output Voltages
- Resistor Programmable Output Voltage
- Resistor Programmable Overcurrent Threshold
- Loss-less Current Limit with High Side $R_{DS(ON)}$ Sensing
- Hiccup Mode Current Limit Protection
- Dual N-Channel MOSFET Synchronous Driver
- Quiescent Current: 500µA, 30µA in Shutdown
- 14 pin TSSOP



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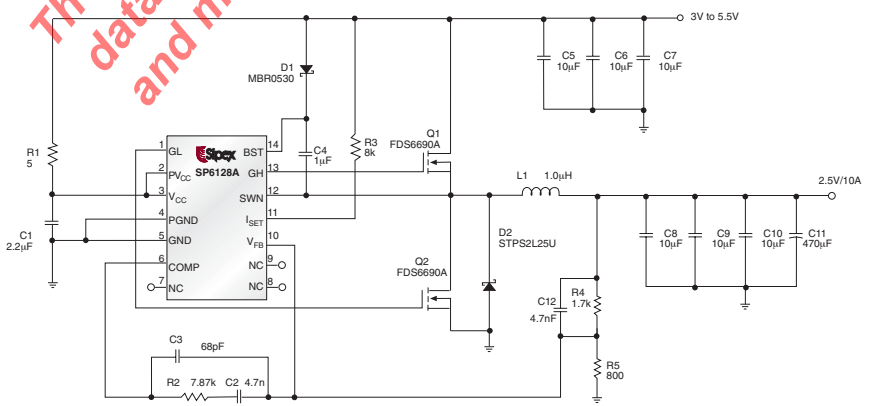
APPLICATIONS

- DSP
- Microprocessor Core
- I/O & Logic
- Industrial Control
- Distributed Power
- Low Voltage Power

DESCRIPTION

The SP6128A is a fixed frequency, voltage mode, synchronous PWM controller designed to work from a single 5V or 3.3V input supply, providing excellent AC and DC regulation for high efficiency power conversion. Requiring only few external components, the SP6128A packaged in an 14-pin TSSOP, is especially suited for low voltage applications where cost, small size and high efficiency are critical. The operating frequency is internally set to 300kHz, allowing small inductor values and minimizing PC board space. The SP6128A drives two N-channel power MOSFETs for improved efficiency and includes an accurate 0.8V reference for low output voltage applications.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

V_{CC}, PV_{CC} 7V
BST 13.2V
BST-SWN 7V
SWN ..... -1V to 7V
GH ..... -0.3V to BST +0.3V
GH-SWN 7V
All other pins ..... -0.3V to V_{CC} + 0.3V
Peak Output Current < 10µs
GH,GL 2A
Storage Temperature ..... -65°C to 150°C
Power Dissipation 1.3W

Junction Temperature, T_J ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating. ..... 2kV HBM
Thermal Resistance θ_{JC} ..... 31.7°C/W

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: -40°C < T_A < 85°C, 3.0V < PV_{CC} = V_{CC} < 5.5V, C_{COMP} = 22nF, C_{GH} = C_{GL} = 3.3nF, V_{FB} = 0.8V, SWN = GND = 0V, typical value for design guideline only.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
QUIESCENT CURRENT					
V_{CC} Supply Current		0.5	1.0	mA	No Switching
PV_{CC} Supply Current		1	20	µA	No Switching, GH = Low
V_{CC} Supply Current(Disabled)		30	60	µA	COMP=0V
PV_{CC} Supply Current (Disabled)		1	20	µA	COMP=0V
ERROR AMPLIFIER					
Error Amplifier Transconductance		0.6		ms	
COMP Sink Current	10	35	65	µA	V_{FB} = 0.9V, COMP = 0.9V, No Faults
COMP Source Current	10	35	65	µA	V_{FB} = 0.7V, COMP = 2V
COMP Output Impedance		3		MΩ	
V_{FB} Input Bias Current			130	nA	
Error Amplifier Reference	0.788	0.8	0.812	V	Trimmed with Error Amp in Unity Gain
OSCILLATOR & DELAY PATH					
Internal Oscillator Frequency	270	300	330	kHz	
Maximum Controlled Duty Cycle		90		%	Loop in control - 100% DC Possible
Minimum Duty Cycle			0	%	Comp=0.7V
Minimum GH Pulse Width		150	250	ns	PV_{CC} > 4.5V, Ramp up COMP voltage until GH starts switching
CURRENT LIMIT					
I_{SET} Pin Sink Current	10	12.5	15	µA	Temp = 25 °C
I_{SET} Current Temperature Coefficient		3400		ppm/°C	
Current Limit Time Constant		15		µs	
Overcurrent Comparator Threshold Voltage	100	125	150	mV	VI_{SET} - V_{SWN}, Temp = 25°C
Threshold Voltage Temperature Coefficient		3400		ppm/°C	

ELECTRICAL CHARACTERISTICS

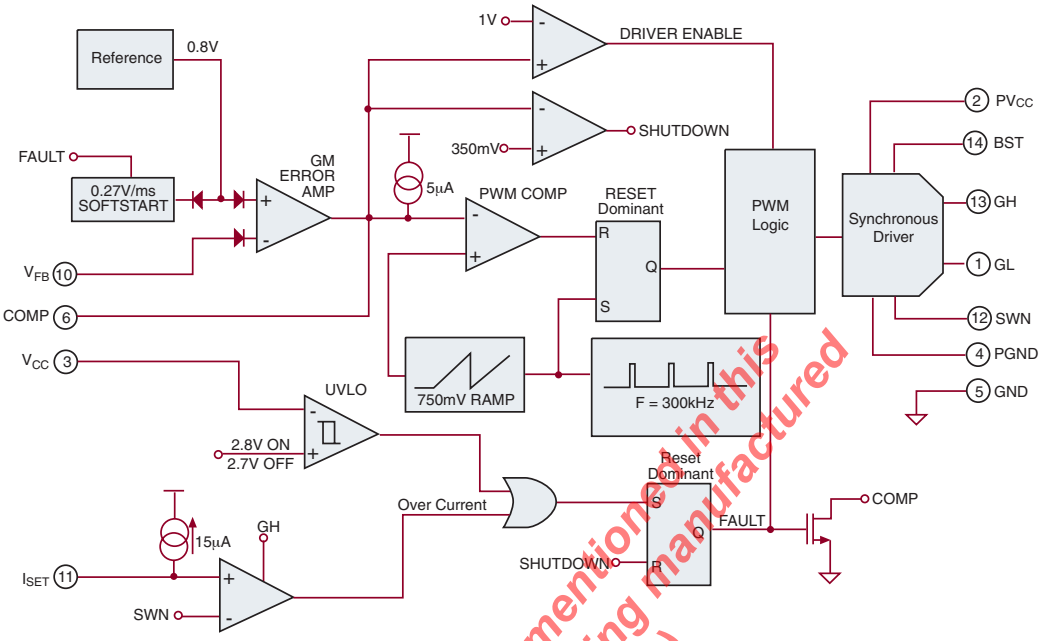
Unless otherwise specified: -40°C < T_A < 85°C, 3.0V < PV_{CC} = V_{CC} < 5.5V, C_{COMP} = 22nF, CGH = CGL = 3.3nF, V_{FB} = 0.8V, SWN = GND = 0V, typical value for design guideline only.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
SOFT START, SHUTDOWN, UVLO					
Internal Soft Start Slew Rate	0.1	0.3	0.6	V/ms	COMP pin, on transition from shutdown
COMP Discharge Current	183			µA	COMP = 0.5V, Fault Initiated
COMP Clamp Voltage	0.55	0.65	0.75	V	V_{FB} = 0.9V
COMP Clamp Current	10	30	65	µA	COMP = 0.5V, V_{FB} = 0.9V
Shutdown Threshold Voltage	0.29	0.34	0.39	V	Measured at COMP Pin
Shutdown Input Pull-up Current	2	5	10	µA	COMP = 0.2V, Measured at COMP pin
V_{CC} Start Threshold	2.63	2.8	2.95	V	
V_{CC} Stop Threshold	2.47	2.7	2.9	V	
GATE DRIVERS					
GH Rise Time		60	110	ns	PV_{CC} > 4.5V
GH Fall Time		60	110	ns	PV_{CC} > 4.5V
GL Rise Time		60	110	ns	PV_{CC} > 4.5V
GL Fall Time		60	110	ns	PV_{CC} > 4.5V
GH to GL Non-Overlap Time	0	100	140	ns	PV_{CC} > 4.5V, measured at 2volt threshold
GL to GH Non-Overlap Time	0	100	140	ns	PV_{CC} > 4.5V, measured at 2volt threshold

PIN DESCRIPTION

PIN N0.	PIN NAME	DESCRIPTION
1	GL	High current driver output for the low side MOSFET switch. It is always low if GH is high. GL swings from PGND to PV_{CC}.
2	PV_{CC}	Positive input supply for the low side gate driver. It's recommended to tie the PV_{CC} to the V_{CC} pin.
3	V_{CC}	Positive input supply for the logic circuitry. Properly bypass this pin to GND with a low ESL/ESR ceramic capacitor or RC filter.
4	PGND	Power ground pin.
5	GND	Signal ground pin.
6	COMP	Output of the Error Amplifier. It is internally connected to the inverting input of the PWM comparator. A lead-lag network is typically connected to the COMP pin to compensate the feedback loop in order to optimize the dynamic performance of the voltage mode control loop. Sleep mode can be invoked by pulling the COMP pin below 0.3V with an external open-drain or open-collector transistor. An internal 5µA pull-up ensures start-up.
7, 8, 9	NC	No connect.
10	V_{FB}	Feedback Voltage Pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck converter. The output voltage is sensed and can be adjusted through an external resistor divider.
11	I_{SET}	Overcurrent program pin. A resistor programs the overcurrent threshold. The overcurrent comparator sets the fault latch and terminates gate pulses when VI_{SET} > V_{SWN} and the high side MOSFET is turned on. This prevents excessive power dissipation in the external power MOSFETs during an overload condition. An internal delay circuit prevents false shutdowns that might otherwise occur during very short, mild overload conditions,due to load transients.
12	SWN	Lower supply rail for the GH high-side gate driver. It also connects to the Current Limit comparator. Connect this pin to the switching node at the junction between the two external power MOSFET transistors. This pin monitors the voltage drop across the $R_{DS(ON)}$ of the high side N-channel MOSFET while it is conducting.
13	GH	High current driver output for the high side MOSFET switch. It is always low if GL is high or during a fault. GH swings from SWN to BST.
14	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the application schematic on page 1.

FUNCTIONAL DIAGRAM



OPERATION

General Overview

The SP6128A is a constant frequency, voltage mode, synchronous PWM controller designed for low voltage, DC/DC step down converters. It is intended to provide complete control for a high power, high efficiency, precisely regulated output voltage from a highly integrated 14-pin solution.

The internal free-running oscillator accurately sets the PWM frequency at 300kHz without requiring any external elements and allows the use of physically small, low value external components without compromising performance. A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a precision, 0.8V reference voltage. The output of the error amplifier (COMP), is compared to a 0.75V peak-to-peak ramp waveform to provide PWM control. The COMP pin provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

High efficiency is obtained through the use of synchronous rectification. Synchronous regulators replace the catch diode in the standard buck converter with a low $R_{DS(ON)}$ N-channel MOSFET switch allowing for significant efficiency improvements. The SP6128A includes two fast MOSFET drivers with internal non-overlap circuitry and drives a pair of N-channel power transistors. The SP6128A includes an internal 0.27V/ms soft-start circuit that provides controlled ramp up of the output voltage, preventing overshoot and inrush current at power up.

Current limiting is implemented by monitoring the voltage drop across the $R_{DS(ON)}$ of the high side N-channel MOSFET while it is conducting, thereby eliminating the need for an external sense resistor. The overcurrent threshold can be programmed by a single resistor.

When the overcurrent threshold is exceeded, the overcurrent comparator sets the fault latch and terminates the output pulses. The controller stops switching and goes through a hiccup sequence. This prevents excessive power dissipation in the external power MOSFETs during an overload condition. An internal delay circuit prevents that very short and mild overload conditions, that could occur during a load transient, activate the current limit circuit.

A low power sleep mode can be invoked in the SP6128A by externally forcing the COMP pin below 0.3V. Quiescent supply current in sleep mode is typically less than 30µA. An internal 5µA pull-up current at the COMP pin brings the SP6128A out of shutdown mode.

An internal 0.8V 1.5% reference allows output voltage adjustment for low voltage applications.

The SP6128A also includes an accurate undervoltage lockout that shuts down the controller when the input voltage falls below 2.7V. Output overvoltage protection is achieved by turning off the high side switch and turning on the low side N-channel MOSFET 100% of the time.

Enable

Low quiescent mode or "Sleep Mode" is initiated by pulling the COMP pin below 0.3V with an external open-drain or open-collector transistor. Supply current is reduced to 30µA (typical) in shutdown. On power-up, assuming that V_{CC} has exceeded the UVLO start threshold (2.8V), an internal 5µA pull-up current at the COMP pin brings the SP6128A out of shutdown mode and ensures start-up. During normal operating conditions and in absence of a fault, an internal clamp prevents the COMP pin from swinging below 0.6V. This guarantees that during mild transient conditions, due either to line or load variations, the SP6128A does not enter shutdown unless it is externally activated.

During Sleep Mode, the high side and low side MOSFETS are turned off and the internal soft start voltage is held low.

UVLO

Assuming that there is not shutdown condition present, then the voltage on the V_{CC} pin determines operation of the SP6128A. As V_{CC} rises, the UVLO block monitors V_{CC} and keeps the high side and low side MOSFETS off and the internal SS voltage low until V_{CC} reaches 2.8V. If no faults are present, the SP6128A will initiate a soft start when V_{CC} exceeds 2.8 V.

Hysteresis (about 100mV) in the UVLO comparator provides noise immunity at start-up.

Soft Start

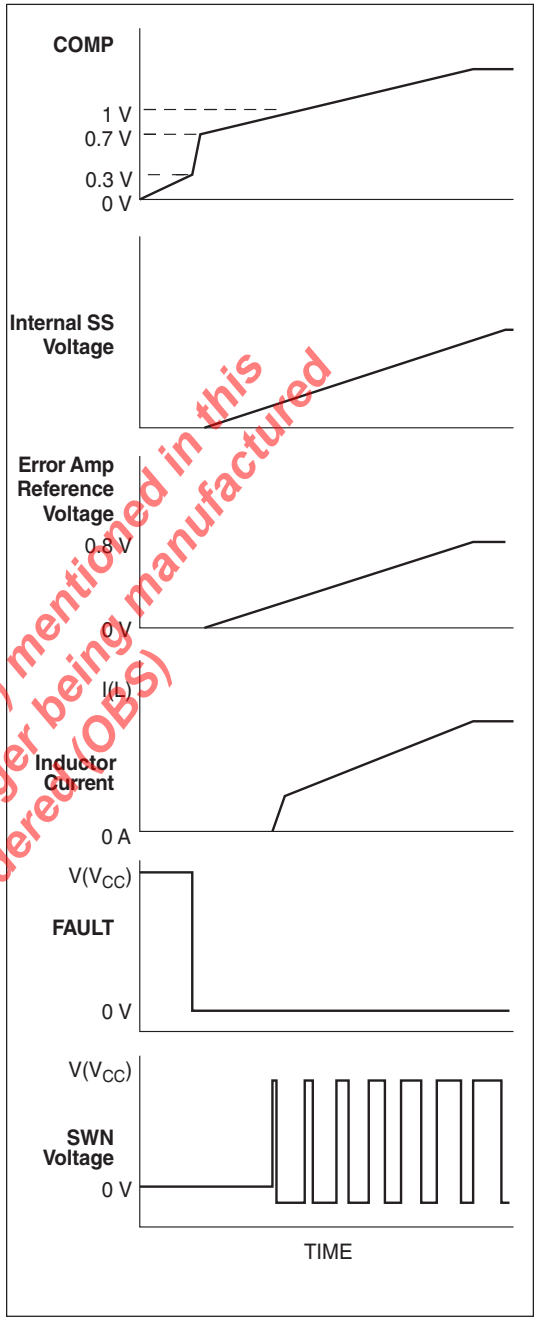
Soft start is required on step-down controllers to prevent excess inrush current through the power train during start-up. Typically this is managed by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up either the error amp reference or the error amp output (COMP). The control loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady-state duty cycle as the output voltage increases to its regulated value. As a result of controlling the inductor volt*second product during startup, inrush current is also controlled.

In the SP6128A the duration of the soft-start is controlled by an internal timing circuit that provides a 0.3V/mS slew-rate, which is used during startup and overcurrent to set the hiccup time. The SP6128A implements soft-start by ramping up the error amplifier reference voltage providing a controlled slew-rate of the output voltage, thereby preventing overshoot and inrush current at power up.

The presence of the output capacitor creates extra current draw during startup. Simply stated, dV_{OUT}/dt requires an average sustained current in the output capacitor and this current must be considered while calculating peak inrush current and over current thresholds. An approximate expression to determine the excess inrush current due to the dV_{OUT}/dt of the output capacitor C_{OUT} is:

$$I_{inrush} = C_{OUT} \times (0.27\ V/ms) \times \frac{V_{OUT}}{0.8V}$$

As the figure shows, the SS voltage controls a variety of signals. First, provided all the external fault conditions are removed, an internal 5µA pull-up at the COMP pin brings the SP6128A out of shutdown mode. The internal timing circuit is then activated and controls the ramp-up of the error amp reference voltage. The COMP pin is pulled to 0.7V by the internal clamp and then gradually charges preventing the error amplifier from forcing the loop to maximum duty cycle. As the COMP voltage crosses about 1V (valley voltage of the PWM ramp), the driver begins to switch the high side MOSFET with narrow pulses in an effort to keep the converter output regulated . The SP6128A operates at low duty cycle as the COMP voltage increases above 1V. As the error amp reference ramps upward, the driver pulses widen until a steady state value is reached and the output voltage is regulated to the final value ending the soft start charge cycle.



Hiccup Mode

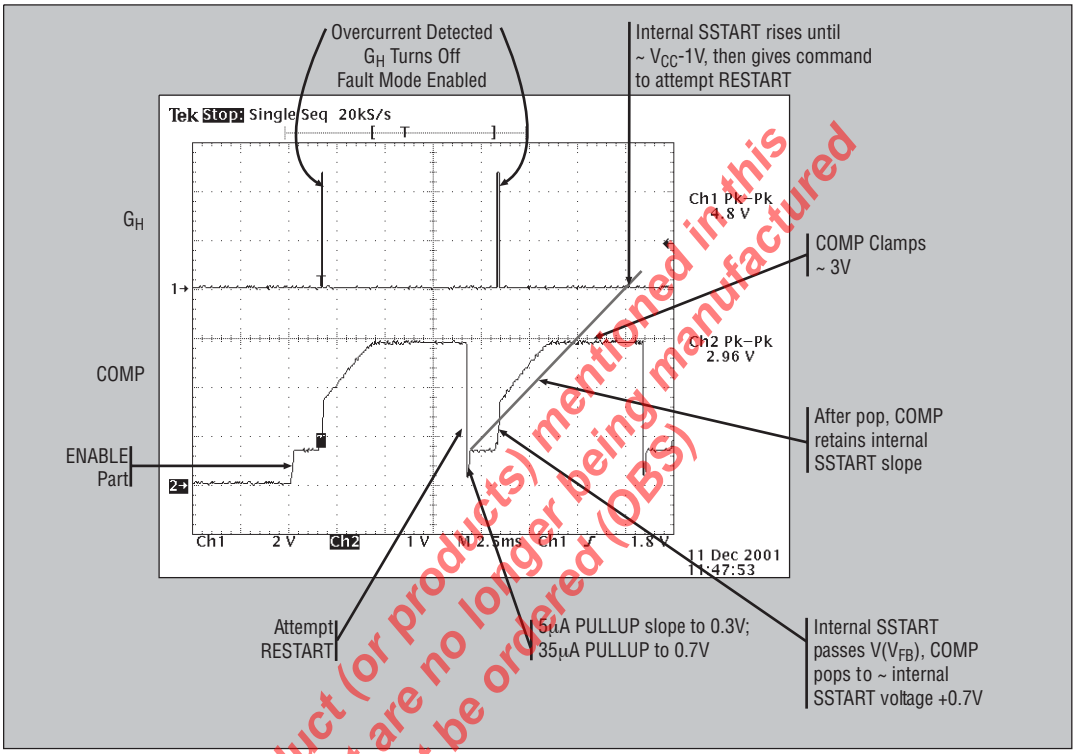
When the converter enters a fault mode, the SP6128A holds the high side and low side MOSFETs off for a finite period of time. Provided that the SP6128A is enabled, this time is set by the internal charge of the soft-start capacitor. In the event of an overcurrent condition, the current sense comparator sets the fault latch, which in turn discharge the internal SS capacitor, the COMP pin and holds the output drivers off. During this condition, the SP6128A stays off for the time it takes to discharge the COMP pin down to the 0.29V shutdown threshold. At this point, the fault latch is reset, but before the SP6128A is allowed to attempt restart, the COMP pin has to charge back to 1V before any output switching can be initiated. Then, the regulator attempts to restart normally by delivering short gate pulses and if the overcurrent condition is still present, the cycle will repeat itself. However, if upon restart, the overcurrent condition is still present, the SP6128A will detect the fault and remain in a fault state until the internal soft start voltage reaches about V_{CC}-1V thereby increasing the MOSFET off-time. This protection scheme minimizes thermal stress to the regulator components as the overcurrent condition persists.

A more detailed description of the waveform is shown below.

SP6128A OVER CURRENT (HICCUP MODE)

Test Conditions

V_{FB} = 0.7V
V_{CC} = PV_{CC} = 5.0V
BST = 5.0V
SWN - tied to GND through 1k Resistor
COMP – released from GND



Over Current Protection

Over current protection on the SP6128A is implemented through detection of an excess voltage condition across the high side NMOS switch during conduction. This is typically referred to as high side $R_{DS(ON)}$ detection and eliminates the need of an external sense resistor. The over current comparator charges an internal sampling capacitor each time V_{SWN} is lower than (V_{ISET} - 140mV) and the GH voltage is high. The discharge/charge current ratio on the sampling capacitor is about 2%. Therefore, provided that the over current condition persists, the capacitor voltage will be pumped up during each time GH switches high. This voltage will trigger an over current condition upon reaching a CMOS inverter threshold. There are many advantages to this approach. First, the filtering action of the gated scheme protects against false and undesirable triggering that could occur during a minor transient overload condition or supply line noise. Furthermore, the total amount of time to trigger the fault depends on the on-time of the high side NMOS switch. Fifteen, 1µs pulses are equivalent to thirty, 500ns pulses or one, 15µs pulse, however, depending on the period, each scenario takes a different amount of total time to trigger a fault. Therefore, the fault becomes an indicator of average power in the high side

switch. The I_{SET} current has a temperature coefficient in an effort to first order match the thermal characteristics of the $R_{DS(ON)}$ of the high side NMOS switch. It assumed that the SP6128A will be used in compact designs where there is a high amount of thermal coupling between the high side switch and the controller.

Discontinuous Start Up

Today's distributed power systems require multiple supply voltages, such as core and I/O voltages. In many applications, there's requirement on the maximum voltage difference allowed between these supplies at any time. This requirement can be potentially violated during power start up when individual power supply ramps up in sequence or in different slew rates. As a solution, system designers often pre-charge power supplies through an external circuit prior to start up. Unfortunately, under this condition many existing synchronous controllers turn on the low side MOSFET during soft start for a long period of time, thereby, discharging the output capacitors. The discharge period creates a number of problems. One is the obvious problem of losing the intended pre-charged output voltage. Another problem is a build up of excessive and unchecked current in the low side MOSFET and inductor. Lastly, this uncontrolled discharge current creates conditions that could damage either the distributed power supplies or the rather expensive "load" ICs.

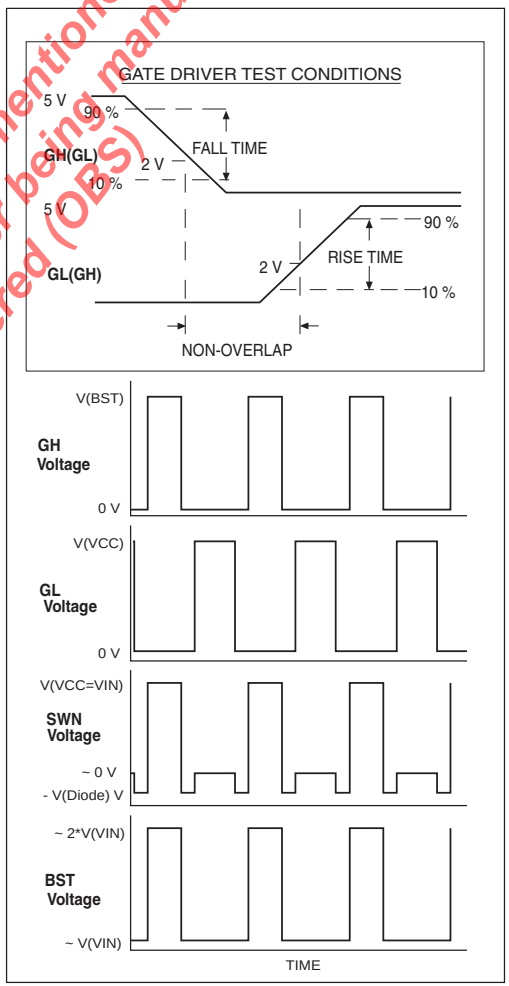
To prevent soft start from discharging the pre-charged output, SP6128A has built-in discontinuous start up. This operation disables the low side MOSFET driver GL during start up until either there is GH pulse or the internal SSTART reaches Vcc-1V. This feature eliminates the output discharging path during start up. During the steady state operation, the GL is fully engaged, and the operation is identical to regular synchronous buck converters.

Output Drivers

The SP6128A, unlike some other bipolar controller IC's, incorporates gate drivers with rail-to-rail swing that help prevent spurious turn on due to capacitive coupling. The driver stage consists of one high side NMOS, 4Ω driver, GH, and one low side, 4 Ω, NMOS driver, GL, optimized for driving external power MOSFET's in a synchronous buck topology. The output drivers also provide gate drive non-overlap mechanism that provides a dead time between GH and GL transitions to avoid potential shoot-through problems in the external MOSFETs.

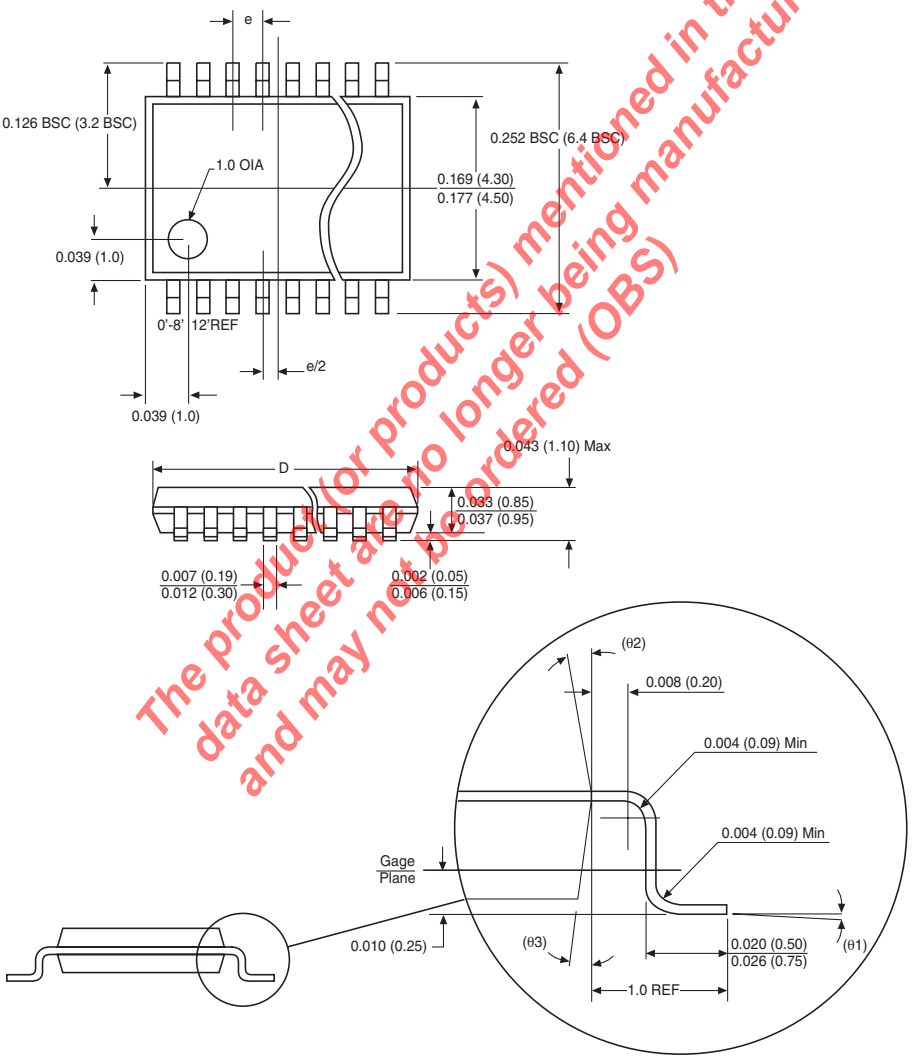
The following figure shows typical waveforms for the output drivers.

As with all synchronous designs, care must be taken to ensure that the MOSFETs are properly chosen for non-overlap time, enhancement gate drive voltage, "on" resistance $R_{DS(ON)}$, reverse transfer capacitance Crss, input voltage and maximum output current.



PLASTIC THIN SMALL OUTLINE (TSSOP)

DIMENSIONS in inches (mm) Minimum/Maximum	
Symbol	**14 Lead**
D	0.193/0.201 (4.90/5.10)
e	0.026 BSC (0.65 BSC)



ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
SP6128AEY	-40˚C to +85˚C	14-Pin TSSOP
SP6128AEY/TR	-40˚C to +85˚C	14-Pin TSSOP
SP6128AHY	-40˚C to +105˚C	14-Pin TSSOP
SP6128AHY/TR	-40˚C to +105˚C	14-Pin TSSOP
SP6128ACY	0˚C to +70˚C	14-Pin TSSOP
SP6128ACY/TR	0˚C to +70˚C	14-Pin TSSOP

Available in lead free packaging. To order add "-L" suffix to part number.
Example: SP6128AEY/TR = standard; SP6128AEY-L/TR = lead free

/TR = Tape and Reel
Pack quantity is 2,500 for TSSOP.

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ANALOG EXCELLENCE

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