



**THE DATASHEET OF
MB95F274HPF-G-SNE2**





MB95260H/270H/280H are series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock (main OSC clock and sub-OSC clock are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K)

- Selectable main clock source
 - Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
 - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
 - Main CR clock (1/8/10 MHz \pm 3%, maximum machine clock frequency: 10 MHz)
- Selectable subclock source
 - Sub-OSC clock (32.768 kHz)
 - External clock (32.768 kHz)
 - Sub CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

Timer

- 8/16-bit composite timer
- Time-base timer
- Watch prescaler

LIN-UART (only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K)

- Full duplex double buffer
- Capable of clock-synchronized serial data transfer and clock-asynchronous serial data transfer

External interrupt

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/10-bit A/D converter

- 8-bit or 10-bit resolution can be selected.

Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port (Max: 17) (MB95F262K/F263K/F264K)

- General-purpose I/O ports (Max):
CMOS I/O: 15, N-ch open drain: 2

I/O port (Max: 16) (MB95F262H/F263H/F264H)

- General-purpose I/O ports (Max):
CMOS I/O: 15, N-ch open drain: 1

I/O port (Max: 5) (MB95F272K/F273K/F274K)

- General-purpose I/O ports (Max):
CMOS I/O: 3, N-ch open drain: 2

I/O port (Max: 4) (MB95F272H/F273H/F274H)

- General-purpose I/O ports (Max):
CMOS I/O: 3, N-ch open drain: 1

I/O port (Max: 13) (MB95F282K/F283K/F284K)

- General-purpose I/O ports (Max):
CMOS I/O: 11, N-ch open drain: 2

I/O port (Max: 12) (MB95F282H/F283H/F284H)

- General-purpose I/O ports (Max):
CMOS I/O: 11, N-ch open drain: 1

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Power-on reset

- A power-on reset is generated when the power is switched on.

Low-voltage detection reset circuit

- Built-in low-voltage detector

Clock supervisor counter

- Built-in clock supervisor counter function

Programmable port input voltage level

- CMOS input level / hysteresis input level

Dual operation Flash memory

- The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

- Protects the content of the Flash memory

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1. Product Line-up
MB95260H Series

| Part number | MB95F262H | MB95F263H | MB95F264H | MB95F262K | MB95F263K | MB95F264K |
|----------------------------------|--|-----------|-----------|--|-----------|-----------|
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected by software | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max) : 16 • CMOS I/O : 15 • N-ch open drain : 1 | | | <ul style="list-style-type: none"> • I/O ports (Max) : 17 • CMOS I/O : 15 • N-ch open drain : 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace three bytes of data. | | | | | |
| LIN-UART | <ul style="list-style-type: none"> • A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. • The LIN function can be used as a LIN master or a LIN slave. | | | | | |
| 8/10-bit A/D converter | 6 channels 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 2 channels <ul style="list-style-type: none"> • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave. | | | | | |
| External interrupt | 6 channels <ul style="list-style-type: none"> • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> • 1-wire serial control • It supports serial writing. (asynchronous mode) | | | | | |

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| Part number | MB95F262H | MB95F263H | MB95F264H | MB95F262K | MB95F263K | MB95F264K |
|-----------------|--|-----------|-----------|-----------|-----------|-----------|
| Parameter | | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | |
| Flash memory | <ul style="list-style-type: none"> • It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | DIP-24P-M07 LCC-32P-M19 FPT-20P-M09 FPT-20P-M10 | | | | | |

MB95270H Series

| Part number | MB95F272H | MB95F273H | MB95F274H | MB95F272K | MB95F273K | MB95F274K |
|----------------------------------|--|-----------|-----------|--|-----------|-----------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected by software | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max) : 4 • CMOS I/O : 3 • N-ch open drain : 1 | | | <ul style="list-style-type: none"> • I/O ports (Max) : 5 • CMOS I/O : 3 • N-ch open drain : 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace three bytes of data. | | | | | |
| LIN-UART | No LIN-UART | | | | | |
| 8/10-bit A/D converter | 2 channels 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 1 channel <ul style="list-style-type: none"> • The timer can be configured as an "8-bit timer \times 2 channels" or a "16-bit timer \times 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave. | | | | | |
| External interrupt | 2 channels <ul style="list-style-type: none"> • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> • 1-wire serial control • It supports serial writing. (asynchronous mode) | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | |
| Flash memory | <ul style="list-style-type: none"> • It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | DIP-8P-M03 FPT-8P-M08 | | | | | |

MB95280H Series

| Part number | MB95F282H | MB95F283H | MB95F284H | MB95F282K | MB95F283K | MB95F284K |
|----------------------------------|--|-----------|-----------|--|-----------|-----------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected by software | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain : 1 | | | <ul style="list-style-type: none"> • I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain : 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-internal CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace three bytes of data. | | | | | |
| LIN-UART | <ul style="list-style-type: none"> • A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. • The LIN function can be used as a LIN master or a LIN slave. | | | | | |
| 8/10-bit A/D converter | 5 channels | | | | | |
| | 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 1 channel | | | | | |
| | <ul style="list-style-type: none"> • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave. | | | | | |
| External interrupt | 6 channels | | | | | |
| | <ul style="list-style-type: none"> • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from standby modes. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> • 1-wire serial control • It supports serial writing. (asynchronous mode) | | | | | |

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| Part number | MB95F282H | MB95F283H | MB95F284H | MB95F282K | MB95F283K | MB95F284K |
|-----------------|--|-----------|-----------|-----------|-----------|-----------|
| Parameter | | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | |
| Flash memory | <ul style="list-style-type: none"> • It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | LCC-32P-M19 DIP-16P-M06 FPT-16P-M06 | | | | | |

2. Packages and Corresponding Products

| Part number Package | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 | MB95F2 |
|------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| | 62H | 62K | 63H | 63K | 64H | 64K | 72H | 72K | 73H | 73K | 74H | 74K |
| DIP-24P-M07 | O | O | O | O | O | O | X | X | X | X | X | X |
| FPT-20P-M09 | O | O | O | O | O | O | X | X | X | X | X | X |
| FPT-20P-M10 | O | O | O | O | O | O | X | X | X | X | X | X |
| DIP-16P-M06 | X | X | X | X | X | X | X | X | X | X | X | X |
| FPT-16P-M06 | X | X | X | X | X | X | X | X | X | X | X | X |
| DIP-8P-M03 | X | X | X | X | X | X | O | O | O | O | O | O |
| FPT-8P-M08 | X | X | X | X | X | X | O | O | O | O | O | O |
| LCC-32P-M19 | O | O | O | O | O | O | X | X | X | X | X | X |

| Part number Package | MB95F282H | MB95F282K | MB95F283H | MB95F283K | MB95F284H | MB95F284K |
|------------------------|-------------|-----------|-----------|-----------|-----------|-----------|
| | DIP-24P-M07 | X | X | X | X | X |
| FPT-20P-M09 | X | X | X | X | X | X |
| FPT-20P-M10 | X | X | X | X | X | X |
| DIP-16P-M06 | O | O | O | O | O | O |
| FPT-16P-M06 | O | O | O | O | O | O |
| DIP-8P-M03 | X | X | X | X | X | X |
| FPT-8P-M08 | X | X | X | X | X | X |
| LCC-32P-M19 | O | O | O | O | O | O |

O: Available
X: Unavailable

3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “24. Electrical Characteristics”.

Package

For details of information on each package, see “2. Packages and Corresponding Products” and “28. Package Dimension”.

Operating voltage

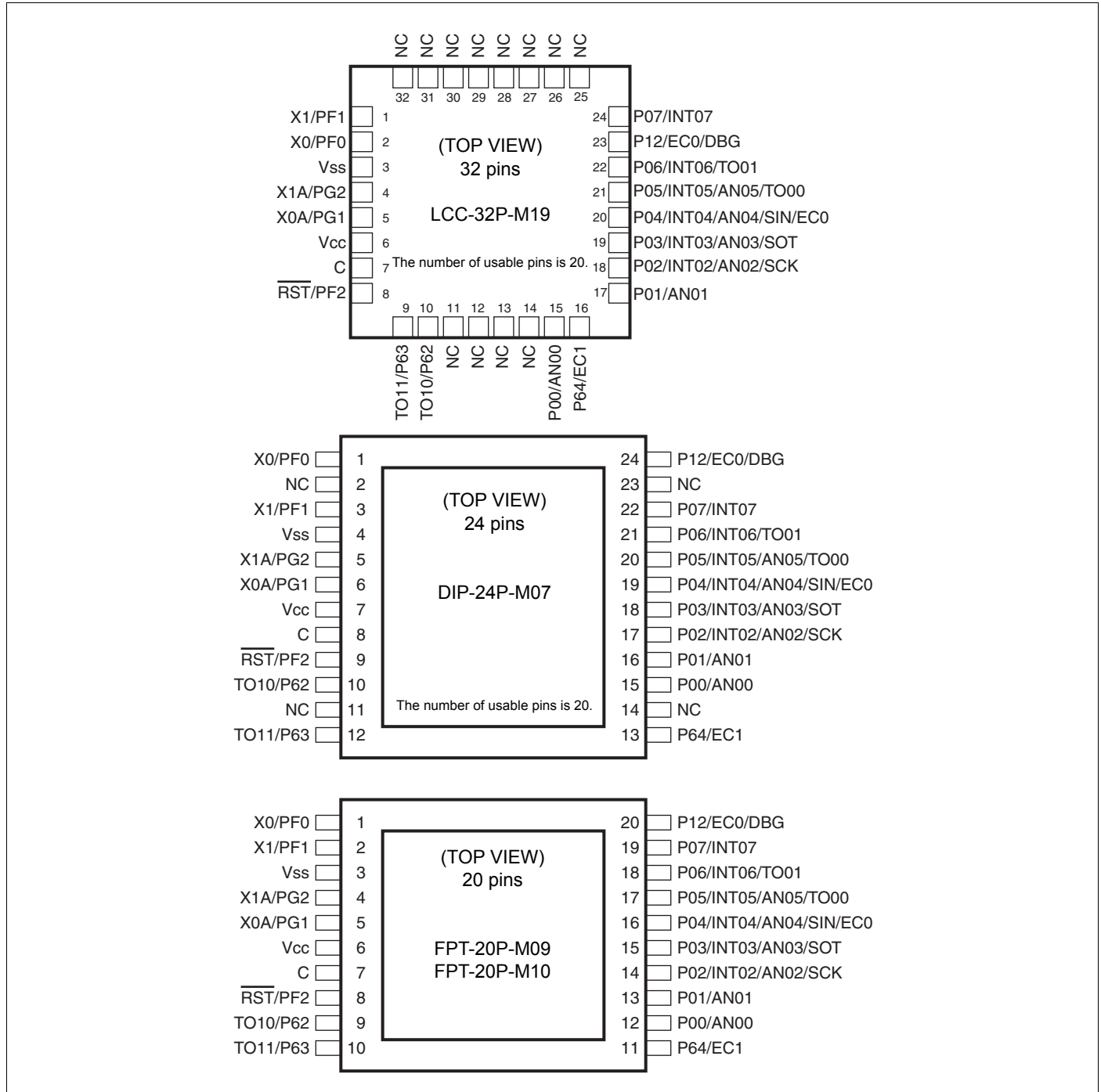
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “24. Electrical Characteristics”.

On-chip debug function

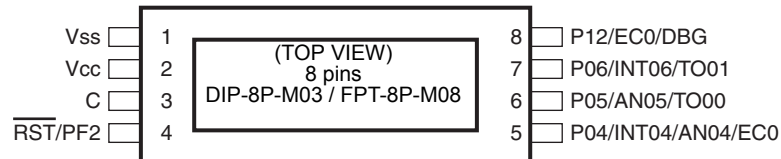
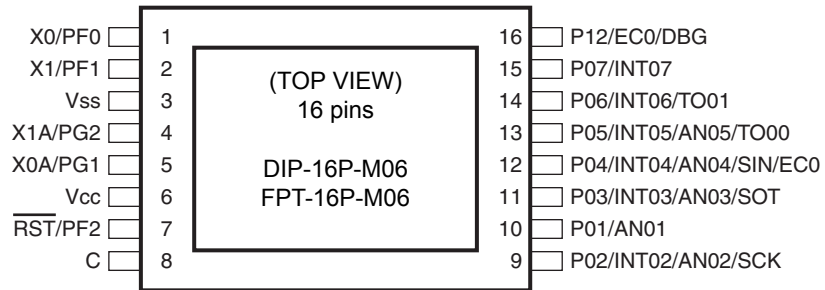
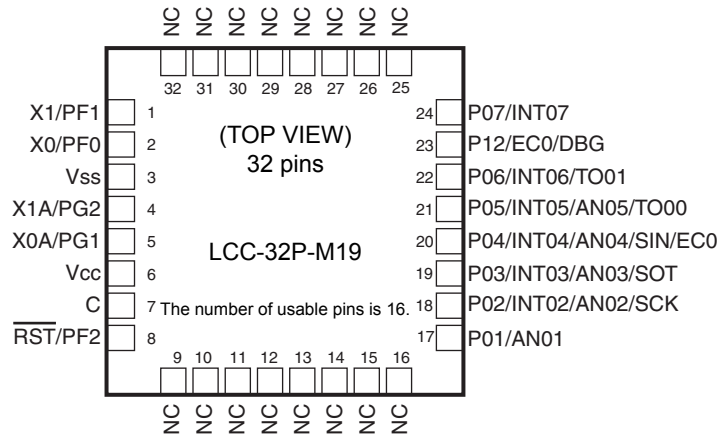
The on-chip debug function requires that V_{CC} , V_{SS} and 1 serial-wire be connected to an evaluation tool. In addition, if the Flash memory data has to be updated, the PF2/RST pin must also be connected to the same evaluation tool.

4. Pin Assignment



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5. Pin Description (MB95260H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | Vss | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | Vcc | — | Power supply pin |
| 7 | C | — | Capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H. |
| 9 | P63 | D | General-purpose I/O port High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 10 | P62 | D | General-purpose I/O port High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 12 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 13 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 14 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 15 | P00 | E | General-purpose I/O port |
| | AN00 | | A/D converter analog input pin |
| 16 | P64 | D | General-purpose I/O port |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 17 | P01 | E | General-purpose I/O port |
| | AN01 | | A/D converter analog input pin |
| 18 | P02 | E | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 19 | P03 | E | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |

(Continued)

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|---|
| 20 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 21 | P05 | E | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | G | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 27 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 28 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 29 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 30 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 31 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 32 | NC | — | It is an internally connected pin. Always leave it unconnected. |

*: For the I/O circuit types, see "11. I/O Circuit Type".

6. Pin Description (MB95260H Series, 24 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 3 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 4 | V _{SS} | — | Power supply pin (GND) |
| 5 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 6 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 7 | V _{CC} | — | Power supply pin |
| 8 | C | — | Capacitor connection pin |
| 9 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H. |
| 10 | P62 | D | General-purpose I/O port High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 12 | P63 | D | General-purpose I/O port High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 13 | P64 | D | General-purpose I/O port |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 14 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 15 | P00 | E | General-purpose I/O port |
| | AN00 | | A/D converter analog input pin |
| 16 | P01 | E | General-purpose I/O port |
| | AN01 | | A/D converter analog input pin |
| 17 | P02 | E | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |

(Continued)

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|---|
| 18 | P03 | E | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 19 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 20 | P05 | E | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 21 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P07 | G | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| 23 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 24 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see “11. I/O Circuit Type”.

7. Pin Description (MB95260H Series, 20 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | V _{SS} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{CC} | — | Power supply pin |
| 7 | C | — | Capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This is a dedicated reset pin in MB95F262H/F263H/F264H. |
| 9 | P62 | D | General-purpose I/O port High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 10 | P63 | D | General-purpose I/O port High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | P64 | D | General-purpose I/O port |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 12 | P00 | E | General-purpose I/O port |
| | AN00 | | A/D converter analog input pin |
| 13 | P01 | E | General-purpose I/O port |
| | AN01 | | A/D converter analog input pin |
| 14 | P02 | E | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 15 | P03 | E | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |

(Continued)

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--|
| 16 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 17 | P05 | E | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 18 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 19 | P07 | G | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| 20 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "11. I/O Circuit Type".

8. Pin Description (MB95270H Series, 8 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | V _{SS} | — | Power supply pin (GND) |
| 2 | V _{CC} | — | Power supply pin |
| 3 | C | — | Capacitor connection pin |
| 4 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This pin is a dedicated reset pin in MB95F272H/F273H/F274H. |
| 5 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 6 | P05 | E | General-purpose I/O port High-current pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 7 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 8 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see “11. I/O Circuit Type”.

9. Pin Description (MB95280H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | Vss | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | Vcc | — | Power supply pin |
| 7 | C | — | Capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This is a dedicated reset pin in MB95F282H/F283H/F284H. |
| 9 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 10 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 11 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 12 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 13 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 14 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 15 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 16 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 17 | P01 | E | General-purpose I/O port |
| | AN01 | | A/D converter analog input pin |
| 18 | P02 | E | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 19 | P03 | E | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 20 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |

(Continued)

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|---|
| 21 | P05 | E | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | G | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 27 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 28 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 29 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 30 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 31 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 32 | NC | — | It is an internally connected pin. Always leave it unconnected. |

*: For the I/O circuit types, see "11. I/O Circuit Type".

10. Pin Description (MB95280H Series, 16 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|--|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | V _{SS} | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | V _{CC} | — | Power supply pin |
| 7 | PF2 | A | General-purpose I/O port |
| | $\overline{\text{RST}}$ | | Reset pin This pin is a dedicated reset pin in MB95F282H/F283H/F284H. |
| 8 | C | — | Capacitor connection pin |
| 9 | P02 | E | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 10 | P01 | E | General-purpose I/O port |
| | AN01 | | A/D converter analog input pin |
| 11 | P03 | E | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 12 | P04 | F | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |

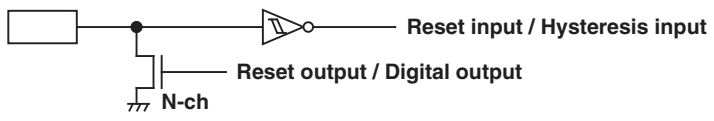
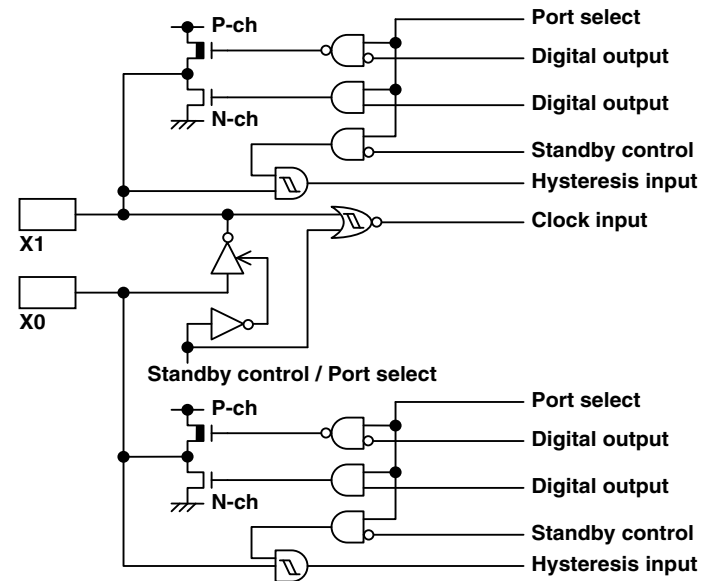
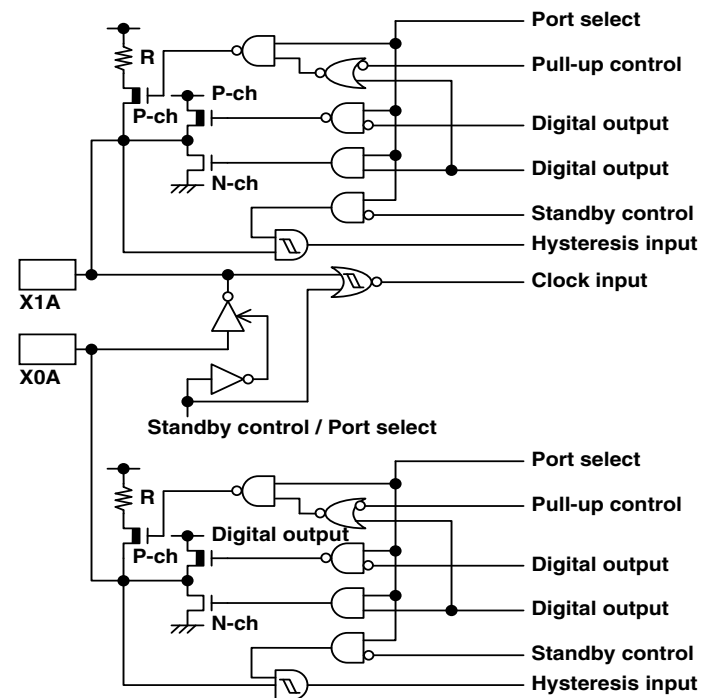
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| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--|
| 13 | P05 | E | General-purpose I/O port High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 clock input pin |
| 14 | P06 | G | General-purpose I/O port High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 clock input pin |
| 15 | P07 | G | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| 16 | P12 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

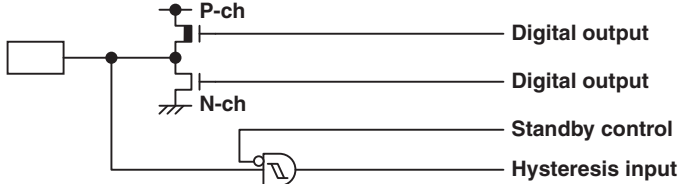
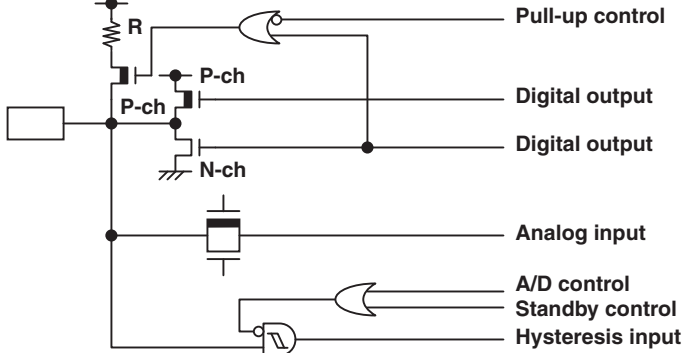
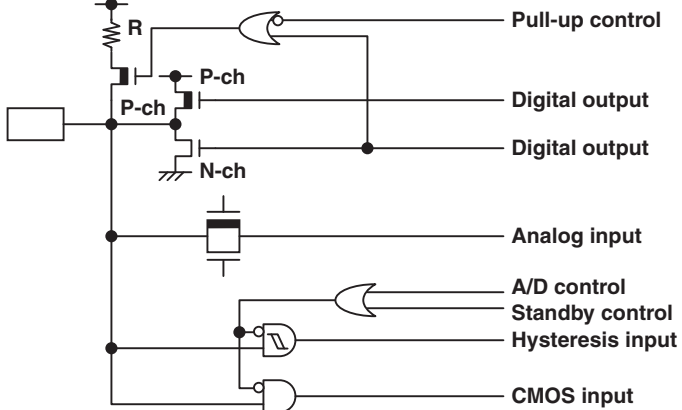
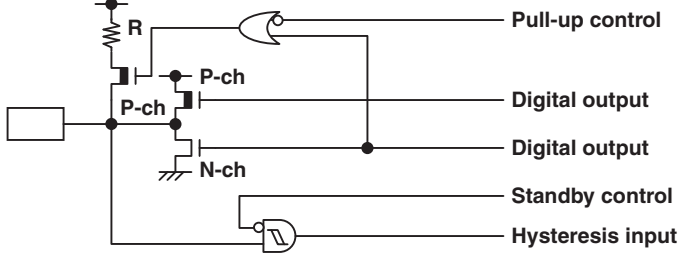
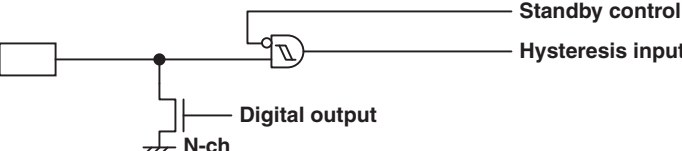
*: For the I/O circuit types, see "11. I/O Circuit Type".

11. I/O Circuit Type

| Type | Circuit | Remarks |
|------|---|---|
| A |  | <ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input • Reset output |
| B |  | <ul style="list-style-type: none"> • Oscillation circuit • High-speed side • Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input |
| C |  | <ul style="list-style-type: none"> • Oscillation circuit • Low-speed side • Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available |

(Continued)

(Continued)

| Type | Circuit | Remarks |
|------|---|--|
| D |  | <ul style="list-style-type: none"> • CMOS output • Hysteresis input |
| E |  | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available |
| F |  | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • CMOS input • Pull-up control available |
| G |  | <ul style="list-style-type: none"> • Hysteresis input • CMOS output • Pull-up control available |
| H |  | <ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input |

12. Notes on Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “24.1 Absolute Maximum Ratings” of “24. Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

13. Pin Connection

Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k Ω . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

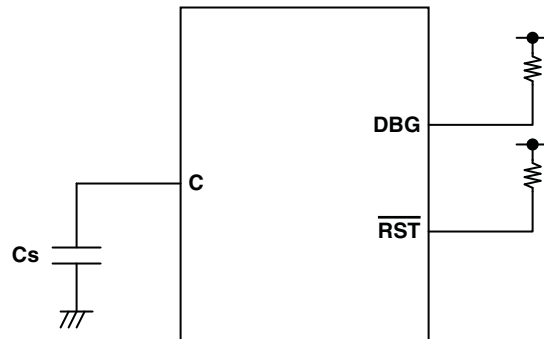
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The PF2/ $\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/ $\overline{\text{RST}}$ pin can be enabled by the RSTOE bit of the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

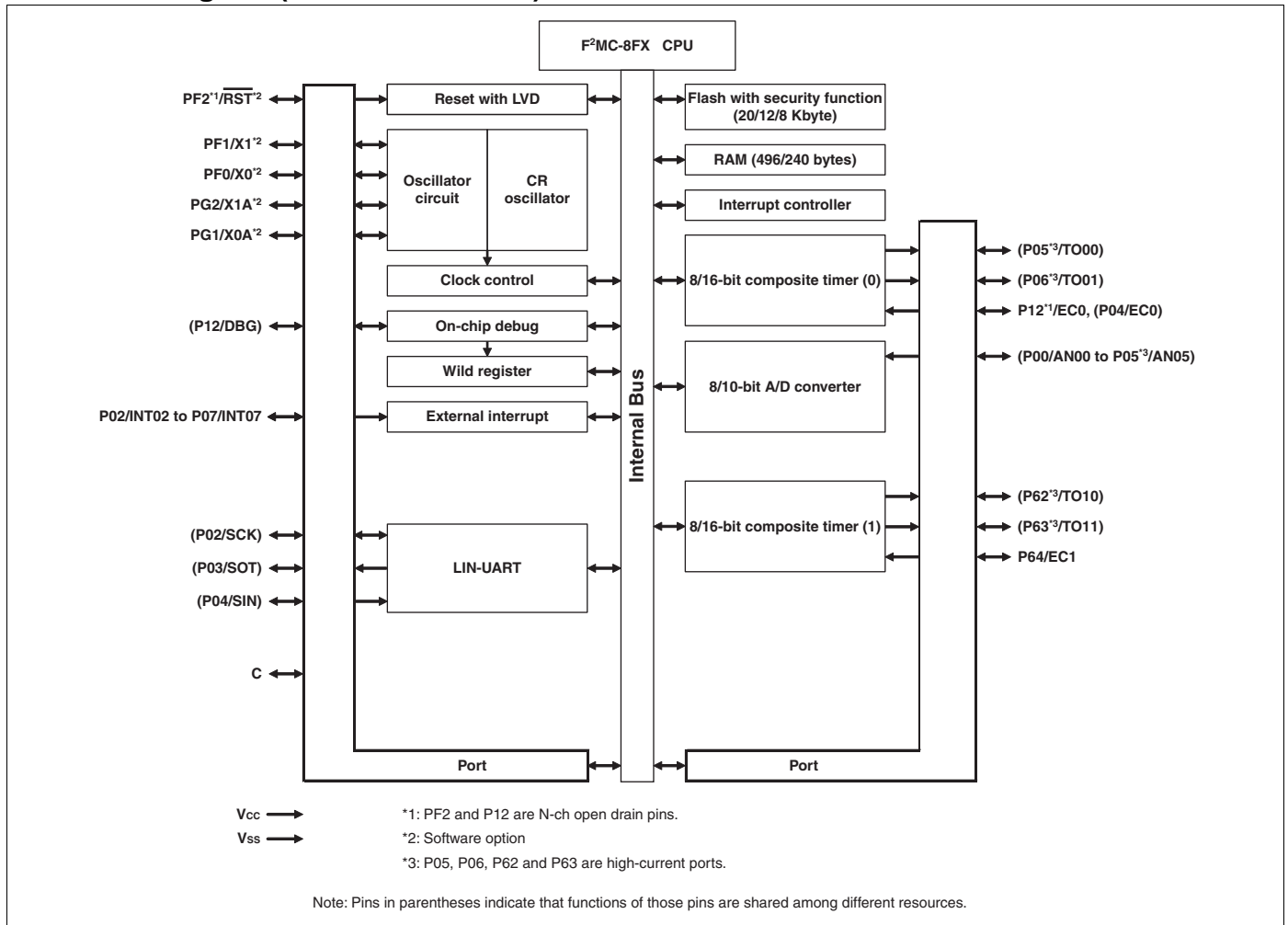
C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S . For the connection to a smoothing capacitor C_S , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

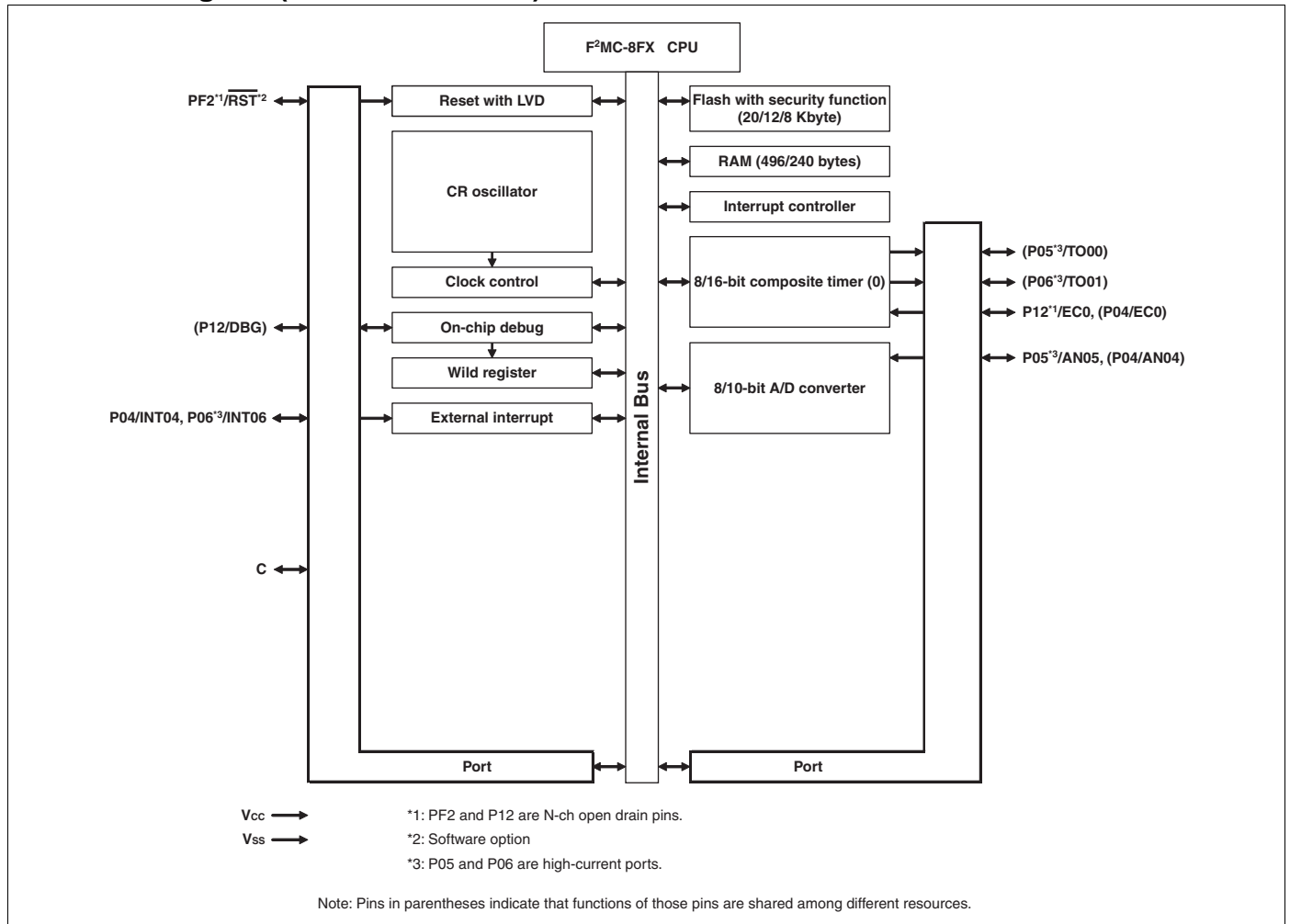
DBG/RST/C pins connection diagram



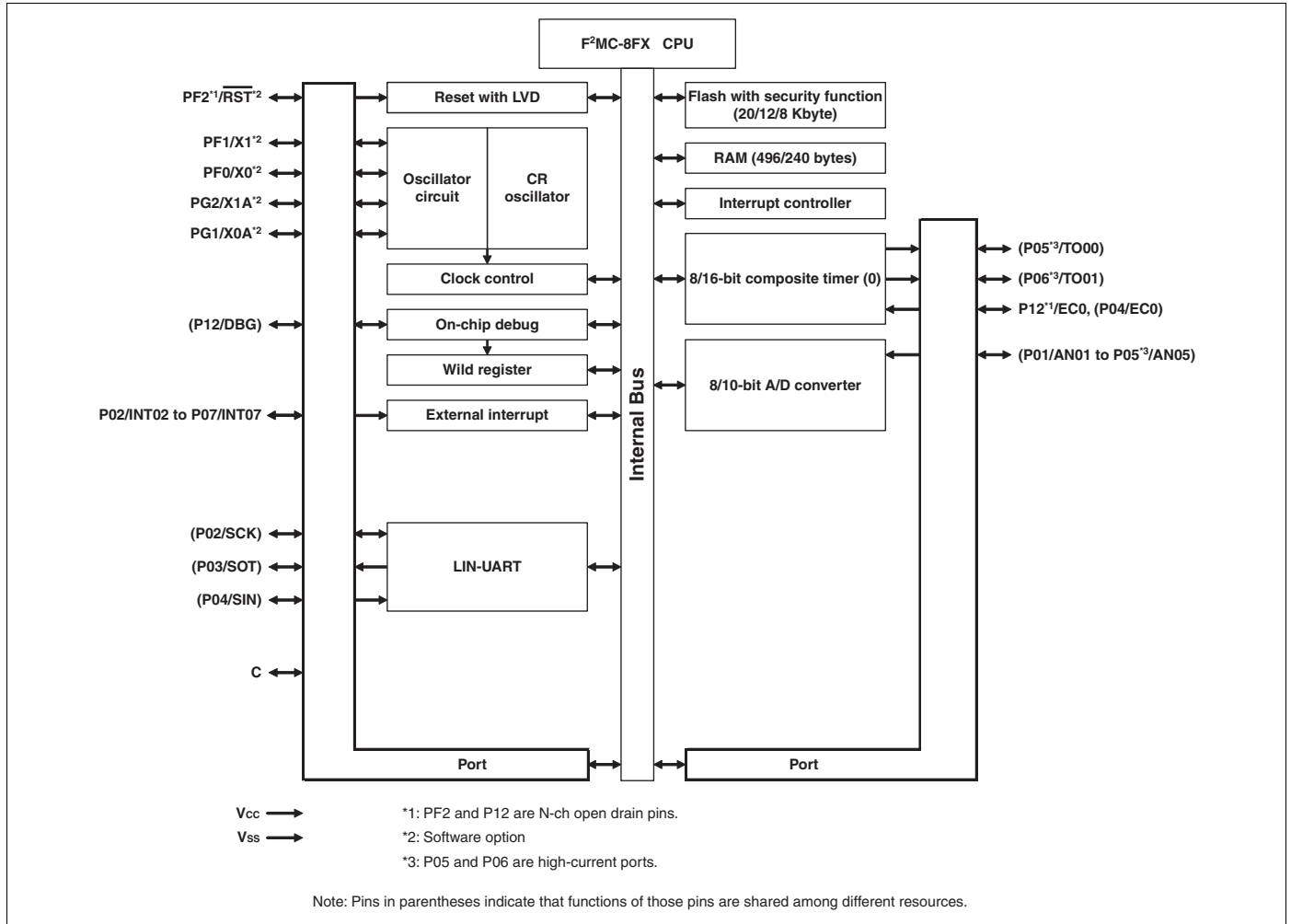
14. Block Diagram (MB95260H Series)



15. Block Diagram (MB95270H Series)



16. Block Diagram (MB95280H Series)



17. CPU Core

Memory Space

The memory space of the MB95260H/270H/280H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95260H/270H/280H Series are shown below.

Memory Maps

| MB95F262H/F262K/F272H/ F272K/F282H/F282K | MB95F263H/F263K/F273H/ F273K/F283H/F283K | MB95F264H/F264K/F274H/ F274K/F284H/F284K |
|---|---|---|
| 0000 _H | 0000 _H | 0000 _H |
| 0080 _H | 0080 _H | 0080 _H |
| 0090 _H | 0090 _H | 0090 _H |
| 0100 _H | 0100 _H | 0100 _H |
| 0180 _H | 0200 _H | 0200 _H |
| | 0280 _H | 0280 _H |
| 0F80 _H | 0F80 _H | 0F80 _H |
| 1000 _H | 1000 _H | 1000 _H |
| | | |
| B000 _H | B000 _H | B000 _H |
| C000 _H | C000 _H | |
| | | |
| F000 _H | E000 _H | |
| FFFF _H | FFFF _H | FFFF _H |

18. I/O Map (MB95260H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | — | (Disabled) | — | — |
| 0007 _H | SYCC | System clock control register | R/W | 0000X011 _B |
| 0008 _H | STBC | Standby control register | R/W | 0000XXXX _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XX100011 _B |
| 000E _H to 0015 _H | — | (Disabled) | — | — |
| 0016 _H | PDR6 | Port 6 data register | R/W | 00000000 _B |
| 0017 _H | DDR6 | Port 6 direction register | R/W | 00000000 _B |
| 0018 _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0034 _H | — | (Disabled) | — | — |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0038 _H | T11CR1 | 8/16-bit composite timer 11 status control register 1 ch. 1 | R/W | 00000000 _B |
| 0039 _H | T10CR1 | 8/16-bit composite timer 10 status control register 1 ch. 1 | R/W | 00000000 _B |
| 003A _H to 0048 _H | — | (Disabled) | — | — |
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H to 004F _H | — | (Disabled) | — | — |
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR/TDR | LIN-UART receive/transmit data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register upper | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register lower | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 0000XXXX _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (Upper) ch. 0 | R/W | 00000000 _B |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0F81 _H | WRARL0 | Wild register address setting register (Lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (Upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (Lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (Upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (Lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register ch. 0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register ch. 0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register ch. 0 | R/W | 00000000 _B |
| 0F97 _H | T11CR0 | 8/16-bit composite timer 11 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F98 _H | T10CR0 | 8/16-bit composite timer 10 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F99 _H | T11DR | 8/16-bit composite timer 11 data register ch. 1 | R/W | 00000000 _B |
| 0F9A _H | T10DR | 8/16-bit composite timer 10 data register ch. 1 | R/W | 00000000 _B |
| 0F9B _H | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register ch. 1 | R/W | 00000000 _B |
| 0F9C _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (Lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRTH | Main CR clock trimming register (Upper) | R/W | 1XXXXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (Lower) | R/W | 000XXXXX _B |

(Continued)

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0FE6 _H , 0FE7 _H | — | (Disabled) | — | — |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R/W | 00000000 _B |
| 0FEB _H | WDTH | Watchdog timer selection ID register (Upper) | R/W | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (Lower) | R/W | XXXXXXXX _B |
| 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H to 0FFF _H | — | (Disabled) | — | — |

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.

19. I/O Map (MB95270H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | — | (Disabled) | — | — |
| 0007 _H | SYCC | System clock control register | R/W | 0000X011 _B |
| 0008 _H | STBC | Standby control register | R/W | 0000XXXX _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XX100011 _B |
| 000E _H to 0015 _H | — | (Disabled) | — | — |
| 0016 _H | — | (Disabled) | — | — |
| 0017 _H | — | (Disabled) | — | — |
| 0018 _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | — | (Disabled) | — | — |
| 002B _H | — | (Disabled) | — | — |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0034 _H | — | (Disabled) | — | — |
| 0035 _H | — | (Disabled) | — | — |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0038 _H | — | (Disabled) | — | — |
| 0039 _H | — | (Disabled) | — | — |
| 003A _H to 0048 _H | — | (Disabled) | — | — |
| 0049 _H | — | (Disabled) | — | — |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|---|-----|-----------------------|
| 004A _H | EIC20 | External interrupt circuit control register ch. 4 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6 | R/W | 00000000 _B |
| 004C _H to 004F _H | — | (Disabled) | — | — |
| 0050 _H | — | (Disabled) | — | — |
| 0051 _H | — | (Disabled) | — | — |
| 0052 _H | — | (Disabled) | — | — |
| 0053 _H | — | (Disabled) | — | — |
| 0054 _H | — | (Disabled) | — | — |
| 0055 _H | — | (Disabled) | — | — |
| 0056 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register upper | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register lower | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 00X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 0000XXXX _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | — | (Disabled) | — | — |
| 007C _H | — | (Disabled) | — | — |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (Upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (Lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0F83 _H | WRARH1 | Wild register address setting register (Upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (Lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (Upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (Lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register ch. 0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register ch. 0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register ch. 0 | R/W | 00000000 _B |
| 0F97 _H | — | (Disabled) | — | — |
| 0F98 _H | — | (Disabled) | — | — |
| 0F99 _H | — | (Disabled) | — | — |
| 0F9A _H | — | (Disabled) | — | — |
| 0F9B _H | — | (Disabled) | — | — |
| 0F9C _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | — | (Disabled) | — | — |
| 0FBD _H | — | (Disabled) | — | — |
| 0FBE _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (Lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRTH | Main CR clock trimming register (Upper) | R/W | 1XXXXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (Lower) | R/W | 000XXXXX _B |
| 0FE6 _H , 0FE7 _H | — | (Disabled) | — | — |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |

(Continued)

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R/W | 00000000 _B |
| 0FEB _H | WDTH | Watchdog timer selection ID register (Upper) | R/W | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (Lower) | R/W | XXXXXXXX _B |
| 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H to 0FFF _H | — | (Disabled) | — | — |

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.

20. I/O Map (MB95280H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | — | (Disabled) | — | — |
| 0007 _H | SYCC | System clock control register | R/W | 0000X011 _B |
| 0008 _H | STBC | Standby control register | R/W | 0000XXX _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00XX0000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XX100011 _B |
| 000E _H to 0015 _H | — | (Disabled) | — | — |
| 0016 _H | — | (Disabled) | — | — |
| 0017 _H | — | (Disabled) | — | — |
| 0018 _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H to 0034 _H | — | (Disabled) | — | — |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0038 _H | — | (Disabled) | — | — |
| 0039 _H | — | (Disabled) | — | — |
| 003A _H to 0048 _H | — | (Disabled) | — | — |
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|---|-----|-----------------------|
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H to 004F _H | — | (Disabled) | — | — |
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR/TDR | LIN-UART receive/transmit data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register upper | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register lower | R/W | 00000000 _B |
| 0070 _H | — | (Disabled) | — | — |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 0000XXXX _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0F80 _H | WRARH0 | Wild register address setting register (Upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (Lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (Upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (Lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (Upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (Lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register ch. 0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register ch. 0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register ch. 0 | R/W | 00000000 _B |
| 0F97 _H | — | (Disabled) | — | — |
| 0F98 _H | — | (Disabled) | — | — |
| 0F99 _H | — | (Disabled) | — | — |
| 0F9A _H | — | (Disabled) | — | — |
| 0F9B _H | — | (Disabled) | — | — |
| 0F9C _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (Lower) | R/W | 00000000 _B |
| 0FC4 _H to 0FE3 _H | — | (Disabled) | — | — |
| 0FE4 _H | CRTH | Main CR clock trimming register (Upper) | R/W | 1XXXXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (Lower) | R/W | 000XXXXX _B |

(Continued)

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|-----------------------|--|-----|-----------------------|
| 0FE6 _H , 0FE7 _H | — | (Disabled) | — | — |
| 0FE8 _H | SYSC | System configuration register | R/W | 11000011 _B |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | 00000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R/W | 00000000 _B |
| 0FEB _H | WDTH | Watchdog timer selection ID register (Upper) | R/W | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (Lower) | R/W | XXXXXXXX _B |
| 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H to 0FFF _H | — | (Disabled) | — | — |

R/W access symbols

R/W : Readable / Writable

R : Read only

Initial value symbols



0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".



X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.


21. Interrupt Source Table (MB95260H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div>   <div style="text-align: center;">Low</div> |
| External interrupt ch. 5 | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (Lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (Upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| 8/16-bit composite timer ch. 1 (Upper) | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| 8/16-bit composite timer ch. 1 (Lower) | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |

22. Interrupt Source Table (MB95270H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div>   <div style="text-align: center;">Low</div> |
| — | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| — | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| — | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| — | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (Lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (Upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| — | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| — | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| — | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| — | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |

23. Interrupt Source Table (MB95280H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | <div style="text-align: center;">High</div>  <div style="text-align: center;">Low</div> |
| External interrupt ch. 5 | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (Lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (Upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| — | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| — | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| — | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| — | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| — | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| — | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| — | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| — | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |

24. Electrical Characteristics

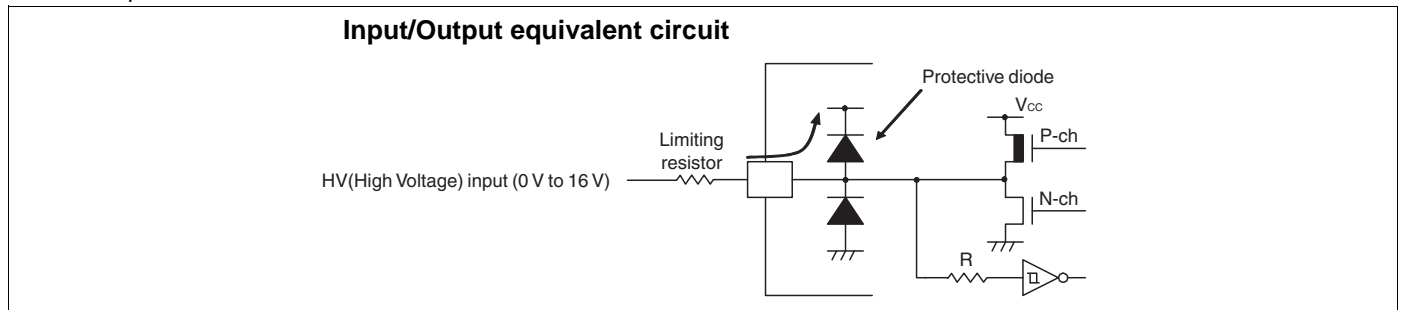
24.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|--------------------|----------------|--------------|------|--|
| | | Min | Max | | |
| Power supply voltage*1 | V_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | |
| Input voltage*1 | V_I | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | *2 |
| Output voltage*1 | V_O | $V_{SS} - 0.3$ | $V_{SS} + 6$ | V | *2 |
| Maximum clamp current | I_{CLAMP} | - 2 | + 2 | mA | Applicable to specific pins*3 |
| Total maximum clamp current | $\sum I_{CLAMP} $ | — | 20 | mA | Applicable to specific pins*3 |
| “L” level maximum output current | I_{OL1} | — | 15 | mA | Other than P05, P06, P62 and P63*4 |
| | I_{OL2} | | 15 | | P05, P06, P62 and P63*4 |
| “L” level average current | I_{OLAV1} | — | 4 | mA | Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin) |
| | I_{OLAV2} | | 12 | | P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin) |
| “L” level total maximum output current | $\sum I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\sum I_{OLAV}$ | — | 50 | mA | Total average output current= operating current × operating ratio (Total number of pins) |
| “H” level maximum output current | I_{OH1} | — | - 15 | mA | Other than P05, P06, P62 and P63*4 |
| | I_{OH2} | | - 15 | | P05, P06, P62 and P63*4 |
| “H” level average current | I_{OHAV1} | — | - 4 | mA | Other than P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin) |
| | I_{OHAV2} | | - 8 | | P05, P06, P62 and P63*4 Average output current= operating current × operating ratio (1 pin) |
| “H” level total maximum output current | $\sum I_{OH}$ | — | - 100 | mA | |
| “H” level total average output current | $\sum I_{OHAV}$ | — | - 50 | mA | Total average output current= operating current × operating ratio (Total number of pins) |
| Power consumption | P_d | — | 320 | mW | |
| Operating temperature | T_A | - 40 | + 85 | °C | |
| Storage temperature | T_{stg} | - 55 | + 150 | °C | |

(Continued)

(Continued)

- *1: These parameters are based on the condition that V_{SS} is 0.0 V.
- *2: V_I and V_O must not exceed $V_{CC} + 0.3$ V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.
- *3: Applicable to the following pins: P00 to P07, P62 to P64, PG1, PG2, PF0, PF1 (P00, P62, P63 and P64 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K. P01, P02, P03, P07, PG1, PG2, PF0 and PF1 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.)
 - Use under recommended operating conditions.
 - Use with DC voltage (current).
 - The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
 - The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
 - When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
 - If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
 - If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
 - Do not leave the HV (High Voltage) input pin unconnected.
 - Example of a recommended circuit:



- *4: P62 and P63 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

24.2 Recommended Operating Conditions

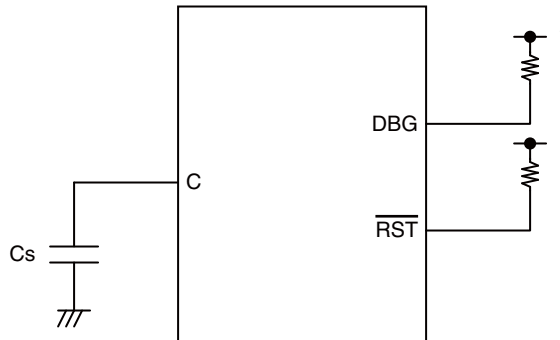
 (V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|-----------------------|-----------------|---------|-------|------|-------------------------------|-------------------------------|
| | | Min | Max | | | |
| Power supply voltage | V _{CC} | 2.4*1*2 | 5.5*1 | V | In normal operation | Other than on-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| | | 2.9 | 5.5 | | In normal operation | On-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| Smoothing capacitor | C _S | 0.022 | 1 | μF | *3 | |
| Operating temperature | T _A | -40 | + 85 | °C | Other than on-chip debug mode | |
| | | + 5 | + 35 | | On-chip debug mode | |

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pins connection diagram


*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device.

All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.

Users considering application outside the listed conditions are advised to contact their representatives beforehand.

24.3 DC Characteristics
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|---|--------------------------|----------------|-----|----------------|------------|--|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V_{IH1} | P04 | *1 | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | When CMOS input level (hysteresis input) is selected |
| | V_{IHS} | P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2 | *1 | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHM} | PF2 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| "L" level input voltage | V_{IL} | P04 | *1 | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | When CMOS input level (hysteresis input) is selected |
| | V_{ILS} | P00 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2 | *1 | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILM} | PF2 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | Hysteresis input |
| Open-drain output application voltage | V_D | PF2, P12 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 5.5$ | V | |
| "H" level output voltage | V_{OH1} | Output pins other than P05, P06, P12, P62, P63, PF2*2 | $I_{OH} = -4 \text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| | V_{OH2} | P05, P06, P62, P63*2 | $I_{OH} = -8 \text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| "L" level output voltage | V_{OL1} | Output pins other than P05, P06, P62, P63*2 | $I_{OL} = 4 \text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL2} | P05, P06, P62, P63*2 | $I_{OL} = 12 \text{ mA}$ | — | — | 0.4 | V | |
| Input leak current (Hi-Z output leak current) | I_{LI} | All input pins | $0.0 V < V_I < V_{CC}$ | - 5 | — | + 5 | μA | When pull-up resistance is disabled |
| Pull-up resistance | R_{PULL} | P00 to P07, PG1, PG2*3*4 | $V_I = 0 V$ | 25 | 50 | 100 | k Ω | When pull-up resistance is enabled |
| Input capacitance | C_{IN} | Other than V_{CC} and V_{SS} | $f = 1 \text{ MHz}$ | — | 5 | 15 | pF | |

(Continued)

$(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------|--|---|---|-------|------|-----|---|--|
| | | | | Min | Typ | Max | | |
| Power supply current*4 | I _{CC} | V _{CC} (External clock operation) | V _{CC} = 5.5 V F _{CH} = 32 MHz F _{MP} = 16 MHz Main clock mode (divided by 2) | — | 13 | 17 | mA | Except during Flash memory programming and erasing |
| | | | — | 33.5 | 39.5 | mA | During Flash memory programming and erasing | |
| | | | — | 15 | 21 | mA | At A/D conversion | |
| | I _{CCS} | | V _{CC} = 5.5 V F _{CH} = 32 MHz F _{MP} = 16 MHz Main sleep mode (divided by 2) | — | 5.5 | 9 | mA | |
| | I _{CCCL} | | V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Subclock mode (divided by 2) T _A = +25°C | — | 65 | 153 | μA | |
| | I _{CCLS} | | V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Subsleep mode (divided by 2) T _A = +25°C | — | 10 | 84 | μA | |
| | I _{CCCT} | | V _{CC} = 5.5 V F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25°C | — | 5 | 30 | μA | |
| | I _{CCMCR} | | V _{CC} = 5.5 V F _{CRH} = 10 MHz F _{MP} = 10 MHz Main CR clock mode | — | 8.6 | — | mA | |
| I _{CCSCR} | V _{CC} = 5.5 V Sub-CR clock mode (divided by 2) T _A = +25°C | — | 110 | 410 | μA | | | |

(Continued)

(Continued)

 ($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------------|------------|--|--|-------|-----|------|---------------|--|
| | | | | Min | Typ | Max | | |
| Power supply current**4 | I_{CCTS} | V_{CC} (External clock operation) | $V_{CC} = 5.5\text{ V}$ $F_{CH} = 32\text{ MHz}$ Time-base timer mode $T_A = +25^\circ\text{C}$ | — | 1.1 | 3 | mA | |
| | I_{CCH} | | $V_{CC} = 5.5\text{ V}$ Substop mode $T_A = +25^\circ\text{C}$ | — | 3.5 | 22.5 | μA | Main stop mode for single external clock selection |
| | I_{LVD} | V_{CC} | Current consumption for low-voltage detection circuit only | — | 37 | 54 | μA | |
| | I_{CRH} | | Current consumption for the main CR oscillator | — | 0.5 | 0.6 | mA | |
| | I_{CRL} | | Current consumption for the sub-CR oscillator oscillating at 100 kHz | — | 20 | 72 | μA | |

*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: P62 and P63 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.

*3: P00 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K. P01, P02, P03, P07, PG1 and PG2 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.

- *4: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH} . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH} , I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See “24.4. AC Characteristics: 24.4.1. Clock Timing” for F_{CH} and F_{CL} .
 - See “24.4. AC Characteristics: 24.4.2. Source Clock / Machine Clock” for F_{MP} and F_{MPL} .

24.4 AC Characteristics
24.4.1 Clock Timing
 $(V_{CC} = 2.4\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks | | |
|------------------|--------------------|----------|-----------|-------|-------|--------|-------|---|--|--|
| | | | | Min | Typ | Max | | | | |
| Clock frequency | F _{CH} | X0, X1 | — | 1 | — | 16.25 | MHz | When the main oscillation circuit is used | | |
| | | X0 | X1 : open | 1 | — | 12 | MHz | When the main external clock is used | | |
| | | X0, X1 | *1 | 1 | — | 32.5 | MHz | | | |
| | F _{CRH} | — | — | — | 9.7 | 10 | 10.3 | MHz | When the main CR clock is used*2 | |
| | | | | | 7.76 | 8 | 8.24 | MHz | 3.3 V ≤ V _{CC} ≤ 5.5 V (-40 °C ≤ T _A ≤ +40 °C) | |
| | | | | | 0.97 | 1 | 1.03 | MHz | 2.4 V ≤ V _{CC} < 3.3 V (0 °C ≤ T _A ≤ +40 °C) | |
| | | | | | 9.55 | 10 | 10.45 | MHz | When the main CR clock is used*2 | |
| | | | | | 7.64 | 8 | 8.36 | MHz | | 3.3 V ≤ V _{CC} ≤ 5.5 V (+40 °C < T _A ≤ +85 °C) |
| | | | | | 0.955 | 1 | 1.045 | MHz | | |
| | | | | | 9.5 | 10 | 10.5 | MHz | When the main CR clock is used*2 | |
| | | | | | 7.6 | 8 | 8.4 | MHz | | 2.4 V ≤ V _{CC} < 3.3 V |
| | | | | | 0.95 | 1 | 1.05 | MHz | | (-40 °C ≤ T _A < 0 °C, +40 °C < T _A ≤ +85 °C) |
| | | | | | 9.7 | 10 | 10.3 | MHz | When the main CR clock is used*3 | |
| | | | | | 7.76 | 8 | 8.24 | MHz | | 2.4 V ≤ V _{CC} ≤ 5.5 V (0 °C ≤ T _A ≤ +40 °C) |
| | | | | | 0.97 | 1 | 1.03 | MHz | | |
| | | | | | 9.5 | 10 | 10.5 | MHz | When the main CR clock is used*3 | |
| | | | | | 7.6 | 8 | 8.4 | MHz | | 2.4 V ≤ V _{CC} ≤ 5.5 V |
| | | | | | 0.95 | 1 | 1.05 | MHz | | (-40 °C ≤ T _A < 0 °C, +40 °C < T _A ≤ +85 °C) |
| | F _{CL} | X0A, X1A | — | — | — | 32.768 | — | kHz | When the sub oscillation circuit is used | |
| | | | | | — | 32.768 | — | kHz | When the sub-external clock is used | |
| F _{CRL} | — | — | — | 50 | 100 | 200 | kHz | When the sub CR clock is used | | |
| Clock cycle time | t _{H CYL} | X0, X1 | — | 61.5 | — | 1000 | ns | When the main oscillation circuit is used | | |
| | | X0 | X1 : open | 83.4 | — | 1000 | ns | When the external clock is used | | |
| | | X0, X1 | *1 | 30.8 | — | 1000 | ns | | | |
| | t _{L CYL} | X0A, X1A | — | — | 30.5 | — | μs | When the subclock is used | | |

(Continued)

(Continued)

 ($V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------------------------|------------------------|----------|-----------|-------|------|-----|---------------|---|
| | | | | Min | Typ | Max | | |
| Input clock pulse width | t_{WH1} | X0 | X1 : open | 33.4 | — | — | ns | When the external clock is used, the duty ratio should range between 40% and 60%. |
| | t_{WL1} | X0, X1 | *1 | 12.4 | — | — | ns | |
| | t_{WH2} t_{WL2} | X0A | — | — | 15.2 | — | μs | |
| Input clock rise time and fall time | t_{CR} | X0 | X1 : open | — | — | 5 | ns | When the external clock is used |
| | t_{CF} | X0, X1 | *1 | — | — | 5 | ns | |
| CR oscillation start time | t_{CRHWK} | — | — | — | — | 80 | μs | When the main CR clock is used |
| | t_{CRLWK} | — | — | — | — | 10 | μs | When the sub CR clock is used |

*1: The external clock signal is input to X0 and the inverted external clock signal to X1.

*2: These specifications are not applicable to the following products: MB95F272HPH, MB95F272KPH, MB95F273HPH, MB95F273KPH, MB95F274HPH, MB95F274KPH, MB95F282HPH, MB95F282KPH, MB95F283HPH, MB95F283KPH, MB95F284HPH and MB95F284KPH.

*3: These specifications are only applicable to the following products: MB95F272HPH, MB95F272KPH, MB95F273HPH, MB95F273KPH, MB95F274HPH, MB95F274KPH, MB95F282HPH, MB95F282KPH, MB95F283HPH, MB95F283KPH, MB95F284HPH and MB95F284KPH.

Input waveform generated when an external clock (main clock) is used

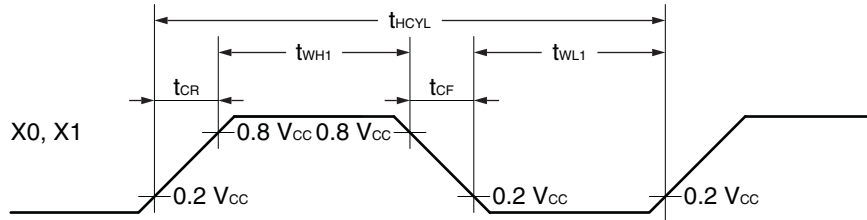
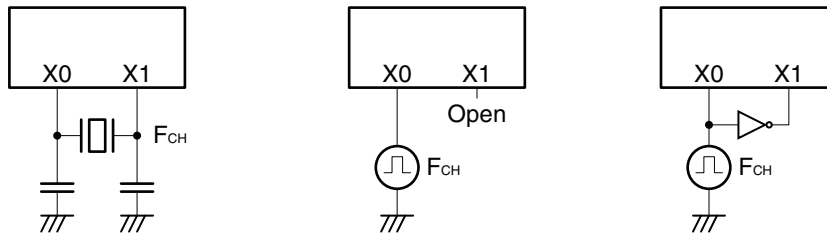


Figure of main clock input port external connection

When a crystal oscillator or a ceramic oscillator is used When an external clock is used (X1 is open) When an external clock is used



Input waveform generated when an external clock (subclock) is used

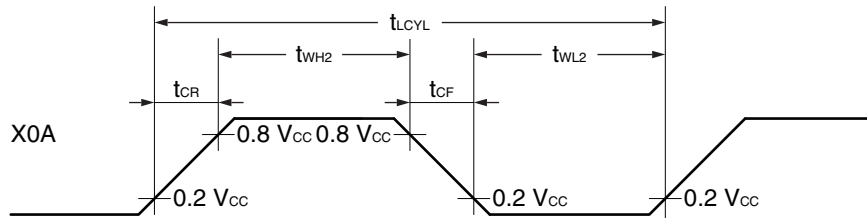


Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used When an external clock is used



24.4.2 Source Clock / Machine Clock

 ($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|--|------------|----------|--------|-----|--------|--|--|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | t_{SCLK} | — | 61.5 | — | 2000 | ns | When the main external clock is used Min: $F_{CH} = 32.5$ MHz, divided by 2 Max: $F_{CH} = 1$ MHz, divided by 2 |
| | | | 100 | — | 1000 | ns | When the main CR clock is used Min: $F_{CRH} = 10$ MHz Max: $F_{CRH} = 1$ MHz |
| | | | — | 61 | — | μs | When the sub-oscillation clock is used $F_{CL} = 32.768$ kHz, divided by 2 |
| | | | — | 20 | — | μs | When the sub CR clock is used $F_{CRL} = 100$ kHz, divided by 2 |
| Source clock frequency | F_{SP} | — | 0.5 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 1 | — | 10 | MHz | When the main CR clock is used |
| | — | | 16.384 | — | kHz | When the sub-oscillation clock is used | |
| | F_{SPL} | | — | 50 | — | kHz | When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2 |
| Machine clock cycle time*2 (minimum instruction execution time) | t_{MCLK} | — | 61.5 | — | 32000 | ns | When the main oscillation clock is used Min: $F_{SP} = 16.25$ MHz, no division Max: $F_{SP} = 0.5$ MHz, divided by 16 |
| | | | 100 | — | 16000 | ns | When the main CR clock is used Min: $F_{SP} = 10$ MHz Max: $F_{SP} = 1$ MHz, divided by 16 |
| | | | 61 | — | 976.5 | μs | When the sub-oscillation clock is used Min: $F_{SPL} = 16.384$ kHz, no division Max: $F_{SPL} = 16.384$ kHz, divided by 16 |
| | | | 20 | — | 320 | μs | When the sub-CR clock is used Min: $F_{SPL} = 50$ kHz, no division Max: $F_{SPL} = 50$ kHz, divided by 16 |
| Machine clock frequency | F_{MP} | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.0625 | — | 10 | MHz | When the main CR clock is used |
| | F_{MPL} | | 1.024 | — | 16.384 | kHz | When the sub-oscillation clock is used |
| | F_{MPL} | | 3.125 | — | 50 | kHz | When the sub-CR clock is used $F_{CRL} = 100$ kHz |

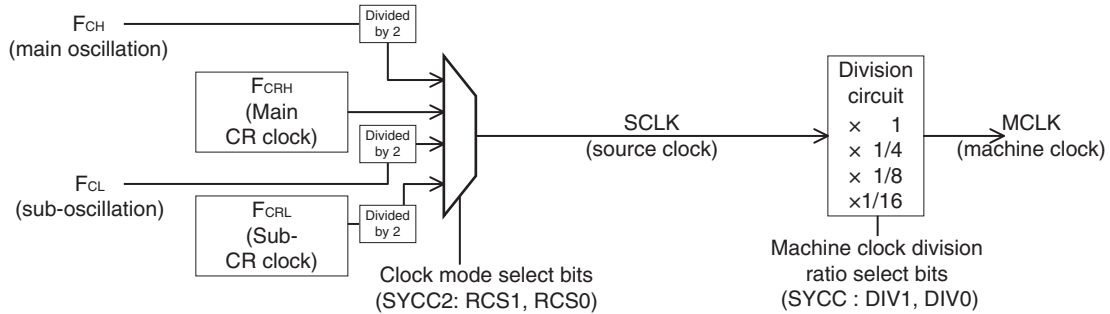
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC : DIV1 and DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

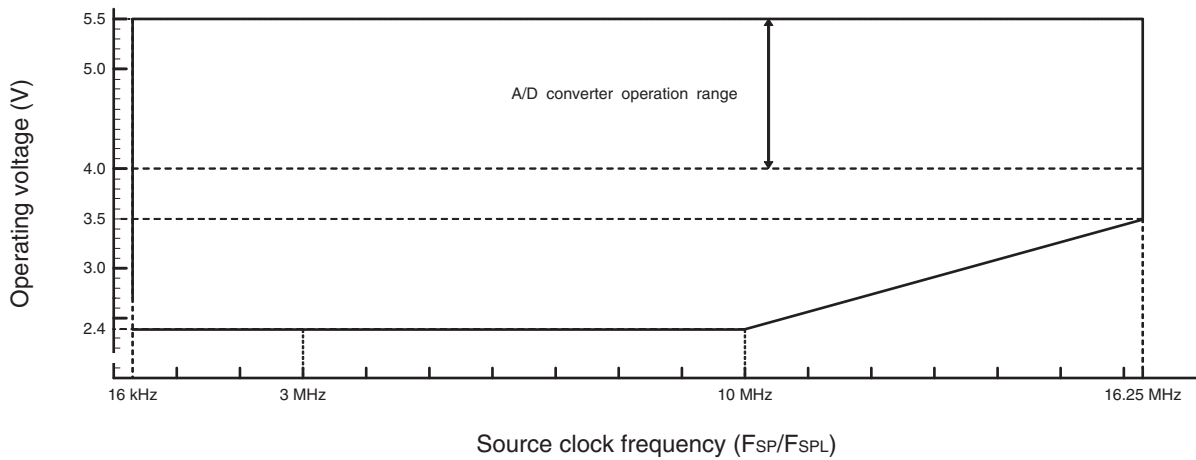
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

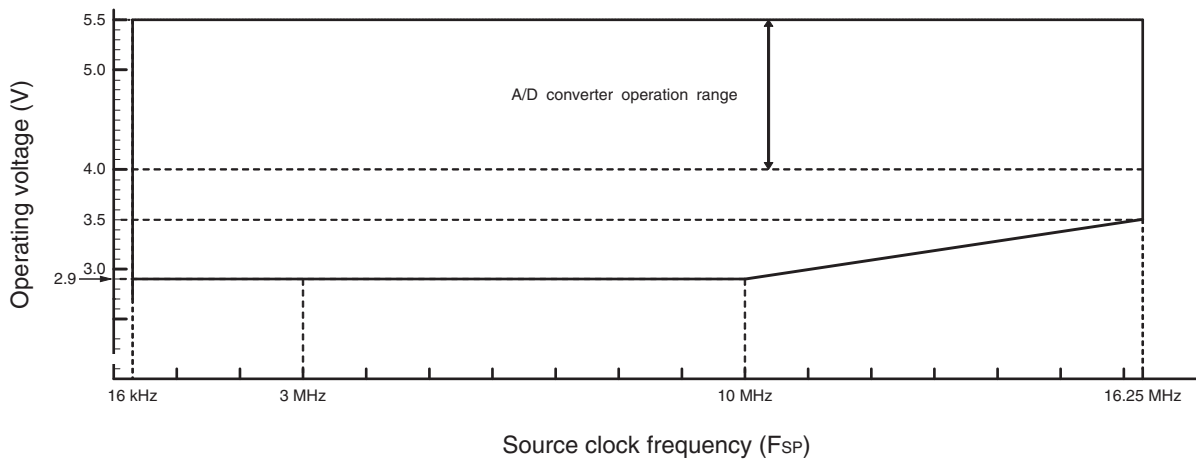
Schematic diagram of the clock generation block



**Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95260H/270H/280H (without the on-chip debug function)**



**Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95260H/270H/280H (with the on-chip debug function)**



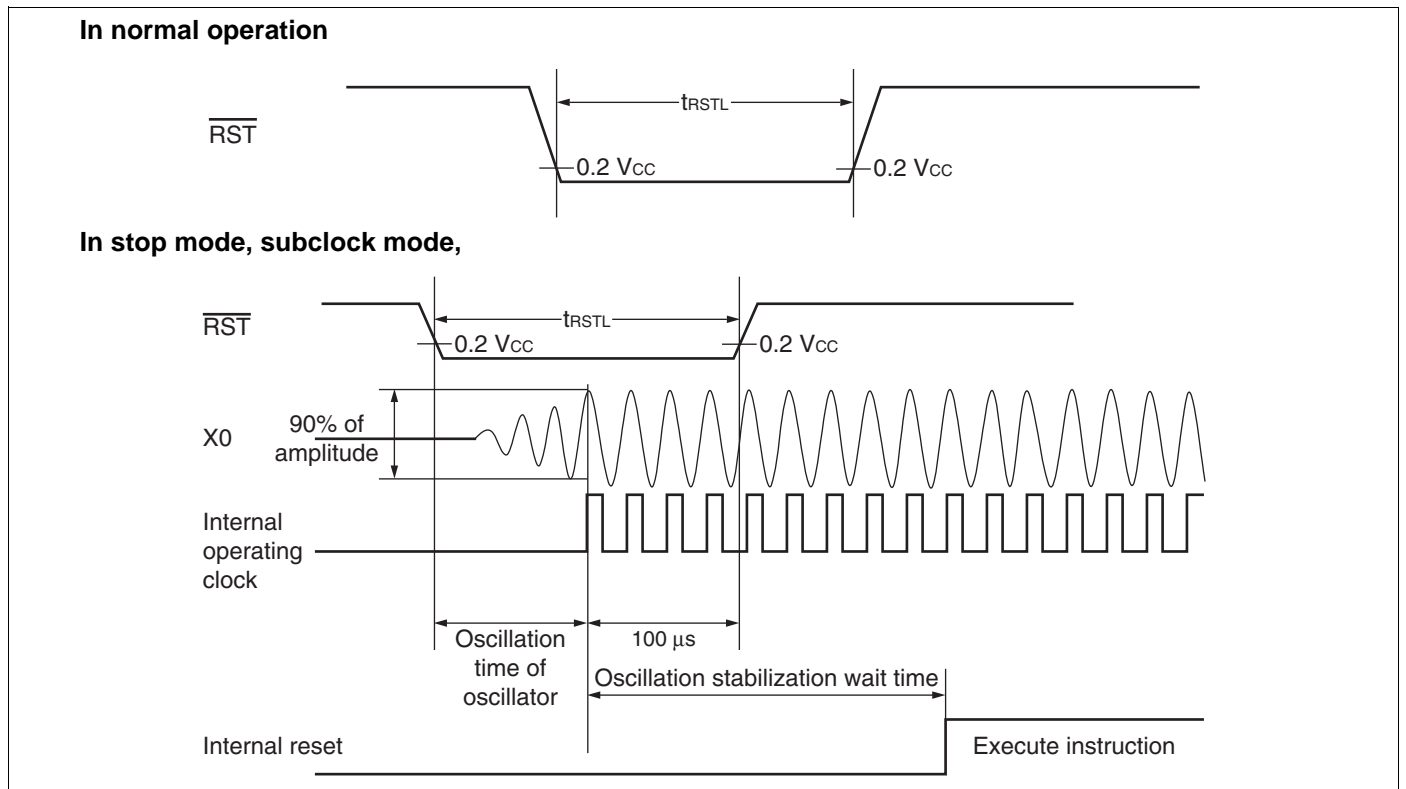
24.4.3 External Reset

($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|------------|--|-----|---------|---|
| | | Min | Max | | |
| \overline{RST} "L" level pulse width | t_{RSTL} | $2 t_{MCLK}^{*1}$ | — | ns | In normal operation |
| | | Oscillation time of the oscillator ^{*2} + 100 | — | μs | In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on |
| | | 100 | — | μs | In time-base timer mode |

*1 : See "24.4.2. Source Clock / Machine Clock" for t_{MCLK} .

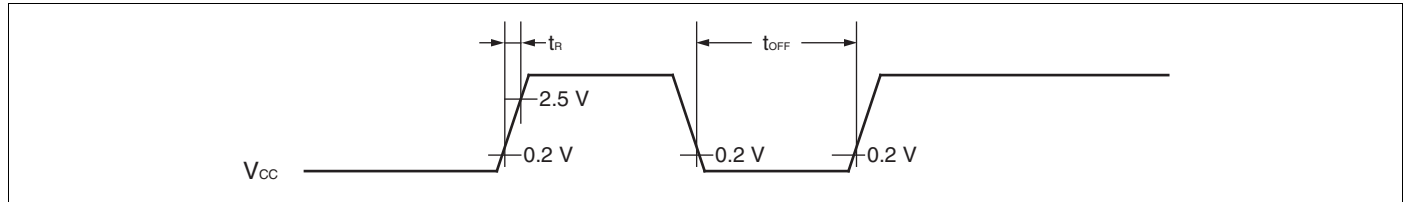
*2 : The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of μs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several μs and several ms.



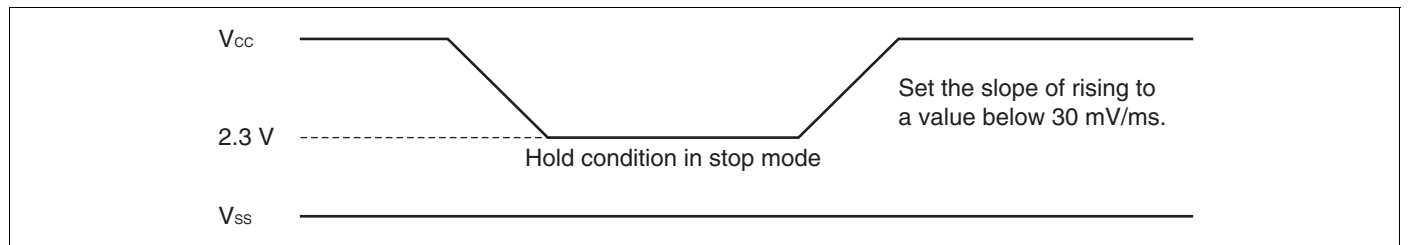
24.4.4 Power-on Reset

($V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|--------------------------|-----------|-----------|-------|-----|------|--------------------------|
| | | | Min | Max | | |
| Power supply rising time | t_R | — | — | 50 | ms | |
| Power supply cutoff time | t_{OFF} | — | 1 | — | ms | Wait time until power-on |



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



24.4.5 Peripheral Input Timing

 ($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

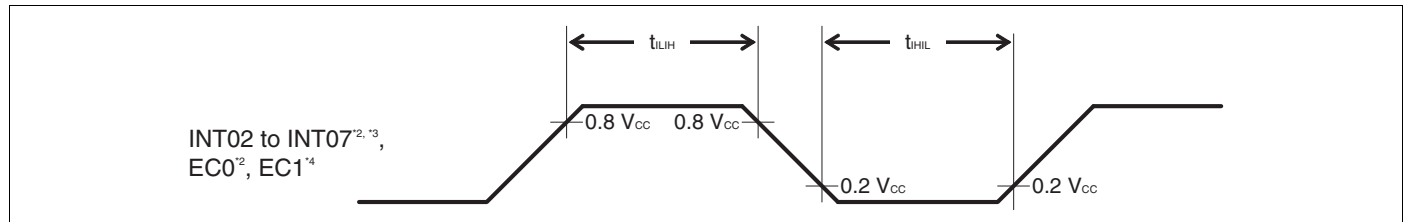
| Parameter | Symbol | Pin name | Value | | Unit |
|----------------------------------|------------|---|-------------------|-----|------|
| | | | Min | Max | |
| Peripheral input "H" pulse width | t_{ILIH} | INT02 to INT07 ^{*2,*3} , EC0 ^{*2} , EC1 ^{*4} | $2 t_{MCLK}^{*1}$ | — | ns |
| Peripheral input "L" pulse width | t_{IHIL} | | $2 t_{MCLK}^{*1}$ | — | ns |

*1: See "24.4.2. Source Clock / Machine Clock" for t_{MCLK} .

*2: INT04, INT06 and EC0 are available in all products.

*3: INT02, INT03, INT05 and INT07 are only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K.

*4: EC1 is only available on MB95F262H/F262K/F263H/F263K/F264H/F264K.



24.4.6 LIN-UART Timing (only available on MB95F262H/F262K/F263H/F263K/F264H/F264K/F282H/F282K/F283H/F283K/F284H/F284K)

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

($V_{CC} = 5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

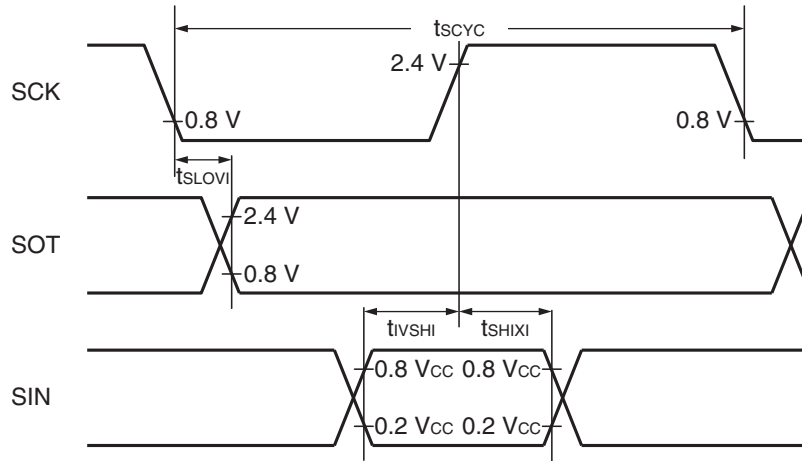
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|---|-------------------------|------------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVI} | SCK, SOT | | - 95 | + 95 | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK | External clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $3 t_{MCLK}^{*3} - t_R$ | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVE} | SCK, SOT | | — | $2 t_{MCLK}^{*3} + 95$ | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHE} | SCK, SIN | | 190 | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXE} | SCK, SIN | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK fall time | t_F | SCK | | — | 10 | ns |
| SCK rise time | t_R | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

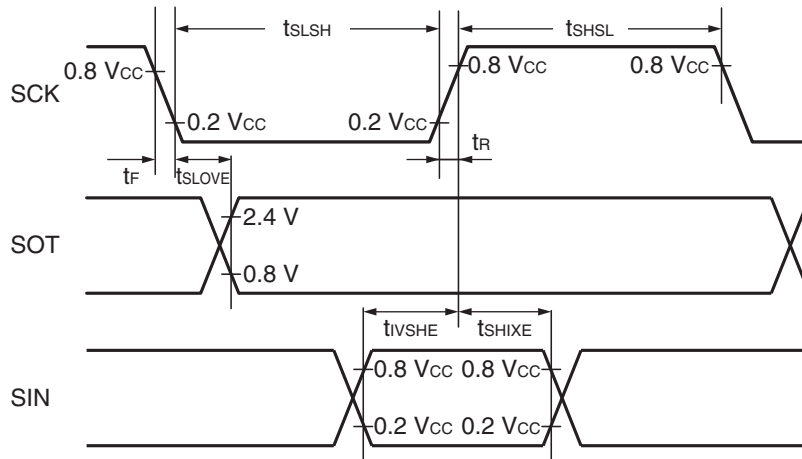
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See "24.4.2. Source Clock / Machine Clock" for t_{MCLK} .

Internal shift clock mode



External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

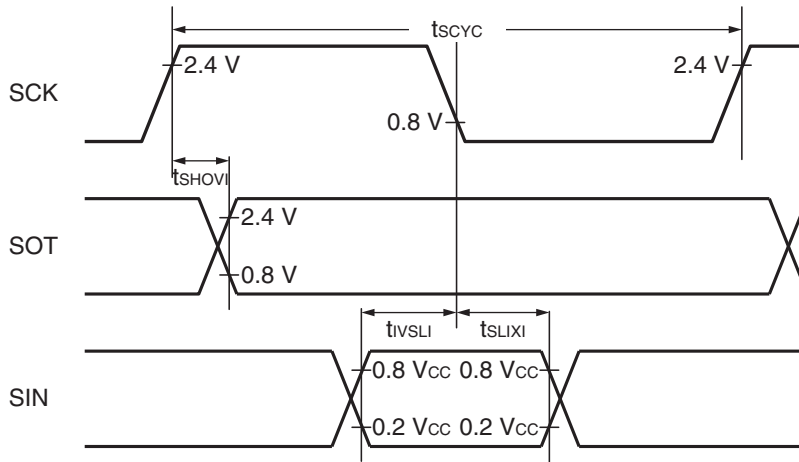
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|---|-------------------------|------------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK $\uparrow \rightarrow$ SOT delay time | t_{SHOVI} | SCK, SOT | | - 95 | + 95 | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK $\downarrow \rightarrow$ valid SIN hold time | t_{SLIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $3 t_{MCLK}^{*3} - t_R$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK $\uparrow \rightarrow$ SOT delay time | t_{SHOVE} | SCK, SOT | | — | $2 t_{MCLK}^{*3} + 95$ | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLE} | SCK, SIN | | 190 | — | ns |
| SCK $\downarrow \rightarrow$ valid SIN hold time | t_{SLIXE} | SCK, SIN | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK fall time | t_F | SCK | | — | 10 | ns |
| SCK rise time | t_R | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

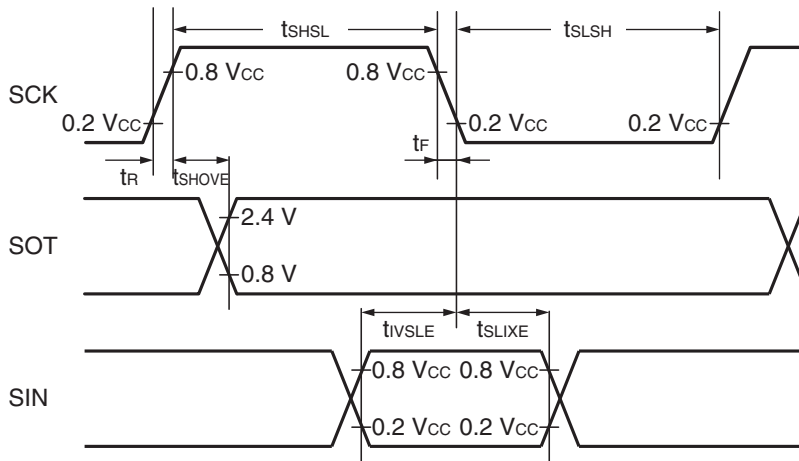
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See "24.4.2. Source Clock / Machine Clock" for t_{MCLK} .

Internal shift clock mode



External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

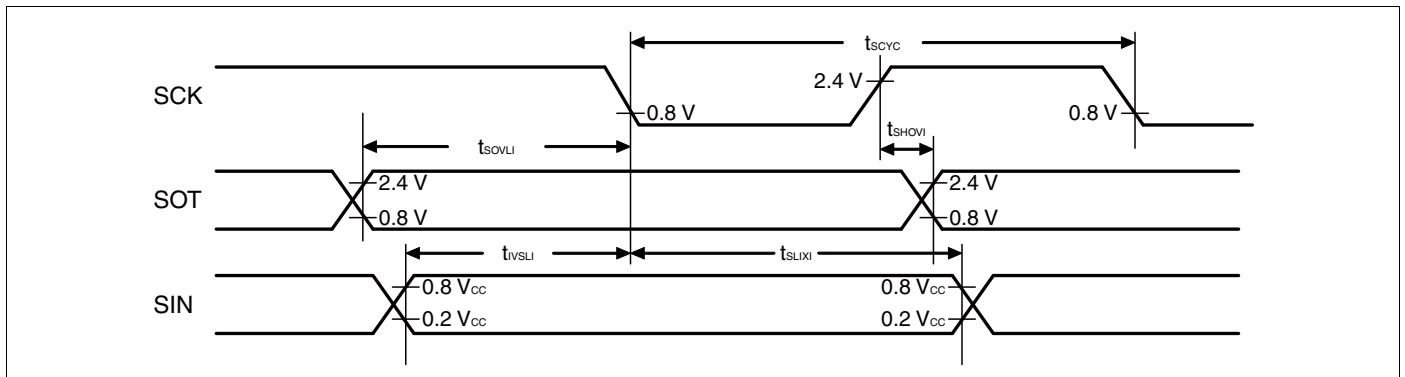
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|--|-----------------------|-------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK \uparrow → SOT delay time | t_{SHOVI} | SCK, SOT | | - 95 | + 95 | ns |
| Valid SIN → SCK \downarrow | t_{IVSLI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK \downarrow → valid SIN hold time | t_{SLIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK \downarrow delay time | t_{SOVLI} | SCK, SOT | | — | $4 t_{MCLK}^{*3}$ | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “24.4.2. Source Clock / Machine Clock” for t_{MCLK} .



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

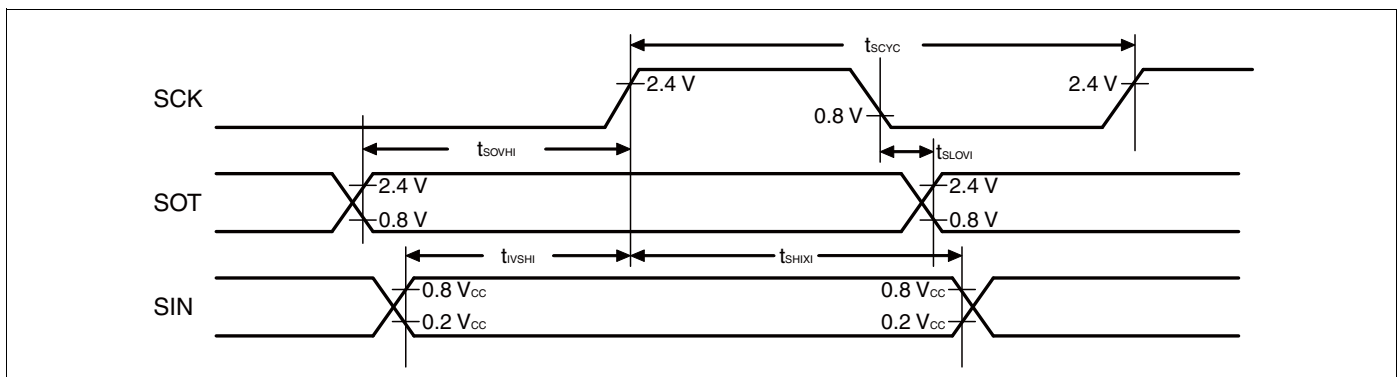
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|--|-----------------------|-------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operating output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVI} | SCK, SOT | | - 95 | + 95 | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXI} | SCK, SIN | | 0 | — | ns |
| SOT \rightarrow SCK \uparrow delay time | t_{SOVHI} | SCK, SOT | | — | $4 t_{MCLK}^{*3}$ | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

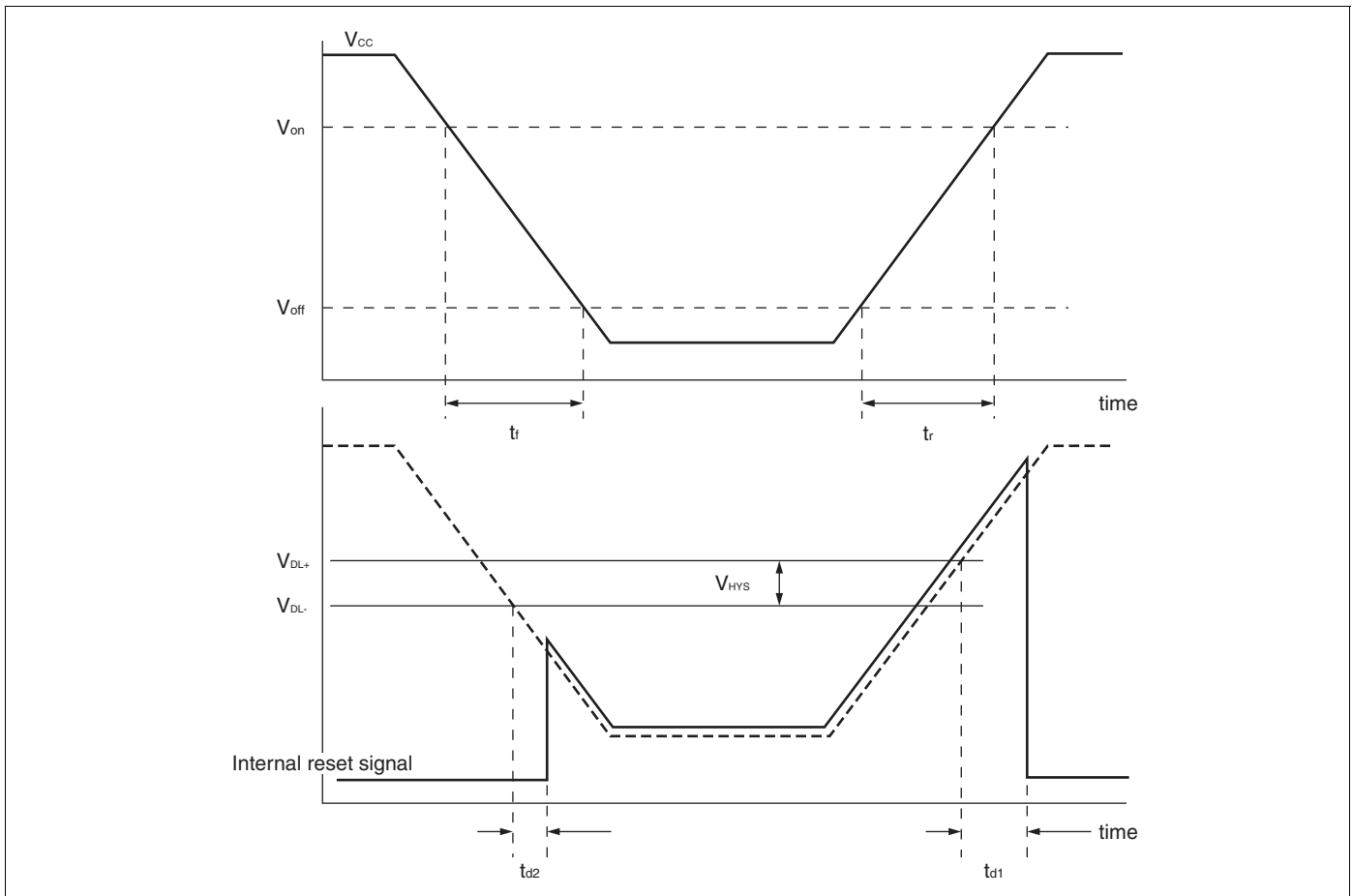
*3: See "24.4.2. Source Clock / Machine Clock" for t_{MCLK} .



24.4.7 Low-voltage Detection

 ($V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|-----------|-------|-----|------|---------------|---|
| | | Min | Typ | Max | | |
| Release voltage | V_{DL+} | 2.52 | 2.7 | 2.88 | V | At power supply rise |
| Detection voltage | V_{DL-} | 2.42 | 2.6 | 2.78 | V | At power supply fall |
| Hysteresis width | V_{HYS} | 70 | 100 | — | mV | |
| Power supply start voltage | V_{off} | — | — | 2.3 | V | |
| Power supply end voltage | V_{on} | 4.9 | — | — | V | |
| Power supply voltage change time (at power supply rise) | t_r | 3000 | — | — | μs | Slope of power supply that the reset release signal generates within the rating (V_{DL+}) |
| Power supply voltage change time (at power supply fall) | t_f | 300 | — | — | μs | Slope of power supply that the reset detection signal generates within the rating (V_{DL-}) |
| Reset release delay time | t_{d1} | — | — | 300 | μs | |
| Reset detection delay time | t_{d2} | — | — | 20 | μs | |



24.5 A/D Converter
24.5.1 A/D Converter Electrical Characteristics
 $(V_{CC} = 4.0\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$

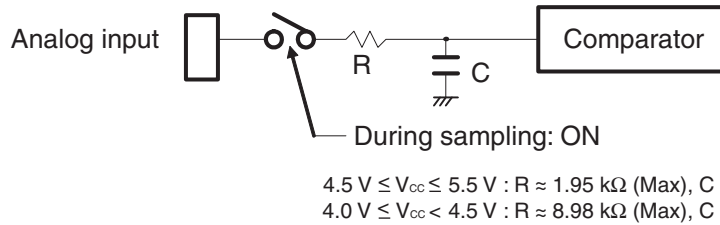
| Parameter | Symbol | Value | | | Unit | Remarks |
|-------------------------------|-----------|---------------------------|---------------------------|---------------------------|---------------|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | - 3 | — | + 3 | LSB | |
| Linearity error | | - 2.5 | — | + 2.5 | LSB | |
| Differential linear error | | - 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | V_{OT} | $V_{SS} - 1.5\text{ LSB}$ | $V_{SS} + 0.5\text{ LSB}$ | $V_{SS} + 2.5\text{ LSB}$ | V | |
| Full-scale transition voltage | V_{FST} | $V_{CC} - 4.5\text{ LSB}$ | $V_{CC} - 2\text{ LSB}$ | $V_{CC} + 0.5\text{ LSB}$ | V | |
| Compare time | — | 0.9 | — | 16500 | μs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ |
| | | 1.8 | — | 16500 | μs | $4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$ |
| Sampling time | — | 0.6 | — | ∞ | μs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, with external impedance < 5.4 k Ω |
| | | 1.2 | — | ∞ | μs | $4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$, with external impedance < 2.4 k Ω |
| Analog input current | I_{AIN} | - 0.3 | — | + 0.3 | μA | |
| Analog input voltage | V_{AIN} | V_{SS} | — | V_{CC} | V | |

24.5.2 Notes on Using the A/D Converter

External impedance of analog input and its sampling time

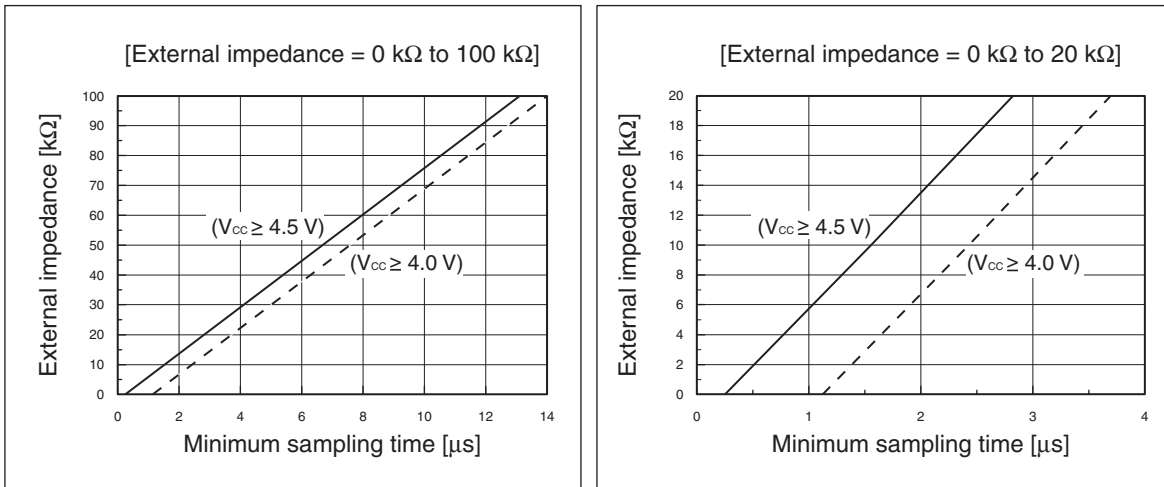
The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μF to the analog input pin.

Analog input equivalent circuit



Note: The values are reference values.

Relationship between external impedance and minimum sampling time



A/D conversion error

As $|V_{CC}-V_{SS}|$ decreases, the A/D conversion error increases proportionately.

24.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter. When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

Linearity error (unit: LSB)

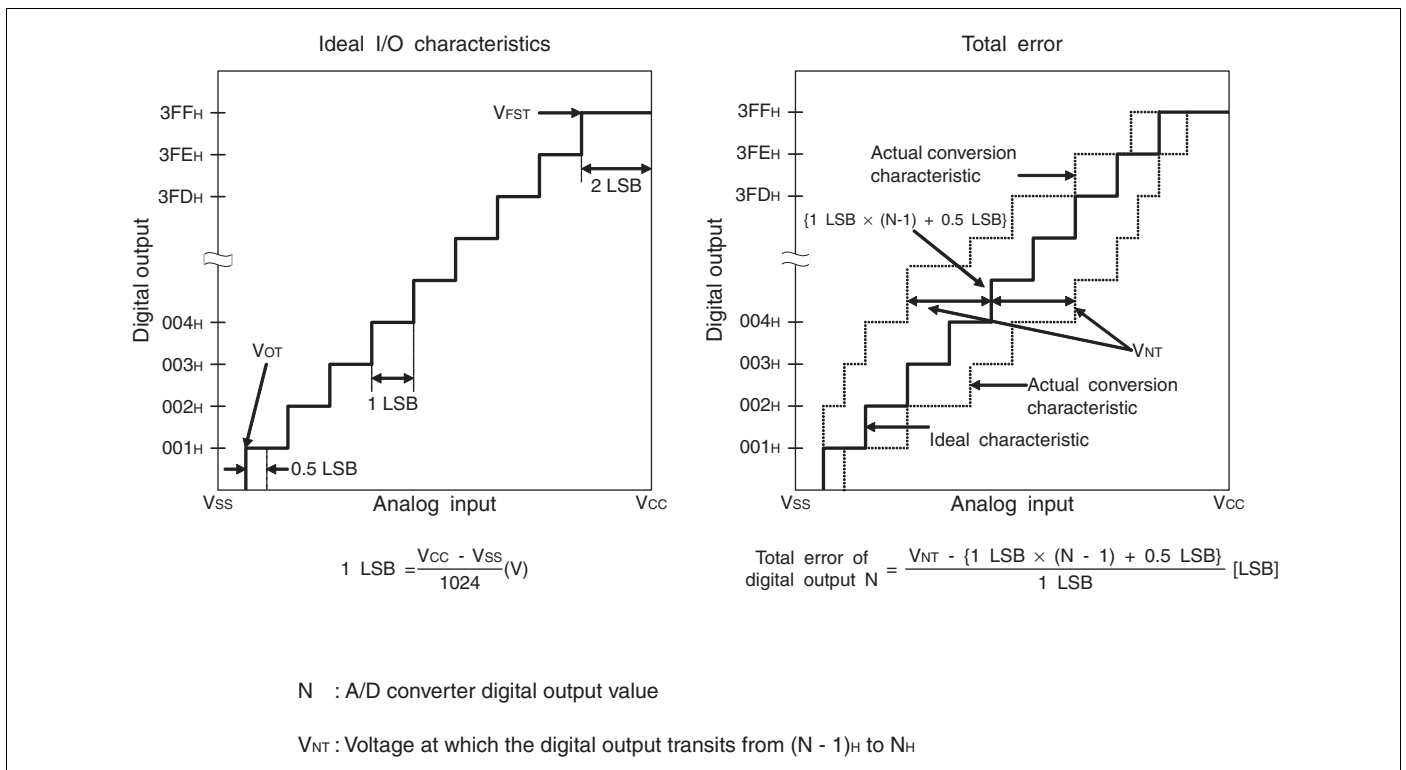
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" \leftrightarrow "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" \leftrightarrow "11 1111 1110") of the same device.

Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

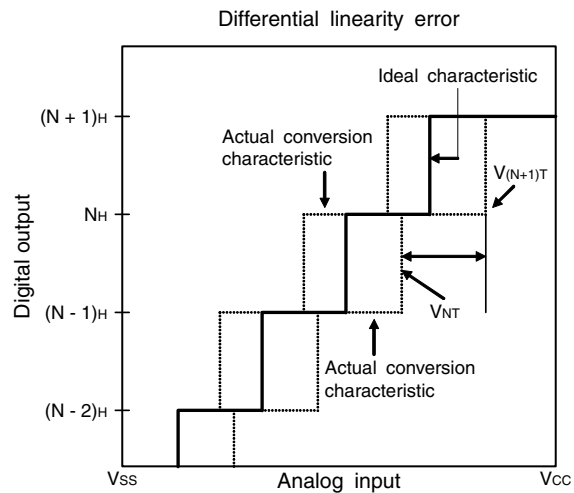
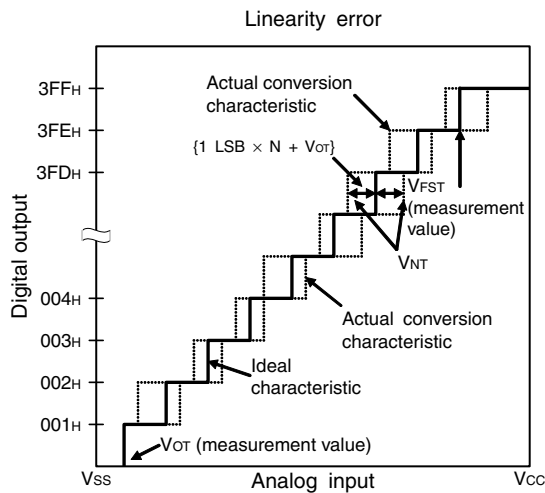
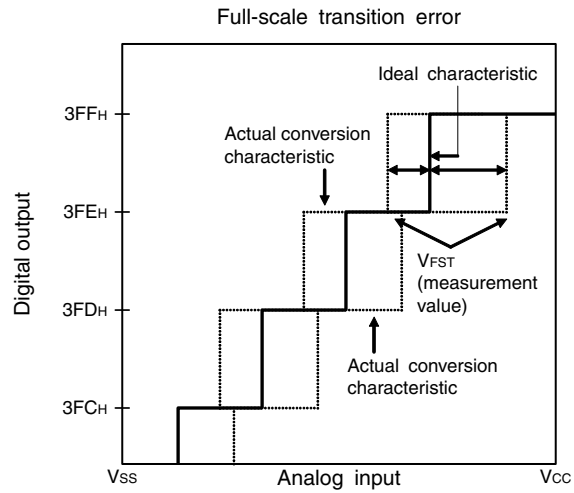
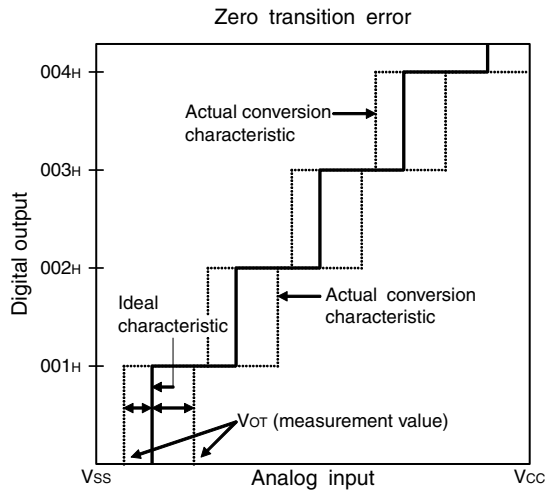
Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from (N - 1)_H to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

24.6 Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|--|------------------|-------------------|--------------------|-------|---|
| | Min | Typ | Max | | |
| Sector erase time (2 Kbyte sector) | — | 0.2* ¹ | 0.5* ² | s | The time of writing 00 _H prior to erasure is excluded. |
| Sector erase time (16 Kbyte sector) | — | 0.5* ¹ | 7.5* ² | s | The time of writing 00 _H prior to erasure is excluded. |
| Byte writing time | — | 21 | 6100* ² | μs | System-level overhead is excluded. |
| Program/erase cycle | 100000 | — | — | cycle | |
| Power supply voltage at program/erase | 3.0 | — | 5.5 | V | |
| Flash memory data retention time | 20* ³ | — | — | year | Average T _A = + 85°C |

*1: T_A = + 25°C, V_{CC} = 5.0 V, 100000 cycles

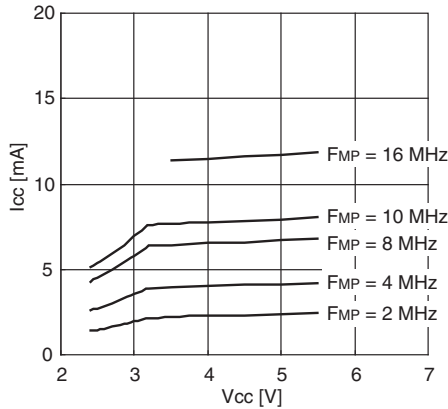
*2: T_A = + 85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being + 85°C) .

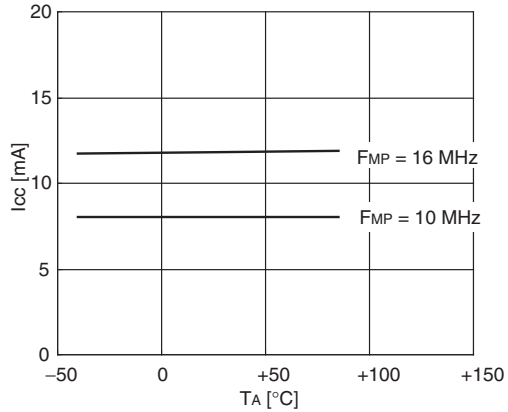
25. Sample Characteristics

Power supply current temperature

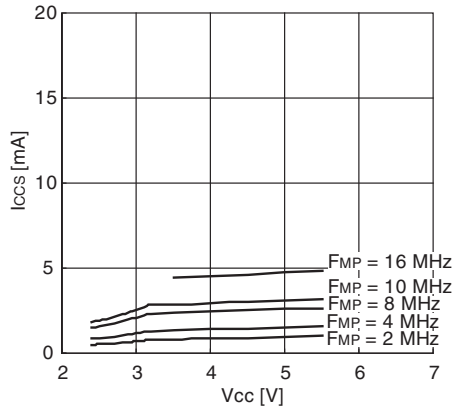
I_{CC} - V_{CC}
 $T_A = +25^\circ\text{C}$ $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2)
 Main clock mode with the external clock operating



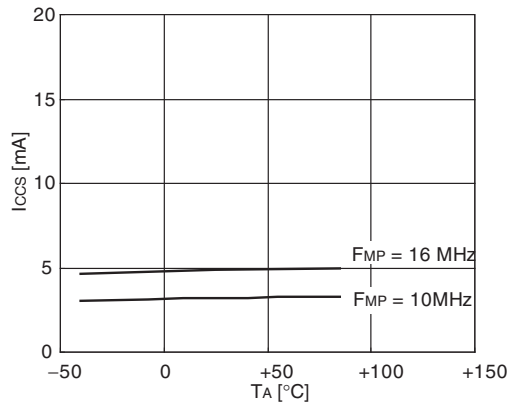
I_{CC} - T_A
 $V_{CC} = 5.5$ V $F_{MP} = 10, 16$ MHz (divided by 2)
 Main clock mode with the external clock operating



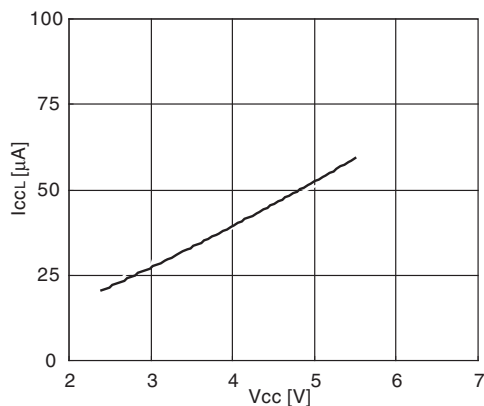
I_{CCS} - V_{CC}
 $T_A = +25^\circ\text{C}$ $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2)
 Main sleep mode with the external clock operating



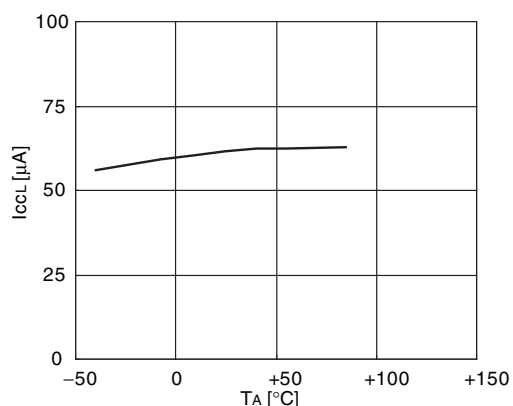
I_{CCS} - T_A
 $V_{CC} = 5.5$ V $F_{MP} = 10, 16$ MHz (divided by 2)
 Main sleep mode with the external clock operating



I_{CCCL} - V_{CC}
 $T_A = +25^\circ\text{C}$ $F_{MPL} = 16$ kHz (divided by 2)
 Subclock mode with the external clock operating

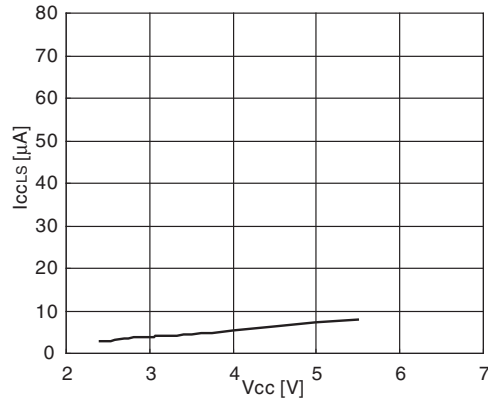


I_{CCCL} - T_A
 $V_{CC} = 5.5$ V $F_{MPL} = 16$ kHz (divided by 2)
 Subclock mode with the external clock operating

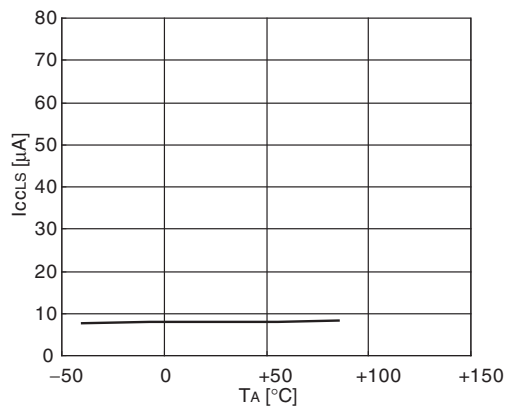


(Continued)

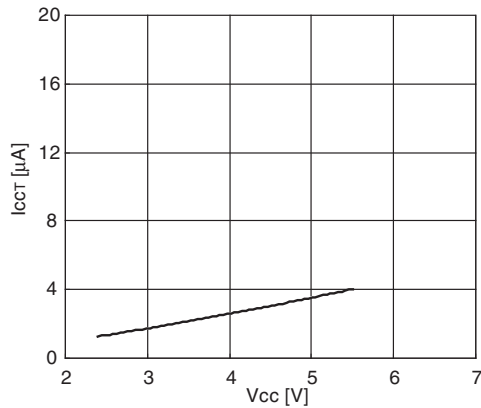
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$ $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



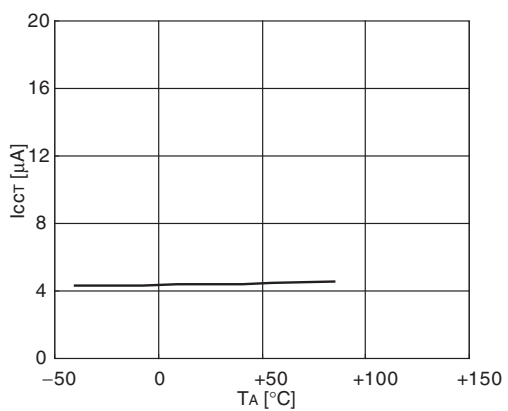
$I_{CCLS} - T_A$
 $V_{CC} = 5.5\text{ V}$ $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



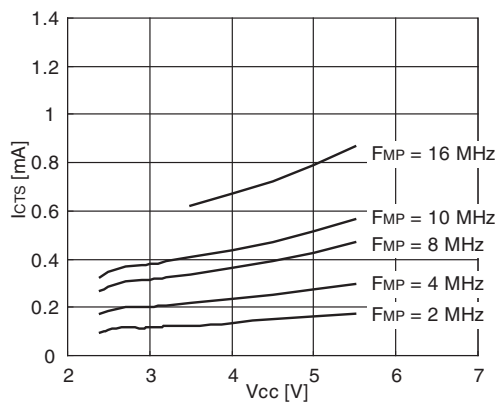
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$ $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



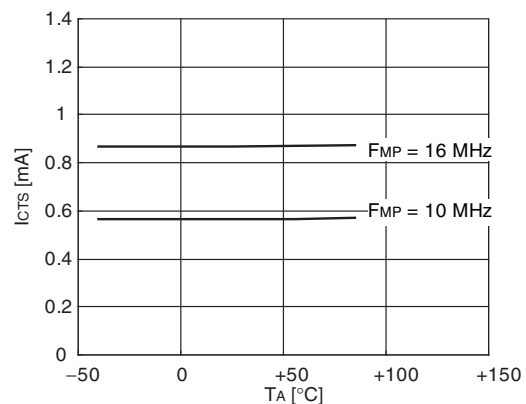
$I_{CCT} - T_A$
 $V_{CC} = 5.5\text{ V}$ $F_{MPL} = 16\text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$ $F_{MP} = 2, 4, 8, 10, 16\text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating

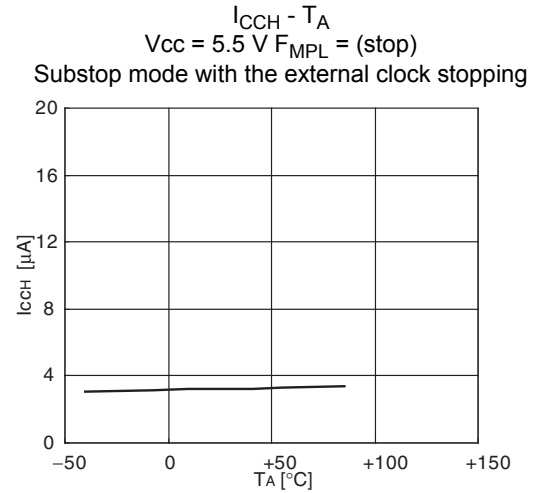
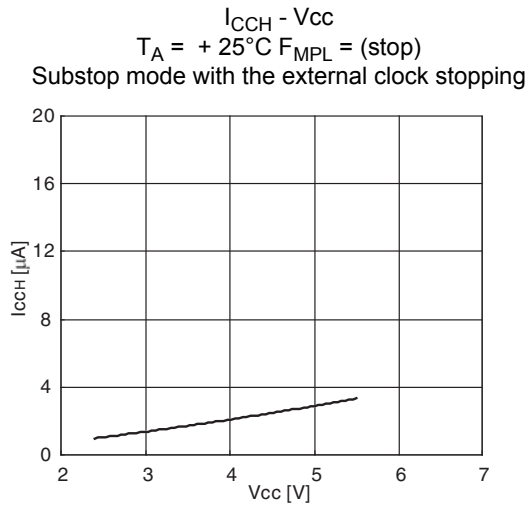


$I_{CTS} - T_A$
 $V_{CC} = 5.5\text{ V}$ $F_{MP} = 10, 16\text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating

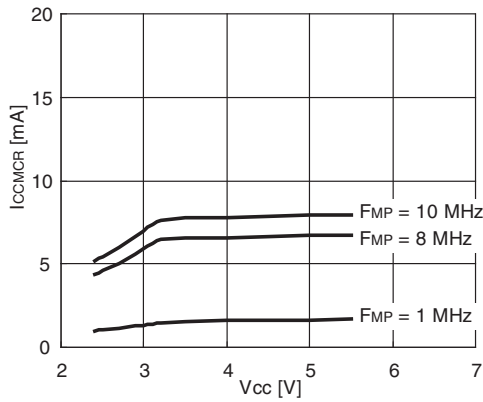


(Continued)

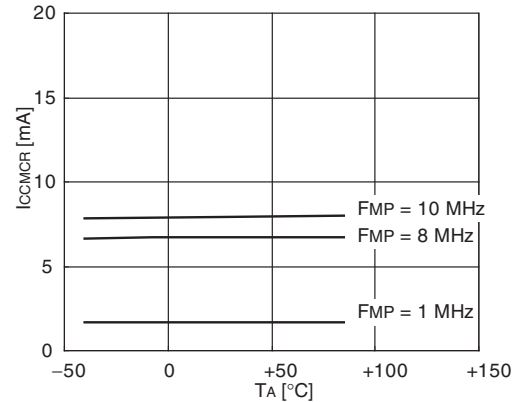
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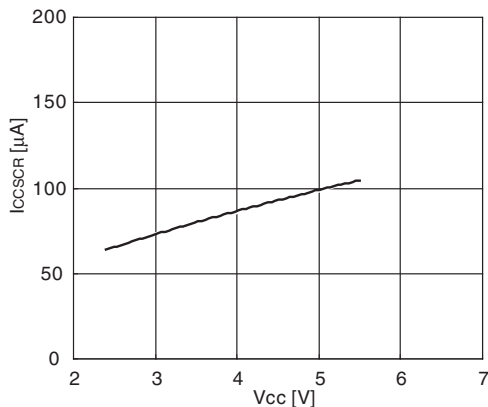
$I_{CCMCR} - V_{CC}$
 $T_A = +25^\circ\text{C}$ $F_{MP} = 1, 8, 10\text{ MHz}$ (no division)
 Main clock mode
 with the main CR clock operating



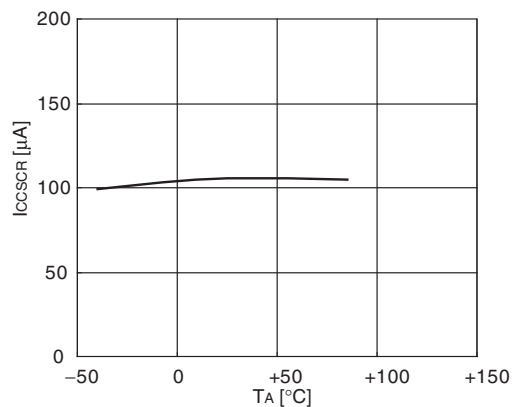
$I_{CCMCR} - T_A$
 $V_{CC} = 5.5\text{ V}$ $F_{MP} = 1, 8, 10\text{ MHz}$ (no division)
 Main clock mode
 with the main CR clock operating



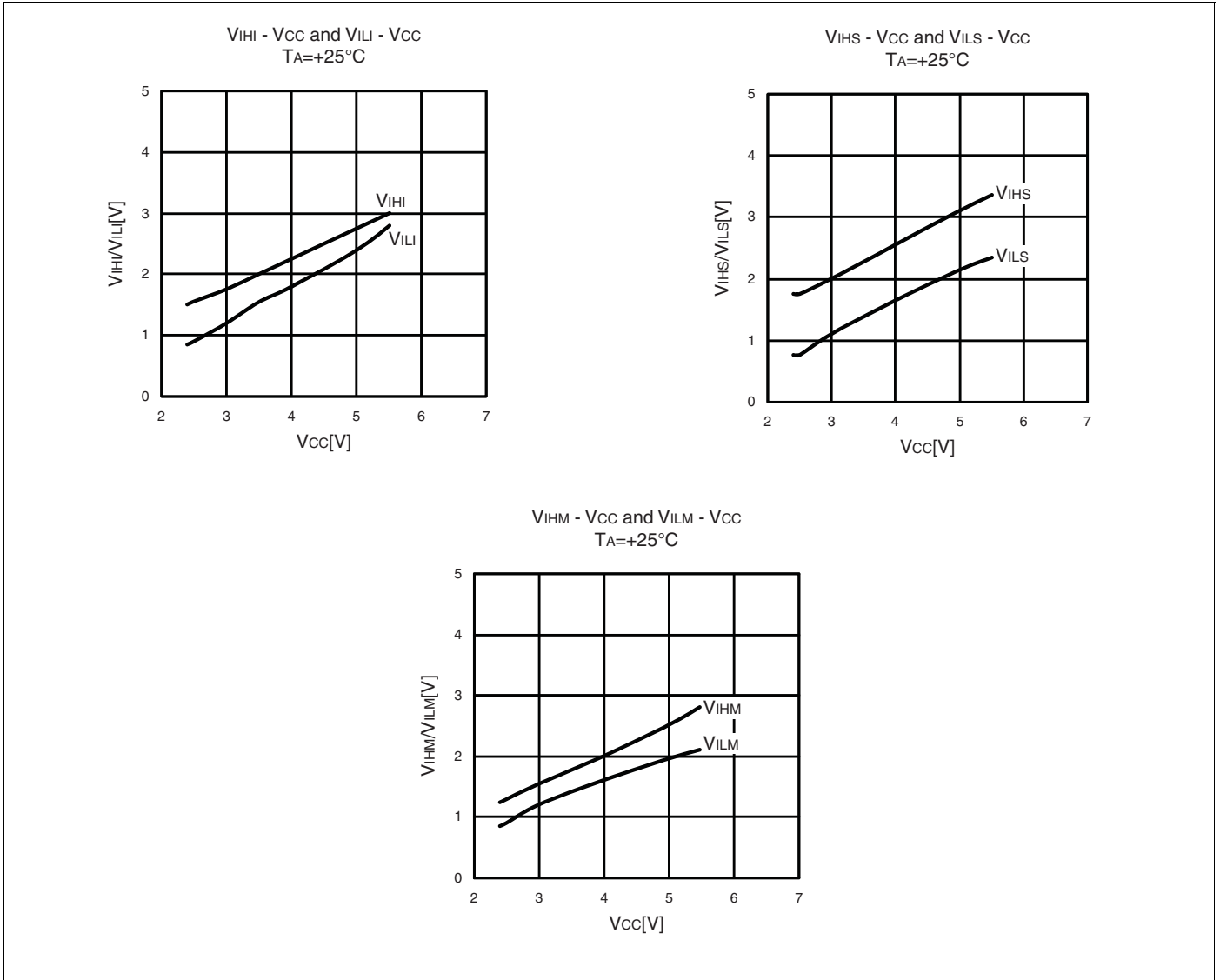
$I_{CCSCR} - V_{CC}$
 $T_A = +25^\circ\text{C}$ $F_{MPL} = 50\text{ kHz}$ (divided by 2)
 Subclock mode with
 the sub-CR clock operating



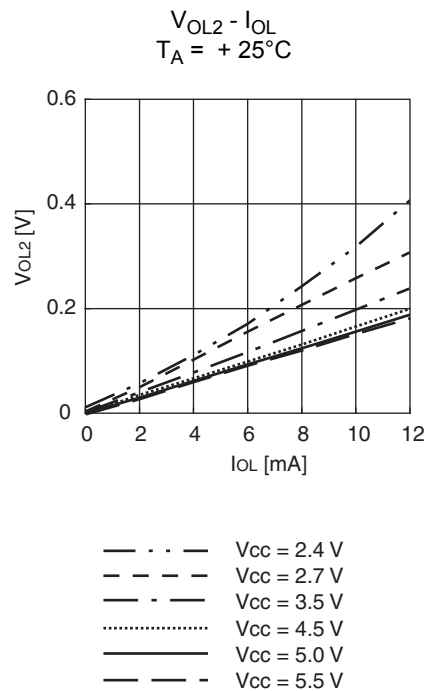
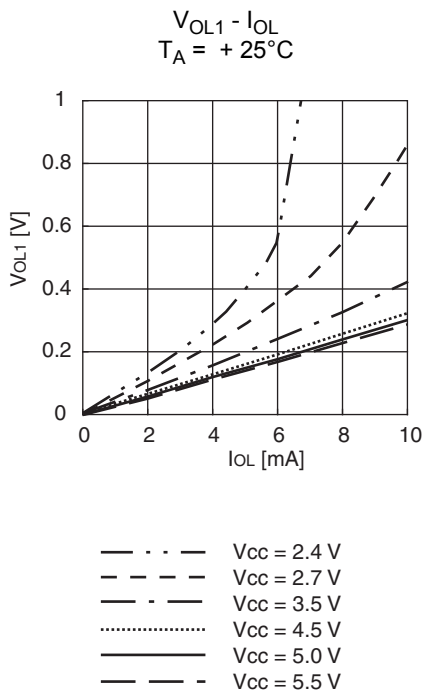
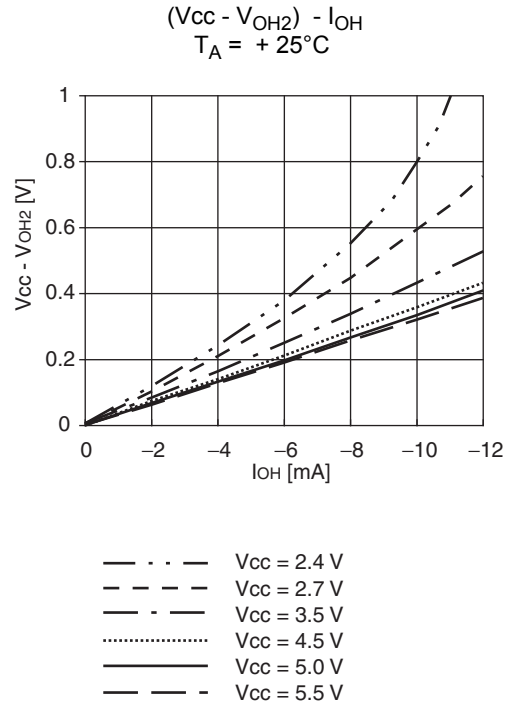
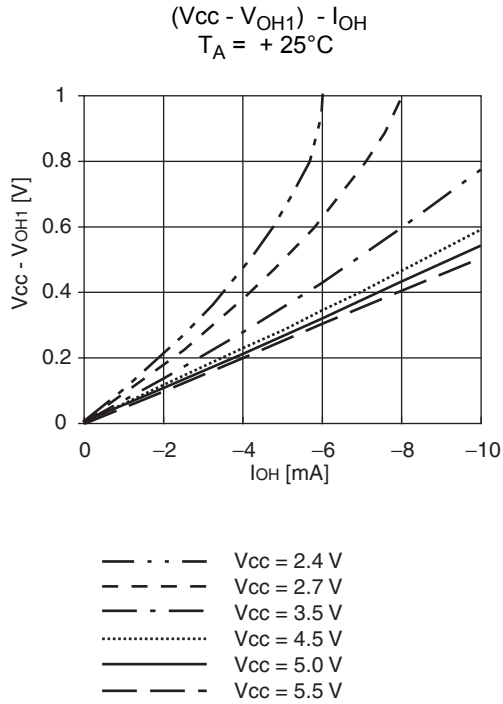
$I_{CCSCR} - T_A$
 $V_{CC} = 5.5\text{ V}$ $F_{MPL} = 50\text{ kHz}$ (divided by 2)
 Subclock mode with
 the sub-CR clock operating



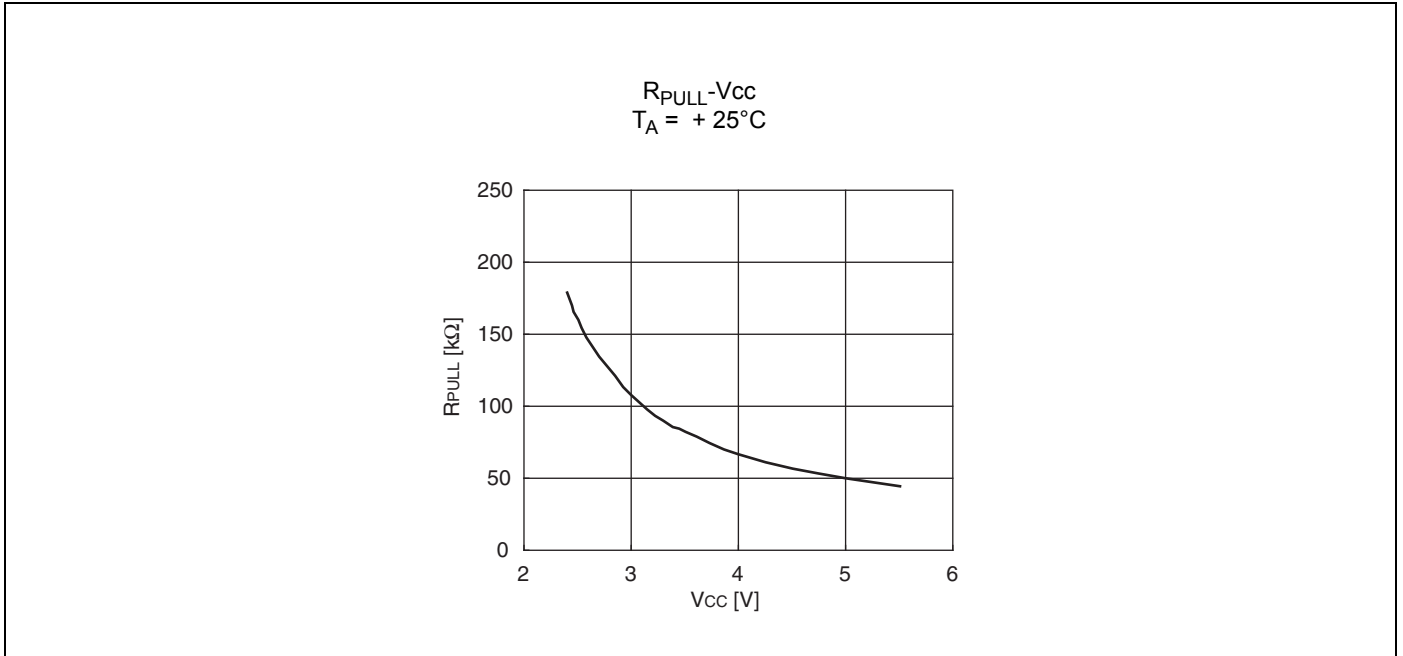
Input voltage



Output voltage



Pull-up



26. Mask Options

| No. | Part Number | MB95F262H MB95F263H MB95F264H MB95F272H MB95F273H MB95F274H MB95F282H MB95F283H MB95F284H | MB95F262K MB95F263K MB95F264K MB95F272K MB95F273K MB95F274K MB95F282K MB95F283K MB95F284K |
|-----|-----------------------------|---|---|
| | Selectable/Fixed | Fixed | |
| 1 | Low-voltage detection reset | Without low-voltage detection reset | With low-voltage detection reset |
| 2 | Reset | With dedicated reset input | Without dedicated reset input |

27. Ordering Information

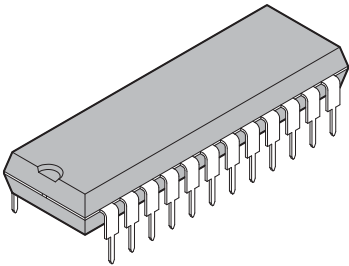
| Part Number | Package |
|--|---------------------------------------|
| MB95F262HWQN-G-SNE1 MB95F262HWQN-G-SNERE1 MB95F262KWQN-G-SNE1 MB95F262KWQN-G-SNERE1 MB95F263HWQN-G-SNE1 MB95F263HWQN-G-SNERE1 MB95F263KWQN-G-SNE1 MB95F263KWQN-G-SNERE1 MB95F264HWQN-G-SNE1 MB95F264HWQN-G-SNERE1 MB95F264KWQN-G-SNE1 MB95F264KWQN-G-SNERE1 | 32-pin plastic QFN (LCC-32P-M19) |
| MB95F262HP-G-SH-SNE2 MB95F262KP-G-SH-SNE2 MB95F263HP-G-SH-SNE2 MB95F263KP-G-SH-SNE2 MB95F264HP-G-SH-SNE2 MB95F264KP-G-SH-SNE2 | 24-pin plastic SDIP (DIP-24P-M07) |
| MB95F262HPF-G-SNE2 MB95F262KPF-G-SNE2 MB95F263HPF-G-SNE2 MB95F263KPF-G-SNE2 MB95F264HPF-G-SNE2 MB95F264KPF-G-SNE2 | 20-pin plastic SOP (FPT-20P-M09) |
| MB95F262HPFT-G-SNE2 MB95F262KPFT-G-SNE2 MB95F263HPFT-G-SNE2 MB95F263KPFT-G-SNE2 MB95F264HPFT-G-SNE2 MB95F264KPFT-G-SNE2 | 20-pin plastic TSSOP (FPT-20P-M10) |
| MB95F282HWQN-G-SNE1 MB95F282HWQN-G-SNERE1 MB95F282KWQN-G-SNE1 MB95F282KWQN-G-SNERE1 MB95F283HWQN-G-SNE1 MB95F283HWQN-G-SNERE1 MB95F283KWQN-G-SNE1 MB95F283KWQN-G-SNERE1 MB95F284HWQN-G-SNE1 MB95F284HWQN-G-SNERE1 MB95F284KWQN-G-SNE1 MB95F284KWQN-G-SNERE1 | 32-pin plastic QFN (LCC-32P-M19) |
| MB95F282HPH-G-SNE2 MB95F282KPH-G-SNE2 MB95F283HPH-G-SNE2 MB95F283KPH-G-SNE2 MB95F284HPH-G-SNE2 MB95F284KPH-G-SNE2 | 16-pin plastic DIP (DIP-16P-M06) |

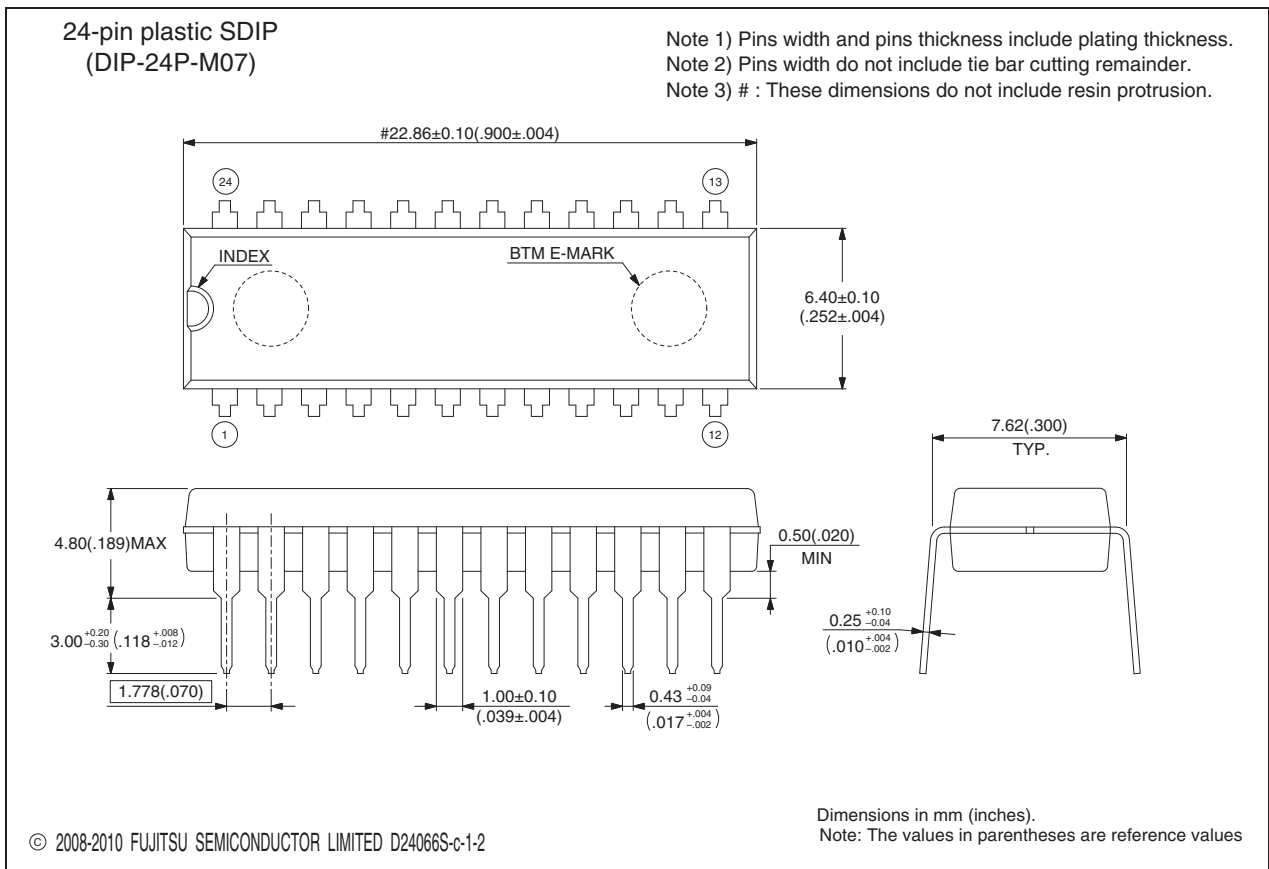
(Continued)

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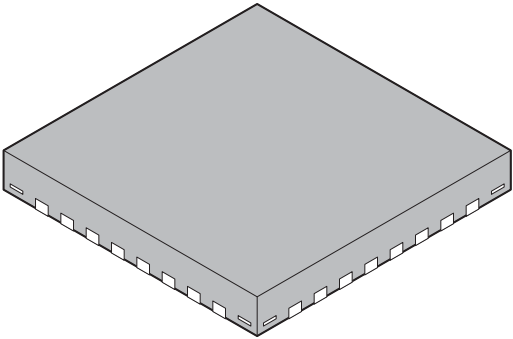
| Part Number | Package |
|--|-------------------------------------|
| MB95F282HPF-G-SNE1 MB95F282KPF-G-SNE1 MB95F283HPF-G-SNE1 MB95F283KPF-G-SNE1 MB95F284HPF-G-SNE1 MB95F284KPF-G-SNE1 | 16-pin plastic SOP (FPT-16P-M06) |
| MB95F272HPH-G-SNE2 MB95F272KPH-G-SNE2 MB95F273HPH-G-SNE2 MB95F273KPH-G-SNE2 MB95F274HPH-G-SNE2 MB95F274KPH-G-SNE2 | 8-pin plastic DIP (DIP-8P-M03) |
| MB95F272HPF-G-SNE2 MB95F272KPF-G-SNE2 MB95F273HPF-G-SNE2 MB95F273KPF-G-SNE2 MB95F274HPF-G-SNE2 MB95F274KPF-G-SNE2 | 8-pin plastic SOP (FPT-8P-M08) |

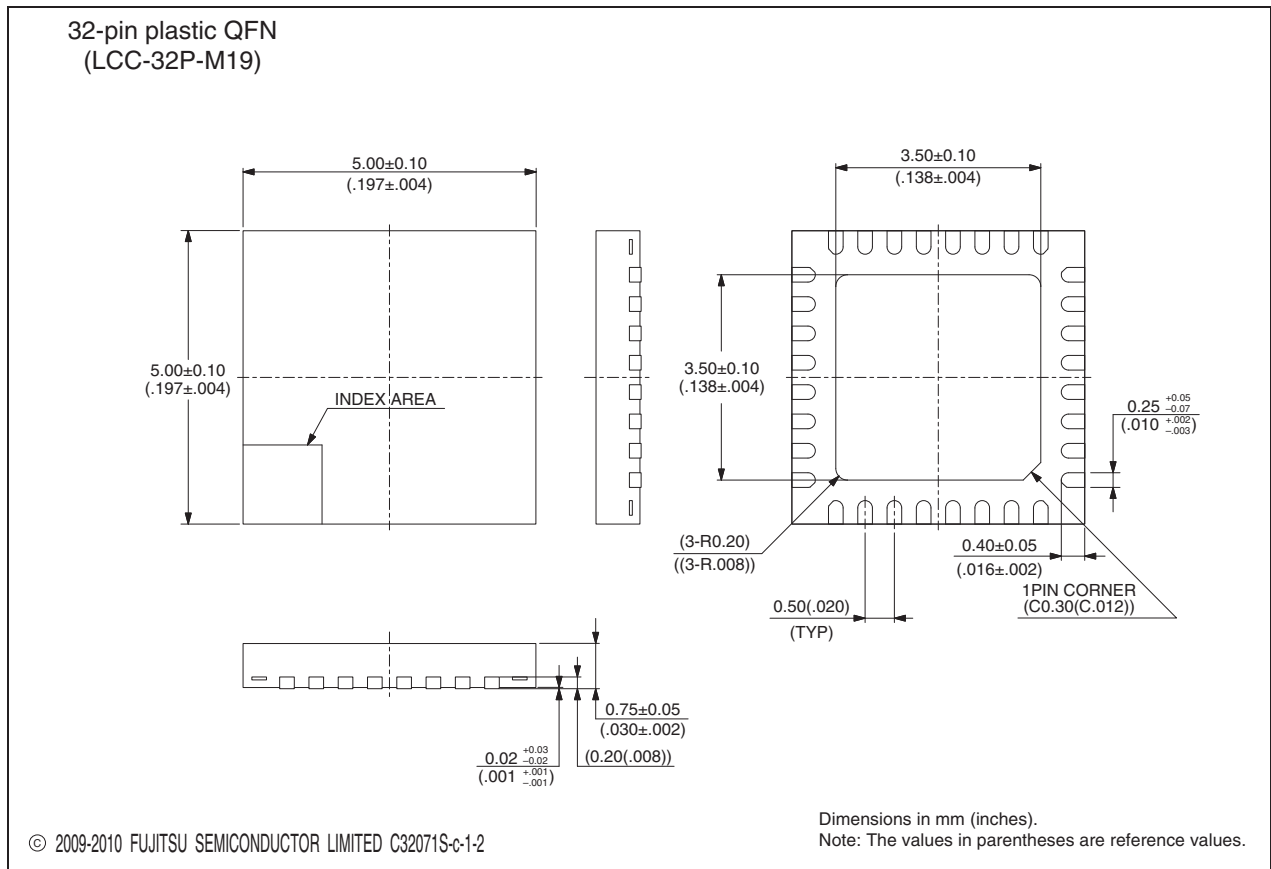
28. Package Dimension

| | | | |
|---|--------------------------------|--------------------|--|
| <p>24-pin plastic SDIP</p>  <p>(DIP-24P-M07)</p> | Lead pitch | 1.778 mm | |
| | Package width × package length | 6.40 mm × 22.86 mm | |
| | Sealing method | Plastic mold | |
| | Mounting height | 4.80 mm Max | |
| | | | |
| | | | |
| | | | |

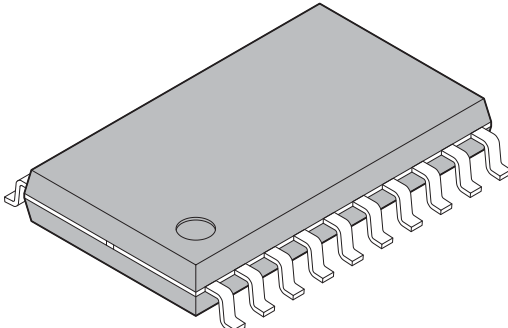


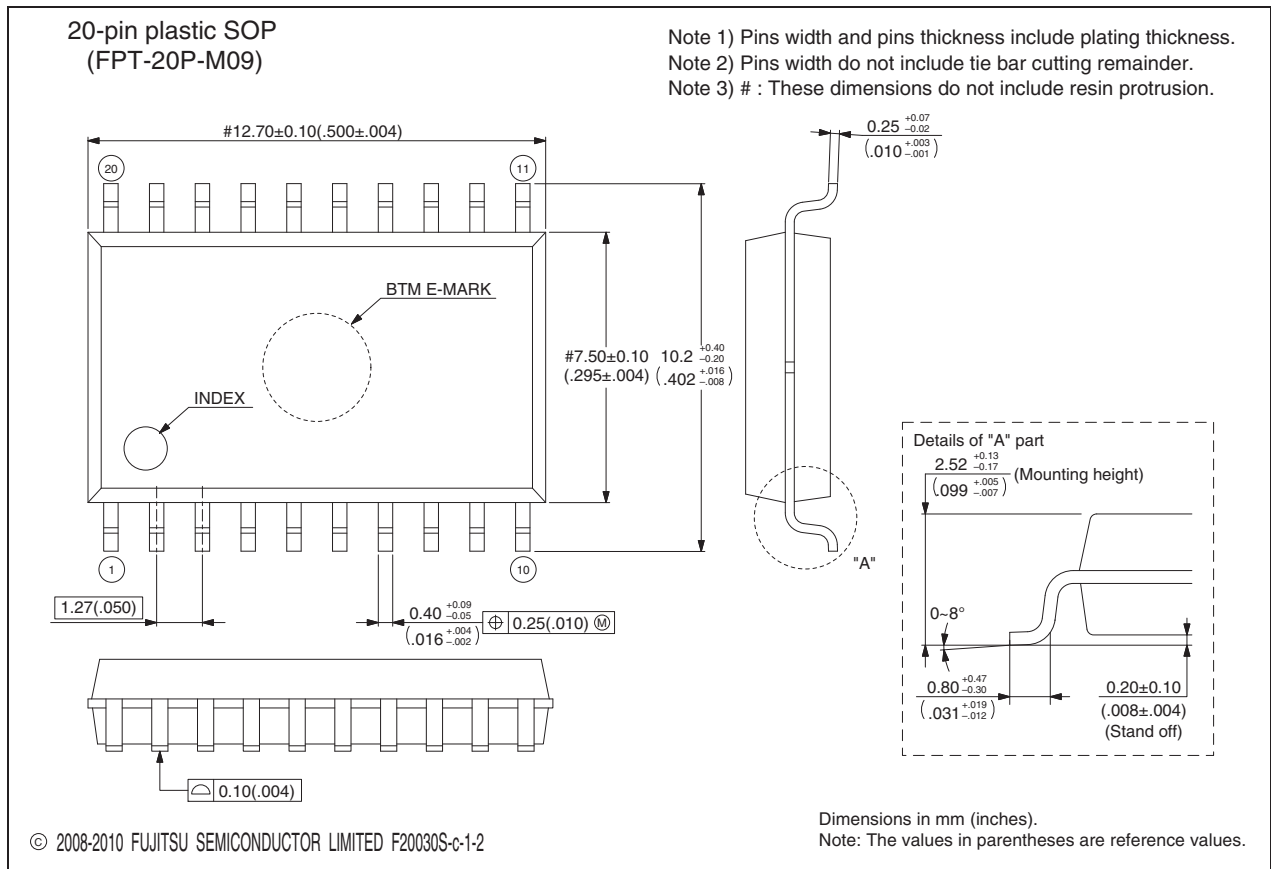
(Continued)

| | | | |
|--|--------------------------------|-------------------|--|
| <p style="text-align: center;">32-pin plastic QFN</p>  <p style="text-align: center;">(LCC-32P-M19)</p> | Lead pitch | 0.50 mm | |
| | Package width × package length | 5.00 mm × 5.00 mm | |
| | Sealing method | Plastic mold | |
| | Mounting height | 0.80 mm MAX | |
| | Weight | 0.06 g | |
| | | | |
| | | | |

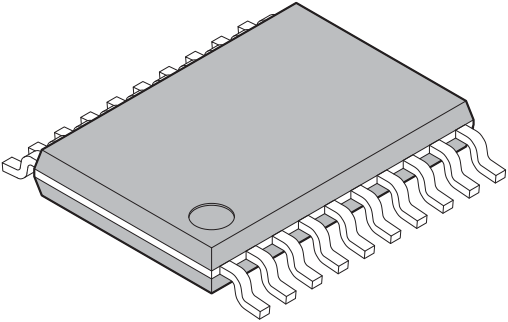


(Continued)

| | | |
|--|--------------------------------|--------------------|
| <p style="text-align: center;">20-pin plastic SOP</p>  <p style="text-align: center;">(FPT-20P-M09)</p> | Lead pitch | 1.27 mm |
| | Package width × package length | 7.50 mm × 12.70 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 2.65 mm Max |
| | | |

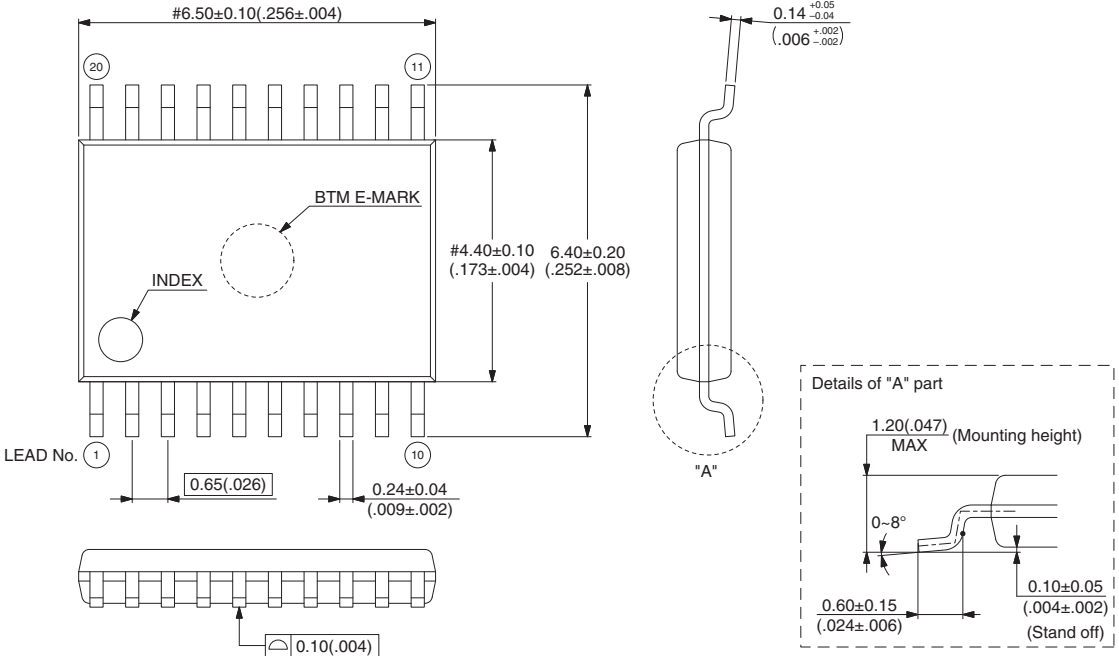


(Continued)

| | | |
|--|--------------------------------|-------------------|
| <p style="text-align: center;">20-pin plastic TSSOP</p>  <p style="text-align: center;">(FPT-20P-M10)</p> | Lead pitch | 0.65 mm |
| | Package width × package length | 4.40 mm × 6.50 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.20 mm MAX |
| | Weight | 0.08 g |
| | | |

20-pin plastic TSSOP (FPT-20P-M10)

Note 1) Pins width and pins thickness include plating thickness.
 Note 2) Pins width do not include tie bar cutting remainder.
 Note 3) #: These dimensions do not include resin protrusion.



Top view dimensions: #6.50±0.10 (.256±.004), #4.40±0.10 (.173±.004), 6.40±0.20 (.252±.008), 0.24±0.04 (.009±.002), 0.65(.026), 0.10(.004)

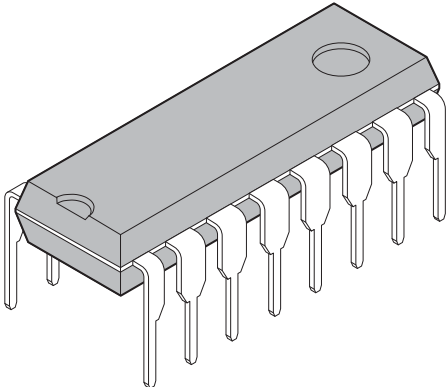
Lead dimensions: 0.14^{+0.05}/_{-0.04} (.006^{+0.002}/_{-0.002})

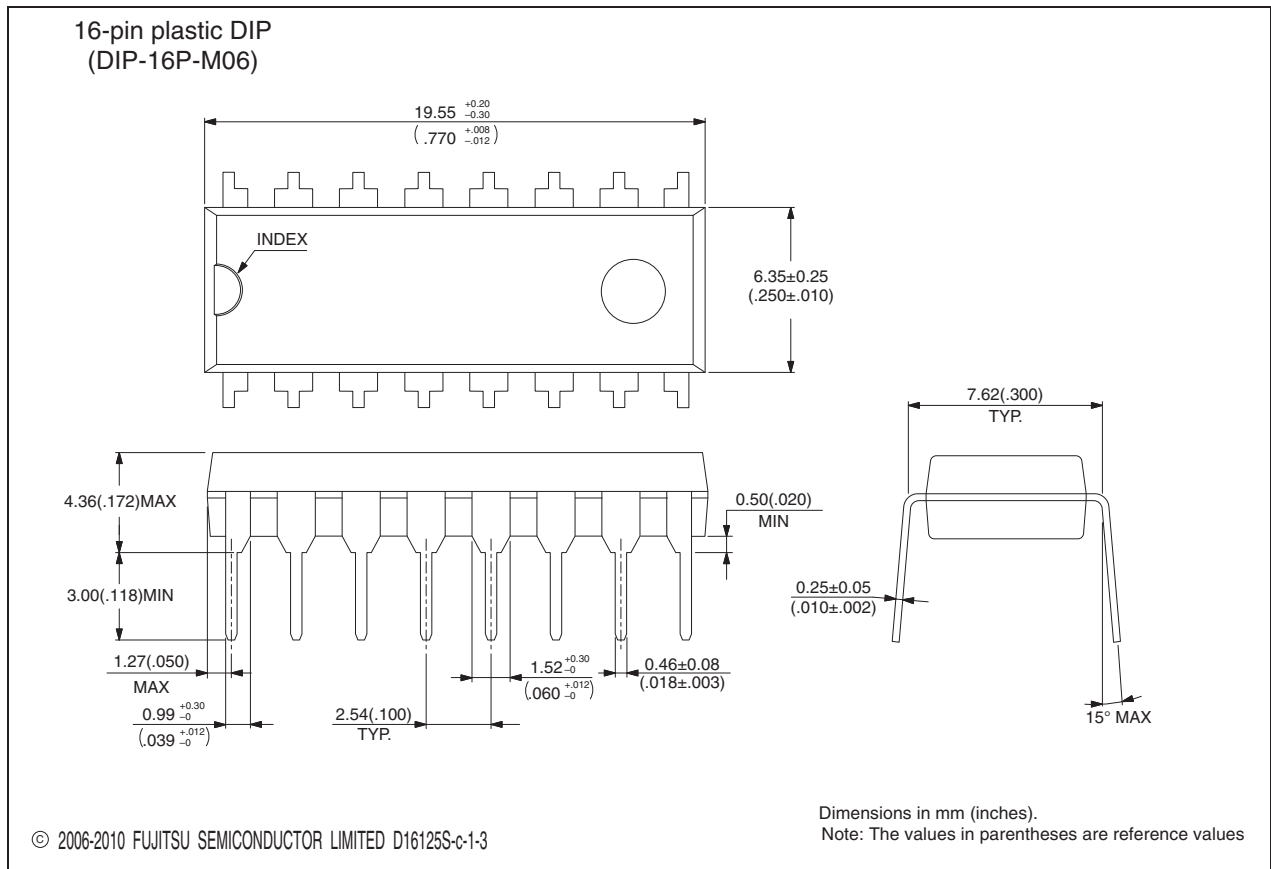
Lead shape details: 1.20(.047) MAX (Mounting height), 0-8°, 0.60±0.15 (.024±.006), 0.10±0.05 (.004±.002) (Stand off)

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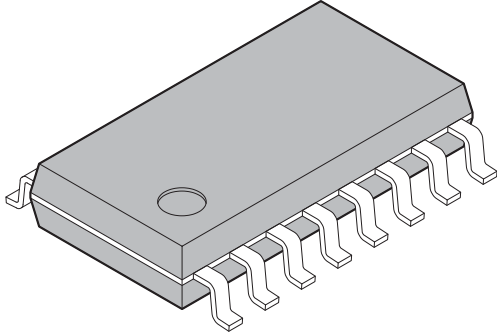
Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

(Continued)

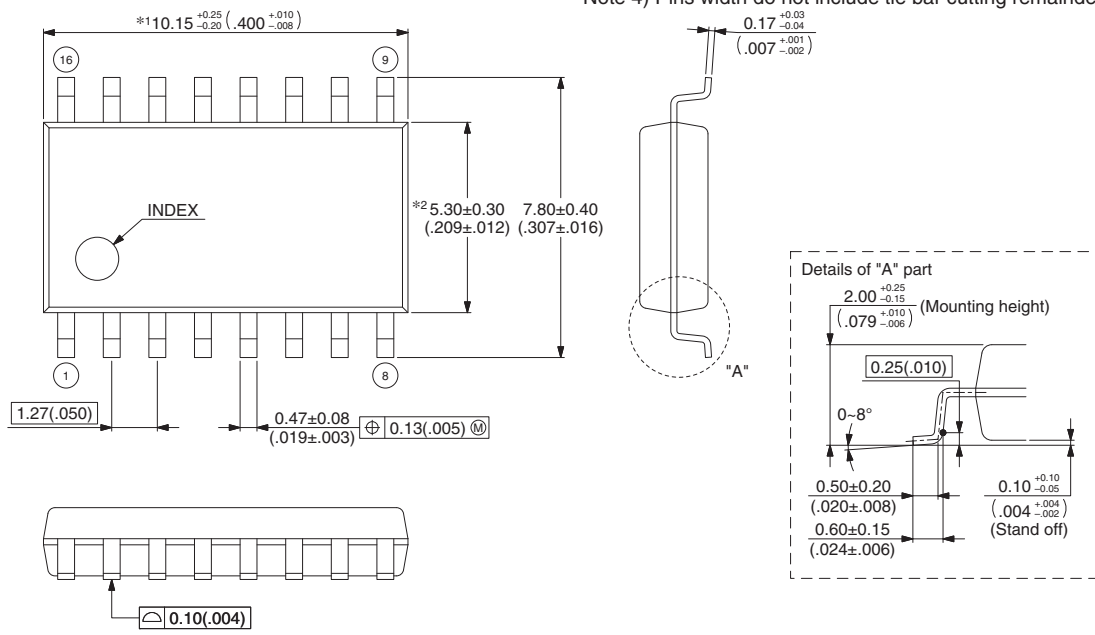
| | | |
|--|----------------|--------------|
| <p style="text-align: center;">16-pin plastic DIP</p>  <p style="text-align: center;">(DIP-16P-M06)</p> | Lead pitch | 2.54 mm |
| | Sealing method | Plastic mold |
| | | |
| | | |
| | | |
| | | |
| | | |



(Continued)

| | | |
|--|--------------------------------|------------------------|
| <p style="text-align: center;">16-pin plastic SOP</p>  <p style="text-align: center;">(FPT-16P-M06)</p> | Lead pitch | 1.27 mm |
| | Package width × package length | 5.3 × 10.15 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 2.25 mm MAX |
| | Weight | 0.20 g |
| | Code (Reference) | P-SOP16-5.3×10.15-1.27 |

16-pin plastic SOP
(FPT-16P-M06)



INDEX

*1 110.15^{+0.25}/_{-0.20} (.400^{+0.10}/_{-0.08})

*2 5.30±0.30 7.80±0.40
(.209±.012) (.307±.016)

1.27(.050) 0.47±0.08
(.019±.003) 0.13(.005) Ⓜ

0.17^{+0.03}/_{-0.04}
(.007^{+0.001}/_{-0.002})

2.00^{+0.25}/_{-0.15} (Mounting height)
(.079^{+0.10}/_{-0.06})

0.25(.010)

0~8°

0.50±0.20 0.10^{+0.10}/_{-0.05}
(.020±.008) (.004^{+0.04}/_{-0.02})
(Stand off)
(.024±.006)

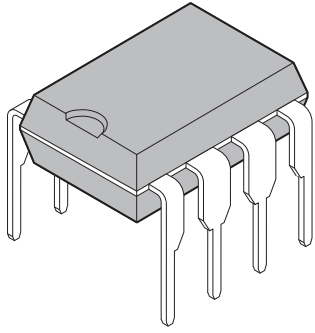
0.10(.004)

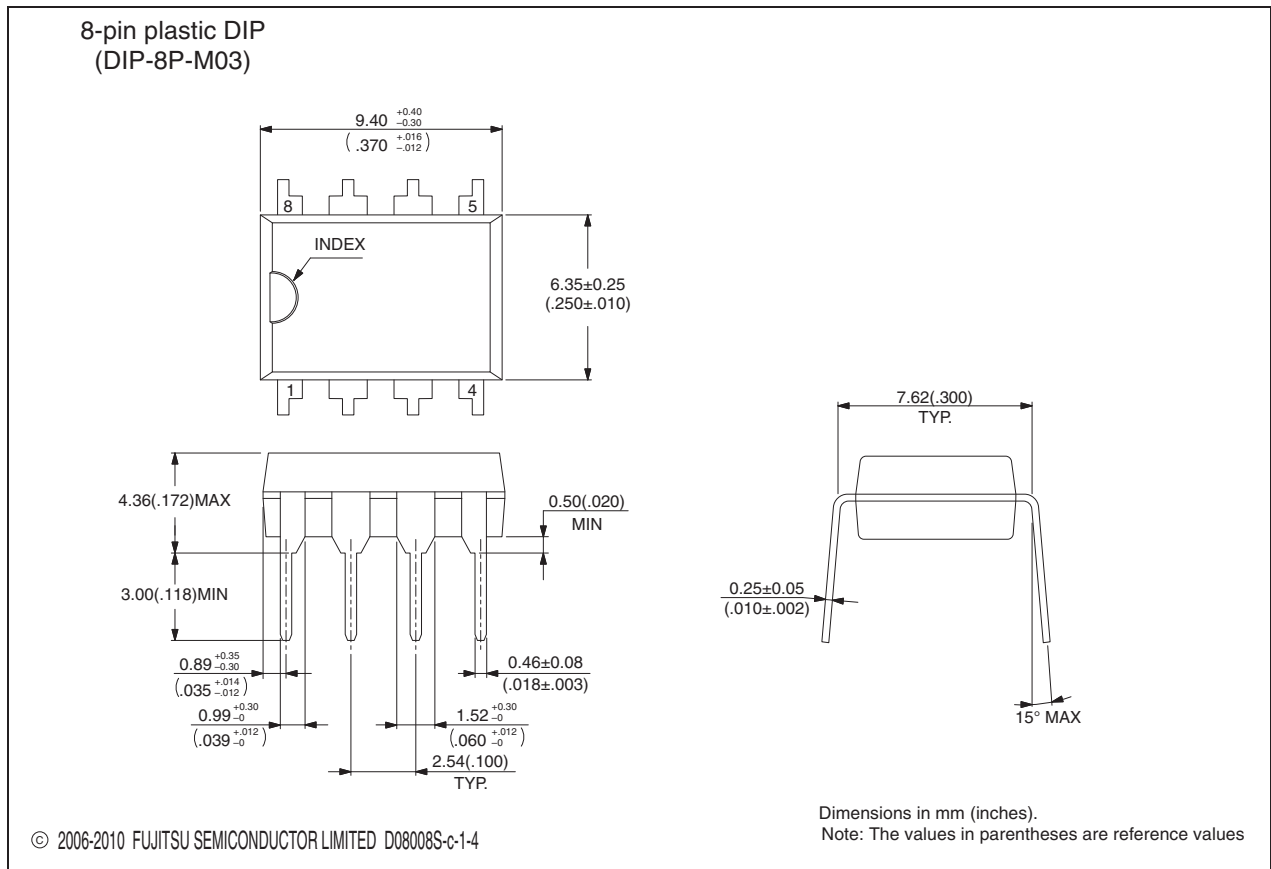
Note 1) *1 : These dimensions include resin protrusion.
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

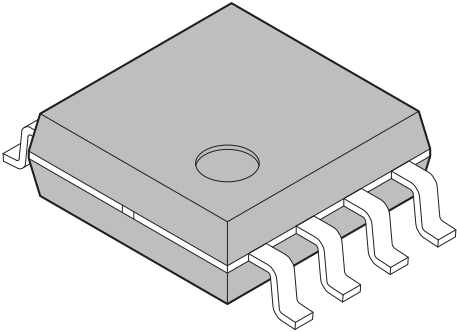
(Continued)

| | | |
|--|----------------|--------------|
| <p>8-pin plastic DIP</p>  <p>(DIP-8P-M03)</p> | Lead pitch | 2.54 mm |
| | Sealing method | Plastic mold |
| | | |
| | | |
| | | |
| | | |

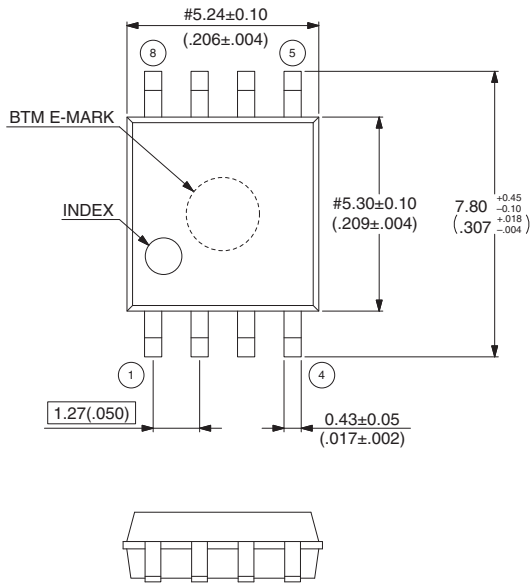


(Continued)

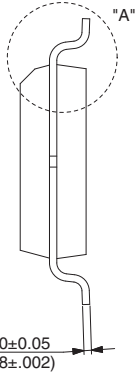
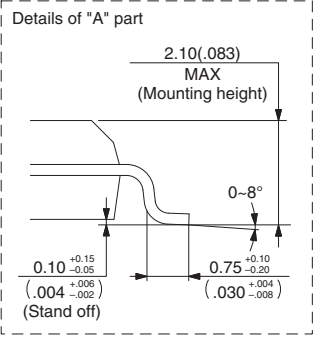
(Continued)

| | | |
|--|--------------------------------|-------------------|
| <p style="text-align: center;">8-pin plastic SOP</p>  <p style="text-align: center;">(FPT-8P-M08)</p> | Lead pitch | 1.27 mm |
| | Package width × package length | 5.30 mm × 5.24 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 2.10 mm Max |
| | | |

8-pin plastic SOP
(FPT-8P-M08)



Note 1) Pins width and pins thickness include plating thickness.
 Note 2) Pins width do not include tie bar cutting remainder.
 Note 3) # : These dimensions do not include resin protrusion.

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

29. Major Changes

Span sion Publication Number: DS07–12627–7E

| Page | Section | Details |
|--------|---|--|
| 1 | — | Changed the family name. F ² MC-8FX → New 8FX |
| 2 | Features | Added “• Power-on reset”. |
| 3 | Product Line-up MB95260H Series | Added the parameter “Power-on reset”. |
| 5 | Product Line-up MB95270H Series | Added the parameter “Power-on reset”. |
| 6 | Product Line-up MB95280H Series | Added the parameter “Power-on reset”. |
| 10 | Pin Assignment | Deleted the HCLK1 pin and the HCLK2 pin. |
| 11 | | Deleted the HCLK1 pin and the HCLK2 pin. |
| 13 | Pin Description (MB95260H Series, 32 pins) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 15 | Pin Description (MB95260H Series, 24 pins) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 17 | Pin Description (MB95260H Series, 20 pins) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 18 | Pin Description (MB95270H Series, 8 pins) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 19 | Pin Description (MB95280H Series, 32 pins) | Deleted the HCLK1 pin. |
| 20 | | Deleted the HCLK2 pin. |
| 21 | Pin Description (MB95280H Series, 16 pins) | Deleted the HCLK1 pin. |
| 22 | | Deleted the HCLK2 pin. |
| 27 | Block Diagram (MB95260H Series) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 28 | Block Diagram (MB95270H Series) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 29 | Block Diagram (MB95280H Series) | Deleted the HCLK1 pin and the HCLK2 pin. |
| 52, 53 | Electrical Characteristics 4. AC Characteristics (1) Clock Timing | Deleted all information about the HCLK1 pin and the HCLK2 pin in the table. |
| 54 | | Deleted the HCLK1 pin and the HCLK2 pin in the “ Input waveform generated when an external clock (main clock) is used”. |
| | | Deleted the external connection diagram for the HCLK1 pin and the HCLK2 pin in “ Figure of main clock input port external connection”. |

NOTE: Please see “Document History” about later revised information.

Document History

| Document Title: MB95260H/270H/280H Series New 8FX 8-bit Microcontrollers | | | | |
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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | — | AKIH | 07/04/2011 | Migrated to Cypress and assigned document number 002-07516. No change to document contents or format. |
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