

Low-Cost, High-Speed, Single-Supply Op Amps with Rail-to-Rail Outputs

MAX4012/MAX4016/ MAX4018/MAX4020

General Description

The MAX4012 single, MAX4016 dual, MAX4018 triple, and MAX4020 quad op amps are unity-gain-stable devices that combine high-speed performance with Rail-to-Rail outputs. The MAX4018 has a disable feature that reduces power-supply current to 400µA and places its outputs into a high-impedance state. These devices operate from a 3.3V to 10V single supply or from ±1.65V to ±5V dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

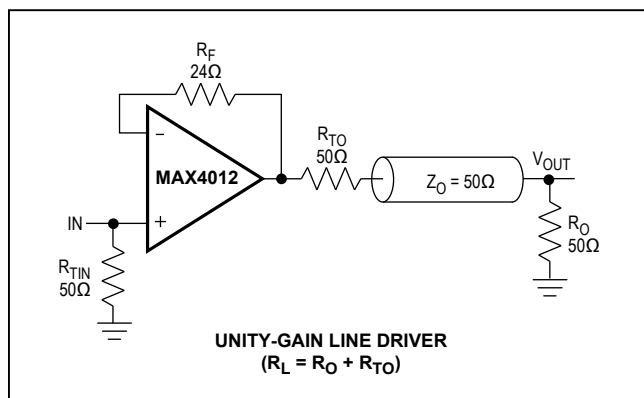
These devices require only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/µs slew rate. These parts are an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation. In addition, when disabled, their high-output impedance makes them ideal for multiplexing applications.

The MAX4012 comes in a miniature 5-pin SOT23 and 8-pin SO package, while the MAX4016 comes in 8-pin µMAX® and SO packages. The MAX4018/MAX4020 are available in a space-saving 16-pin QSOP, as well as a 14-pin SO.

Applications

- Set-Top Boxes
- Surveillance Video Systems
- Battery-Powered Instruments
- Video Line Driver
- Analog-to-Digital Converter Interface
- CCD Imaging Systems
- Video Routing and Switching Systems

Typical Operating Circuit



Features

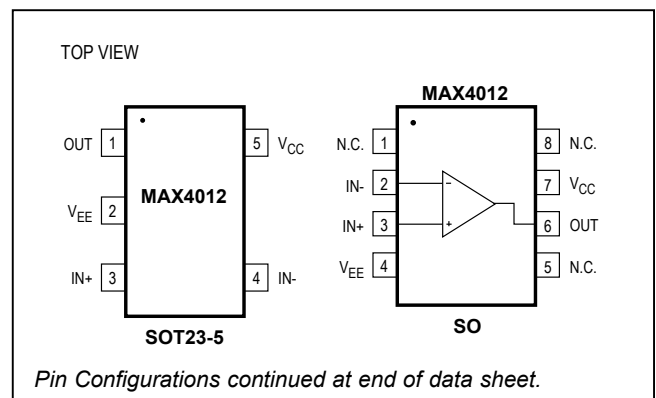
- Low-Cost
- High Speed:
 - 200MHz -3dB Bandwidth (MAX4012)
 - 150MHz -3dB Bandwidth
 - (MAX4016/MAX4018/MAX4020)
 - 30MHz 0.1dB Gain Flatness
 - 600V/µs Slew Rate
- Single 3.3V/5.0V Operation
- Rail-to-Rail Outputs
- Input Common-Mode Range Extends Beyond V_{EE}
- Low Differential Gain/Phase: 0.02%/0.02°
- Low Distortion at 5MHz:
 - -78dBc SFDR
 - -75dB Total Harmonic Distortion
- High-Output Drive: ±120mA
- 400µA Shutdown Capability (MAX4018)
- High-Output Impedance in Off State (MAX4018)
- Space-Saving SOT23, SO, µMAX, or QSOP Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4012EUK+T	-40°C to +85°C	5 SOT23-5	AMKD
MAX4012ESA+T	-40°C to +85°C	8 SO	—
MAX4016ESA+T	-40°C to +85°C	8 SO	—
MAX4016EUA+T	-40°C to +85°C	8 µMAX	—

Ordering Information continued at end of data sheet.

Pin Configurations



Absolute Maximum Ratings

Supply Voltage (V_{CC} to V_{EE}) 12V	8-Pin μ MAX (derate 4.1mW/°C above +70°C)330mW
IN_- , IN_+ , OUT_- , EN_- ($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)	14-Pin SO (derate 8.3mW/°C above +70°C)667mW
Output Short-Circuit Duration to V_{CC} or V_{EE} Continuous	16-Pin QSOP (derate 8.3mW/°C above +70°C)667mW
Continuous Power Dissipation ($T_A = +70^\circ C$)		Operating Temperature Range -40°C to +85°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C)571mW	Storage Temperature Range -65°C to +150°C
8-Pin SO (derate 5.9mW/°C above +70°C)471mW	Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

($V_{CC} = 5V$, $V_{EE} = 0$, $EN_- = 5V$, $R_L = \infty$ to $V_{CC}/2$, $V_{OUT} = V_{CC}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	$V_{EE} - 0.20$		$V_{CC} - 2.25$	V	
Input Offset Voltage (Note 2)	V_{OS}			4	20	mV	
Input Offset Voltage Temperature Coefficient	TC_{VOS}			8		$\mu V/^\circ C$	
Input Offset Voltage Matching		Any channels for MAX4016/MAX4018/MAX4020		± 1		mV	
Input Bias Current	I_B	(Note 2)		5.4	20	μA	
Input Offset Current	I_{OS}	(Note 2)		0.1	20	μA	
Input Resistance	R_{IN}	Differential mode ($-1V \leq V_{IN} \leq +1V$)		70		k Ω	
		Common mode ($-0.2V \leq V_{CM} \leq +2.75V$)		3		M Ω	
Common-Mode Rejection Ratio	CMRR	($V_{EE} - 0.2V$) $\leq V_{CM} \leq (V_{CC} - 2.25V)$	70	100		dB	
Open-Loop Gain (Note 2)	A_{VOL}	$0.25V \leq V_{OUT} \leq 4.75V$, $R_L = 2k\Omega$		61		dB	
		$0.5V \leq V_{OUT} \leq 4.5V$, $R_L = 150\Omega$	52	59			
		$1.0V \leq V_{OUT} \leq 4V$, $R_L = 50\Omega$		57			
Output Voltage Swing (Note 2)	V_{OUT}	$R_L = 2k\Omega$	$V_{CC} - V_{OH}$		0.06	V	
			$V_{OL} - V_{EE}$		0.06		
		$R_L = 150\Omega$	$V_{CC} - V_{OH}$		0.30		
			$V_{OL} - V_{EE}$		0.30		
		$R_L = 75\Omega$	$V_{CC} - V_{OH}$		0.6		1.5
			$V_{OL} - V_{EE}$		0.6		1.5
		$R_L = 75\Omega$ to ground	$V_{CC} - V_{OH}$		1.1		2.0
			$V_{OL} - V_{EE}$		0.05		0.50
Output Current	I_{OUT}	$R_L = 20\Omega$ to V_{CC} or V_{EE}	$T_A = +25^\circ C$	± 70	± 120	mA	
			$T_A = T_{MIN}$ to T_{MAX}	± 60			
Output Short-Circuit Current	I_{SC}	Sinking or sourcing		± 150		mA	
Open-Loop Output Resistance	R_{OUT}			8		Ω	

DC Electrical Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, $EN_{-} = 5V$, $R_L = \infty$ to $V_{CC}/2$, $V_{OUT} = V_{CC}/2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 3)	PSRR	$V_{CC} = 5V$, $V_{EE} = 0$, $V_{CM} = 2.0V$	46	57		dB
		$V_{CC} = 5V$, $V_{EE} = -5V$, $V_{CM} = 0$	54	66		
		$V_{CC} = 3.3V$, $V_{EE} = 0$, $V_{CM} = 0.90V$		45		
Operating Supply-Voltage Range	V_S	V_{CC} to V_{EE}	3.15		11.0	V
Disabled Output Resistance	$R_{OUT(OFF)}$	$EN_{-} = 0$, $0 \leq V_{OUT} \leq 5V$ (Note 4)	28	35		k Ω
EN_ Logic-Low Threshold	V_{IL}				$V_{CC} - 2.6$	V
EN_ Logic-High Threshold	V_{IH}		$V_{CC} - 1.6$			V
EN_ Logic Input Low Current	I_{IL}	$(V_{EE} + 0.2V) \leq EN_{-} \leq V_{CC}$		0.5		μA
		$EN_{-} = 0$		200	400	
EN_ Logic Input High Current	I_{IH}	$EN_{-} = 5V$		0.5	10	μA
Quiescent Supply Current (per Amplifier)	I_S	Enabled		5.5	7.0	mA
		MAX4018, disabled ($EN_{-} = 0$)		0.40	0.65	

AC Electrical Characteristics

($V_{CC} = 5V$, $V_{EE} = 0$, $V_{CM} = 2.5V$, $EN_{-} = 5V$, $R_F = 24\Omega$, $R_L = 100\Omega$ to $V_{CC}/2$, $V_{OUT} = V_{CC}/2$, $A_{VCL} = 1$, $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{OUT} = 20mV_{P-P}$	MAX4012	200		MHz
			MAX4016/MAX4018/ MAX4020	150		
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{OUT} = 2V_{P-P}$		140		MHz
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	$V_{OUT} = 20mV_{P-P}$ (Note 5)	6	30		MHz
Slew Rate	SR	$V_{OUT} = 2V$ step		600		V/ μ s
Settling Time to 0.1%	t_S	$V_{OUT} = 2V$ step		45		ns
Rise/Fall Time	t_R, t_F	$V_{OUT} = 100mV_{P-P}$		1		ns
Spurious-Free Dynamic Range	SFDR	$f_C = 5MHz$, $V_{OUT} = 2V_{P-P}$		-78		dBc
Harmonic Distortion	HD	$f_C = 5MHz$, $V_{OUT} = 2V_{P-P}$	2nd harmonic	-78		dBc
			3rd harmonic	-82		
			Total harmonic distortion	-75		dB
Two-Tone, Third-Order Intermodulation Distortion	IP3	$f_1 = 10.0MHz$, $f_2 = 10.1MHz$, $V_{OUT} = 1V_{P-P}$		35		dBc
Input 1dB Compression Point		$f_C = 10MHz$, $A_{VCL} = 2$		11		dBm
Differential Phase Error	DP	NTSC, $R_L = 150\Omega$		0.02		degrees
Differential Gain Error	DG	NTSC, $R_L = 150\Omega$		0.02		%
Input Noise-Voltage Density	e_n	$f = 10kHz$		10		nV/ \sqrt{Hz}
Input Noise-Current Density	i_n	$f = 10kHz$		1.3		nV/ \sqrt{Hz}
Input Capacitance	C_{IN}			1		pF
Disabled Output Capacitance	$C_{OUT(OFF)}$	MAX4018, $EN_{-} = 0$		2		pF
Output Impedance	Z_{OUT}	$f = 10MHz$		6		Ω
Amplifier Enable Time	t_{ON}	MAX4018		100		ns
Amplifier Disable Time	t_{OFF}	MAX4018		1		μ s
Amplifier Gain Matching		MAX4016/MAX4018/MAX4020, $f = 10MHz$, $V_{OUT} = 20mV_{P-P}$		0.1		dB
Amplifier Crosstalk	X_{TALK}	MAX4016/MAX4018/MAX4020, $f = 10MHz$, $V_{OUT} = 2V_{P-P}$, $R_S = 50\Omega$ to ground		-95		dB

Note 1: The MAX4012EUT is 100% production tested at $T_A = +25^{\circ}C$. Specifications over temperature limits are guaranteed by design.

Note 2: Tested with $V_{CM} = 2.5V$.

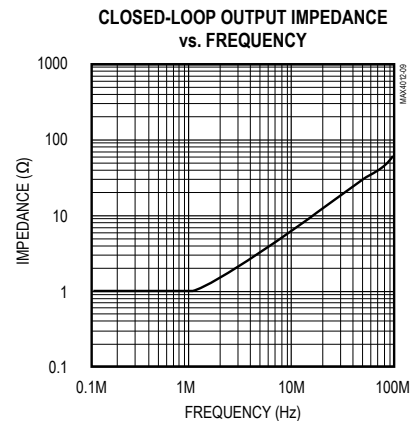
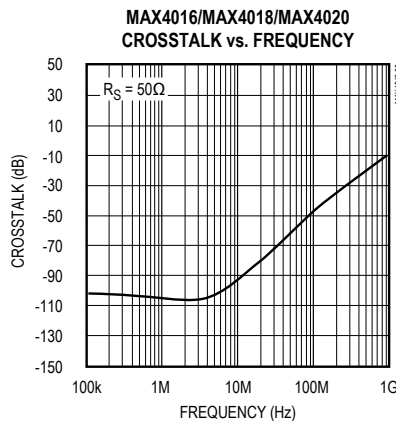
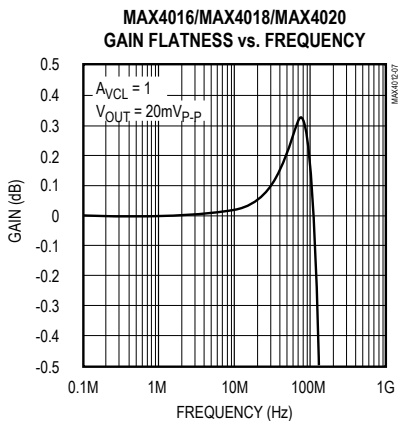
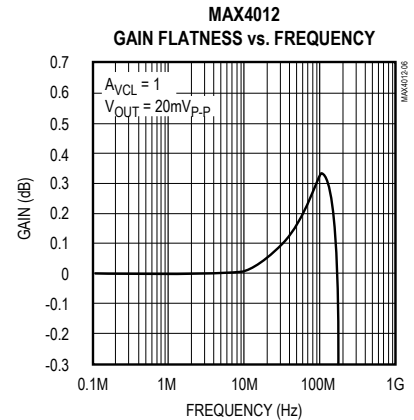
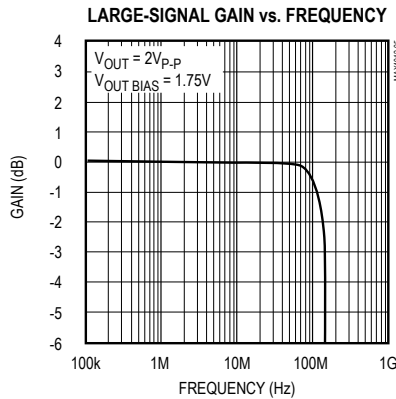
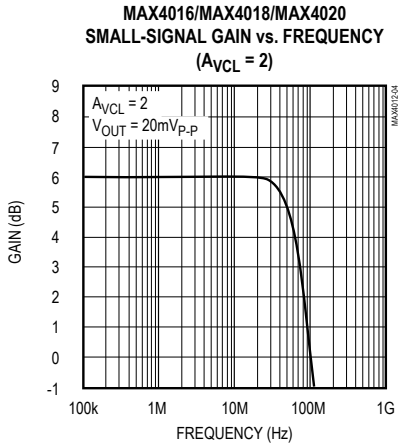
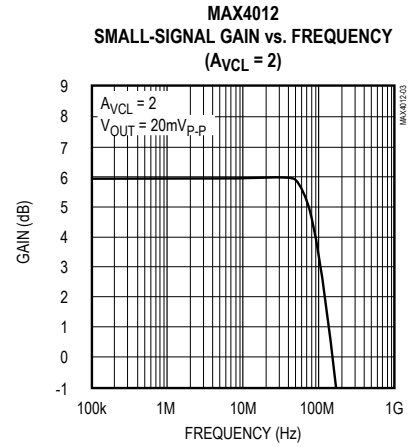
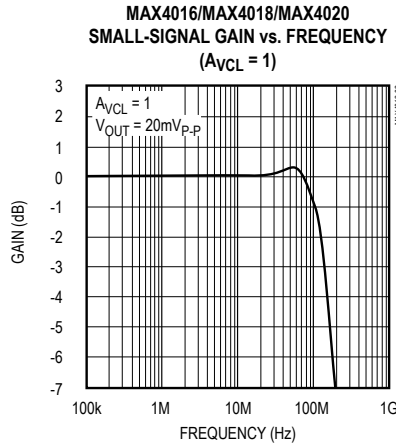
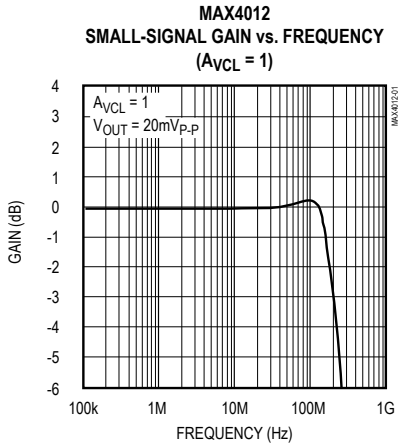
Note 3: PSR for single 5V supply tested with $V_{EE} = 0$, $V_{CC} = 4.5V$ to $5.5V$; for dual $\pm 5V$ supply with $V_{EE} = -4.5V$ to $-5.5V$, $V_{CC} = 4.5V$ to $5.5V$; and for single 3.3V supply with $V_{EE} = 0$, $V_{CC} = 3.15V$ to $3.45V$.

Note 4: Does not include the external feedback network's impedance.

Note 5: Guaranteed by design.

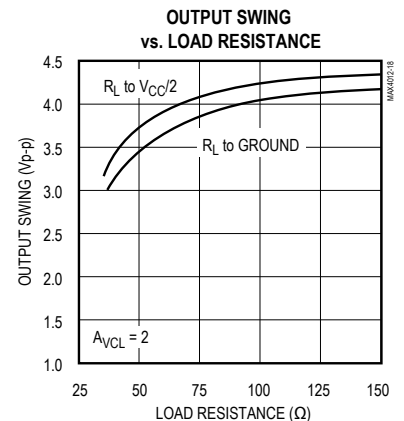
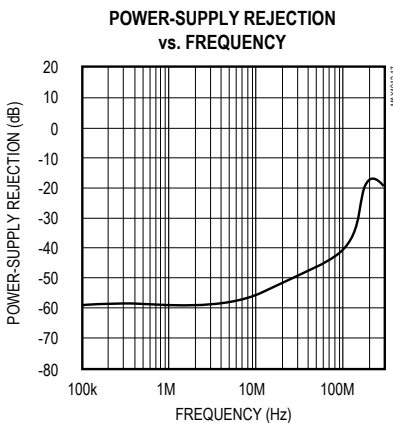
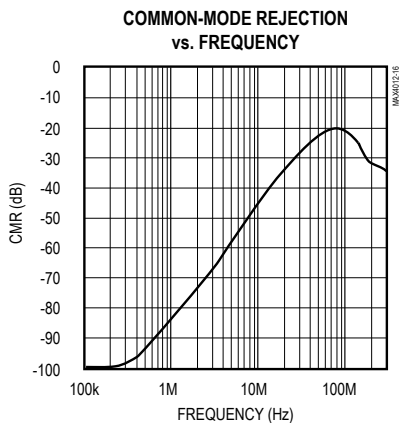
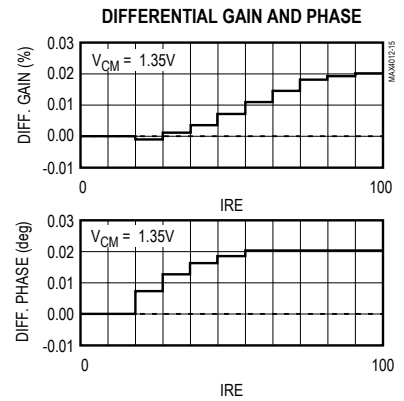
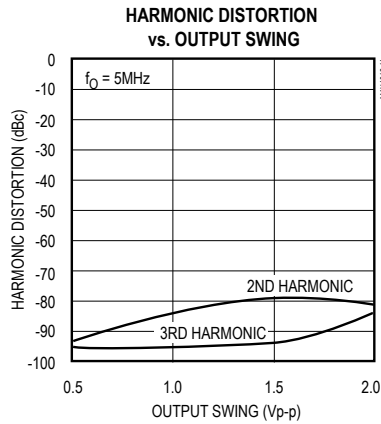
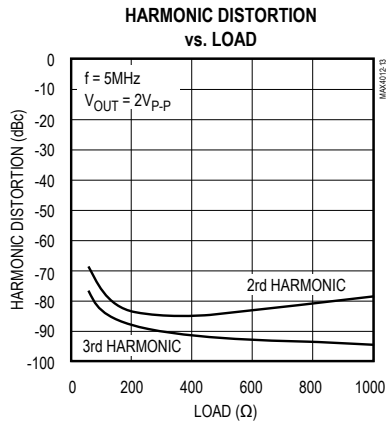
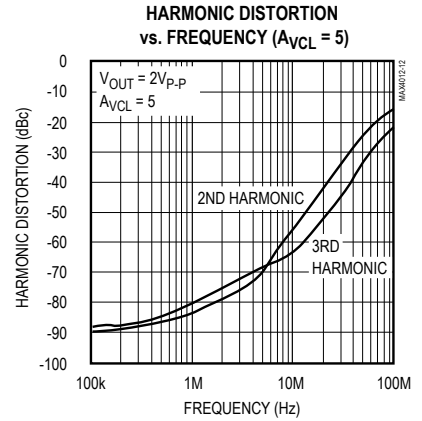
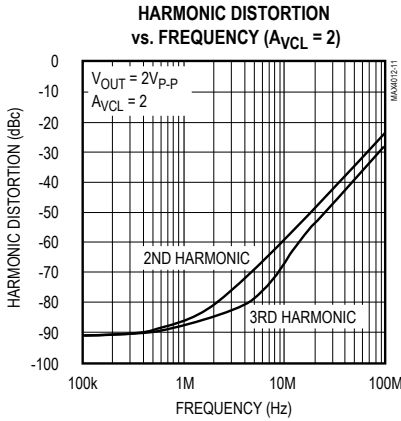
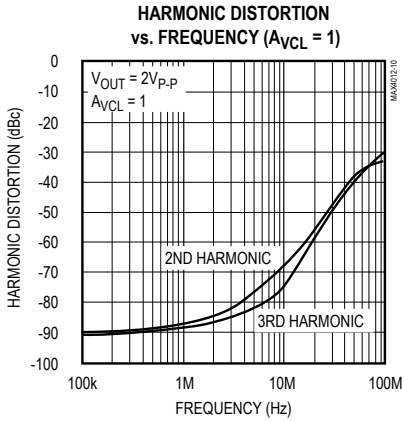
Typical Operating Characteristics

($V_{CC} = 5V$, $V_{EE} = 0$, $A_{VCL} = 1$, $R_F = 24\Omega$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

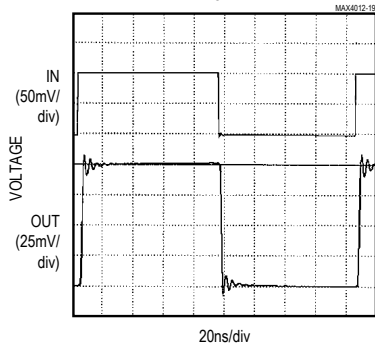
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Typical Operating Characteristics (continued)

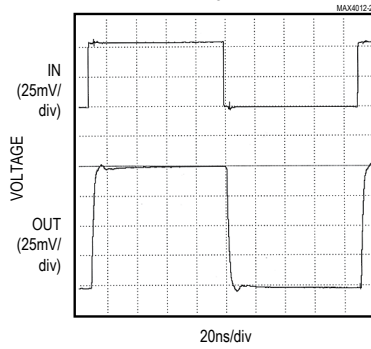
($V_{CC} = 5V$, $V_{EE} = 0$, $A_{VCL} = 1$, $R_F = 24\Omega$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

**SMALL-SIGNAL PULSE RESPONSE
($A_{VCL} = 1$)**



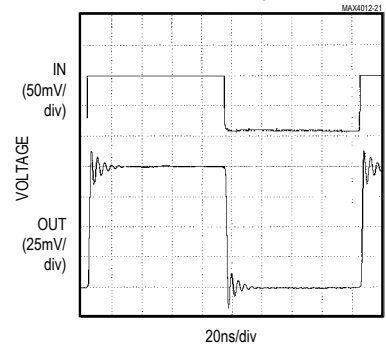
$V_{CM} = 2.5V$, $R_L = 100\Omega$ to GROUND

**SMALL-SIGNAL PULSE RESPONSE
($A_{VCL} = 2$)**



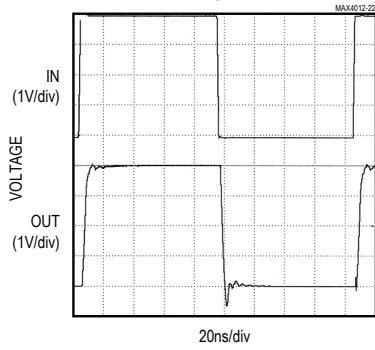
$V_{CM} = 1.25V$, $R_L = 100\Omega$ to GROUND

**SMALL-SIGNAL PULSE RESPONSE
($C_L = 5pF$, $A_{VCL} = 1$)**



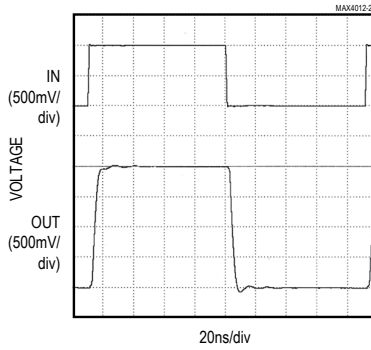
$V_{CM} = 1.75V$, $R_L = 100\Omega$ to GROUND

**LARGE-SIGNAL PULSE RESPONSE
($A_{VCL} = 1$)**



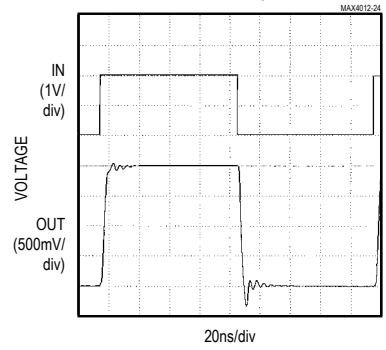
$V_{CM} = 1.75V$, $R_L = 100\Omega$ to GROUND

**LARGE-SIGNAL PULSE RESPONSE
($A_{VCL} = 2$)**



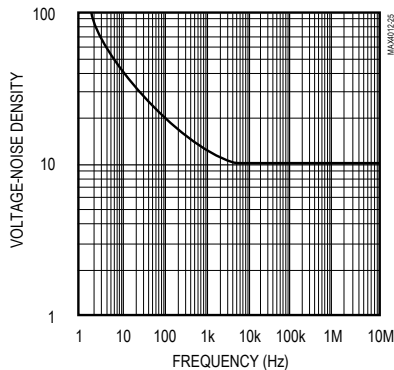
$V_{CM} = 0.9V$, $R_L = 100\Omega$ to GROUND

**LARGE-SIGNAL PULSE RESPONSE
($C_L = 5pF$, $A_{VCL} = 2$)**

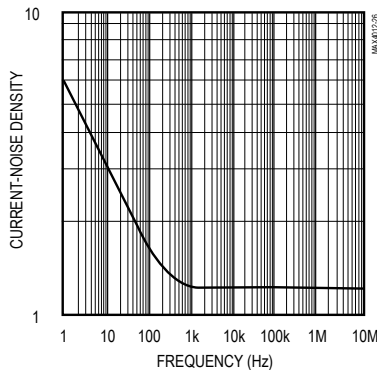


$V_{CM} = 1.75V$, $R_L = 100\Omega$ to GROUND

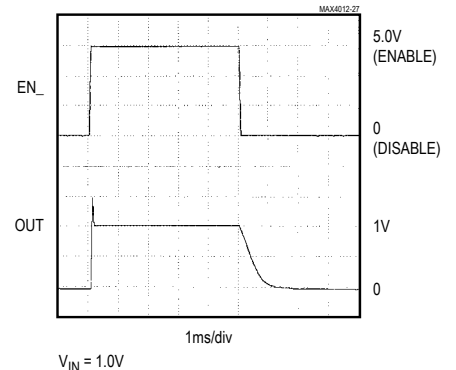
**VOLTAGE-NOISE DENSITY
vs. FREQUENCY**



**CURRENT-NOISE DENSITY
vs. FREQUENCY**

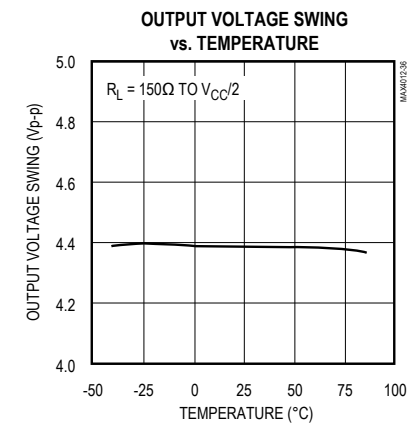
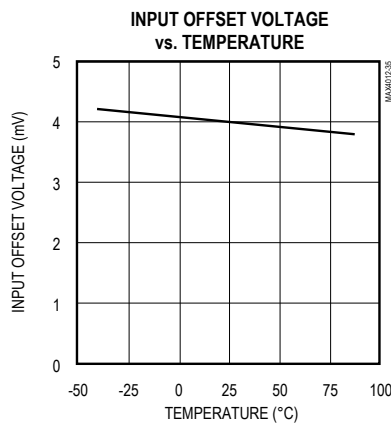
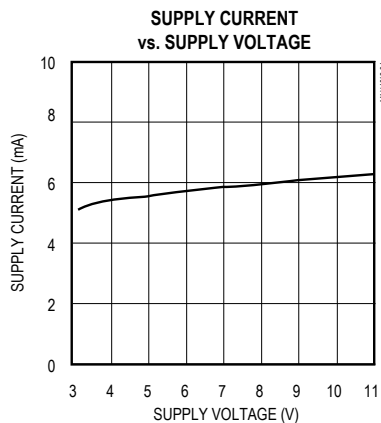
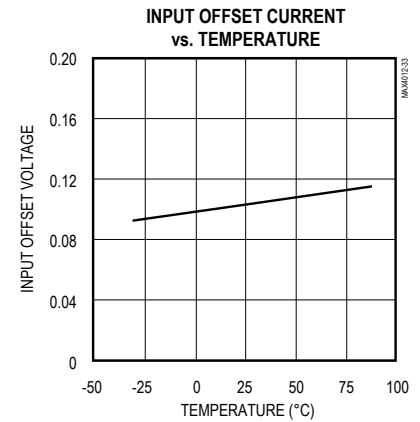
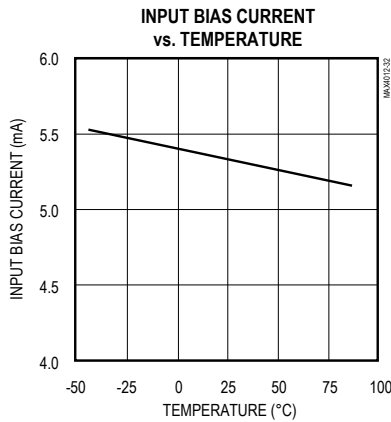
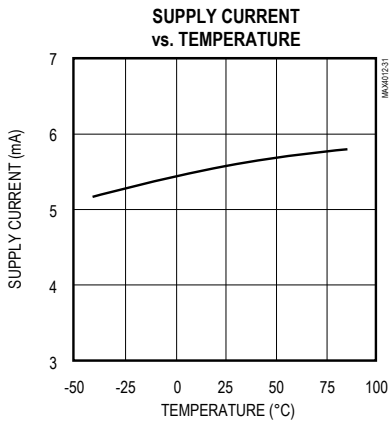
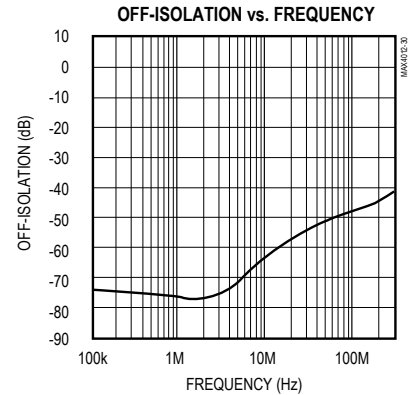
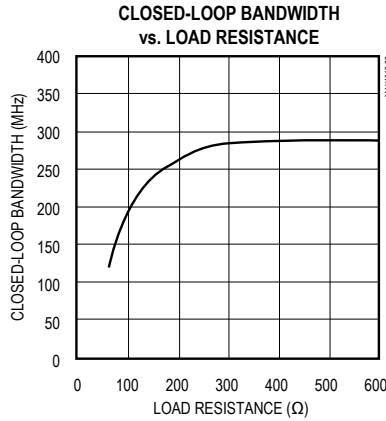
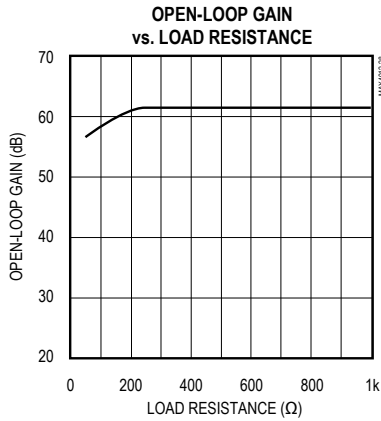


ENABLE RESPONSE TIME



Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, $A_{VCL} = 1$, $R_F = 24\Omega$, $R_L = 100\Omega$ to $V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN							NAME	FUNCTION
MAX4012 SO-8	MAX4012 SOT23	MAX4016 SO/ μ MAX	MAX4018		MAX4020			
			SO	QSOP	SO	QSOP		
1, 5, 8	—	—	—	8, 9	—	8, 9	N.C.	No Connection. Not internally connected. Tie to ground or leave open.
6	1	—	—	—	—	—	OUT	Amplifier Output
4	2	4	11	13	11	13	V _{EE}	Negative Power Supply or Ground (in single-supply operation)
3	3	—	—	—	—	—	IN+	Noninverting Input
2	4	—	—	—	—	—	IN-	Inverting Input
7	5	8	4	4	4	4	V _{CC}	Positive Power Supply
—	—	1	7	7	1	1	OUTA	Amplifier A Output
—	—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	—	7	8	10	7	7	OUTB	Amplifier B Output
—	—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	—	12	14	IND+	Amplifier D Noninverting Input
—	—	—	—	—	—	—	EN	Enable Amplifier
—	—	—	1	1	—	—	ENA	Enable Amplifier A
—	—	—	3	3	—	—	ENB	Enable Amplifier B
—	—	—	2	2	—	—	ENC	Enable Amplifier C

MAX4012/MAX4016/ MAX4018/MAX4020

Detailed Description

The MAX4012/MAX4016/MAX4018/MAX4020 are single-supply, rail-to-rail, voltage-feedback amplifiers that employ current-feedback techniques to achieve 600V/ μ s slew rates and 200MHz bandwidths. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

The output voltage swing comes to within 50mV of each supply rail. Local feedback around the output stage assures low open-loop output impedance to reduce gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for ± 120 mA drive capability, while constraining total supply current to less than 7mA. The input stage permits common-mode voltages beyond the negative supply and to within 2.25V of the positive supply rail.

Applications Information

Choosing Resistor Values

Unity-Gain Configuration

The MAX4012/MAX4016/MAX4018/MAX4020 are internally compensated for unity gain. When configured for unity gain, the devices require a 24 Ω resistor (R_F) in series with the feedback path. This resistor improves

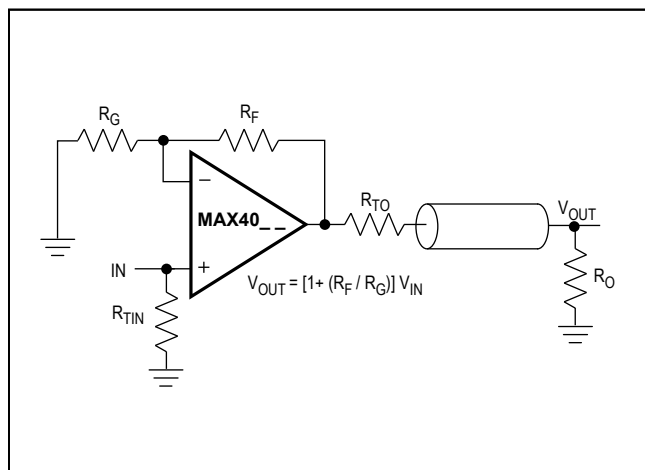


Figure 1a. Noninverting Gain Configuration

Low-Cost, High-Speed, Single-Supply Op Amps with Rail-to-Rail Outputs

AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and inductance.

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration ($R_F = R_G$) using 1k Ω resistors, combined with 1pF of amplifier input capacitance and 1pF of PC board capacitance, causes a pole at 159MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 1k Ω resistors to 100 Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200 Ω in parallel with the amplifier's load resistor. Table 1 shows suggested feedback, gain resistors, and bandwidth for several gain values in the configurations shown in Figures 1a and 1b.

Layout and Power-Supply Bypassing

These amplifiers operate from a single 3.3V to 11V power supply or from dual supplies to ± 5.5 V. For single-supply operation, bypass V_{CC} to ground with a 0.1 μ F capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1 μ F capacitor.

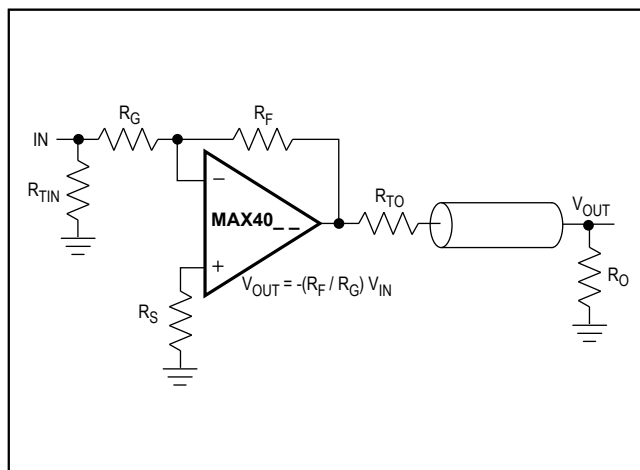


Figure 1b. Inverting Gain Configuration

Analog Devices recommends using microstrip and strip-line techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrap boards because they are too inductive.
- Don't use IC sockets because they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

**Rail-to-Rail Outputs,
Ground-Sensing Input**

The input common-mode range extends from (V_{EE} - 200mV) to (V_{CC} - 2.25V) with excellent common-mode rejection. Beyond this range, the amplifier output is a non-linear function of the input, but does not undergo phase reversal or latchup.

The output swings to within 60mV of either power-supply rail with a 2kΩ load. The input ground-sensing and the rail-to-rail output substantially increase the dynamic range. With a symmetric input in a single 5V application, the input can swing 2.95V_{P-P}, and the output can swing 4.9V_{P-P} with minimal distortion.

Enable Input and Disabled Output

The enable feature (EN_) allows the amplifier to be placed in a low-power, high-output-impedance state. Typically, the EN_ logic low input current (I_{IL}) is small. However, as the EN voltage (V_{IL}) approaches the negative supply rail, I_{IL} increases (Figure 2). A single resistor connected as shown in Figure 3 prevents the rise in the logic-low input current. This resistor provides a feedback mechanism that increases V_{IL} as the logic input is brought to V_{EE}. Figure 4 shows the resulting input current (I_{IL}).

When the MAX4018 is disabled, the amplifier's output impedance is 35kΩ. This high resistance and the low 2pF output capacitance make this part ideal in RF/video multiplexer or switch applications. For larger arrays, pay careful attention to capacitive loading. See the *Output Capacitive Loading and Stability* section for more information.

Table 1. Recommended Component Values

COMPONENT	GAIN (V/V)									
	+1	-1	+2	-2	+5	-5	+10	-10	+25	-25
R _F (Ω)	24	500	500	500	500	500	500	500	500	1200
R _G (Ω)	∞	500	500	250	124	100	56	50	20	50
R _S (Ω)	—	0	—	0	—	0	—	0	—	0
R _{TIN} (Ω)	49.9	56	49.9	62	49.9	100	49.9	∞	49.9	∞
R _{TO} (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
Small-Signal -3dB Bandwidth (MHz)	200	90	105	60	25	33	11	25	6	10

Note: R_L = R_O + R_{TO}; R_{TIN} and R_{TO} are calculated for 50Ω applications. For 75Ω systems, R_{TO} = 75Ω; calculate R_{TIN} from the following equation:

$$R_{TIN} = \frac{75}{1 - \frac{75}{R_G}} \Omega$$

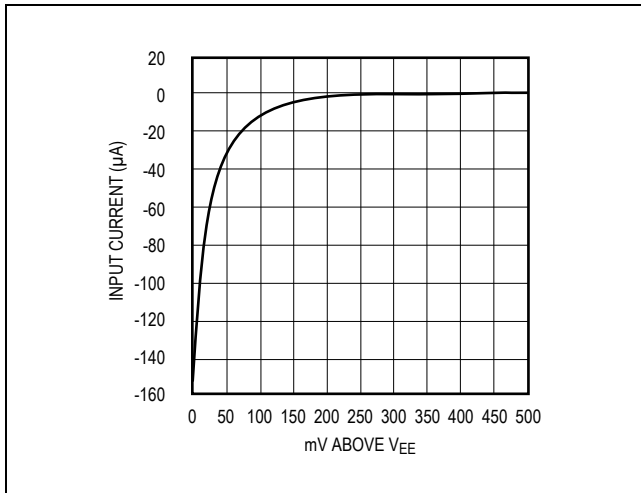


Figure 2. Enable Logic-Low Input Current vs. V_{IL}

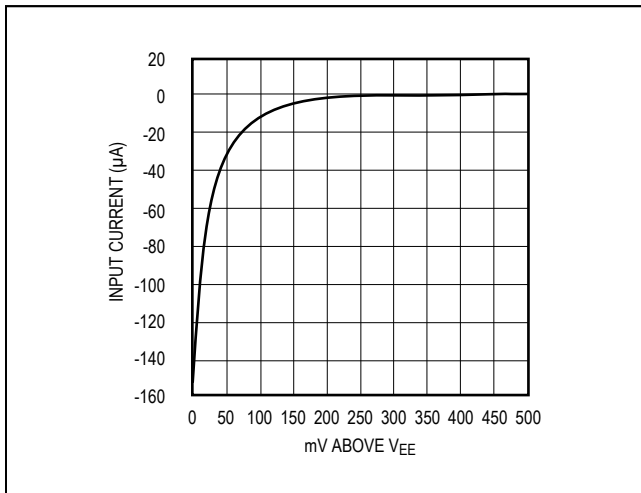


Figure 4. Enable Logic-Low Input Current vs. V_{IL} with 10kΩ Series Resistor

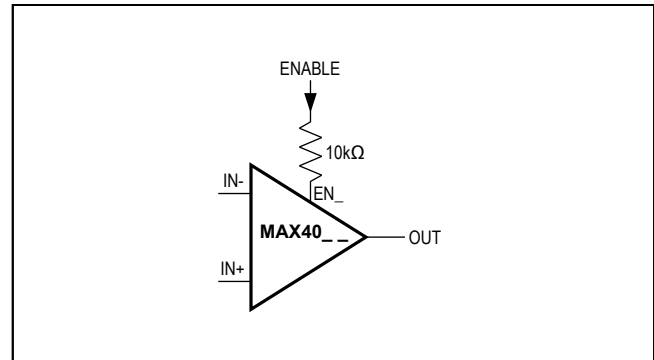


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

To implement the mux function, the outputs of multiple amplifiers can be tied together, and only the amplifier with the selected input will be enabled. All of the other amplifiers will be placed in the low-power shutdown mode, with their high output impedance presenting very little load to the active amplifier output. For gains of +2 or greater, the feedback network impedance of all the amplifiers used in a mux application must be considered when calculating the total load on the active amplifier output.

Output Capacitive Loading and Stability

The MAX4012/MAX4016/MAX4018/MAX4020 are optimized for AC performance. They are not designed to drive highly reactive loads, which decreases phase margin and may produce excessive ringing and oscillation. Figure 5 shows a circuit that eliminates this problem. Figure 6 is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figure 7 shows how a capacitive load causes excessive peaking of the amplifier’s frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 20Ω to 30Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Figure 8 shows the effect of a 27Ω isolation resistor on closed-loop response.

Coaxial cable and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the line’s capacitance.

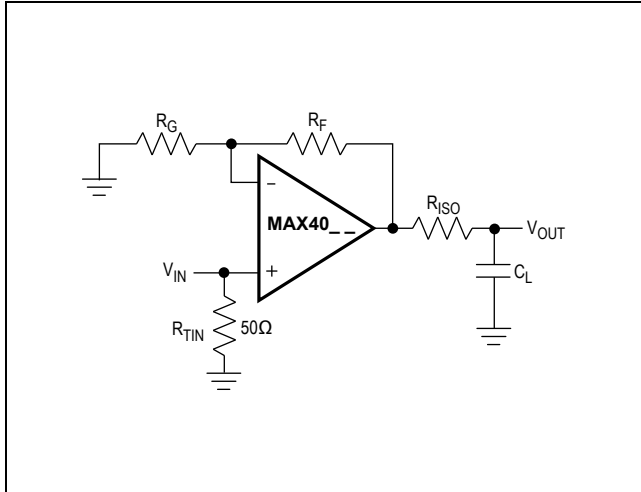


Figure 5. Driving a Capacitive Load through an Isolation Resistor

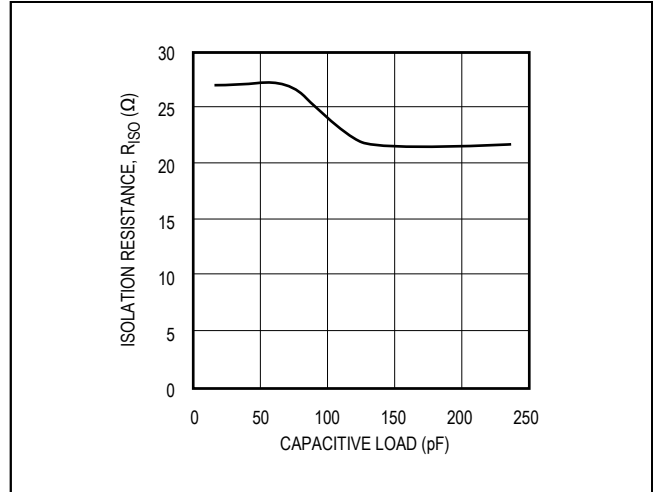


Figure 6. Capacitive Load vs. Isolation Resistance

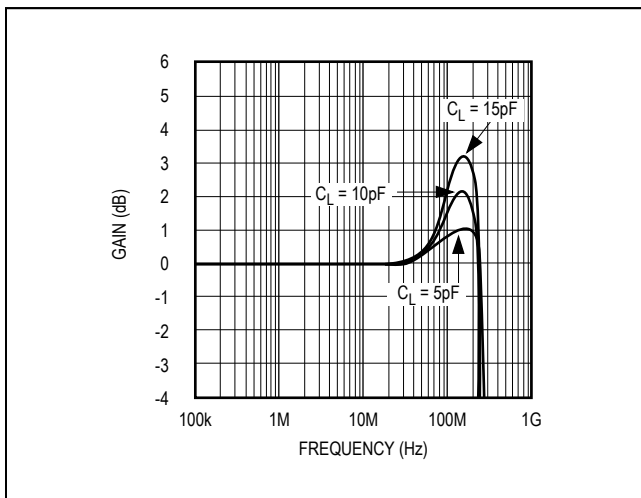


Figure 7. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

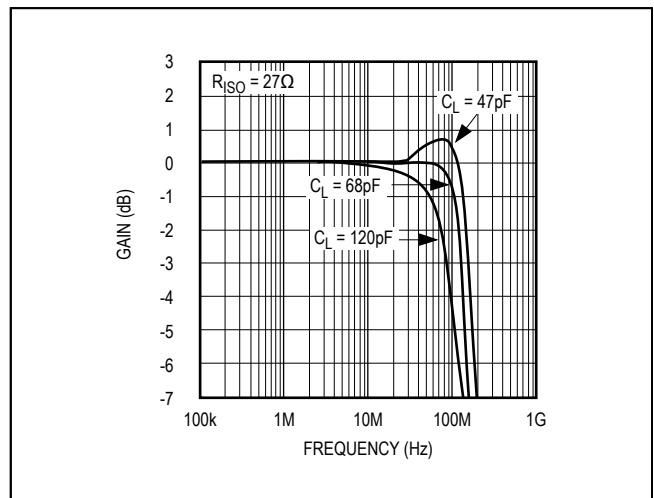
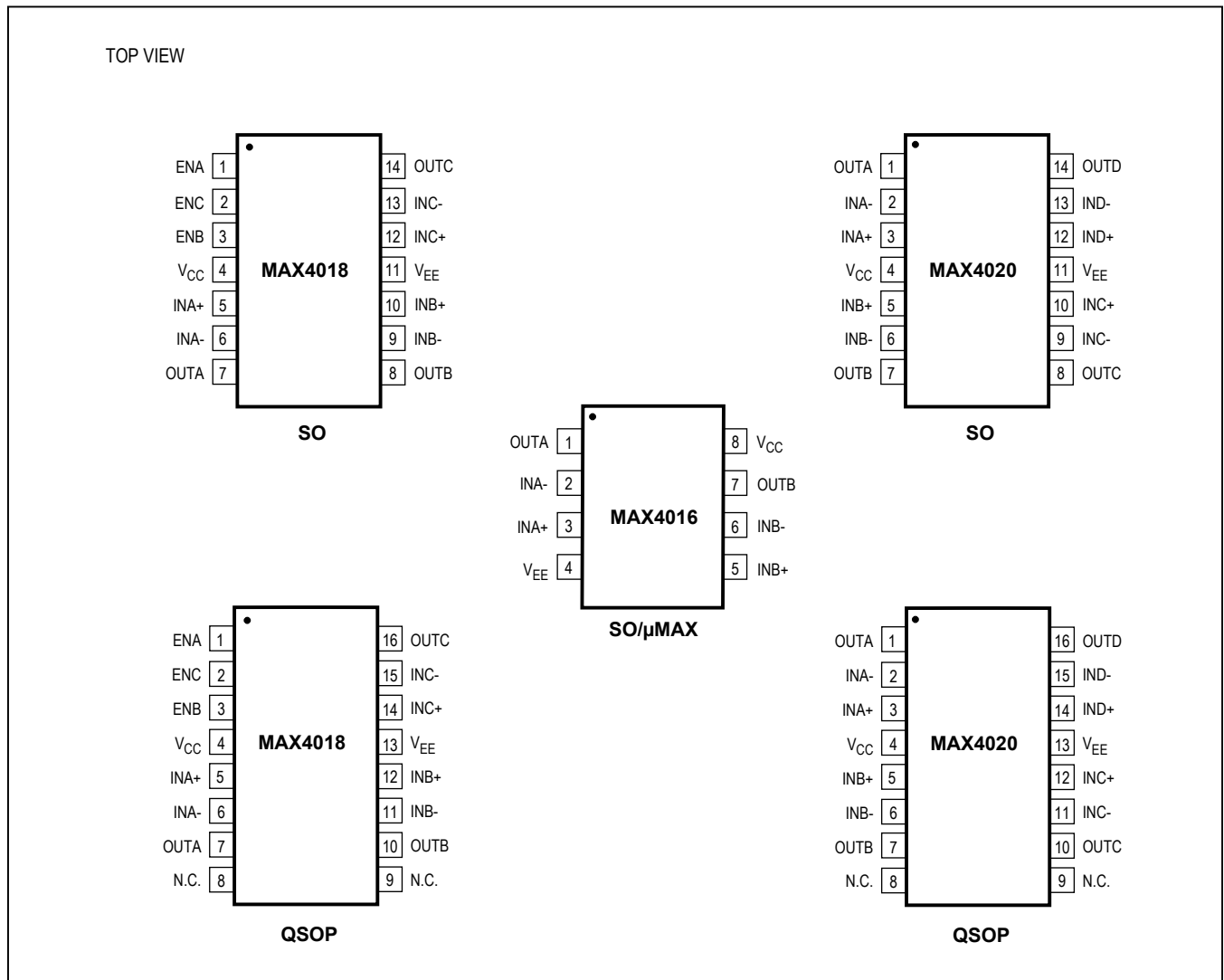


Figure 8. Small-Signal Gain vs. Frequency with Load Capacitance and 27 Ω Isolation Resistor

Pin Configurations (continued)



MAX4012/MAX4016/ MAX4018/MAX4020

Low-Cost, High-Speed, Single-Supply Op Amps with Rail-to-Rail Outputs

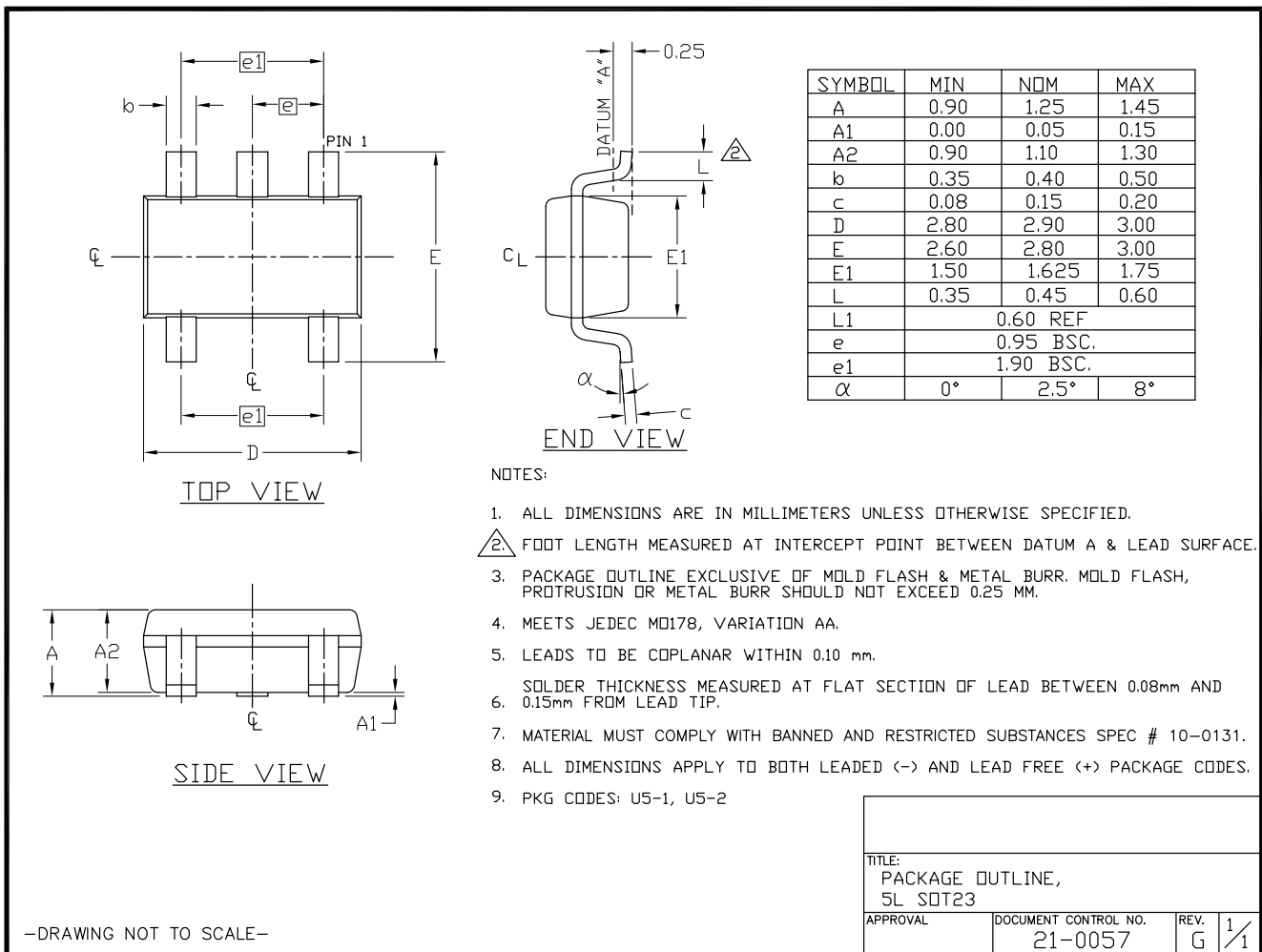
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4018ESD+T	-40°C to +85°C	14 SO	—
MAX4018EEE+T	-40°C to +85°C	16 QSOP	—
MAX4020ESD+T	-40°C to +85°C	14 SO	—
MAX4020EEE+T	-40°C to +85°C	16 QSOP	—

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T Denotes tape-and-reel.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

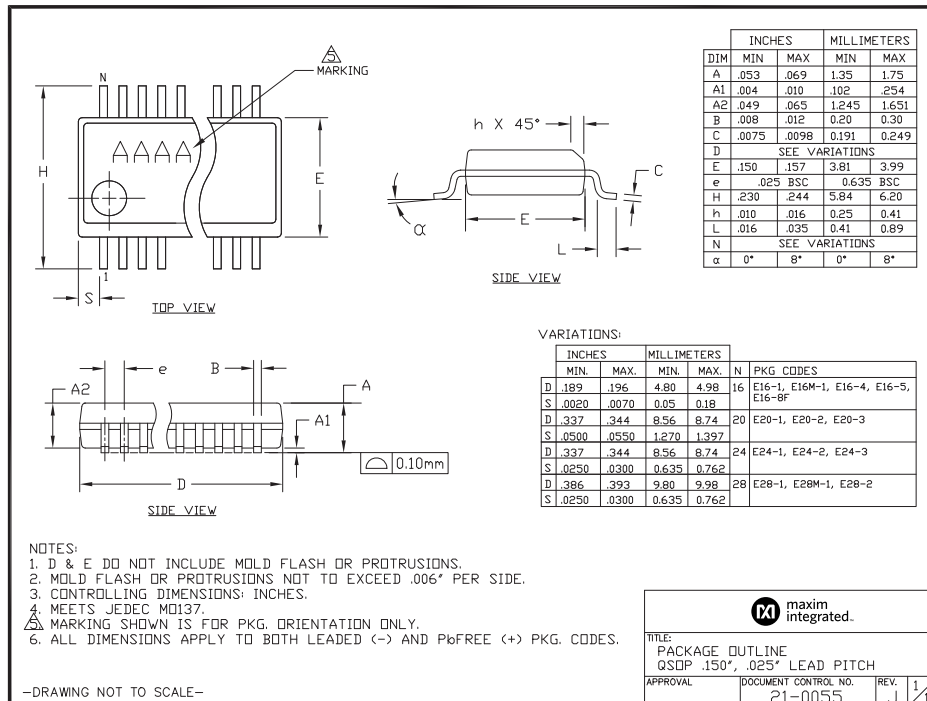
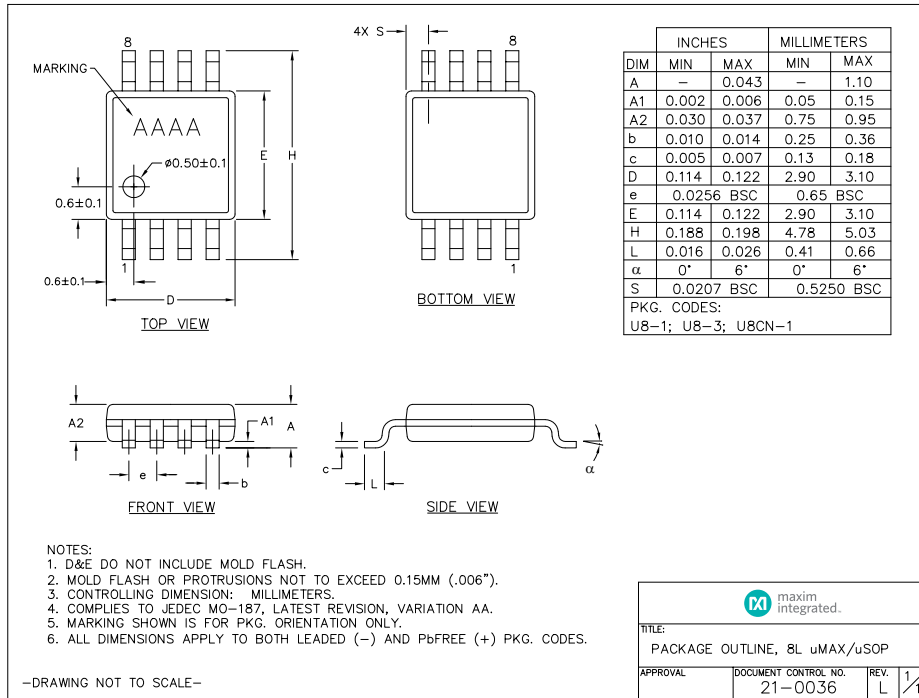


MAX4012/MAX4016/ MAX4018/MAX4020

Low-Cost, High-Speed, Single-Supply Op Amps with Rail-to-Rail Outputs

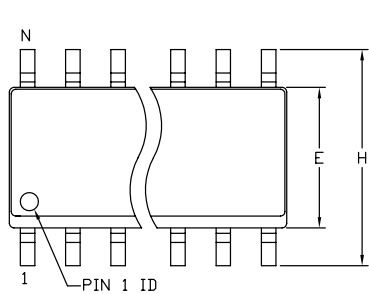
Package Information (continued)

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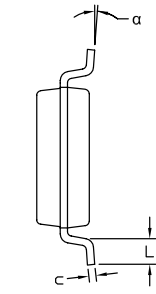


Package Information (continued)

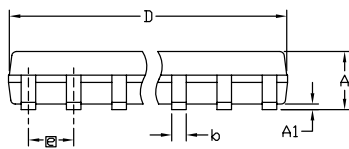
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TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050	BSC	1.27	BSC
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
alpha	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			


VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6; S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F; S16M-3, S16M-6			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-



TITLE:
PACKAGE OUTLINE,
8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO. 21-0041	REV. C	1/1
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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/97	Initial release	—
1	8/01	Updated Electrical Characteristics table	2
2	10/03	Updated Electrical Characteristics table	3
3	8/04	Added 8 SO package	All
4	8/22	Updated Ordering Information table, deleted Chip Information	1, 15



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