



**THE DATASHEET OF  
MADR-009269-000100**



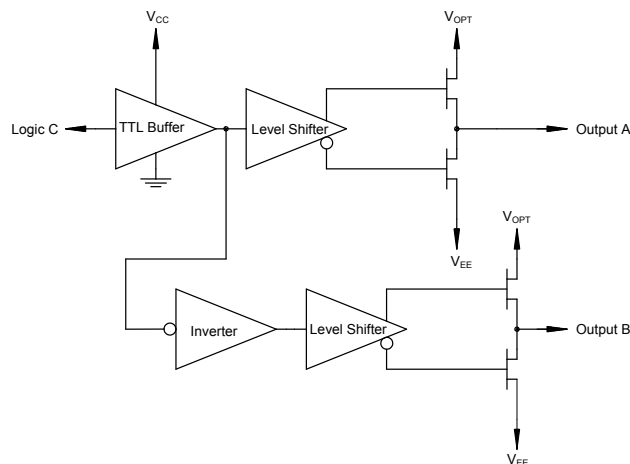
### Features

- High Voltage CMOS Technology
- Complementary Outputs
- Positive Voltage Control
- CMOS device using TTL input levels
- Low Power Dissipation
- Low Cost Plastic SOIC-8 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- RoHS\* Compliant

### Description

The MADR-009269 is a single channel CMOS driver used to translate TTL control inputs into complementary gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to 2 V (relative to GND) to optimize the intermodulation products of FET control devices at low frequencies. For driving PIN diode circuits, the outputs are nominally switched between +5 V & -5 V.

### Functional Schematic



### Pin Configuration<sup>2</sup>

Pin No.	Function
1	Output A
2	GND
3	V <sub>CC</sub>
4	C, Logic
5	V <sub>EE</sub>
6	V <sub>OPT</sub>
7	GND
8	Output B

2. The bottom of the die should be isolated for part number MADR-009269-000DIE and MADR-009269-00GDIE.

### Ordering Information<sup>1</sup>

Part Number	Package
MADR-009269-000100	bulk packaging
MADR-009269-00GDIE	100 piece gel pack
MADR-009269-000DIE	100 piece waffle pack
MADR-009269-0001TR	1000 piece reel

1. Reference Application Note M513 for reel size information.

\* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

## Single Driver for GaAs FET or PIN Diode Switches and Attenuators

Rev. V3

## DC Characteristics over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Units	Min.	Typ.	Max.
V <sub>IH</sub>	Input High Voltage	Guaranteed High Input Voltage	V	2.0	—	—
V <sub>IL</sub>	Input Low Voltage	Guaranteed Low Input Voltage	V	—	—	0.8
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1 mA	V	V <sub>OPT</sub> -0.1	—	—
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +1 mA	V	—	—	V <sub>EE</sub> +0.1
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = min, V <sub>CC</sub> = max, V <sub>OPT</sub> = min or max	μA	-1	—	1
R <sub>NFET</sub>	Output Resistance NFET On (to V <sub>EE</sub> )	V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = -5.0 V, V <sub>OPT</sub> = 5.0 V, V <sub>OUT</sub> = -4.9 V +25°C	Ω	—	30	—
R <sub>PFET</sub>	Output Resistance PFET On (to V <sub>OPT</sub> )	V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = -5.0 V, V <sub>OPT</sub> = 5.0 V, V <sub>OUT</sub> = 4.9 V +25°C	Ω	—	30	—
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = -10.5 V, V <sub>CC</sub> = 5.5 V, V <sub>OPT</sub> = 5.5 V, No Output Load	μA	—	1	—
D I <sub>CC</sub>	Additional Supply Current (per TTL Input pin)	V <sub>CC</sub> = max, V <sub>IN</sub> = V <sub>CC</sub> -2.1 V	mA	—	1	—
I <sub>EE</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = -10.5 V, V <sub>CC</sub> = 5.5 V, V <sub>OPT</sub> = 5.5 V, No Output Load	μA	—	1	—
I <sub>OPT</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>EE</sub> = -10.5 V, V <sub>CC</sub> = 5.5 V, V <sub>OPT</sub> = 5.5 V, No Output Load	μA	—	1	—

AC Characteristics Over Guaranteed Operating Range<sup>3</sup>

Symbol	Parameter	Unit	Typical performance		
			-40°C	+25°C	+85°C
T <sub>PLH</sub>	Propagation Delay	ns	20	22	25
T <sub>PHL</sub>	Propagation Delay	ns	20	22	25
T <sub>TLH</sub>	Output Transition Time (Rising Edge)	ns	5	5	8
T <sub>THL</sub>	Output Transition Time (Falling Edge)	ns	4	4	5
T <sub>skew</sub>	Delay Skew	ns	2.5	2.5	2.5
PRF (max)	50% Duty Cycle	MHz	DC	—	10
C <sub>IN</sub>	Input Capacitance	pF	5	5	5

3. V<sub>CC</sub> = +4.5 V, V<sub>EE</sub> = -4.5 V, V<sub>OPT</sub> = 0 V or +4.5 V, C<sub>L</sub> = 25 pF, T<sub>RISE</sub>, T<sub>FALL</sub> = 6 ns

### Truth Table

Input	Outputs	
C	A	B
Logic "0"	$V_{EE}$	$V_{OPT}$
Logic "1"	$V_{OPT}$	$V_{EE}$

### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

### Guaranteed Operating Ranges<sup>4,5,6</sup>

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{CC}$	Positive DC Supply Voltage	V	4.5	5.0	5.5
$V_{EE}$	Negative DC Supply Voltage	V	-10.5	-5.0	-4.5
$V_{OPT}^{7,8}$	Optional DC Output Supply Voltage	V	0	—	$V_{CC}$
$V_{OPT} - V_{EE}$	Negative Supply Voltage Range	V	4.5	Note 7,8	16.0
$V_{CC} - V_{EE}$	Positive to negative Supply Range	V	9	10	16
$T_{OPER}$	Operating Temperature	°C	-40	+25	+85
$I_{OH}$	DC Output Current - High	mA	-50	—	—
$I_{OL}$	DC Output Current - Low	mA	—	—	50
$T_{RISE}, T_{FALL}$	Maximum Input Rise or Fall Time	ns	—	—	500

4. Unused logic inputs must be tied to either GND or  $V_{CC}$ .
5. MACOM recommends that  $V_{CC}$  be powered on before  $V_{EE}$ , and powered off after  $V_{EE}$ .
6. 0.01  $\mu$ F decoupling capacitors are required on the power supply lines.
7.  $V_{OPT}$  is grounded in most cases when FETs are driven. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies,  $V_{OPT}$  can be increased to between 1 and 2 V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.
8. When this driver is used to drive PIN diodes,  $V_{OPT}$  is often set to +5 V, with  $V_{EE}$  set to -5 V.

Absolute Maximum Ratings<sup>9</sup>

Symbol	Parameter	Unit	Min.	Max.
$V_{CC}$	Positive DC Supply Voltage	V	-0.5	7.0
$I_{CC}$	Positive DC Supply Current ( $-0.5\text{ V} \leq V_{IN} \leq 0.8\text{ V}$ ; $2.0\text{ V} \leq V_{IN} \leq V_{CC} + 0.5\text{ V}$ ; $V_{CC} - V_{IN} \leq 7.0\text{ V}$ )	mA	—	20
$V_{EE}$	Negative DC Supply Voltage	V	-11.0	0.5
$I_{EE}$	Negative DC Supply Current (per output) <sup>10</sup>	mA	-60	—
$V_{OPT}$	Optional DC Output Supply Voltage	V	-0.5	Note 11
$I_{OPT}$	Optional DC Output Supply Current (per output) <sup>10</sup>	mA	—	60
$V_{OPT} - V_{EE}$	Output to Negative Supply Voltage Range	V	-0.5	18.0
$V_{CC} - V_{EE}$	Positive to Negative Supply Voltage Range	V	-0.5	18.0
$V_{IN}$	DC Input Voltage	V	-0.5 Note 12	$V_{CC} + 0.5$
$V_O$	DC Output Voltage	V	$V_{EE} - 0.5$	$V_{OPT} + 0.5$
$P_D$ <sup>13</sup>	Power Dissipation in Still Air	mW	—	500
$T_{OPER}$	Operating Temperature	°C	-55	125
$T_{STG}$	Storage Temperature	°C	-65	150
ESD	ESD Sensitivity	kV	2.0	—

9. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.

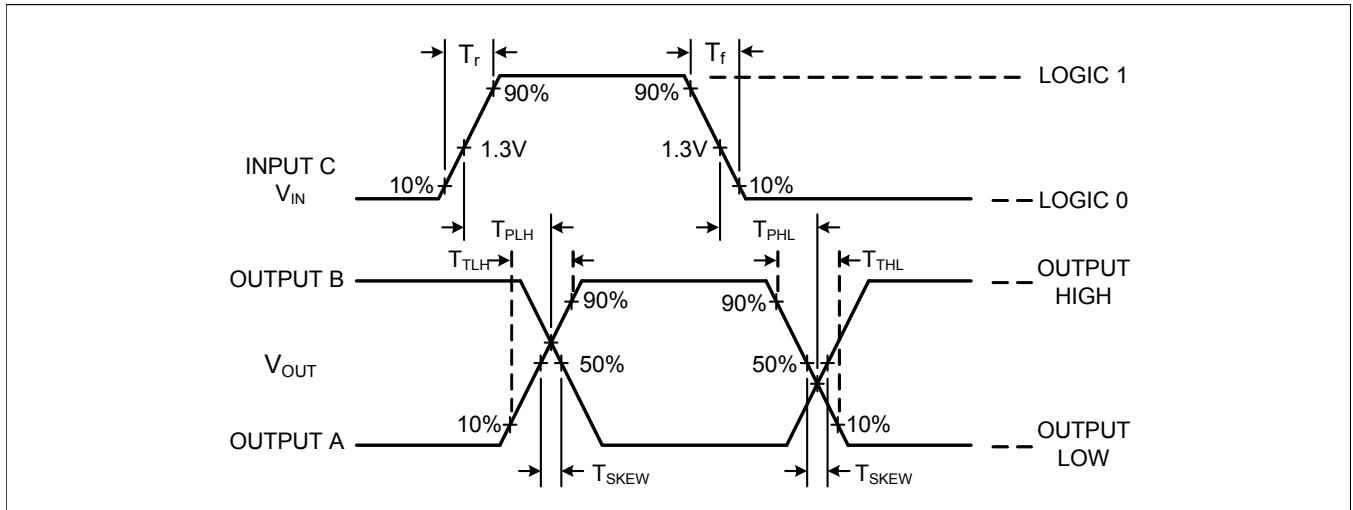
10. The maximum  $I_{EE}$  and  $I_{OPT}$  are specified under the condition of  $V_{CC} = 5.5\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$ ,  $V_{OPT} = 5.5\text{ V}$ , and the total power dissipation is within 500 mW in still air.

11. The absolute maximum rating for  $V_{OPT}$  is  $V_{CC} + 0.5\text{ V}$ , or  $+7.0\text{ V}$ , whichever is less.

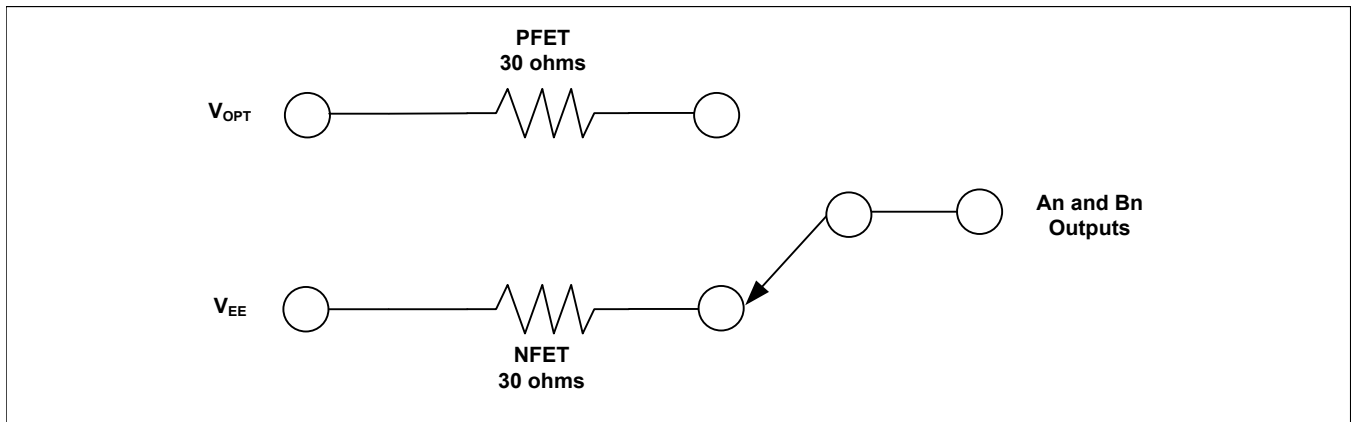
12. If  $V_{CC} \geq 6.5\text{ V}$ , then the minimum for  $V_{IN}$  is  $V_{CC} - 7.0\text{ V}$ .

13. Derate  $-7\text{ mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$ .

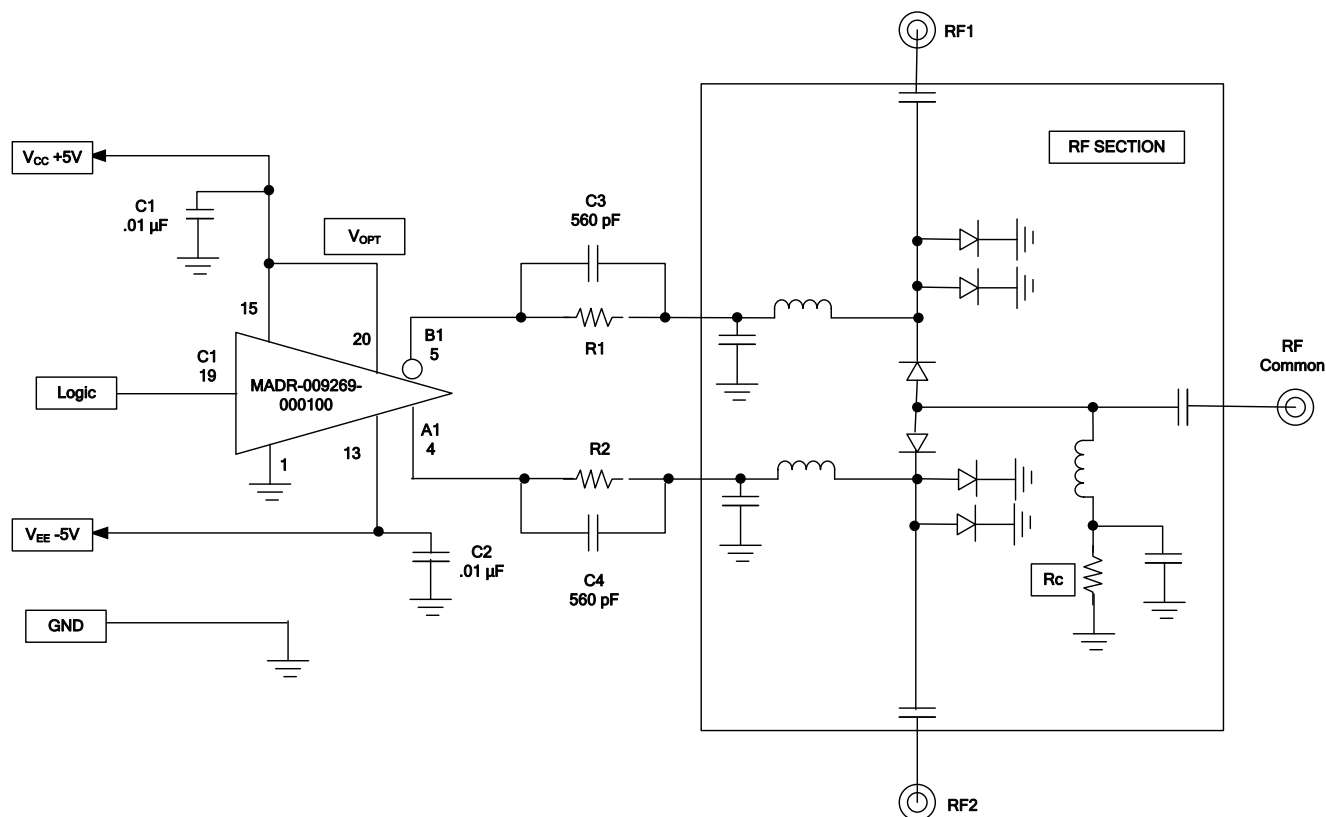
### Switching Waveforms



### Equivalent Output Circuit for A and B Outputs (50 mA load at 25°C)



### Typical Application for a SPDT Switch

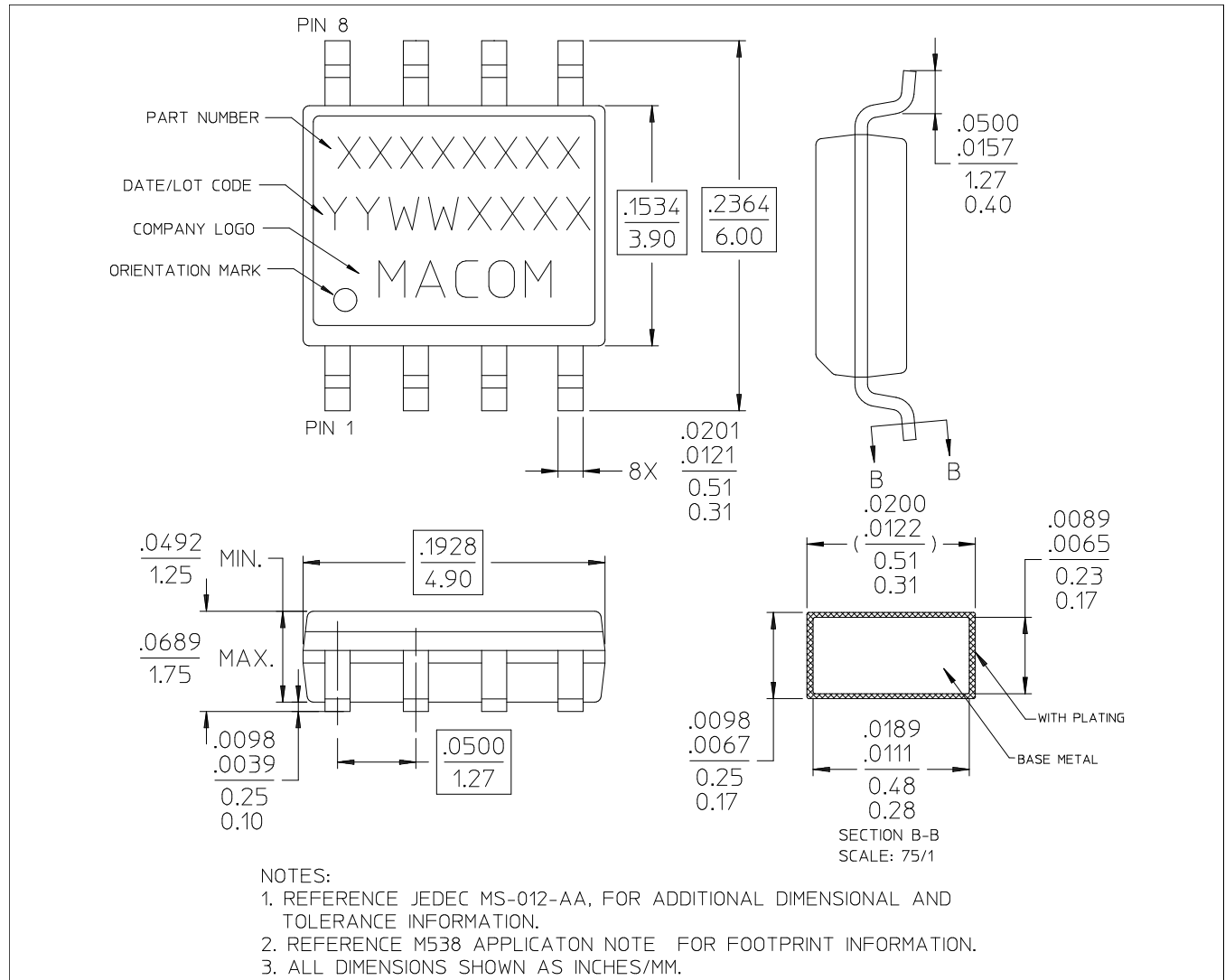


### Description of Circuit

The MADR-009269 provides a pair of complementary outputs that are each capable of driving a maximum of  $\pm 50$  mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), additional spiking current can be achieved.

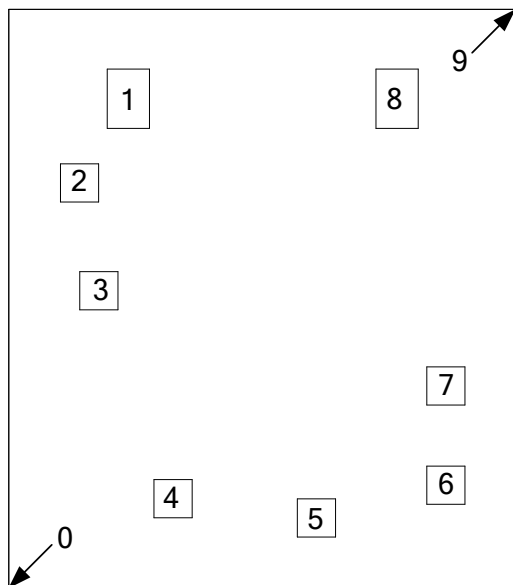
To achieve the non-inverting and inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to  $V_{OPT}$  for the positive output and  $V_{EE}$  for the negative output.  $V_{OPT}$  and  $V_{EE}$  are adjustable for various configurations and have the following limitations:  $V_{EE}$  can be no more negative than -10.5 volts;  $V_{OPT}$  can be no more positive than +5.5 volts and  $V_{OPT}$  must always be less than or equal to  $V_{CC}$ . Increasing  $V_{OPT}$  beyond  $V_{CC}$  will prevent the device from switching states when commanded to by the logic input. The most common configuration is to drive  $V_{EE}$  at -5.0 volts with  $V_{CC}$  and  $V_{OPT}$  tied together at +5.0 volts.

### Lead-Free, SOIC-8<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations. Plating is 100% matte tin over copper.

### Die Outline



### Pad Configuration<sup>14,15</sup>

Die Size: 1130 x 1290  $\mu\text{m}$  (nominal)

Pad No.	X ( $\mu\text{m}$ ) nominal	Y ( $\mu\text{m}$ ) nominal	Pad Size ( $\mu\text{m}$ ) X x Y
0	0	0	Lower left edge of die
1	266.40	1092.35	94 x 132
2	157.50	903.70	85 x 85
3	200.40	663.65	85 x 85
4	365.30	200.45	85 x 85
5	684.35	157.50	85 x 85
6	972.50	230.50	85 x 85
7	972.50	451.45	85 x 85
8	863.60	1092.35	94 x 132
9	1130	1290	Upper right edge of die

- 14. All X,Y dimensions are at bond pad center.
- 15. Die thickness is 8.0 mils.

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