THE DATASHEET OF

LYT6068C-TL

LYTSwitch-6 Family

Flyback CV/CC LED Driver IC with Integrated High-Voltage Switch and FluxLink Feedback

Product Highlights

Highly Integrated, Compact Footprint

- Up to 94% efficiency across full load range
- Incorporates a multi-mode Quasi-Resonant (QR) / CCM / DCM flyback controller, high-voltage switch, secondary-side control and synchronous rectification driver
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Exceptional CV/CC accuracy, independent of transformer design or external components
- Adjustable accurate output current sense using external sense resistor
- PowiGaN™ technology – up to 100 W without heat sinks (LYT6079C and LYT6070C)

EcoSmart™ – Energy Efficient

- Less than 30 mW no-load including line sense (without PF front end)
- Designs using LYTSwitch-6 easily meet Energy Star and all global lighting energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Input line OV with auto-restart
- Output fault OVP/UVP with auto-restart
- Open SR FET gate detection
- Input voltage monitor with accurate brown-in
- Thermal foldback ensures that power continues to be delivered (lower level) at elevated temperatures

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 and TUV (EN60950 and EN62368) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- Isolated off-line LED driver
- Smart LED lighting
- High-voltage flyback post regulator

Description

The LYTSwitch™-6 series family of ICs dramatically simplifies the development and manufacturing of off-line LED drivers, particularly those in compact enclosures or with high efficiency requirements. The LYTSwitch-6 architecture is revolutionary in that the devices incorporate both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link, FluxLink, permit accurate control of a secondary-side synchronous rectification MOSFET with Quasi-Resonant switching of primary integrated high-voltage switch to maintain high efficiency across the entire load range.

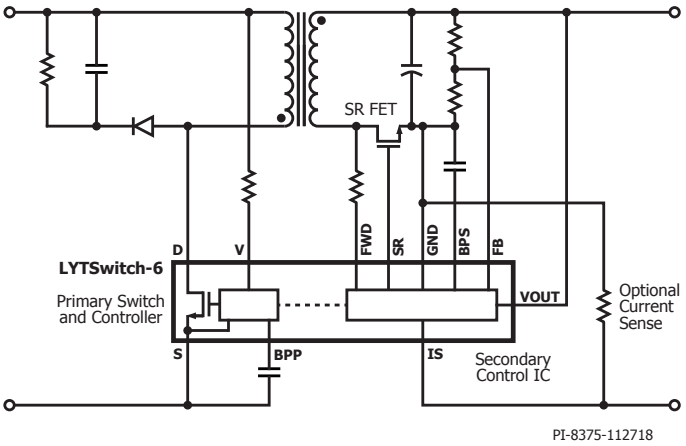


Figure 1. Typical Application/Performance.

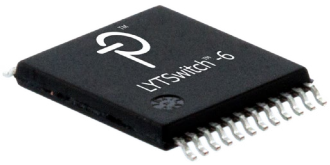


Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table

Product[2,3]	277 VAC ± 15%	85-305 VAC	380 VDC / 450 VDC[2]
	Open Frame[1]	**Open Frame[1]**	**Open Frame[1]**
LYT6063C/6073C	15 W	12 W	25 W
LYT6065C/6075C	30 W	25 W	40 W
LYT6067C/6077C	50 W	45 W	60 W
LYT6068C	65 W	55 W	
Product[2]	750 V PowiGaN Switch		
LYT6078C	75 W	65 W	90 W
LYT6079C	85 W	75 W	100 W
LYT6070C	95 W	85 W	110 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated and PCB size measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Package: InSOP-24D.
3. LYT606x – 650 V MOSFET, LYT607x – 725 V MOSFET.

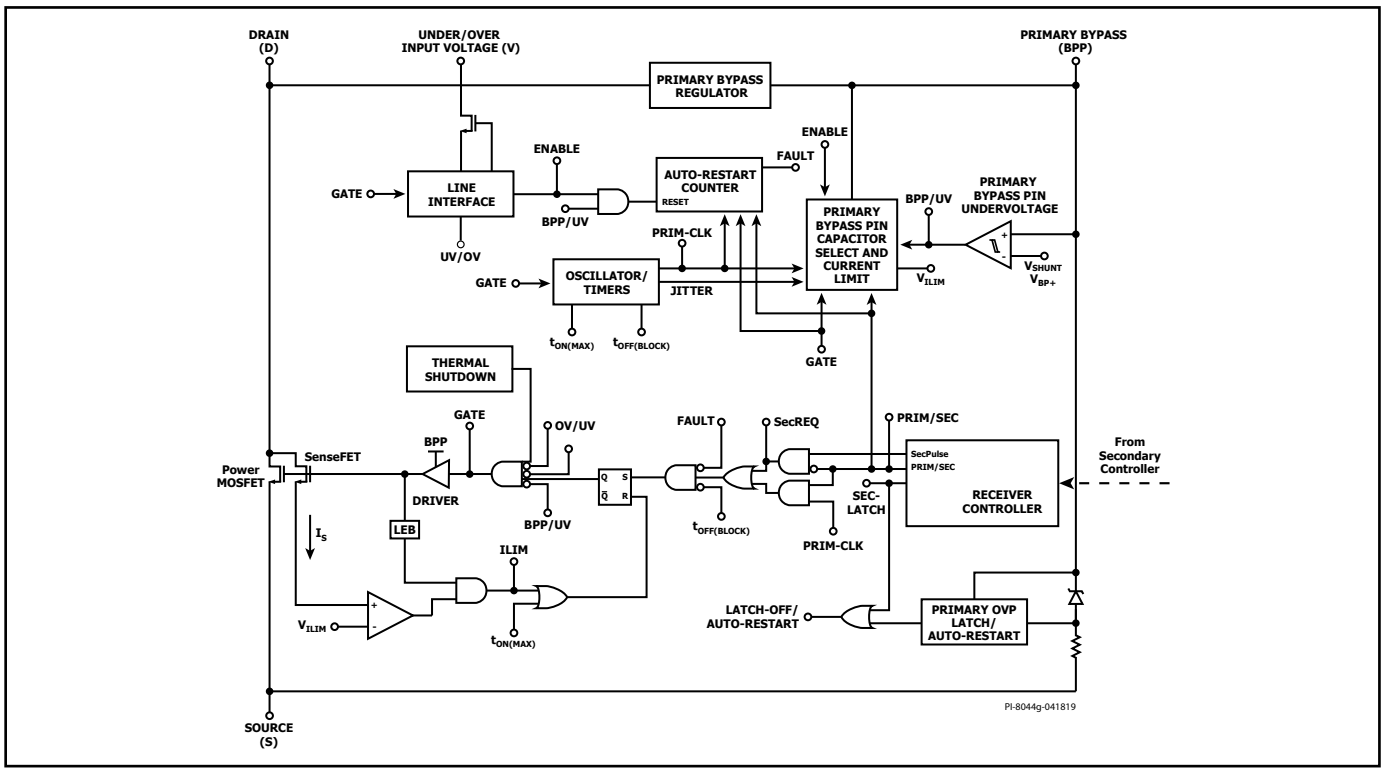


Figure 3. Primary Controller Block Diagram.

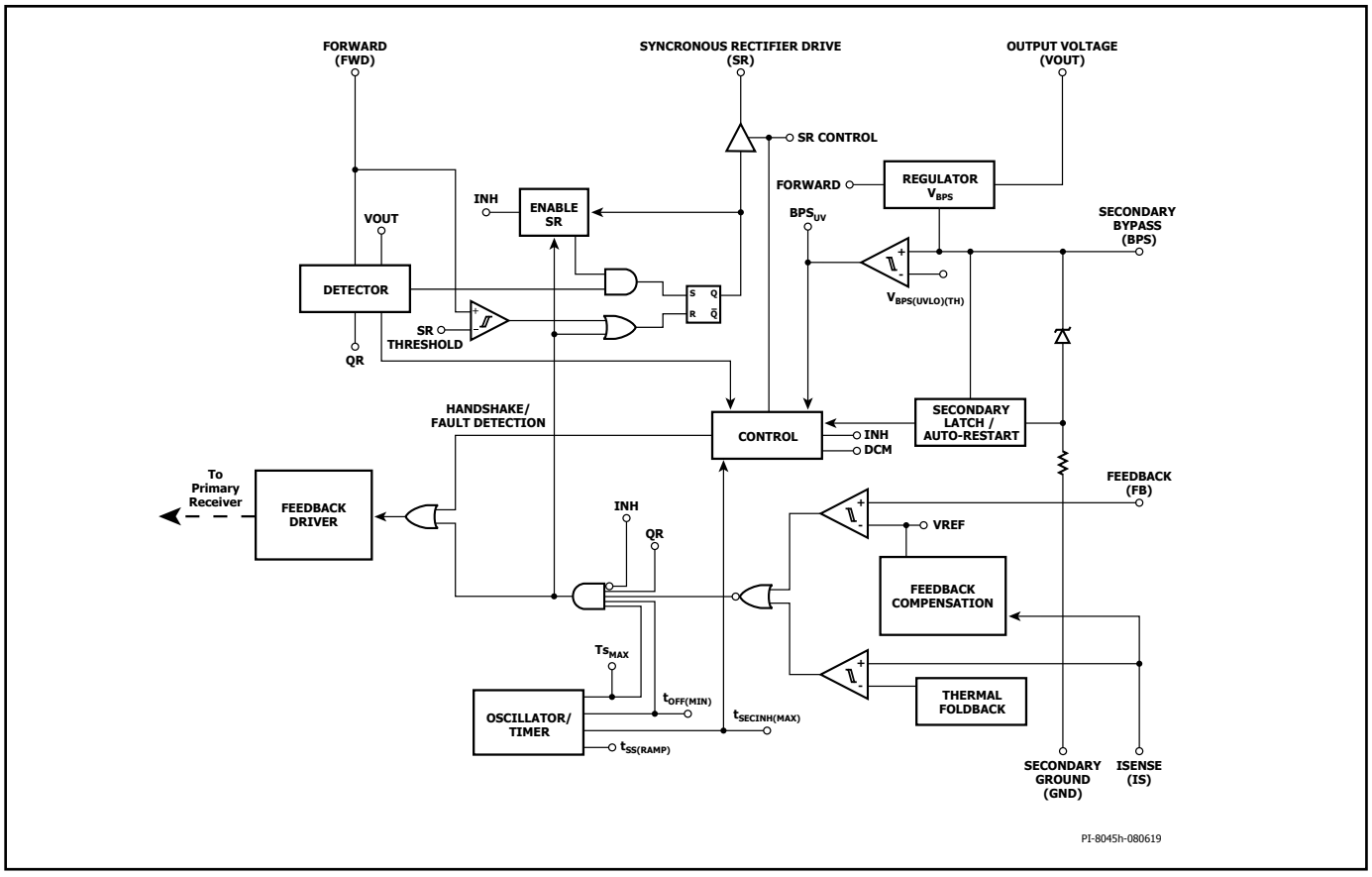


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
Connected directly to the output voltage to provide current for the controller on the secondary-side.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing. Provides power for the secondary-side controller when V_{OUT} is below a threshold.

NC Pin (Pin 8-12)
Leave open. Should not be connected to any other pins.

Input Overvoltage (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting overvoltage conditions at the power supply input. This pin should be tied to Source to disable OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch drain connection.

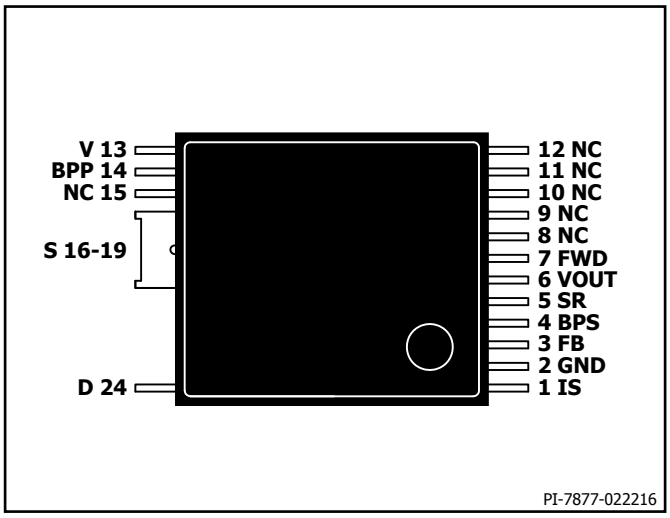


Figure 5. Pin Configuration.

LYTSwitch-6 Functional Description

The LYTSwitch-6 combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to communicate accurate direct sensing of the output voltage and output current on the secondary controller to the primary controller.

LYTSwitch-6 is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, and a 650 V, 725 V or 750 V power switch.

The LYTSwitch-6 secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the secondary SECONDARY BYPASS pin, synchronous rectifier MOSFET driver, QR mode circuit, oscillator and timing functions, thermal foldback control and a host of integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

The LYTSwitch-6 features variable frequency QR controller + CCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the voltage on the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, there is a shunt regulator clamping the PRIMARY BYPASS pin voltage to V_{SHUNT} when the current is provided to the PRIMARY BYPASS pin through an external resistor. This facilitates powering the LYTSwitch-6 externally through a bias winding to decrease the no-load consumption to less than 30 mW.

Primary Bypass ILIM Programming

LYTSwitch-6 has user programmable current limit (ILIM) settings through the selection of PRIMARY BYPASS pin capacitor value. The PRIMARY BYPASS pin can use a ceramic capacitor for decoupling the internal supply of the device.

There are (2) programmable settings using 0.47 µF and 4.7 µF for standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power Switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise back to V_{SHUNT} to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Auto-Restart Function

The PRIMARY BYPASS pin has an OV protection auto-restart feature. A Zener diode in parallel to the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding to activate this protection mechanism. In the event the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will disable the power switch switching for a time $t_{AR(OFF)}$. After this time the controller will restart operation and attempt to return to regulation.

This VOUT OV protection is also available as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is typically set to T_{SD} with $T_{SD(H)}$ hysteresis. When the die temperature rises above this threshold the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point it is re-enabled. A large hysteresis of $T_{SD(H)}$ is provided to prevent over-heating of the PCB due to continuous fault condition.

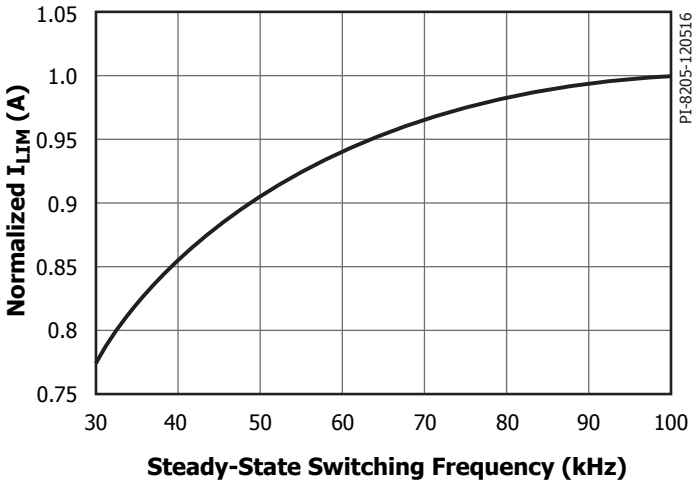


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is inversely proportional to time from the end of the last primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

The characteristic produces a primary current limit that increases as the load increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with immediate response when a feedback switching cycle request is received.

At high load, switching cycle have a maximum current approaching 100% ILIM gradually reduced to 30% of the full current limit as the load reduces. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise) but the time between switching cycles will continue to increase as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs such as an output overload, output short-circuit, or external component/pin fault, the LYTSwitch-6 enters into auto-restart (AR) operation. In auto-restart the power switch switching is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 80 ms.
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second was included to ensure that if communication is lost, the primary tries to restart again. Although this should never be the case in normal operation, this can be useful in the case of system ESD events for example where a loss of communication due to noise disturbing the secondary controller, the issue is resolved when the primary restarts after an auto-restart off time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event there are two consecutive cycles where the ILIM is reached within the blanking time and current limit delay time (including leading edge current spike ~500 ns), the controller will skip approximately 2.5 cycles or ~25 μs (based on full frequency of 100 kHz). This provides sufficient time for reset of the transformer during start-up into large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The INPUT OVERVOLTAGE pin is used for input overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the INPUT OVERVOLTAGE pin to enable this functionality. This pin functionality can be disabled by shorting INPUT OVERVOLTAGE pin to primary Source.

Primary/Secondary-Side Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default into a start-up condition and attempt to detect handshake pulses from the secondary.

If the secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of SF FET while the primary is switching.

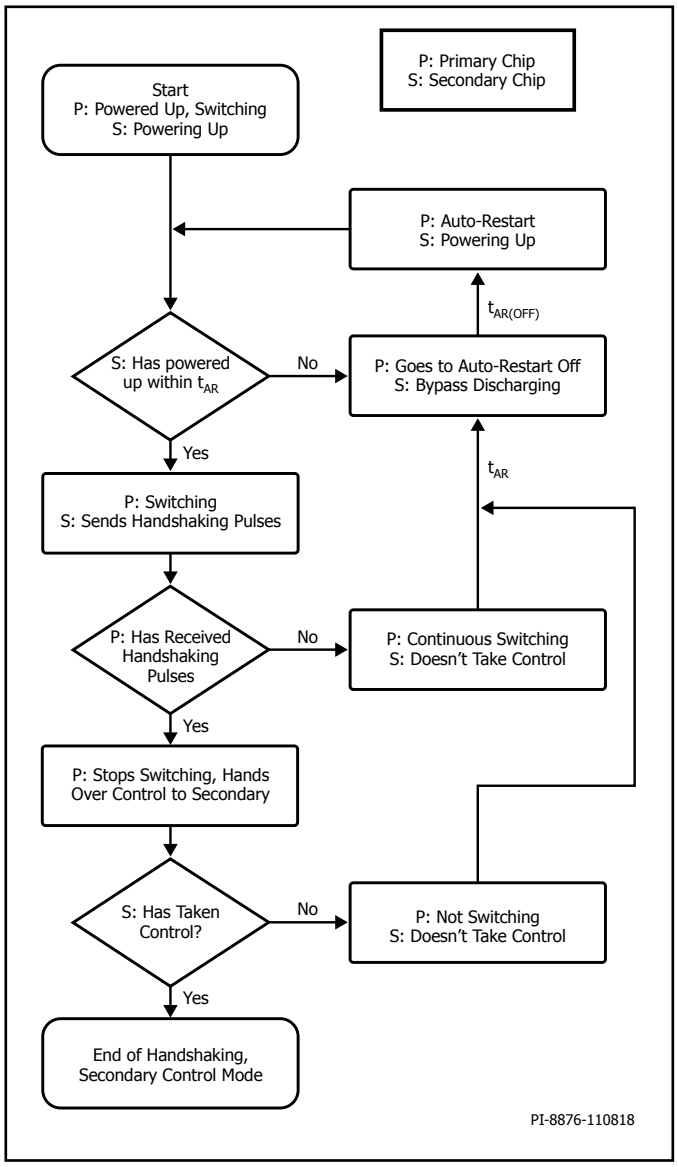


Figure 7. Primary-Secondary Handshake Flow Chart.

This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from input line voltage fault or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by 30 µs, the primary will enter secondary control and begins switching in slave mode. If no such pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine
The LYTSwitch-6 features and active audible noise reduction mode wherein the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 5 kHz and 12 kHz – 200 µs and 83 µs period respectively. If a secondary controller request occur within this window from the last conduction cycle, the gate drive of the power switch is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered through regulator 4.4 V (V_{BPS}) by either VOUT or FW. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SF FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SF FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off when the feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of the any overlap for the FET turn-off.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{REF} (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins to regulate the output current in constant current regulator mode.

Minimum Off-Time
The secondary controller initiates cycle request using the inductive connection to the primary. The maximum frequency of the secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after the primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ($V_{FB(OFF)}$) until the end of the soft-start ($t_{SS(RAMP)}$) timer. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will regulate directly into CC (constant-current mode). The device will go into auto-restart (AR), if the output voltage does not rise above the $V_{O(AR)}$ threshold before the expiration of the V_{OUT} AR timer ($t_{FB(AR)}$) after handshake has occurred.

The secondary controller enables the FEEDBACK pin short protection mode ($V_{FB(OFF)}$) at the end of the $t_{SS(RAMP)}$ time period. If the output short maintains the FEEDBACK pin to be below short-circuit threshold the secondary will stop requesting pulses to trigger an auto-restart cycle.

If output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary-cycle requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Thermal Foldback
When the secondary controller die temperature reaches 124 °C, the output power is reduced by reducing the constant current reference threshold (see Figure 8).

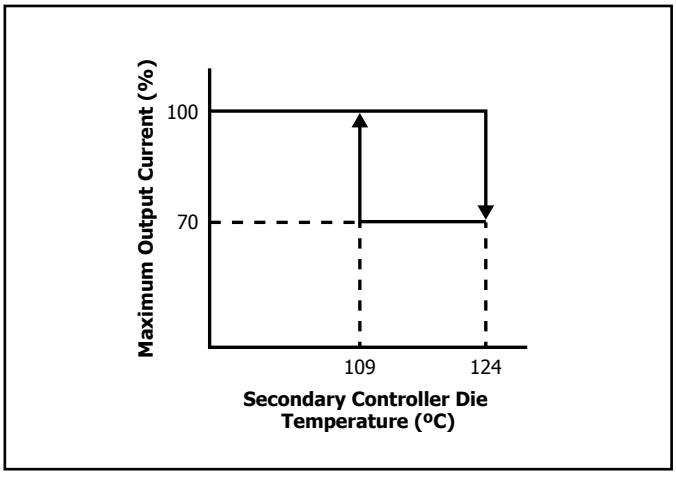


Figure 8. Maximum Output Current vs. Secondary Die Temperature.

Output Voltage Protection
In the event the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA in the event the FEEDBACK pin voltage is raised to beyond ~10% (strong bleed) of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage for momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to begin an auto-restart sequence. This integrated V_{OUT} OVP can be used independently from the primary sensed OVP or in conjunction.

FEEDBACK Pin Short Detection
If the sensed FEEDBACK pin voltage is below $V_{FB(OFF)}$ at start-up, the secondary controller will complete the handshake to take control of the primary complete $t_{SS(RAMP)}$ and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below $V_{FB(OFF)}$ threshold. The deglitch filter on the protection mode is less than 10 µs. By this mechanism, the secondary will relinquish control after detecting the FEEDBACK pin is shorted to ground.

Auto-Restart Thresholds
The OUTPUT VOLTAGE pin includes a comparator to detect when the output voltage falls below $V_{VO(AR)}$ of V_{VO}, for a duration exceeding $t_{VOUT(AR)}$. The secondary controller will relinquish control when this fault condition is sensed. This threshold is meant to limit the range of constant current (CC) operation.

SECONDARY BYPASS Overvoltage Protection
The LYTSwitch-6 secondary controller features SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control: in the event the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ (~7 mA) the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$) event.

Output Constant Current
The LYTSwitch-6 regulates the output current through an external current sense resistor between the ISENSE and SECONDARY GROUND pins where the voltage generated across the resistor is compared to internal of $I_{SV(TH)}$ (~35 mV). If constant current regulation is not required, the ISENSE pin must be tied to SECONDARY GROUND pin.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and discharge any voltage accumulation on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
The secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external MOSFET to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault. At start-up the controller will sink a current from the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF (the resulting voltage is below the reference voltage), the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected to be above 100 pF (the resulting voltage is above the reference voltage), the controller will assume an SR FET is populated.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses to the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the LYTSwitch-6 features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation automatically engages in DCM and disabled once the converter moves to continuous-conduction mode (CCM).

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary request to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-Resonant (QR) mode is enabled for 20 µsec after DCM is detected or ring amplitude (pk-pk) >2 V. Afterward QR switching is disabled, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

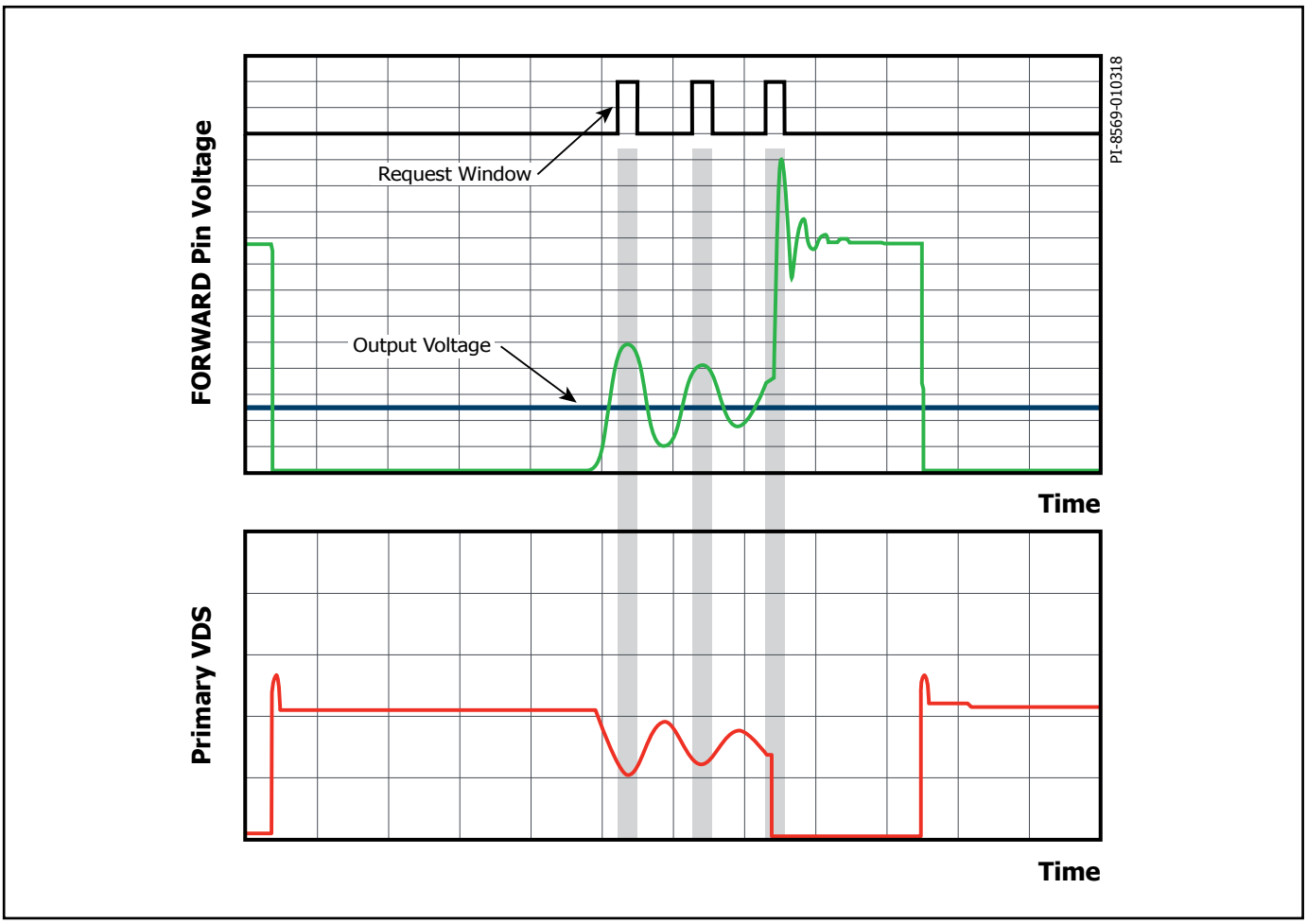


Figure 9. Intelligent Quasi-Resonant Mode Switching.

Application Example

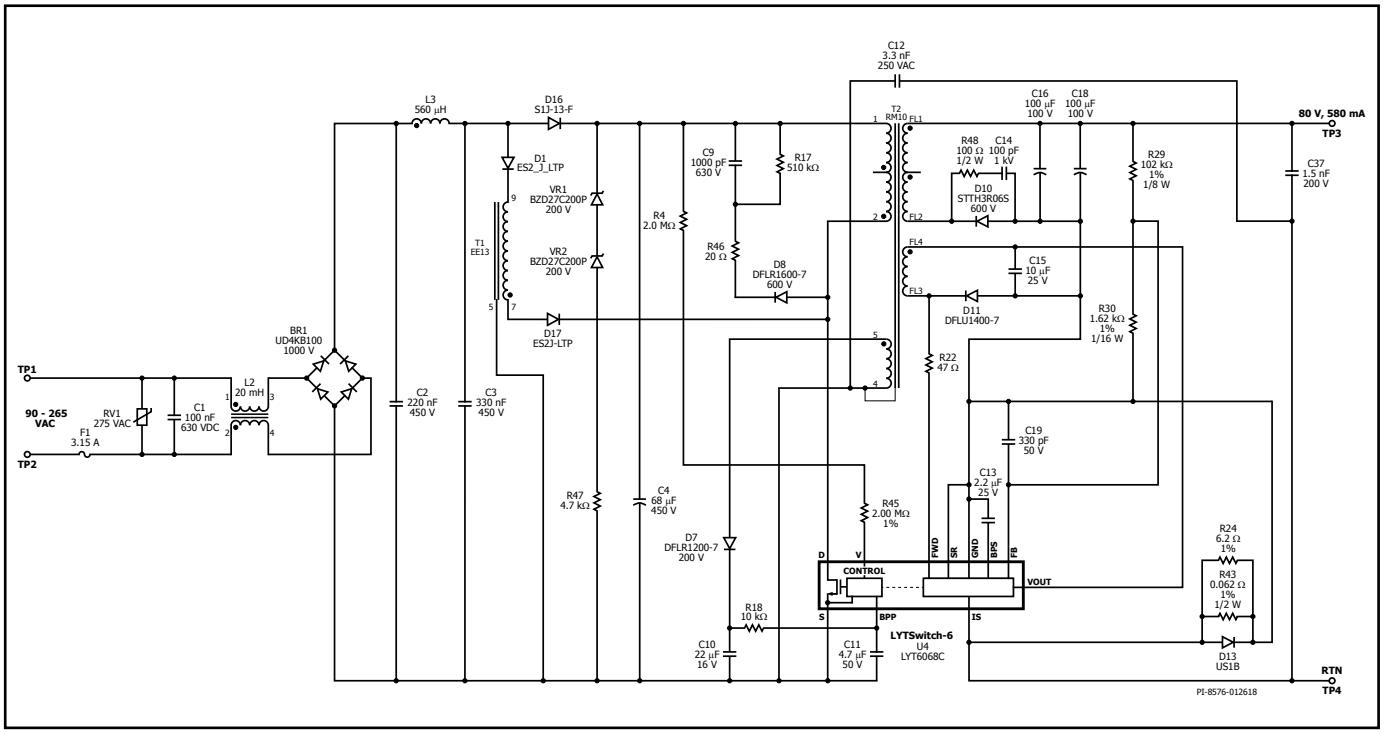


Figure 10. Schematic DER-657, 46.4 W, 80 V, 0.58 A for Universal External LED Driver Application.

The circuit shown on Figure 10 is a 46 W isolated flyback power supply with a single-stage power factor correction circuit for LED lighting applications. It provides an accurately regulated 80 V, 580 mA output for multi-LED-string applications where a post regulator is used – such as in RGBW smart-lighting fixtures. The design is also ideal for single string applications as it also provides a constant 580 mA output current with accurate regulation and no line-induced ripple across a load-voltage range of 80 V to 20 V. The circuit is highly efficient offering accurate load regulation and is stable over line (90 VAC to 265 VAC). The circuit also delivers a PF of greater than 0.9 with less than 20% A-THD (measured at 230 VAC).

Input Stage

Fuse F1 provides open-circuit protection which isolates the circuit from the input line in the event of catastrophic component failures. Varistor RV1 clamps any voltage spikes to protect the circuitry located after the fuse from damage due to overvoltage caused by a line transient or surge. Bridge diode BR1 rectifies the AC line voltage and provides a full-wave rectified DC voltage across the input film capacitors C2 and C3. The EMI filter is a 2-stage LC circuit comprising C1, L2, C2, L3, and C3 and suppress differential and common mode noise generated from the PFC and flyback switching stages.

Primary Flyback Stage

The bulk capacitor C4 completes the input stage. It filters the line ripple voltage and provides energy storage. This component also filters differential current, further reducing conducted EMI. The input stage provides a DC voltage to the flyback converter. One end of the primary winding of transformer (T2) is connected to the positive terminal of the bulk capacitor (C4) while the other is connected to the DRAIN pin of the integrated 650 V power switch in the LYTSwitch-6 IC (U1). A low-cost RCD primary clamp made up of D8, R46, R17 and C9 limits the voltage spike developed across the switch that is caused by the transformer leakage inductance. The RCD primary clamp also reduces radiated and conducted EMI.

In order to provide line overvoltage detection, the bulk capacitor voltage is sensed and converted into a current by the INPUT VOLTAGE pin resistors R4 and R45. The INPUT VOLTAGE pin line overvoltage threshold current (I_{OV-}) determines the input overvoltage shutdown point.

The LYTSwitch-6 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C11) when AC is first applied. During normal operation the primary-side circuitry is powered from an auxiliary winding on transformer T2. A value of 4.7 µF was selected for the BPP capacitor (C11) to select increased-current-limit operation. During normal operation the output of the auxiliary (bias) winding is rectified using diode D7 and filtered using capacitor C10. Resistor R18 limits the current being supplied to the PRIMARY BYPASS pin.

Power Factor Correction Stage

The Power Factor Correction circuit comprises an inductor (T1) in series with blocking diodes (D1 and D17) and is connected to the DRAIN pin of the LYTSwitch-6 IC. High PF is achieved using a Switched Valley-Fill Single Stage PFC (SVF S^2PFC) circuit operating in discontinuous conduction mode (DCM). In DCM the switched current from inductor T1 shapes the input current waveform to create a quasi-sinusoid when the rectified voltage on C3 is less than the DC voltage on C4, this results in a high power factor.

During switch on-time, energy is stored in the PFC inductor (T1) and the leakage inductance of the flyback transformer (T2). During switch off-time, the energy from both the PFC and flyback inductors is transferred to the secondary-side through the flyback transformer T2. Diode D16 isolates the rectified AC input on C3 from C4 and

provides current path for the charging of the bulk capacitor C4 – especially at low-line, which improves efficiency. Free-wheel diodes D1 and D17 provide a current path for the energy stored in the PFC inductor that must be transferred to the secondary-side during switch off-time. The series connection of D1 and D17 are able to withstand the resonant voltage ring from the PFC inductor when the switch turns off.

During a no-load or light load condition (<10% load) the energy stored in the PFC inductor is greater than required by the secondary load. The excess energy from the PFC inductor is therefore recycled to the bulk capacitor C4 boosting the voltage level. A Zener-resistor clamp comprising of VR1 and VR2 in series with R47 is connected across the bulk capacitor C4 to clamp this voltage below the voltage-rating of C4. This Zener clamp voltage should be ≤450 V (the maximum voltage rating of bulk capacitor C4). In the event of an input line surge or transient event, the primary switch is protected from overvoltage by the INPUT VOLTAGE pin sense resistors which trigger a line overvoltage shutdown at 460 V.

Secondary Stage

The secondary-side control of the LYTSwitch-6 IC provides constant output voltage and constant output current. The voltage produced on the secondary winding of transformer T2 is rectified by D10 and filtered by the output capacitors C16 and C18. Adding an RC snubber (R48 and C14) across the output diode reduces voltage stress. In this design, the SYNCHRONOUS RECTIFIER DRIVE pin is connected to the SECONDARY GROUND pin to allow the use of a low-cost ultrafast output diode instead of an SR FET.

The IC secondary is self-powered from either the secondary winding forward voltage via the FORWARD pin, or the output voltage via the OUTPUT VOLTAGE pin. Decoupling capacitor C13 is connected to the SECONDARY BYPASS pin. In order to meet the maximum voltage limits of OUTPUT VOLTAGE pin in this design, the secondary-side of the IC needs to be powered from a low voltage auxiliary supply (winding FL3 and FL4). The FORWARD pin has to be connected to the same output to insure good regulation and high efficiency. This auxiliary supply is rectified and filtered by D11 and C15 respectively.

During constant voltage operation, output voltage regulation is achieved by sensing the output voltage via a resistor network comprising R29 and R30. The voltage across R30 is monitored at the FEEDBACK pin and compared to an internal reference voltage threshold of 1.265 V. Bypass capacitor C19 is placed across the FEEDBACK and SECONDARY GROUND pins to attenuate high frequency noise that would otherwise couple to the feedback signal and cause unwanted behavior such as pulse bunching.

During constant current operation, the maximum output current is set by the sense resistors R43 and R24. The voltage across the sense resistor is applied to the ISENSE pin internal reference threshold of 35 mV to maintain constant current regulation. Diode D13 in parallel with the current sense resistors clamps the voltage across the ISENSE and SECONDARY GROUND pin. This shunts the high current surge from the output capacitor seen during an output short-circuit and prevents damage.

Key Applications Design Considerations

Output Power Table

The output power table (Table 1) represents the maximum continuous output power level that can be obtained under the following conditions:

1. Minimum DC input voltage is ≥90 V for 85 VAC input and ≥220 V for 230 VAC input (or 115 VAC with a voltage doubler). The voltage rating of the input capacitor should be set to meet these criteria.
2. Efficiency assumptions depend on power level. Smallest device power levels assume efficiency >84% increasing to >89% for the largest device.
3. Transformer primary inductance tolerance is ±10%.
4. Reflected output voltage (VOR) is set to maintain KP = 0.8 at minimum input voltage for universal line, and KP = 1 for high input line (only) designs.
5. Maximum conduction loss for adapters is limited to 0.6 W and to 0.8 W for open frame designs.
6. Increased current limit is selected for peak and open-frame power columns, while standard current limit is used for adapter columns.
7. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature ≤110 °C.
8. Ambient temperature limit is 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, KP is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient KP limit of ≥0.6 is specified. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.
10. LYTSwitch-6 parts are unique in that the designer can set the switching frequency between 25 kHz to 95 kHz by adjusting transformer design. One way to lower device temperature is to design the transformer to reduce switching frequency; a good starting point is 50 kHz.

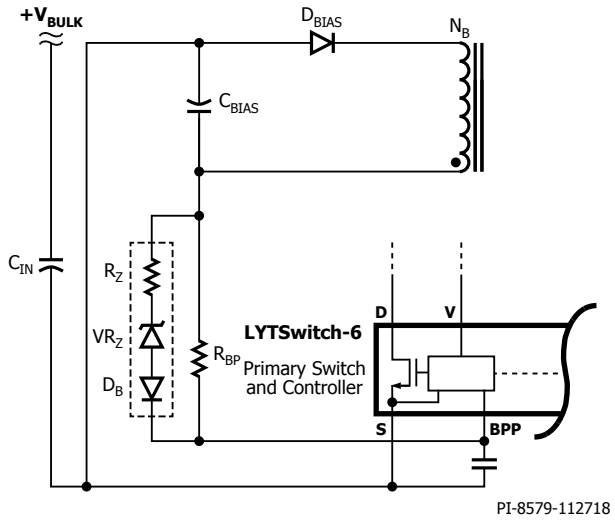
Primary-Side Overvoltage Protection

Primary-side output overvoltage protection provided by the LYTSwitch-6 IC uses an internal protection that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

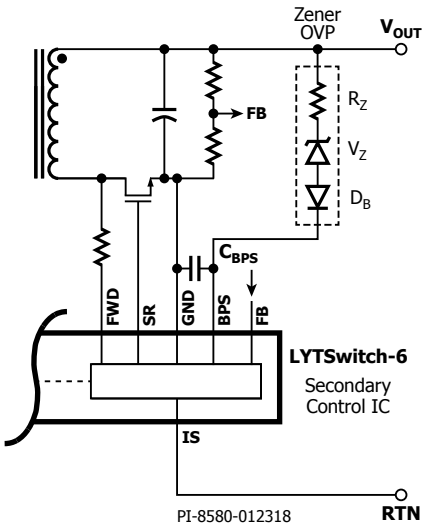
The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias-winding-voltage supply to the PRIMARY BYPASS pin (see Figure 11-a). The rectified and filtered bias winding output voltage may be higher than anticipated (up to 2 times the desired value) and is dependent on the coupling of the bias winding to the output winding and the resultant ringing of the bias winding voltage waveform. It is recommended that the rectified bias winding voltage be measured. Ideally this measurement should be made at the lowest input voltage and with maximum load applied the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode is selected with a clamping voltage approximately 6 V lower than the rectified bias winding voltage at which OVP is expected to be triggered. A forward voltage drop of 1 V can be assumed for the blocking diode. A small-signal standard recovery diode is recommended for this task. The blocking diode prevents any reverse current from charging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage event.

Secondary-Side Overvoltage Protection

Secondary-side output overvoltage protection is provided by the LYTSwitch-6 IC which uses an internal auto-restart circuit triggered by an input current into the SECONDARY BYPASS pin exceeding a threshold of $I_{BPS(SD)}$. The direct sensed output OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the



a. Primary-side OVP with High Current Pushed into BPP via Zener V_z.



b. Secondary-side OVP with High Current Pushed into BPS via Zener V_z and Resistor R_z.

Figure 11. Output Overvoltage Protection Circuits.

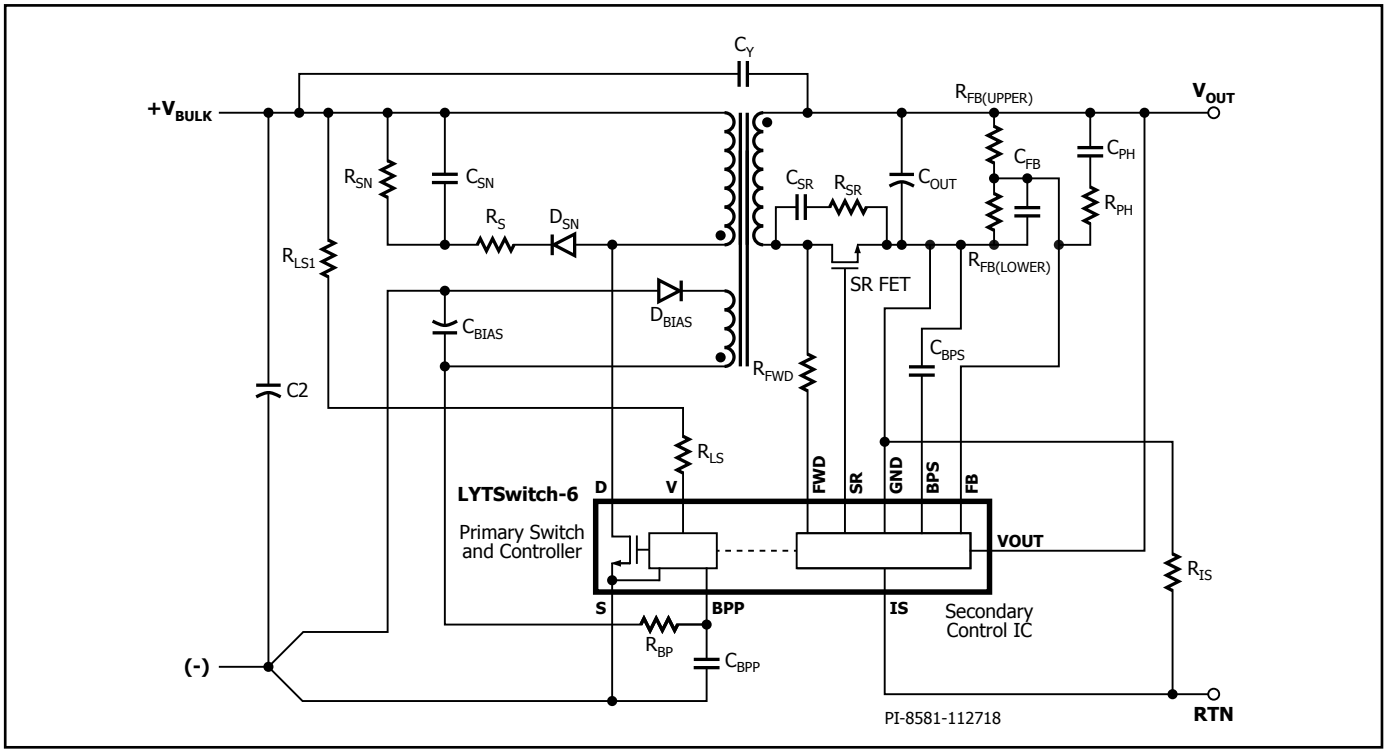


Figure 12. Typical Schematic of LYTSwitch-6 Flyback Power Supply (DC-DC Stage).

absolute value of (1.25 x V_{OUT}) – (4.4 V – SECONDARY BYPASS pin voltage). It is necessary to add a low value resistor, in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin (see Figure 11-b.)

Selecting Critical External Components

The schematic in Figure 12 shows the essential external components required for a working single output LYTSwitch-6 based power supply. The selection criteria for these components is as follows:

Primary-Side Components

PRIMARY BYPASS Pin Capacitor (C_{BPP})
This capacitor works as the supply decoupling capacitor for the internal primary-side controller and also determines current limit for the internal switch. 4.7 µF or 0.47 µF capacitance will select INCREASED or STANDARD current limits respectively. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double-sided boards as they allow the capacitors to be placed close to the IC. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Line Overvoltage / Brown-In Sense Resistor (R_{LS})
Both line overvoltage and brown-in voltage are sensed by the INPUT VOLTAGE pin. The current from the DC input bus is monitored via resistor R_{LS} and compared to an internal current threshold.

Typical value range for R_{LS} is in the range of 3.8 MΩ to 4 MΩ. R_{LS} is approximately equal to $V_{LOV} \times 1.414 / I_{OV-}$.

V_{LOV} is the input line voltage at which the power supply will stop switching because the overvoltage threshold (I_{OV-}) is exceeded. Switching will be re-enabled when line overvoltage hysteresis ($I_{OV(H)}$) is reached. Line OV (V_{LOV}) is approximately equal to $I_{OV-} \times R_{LS} / 1.414$.

The power supply will turn on once the brown-in threshold (I_{UV+}) is exceeded. Brown-in voltage is approximately equal to $I_{UV+} \times R_{LS} / 1.414$.

External Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BP})
The LYTSwitch-6 IC has an internal bypass regulator from the DRAIN pin of the primary-side switch to the PRIMARY BYPASS pin. This internal regulator is active during the switch off-time and keeps the PRIMARY BYPASS pin voltage from dropping below 5 V. This ensures that the IC will operate normally especially during start-up time. During start-up, the IC is powered from the internal regulator. When the output voltage has risen sufficiently, the primary controller will draw power from the external bias supply via the auxiliary winding rather than from the internal tap. This will reduce energy consumption as the auxiliary supply is at much lower voltage than the tap (which is driven by the high-voltage of the DRAIN pin). If the coupling between the bias winding and secondary winding is poor, the bias supply voltage may can drop significantly during no-load operation and may not be able to supply current to the PRIMARY BYPASS pin and keep the internal regulator off. If this condition causes the internal tap to turn on, no-load power consumption will increase. It is therefore recommended that the bias voltage be set close to the maximum of 12 V. Higher voltage may also increase no-load power consumption. For the bias supply, there is a trade-off between using a standard-recovery diode and a fast signal diode for the bias winding rectifier diode, D_{BIAS}. The standard recovery diode will tend to give lower radiated EMI while the fast diode will reduce no-load power consumption. Since LYTSwitch-6 ICs inherently use very little power, it is recommended that the standard recovery diode is used for the bias supply, trading a small increase in power dissipation for improved EMI performance.

A 22 µF 50 V low ESR aluminum electrolytic capacitor is recommended for the bias supply filter, C_{BIAS}. A low ESR electrolytic capacitor reduces no-load power consumption. Use of a ceramic surface mount capacitor is not recommended as this may cause audible noise due to piezoelectric excitation of the ceramic capacitors mechanical structure.

To ensure minimum no-load input power and high full load efficiency, resistor R_{BP} (Figure 12) should be selected such that the current through this resistor is higher than the PRIMARY BYPASS pin supply current.

The PRIMARY BYPASS pin supply can be calculated as shown below;

$$I_{SSW} = \left(\frac{f_{SW}}{132\,K}\right) \times (I_{S2} - I_{S1}) + I_{S1}$$

Where;
I_{SSW}: PRIMARY BYPASS pin supply current at operating switching frequency
f_{SW}: Operating switching frequency (kHz)
I_{S1}: Non-switching PRIMARY BYPASS pin supply current (refer to data sheet specification tables)
I_{S2}: PRIMARY BYPASS pin supply current at 132 kHz (refer to data specification sheet)

The PRIMARY BYPASS pin voltage will be ~5.3 V if the bias current is higher than PRIMARY BYPASS pin supply current. A PRIMARY BYPASS pin voltage of ~5.0 V, indicates that the current through R_{BP} is less than the PRIMARY BYPASS pin supply current and the IC is drawing current from the DRAIN pin. Ensure that the voltage on the PRIMARY BYPASS pin never falls below 5.3 V – except during start-up.

To determine maximum value of R_{BP};

$$R_{BP} = [V_{BIAS\,(NO-LOAD)} - V_{BPP}]/I_{SSW;}$$

where V_{BPP} = 5.3 V.

Clamp Network Across Primary Winding (D_{SN}, R_S, R_{SN}, and C_{SN})
Figure 13, shows the low cost R2CD clamp which is used in most low power circuits. For higher power designs, a Zener clamp or an R2CD plus Zener clamp can be used to achieve better efficiency. It is advisable to limit the peak Drain voltage to 90% of BV_{DSS} under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit). The clamp diode, D_{SN} shown in Figure 13 must be either a standard recovery glass passivated diode or a fast recovery type with a reverse recovery time of less than 500 ns. Use of standard recovery switch passivated diodes allows the recovery of some of the clamp energy from each cycle and improves average efficiency. The diode momentarily conducts each time the primary switch inside the LYTSwitch-6 IC turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{SN}. Resistor R_S, which is in the series path, acts as a damper preventing excessive ringing due to resonance between the leakage reactance and the clamp capacitor C_{SN}. Resistor R_S dissipates the energy stored in capacitor C_{SN}. Designs employing different sized LYTSwitch-6 devices will have different peak primary currents and leakage inductances and will therefore result in different amounts of leakage energy. Capacitor C_{SN}, R_{SN} and R_S must therefore be optimized for each design. As a general rule the value of capacitor C_{SN} should be minimized and the value of resistors R_{SN} and R_S maximized, while still meeting the 90% derating of the BV_{DSS} limit. R_S should be sufficiently large to damp the ring, but small enough to prevent the drain voltage from rising too far. A ceramic capacitor that uses a dielectric such as Z5U if used as the C_{SN} capacitor in the clamp circuit may generate audible noise, so the use of a polyester film type capacitor is preferred.

Common Primary Clamp Configurations

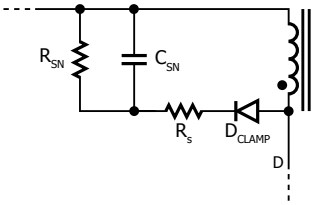
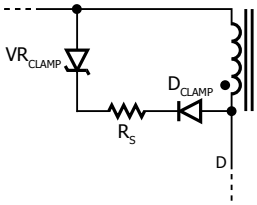
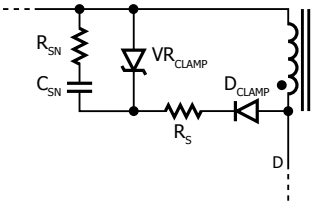
R2CD	Zener	R2CD + Zener
		

Figure 13. Recommended Primary Clamp Components.

Primary Clamp Circuit			
Benefits	**R2CD**	**Zener**	**R2CD + Zener**
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 2. Benefits of Primary Clamp Circuits.

Secondary-Side Components Driving LYTSwitch-6

SECONDARY BYPASS Pin Capacitor (C_{BPS})

This capacitor works as a voltage supply decoupling capacitor for the integrated secondary-side controller. A surface mount, 2.2 µF, 10 V / X7R or X5R / 0805 or larger size, multi-layer ceramic capacitor is recommended for this application. The SECONDARY BYPASS pin voltage needs to reach 4.4 V before the output voltage reaches its target voltage. A significantly higher value of SECONDARY BYPASS pin capacitor may prevent this from occurring and induce an output voltage overshoot during start-up. Values lower than 1.5 µF may not be provide sufficient energy storage, leading to unpredictable device operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

FORWARD Pin Resistor (R_{FWD})

The FORWARD pin is connected to the drain terminal of the synchronous rectifier MOSFET (SR FET). This pin is used to monitor the Drain voltage of the SR FET to precisely control turn-on and turn-off of the device. This pin is also used to charge the SECONDARY BYPASS pin capacitor whenever the output voltage falls below the SECONDARY BYPASS pin voltage. The use of a 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current and works well across a wide range of output voltages. A different resistor value will interfere with the timing of the synchronous rectifier drive and should not be used. Care must be taken to ensure that the voltage at the FORWARD pin never exceeds its absolute maximum voltage rating. If the FORWARD pin voltage exceeds the FORWARD pin absolute maximum voltage, the IC will be damaged. Figures 14, 15, 16 and 17 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR FET.

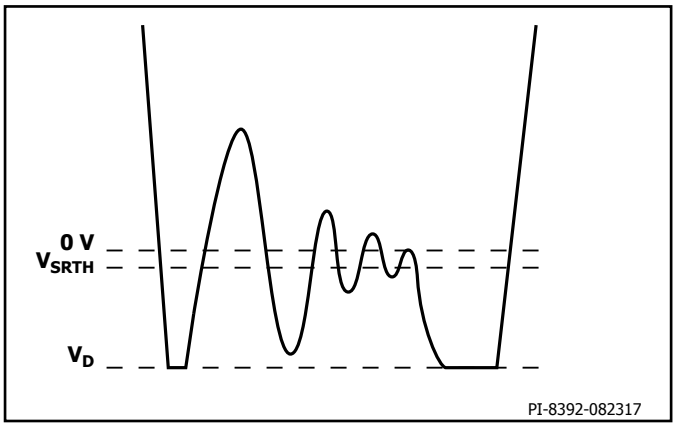


Figure 14. Unacceptable FORWARD Pin Waveform After Handshake with SR FET Conduction During Flyback Cycle.

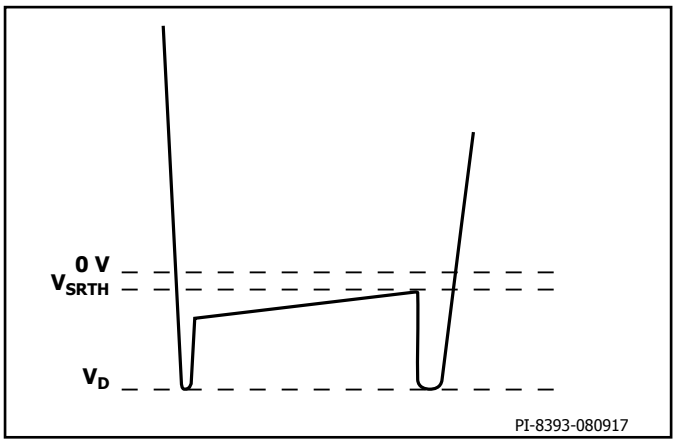


Figure 15. Acceptable FORWARD Pin Waveform After Handshake with SR FET Conduction During Flyback Cycle.

FEEDBACK Pin Divider Network ($R_{FB(UPPER)}$, $R_{FB(LOWER)}$)

A suitable resistive voltage divider should be connected from the output of the power supply to the FEEDBACK pin of the LYTSwitch-6 IC and sized such that at the desired output voltage, the FEEDBACK pin will be at 1.265 V. A decoupling capacitor (C_{FB}) of 330 pF is recommended and should be connected from the FEEDBACK pin to SECONDARY GROUND pin. C_{FB} acts as a decoupling capacitor for the FEEDBACK pin to prevent switching noise from affecting IC operation.

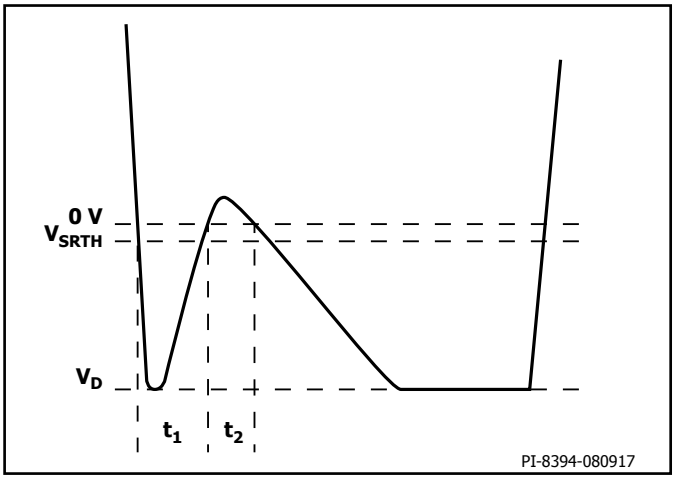


Figure 16. Unacceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

Note:

If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off.

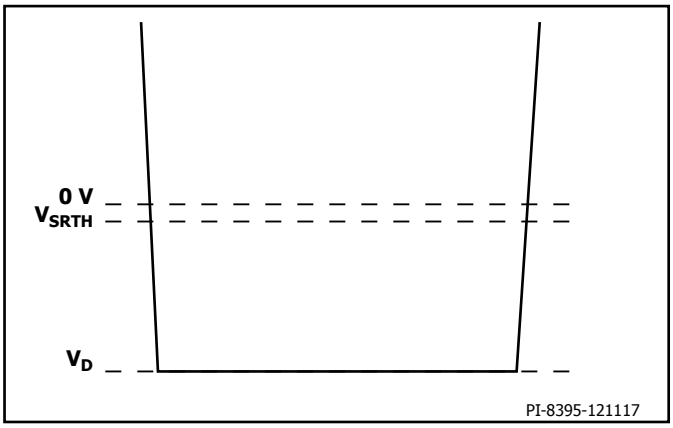


Figure 17. Acceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

SR FET Operation and Selection

Although a simple diode rectifier and snubber is effective, the use of a SR FET significantly improves efficiency. The secondary-side controller turns the SR FET on at the beginning of the flyback cycle. The gate of the SR FET should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the LYTSwitch-6 IC (no additional resistors should be connected to the gate drive of the SR FET). The SR FET is turned off when its V_{DS} reaches 0 V. The SR FET driver uses the SECONDARY BYPASS pin as its supply rail; this voltage is typically 4.4 V. A FET with a high gate threshold voltage is not therefore appropriate for this application; FETs with a threshold voltage of 1.5 – 2.5 V are ideal. MOSFETs with a threshold voltage as high as 4 V may also be used provided that the data sheet specifies $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

There is a short delay between the start of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET will conduct. If an external Schottky diode is connected in parallel, current flows mostly through the Schottky diode. A parallel Schottky diode will therefore increase efficiency. A 1 A surface-

mount Schottky diode is usually adequate for this task; however the gains are modest, for a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.3 times the expected peak inverse voltage (PIV) calculated from the turns ratio of the transformer.

The interaction between the leakage reactance of the output winding(s) and the output capacitance (COSS) of the SR FET leads to voltage ringing at the instance of winding voltage reversal when the primary switch turns on. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω should be used (higher resistance values lead to a noticeable drop in efficiency). A capacitor value of 1 nF to 2.2 nF is adequate for most designs.

Output Filter Capacitance (C_{OUT})
Aluminium electrolytic capacitors with low ESR and high RMS ripple current rating are suitable for use with most high frequency flyback switching power supplies intended for ballast applications. Typically, 300 µF to 400 µF capacitance per ampere of output current is appropriate. This value may be adjusted to reflect the amount of output current ripple required. Ensure that capacitors with a voltage rating higher than the highest output voltage (plus sufficient margin) are used.

Output Current Sense Resistor (R_{IS})
For output constant current (CC) operation, external current sense resistor R_{IS} should be connected between the ISENSE pin and the SECONDARY GROUND pin of the IC as shown in Figure 18. If constant current (CC) regulation is not required, this pin should be connected to the SECONDARY GROUND pin of the IC.

The voltage generated across the resistor is compared to an internal reference the Current Limit Voltage Threshold ($I_{SV(TH)}$) which is approximately 35 mV. The size of R_{IS} can be calculated;

$$R_{IS} = I_{SV(TH)} / I_{OUT(CC)}$$

The R_{IS} resistor must be placed close to the ISENSE and SECONDARY GROUND pins with short traces. This prevents ground impedance noise interference that may cause instability which would be most apparent during constant current operation.

Output Post Filter Components (L_{PF}, C_{PF})
If necessary a post filter (L_{PF} and C_{PF}) can be added to attenuate high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 mH – 3.3 mH with a current rating greater than peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥ 1.25 × V_{OUT}. If a post filter is used then the output voltage sense resistor should be connected before the post filter inductor.

PCB Layout Recommendations

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. See Figure 18.

Bypass Capacitors
The PRIMARY BYPASS (C_{BPP}) pin, SECONDARY BYPASS (C_{BPS}) pin and feedback decoupling capacitors must be located adjacent to and between those pins and their respective returns with short traces.

PRIMARY BYPASS pin – SOURCE pin.
SECONDARY BYPASS pin – SECONDARY GROUND pin.
FEEDBACK pin – SECONDARY GROUND pin.

Signal Components
Resistors R_{LS}, R_{BP}, $R_{FB(UPPER)}$, $R_{FB(LOWER)}$ and R_{IS} which provide feedback information must be placed as close as possible to the IC pin with short traces.

Critical Loop Area
Loops for circuits with high dv/dt or di/dt should be kept as small as possible. The area of the primary loop – input filter capacitor to transformer primary winding to IC should be kept small. Ideally, no loop should be inside another loop (see Figure 18). This will minimize cross-talk between circuits.

Primary Clamp Circuit
A clamp is used to limit the peak voltage on the DRAIN pin at turn-off. This can be achieved by placing an RCD or Zener diode clamp across the primary winding. Positioning the clamp components close to the transformer and IC will minimize the size of this loop and reduce EMI.

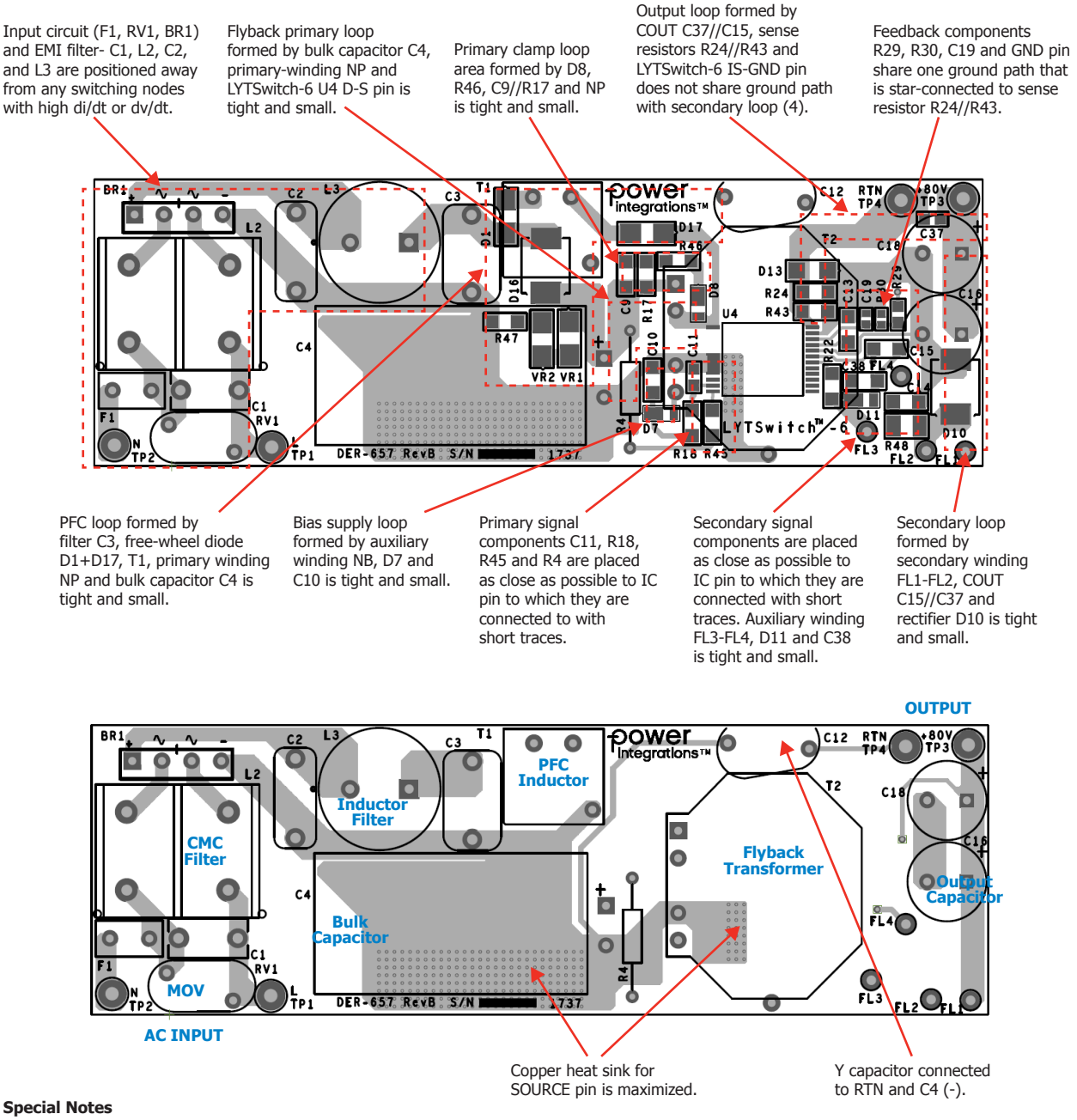
Y Capacitor
The Y capacitor should be connected directly between the positive terminal of the primary input filter capacitor and the output positive or return of the transformer main secondary winding. This will route high magnitude common mode surge currents away from the IC. If an input π filter (C1, L_F and C2) is used, the filter inductor should be placed between the negative terminals of the filter capacitors.

Output Rectifier Diode
For best performance, the area of the loop connecting the secondary winding, the output rectifier diode, and the output filter capacitor should be minimized. Sufficient copper area should be provided at the terminals of the rectifier diode for heat sinking.

ESD Immunity
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD or hi-pot test requirements. A spark gap is best placed between the output return (and/or positive terminals) and one of the AC inputs after the fuse. In this configuration a 6.4 mm (5.5 mm may be acceptable in some applications) spark gap is suitable to meet creepage and clearance requirements of the applicable safety standards. This is less than the typical primary to secondary spacing because the voltage across a spark gap does not exceed the peak of the AC input.

Drain Node
The drain switching node is the dominant noise generator. As such components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located away from the PRIMARY BYPASS pin, and employ minimum trace width and length.

PCB Layout Example



Special Notes

- All loops are separated; no loop is inside a loop. This will avoid ground impedance noise coupling.
- Maintain trace surface area and length of high dv/dt nodes such as DRAIN, as small and short as possible to minimized RFI generation.
- No signal trace (quiet trace) such as Y capacitor and feedback return must be routed near or across noisy nodes (high dv/dt or di/dt) such as DRAIN, underneath transformer belly, switching side of any winding or output rectifier diode to avoid capactively or magnetically coupled noise.
- No signal trace must share path with traces having an AC switching current such as output capacitor. Connection must be star-connected to capacitor pad in order to avoid ground impedance coupled noise.

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Figure 18. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt and di/dt, Component Placement.

Recommendations in Reducing No-load Consumption

The LYTSwitch-6 IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is used to provide supply current to the PRIMARY BYPASS pin once the LYTSwitch-6 IC has started switching. An auxiliary (bias) winding from the switching transformer serves this purpose. The bias-winding-derived supply to the PRIMARY BYPASS pin enables designs with no-load consumption of less than 100 mW. Resistor R_{BP} (shown in Figure 12) can be adjusted to achieve lowest no-load input power.

Other components that may further reduce no-load consumption are;

1. Low value of primary clamp capacitor, C_{SN}.
2. Schottky or ultrafast diode for bias supply rectifier, D_{BIAS}.
3. Low ESR capacitor for bias supply filter capacitor, C_{BIAS}.
4. Low value SR FET RC snubber capacitor, C_{SR}.
5. Transformer construction: Tape between primary winding layers, and multi-layers of tape between primary and secondary windings reduces inter-winding capacitance.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas for the primary and secondary power circuits minimizes radiated and conducted EMI. Care should be taken to achieve a compact loop area. (See Figure 18)
2. A small capacitor in parallel to the primary-side-clamp diode can reduce radiated EMI.
3. A resistor (2 Ω – 47 Ω) in series with the bias winding helps reduce radiated EMI.
4. A series connection of a small resistor and ceramic capacitor (<22 pf) across the primary (Figure 21) or across the secondary winding (<100 pf) reduces conducted and radiated EMI. Larger capacitor values may increase no-load consumption.
5. Common mode chokes are typically required at the input of a power supply to attenuate common mode noise. However, the same effect can be achieved by using shield windings on the transformer. Shield windings can be used in conjunction with common mode filter inductors at the input to reduce conducted and radiated EMI.
6. Adjusting the values of the SR FET RC snubber components reduces high frequency radiated and conducted EMI.
7. A π filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI. A ferrite bead (Figure 18) can be added to further improve EMI.
8. A resistor across a differential inductor reduces the Q factor and reduce EMI above 10 MHz; however this may increase the EMI below 5 MHz.
9. A 1 μF ceramic capacitor connected across the output of the power supply reduces radiated EMI.
10. A slow bias rectifier-diode (250 ns < t_{RR} < 500 ns) reduces conducted EMI above 20 MHz and radiated EMI above 30 MHz.

Heat Spreader

For enclosed power supplies such as LED ballast that experience high ambient conditions, using the PCB alone as a heat sink may not be sufficient to keep IC within temperature limits. The addition of a metal heat spreader may be required to limit the maximum IC temperature.

Unless a ceramic insulator material is used as a heat sink, care should be taken to avoid compromising the isolation barrier. Typically the heat spreader is formed by the combination of heat spreader material (copper or aluminum) a 0.4 mm mylar pad for reinforced isolation and a thermally conductive pad to better transfer heat from the device to the heat-spreader. Figure 19 suggests a simple method to attach a heat spreader to an InSOP-24D package while maintaining appropriate creepage and clearance.

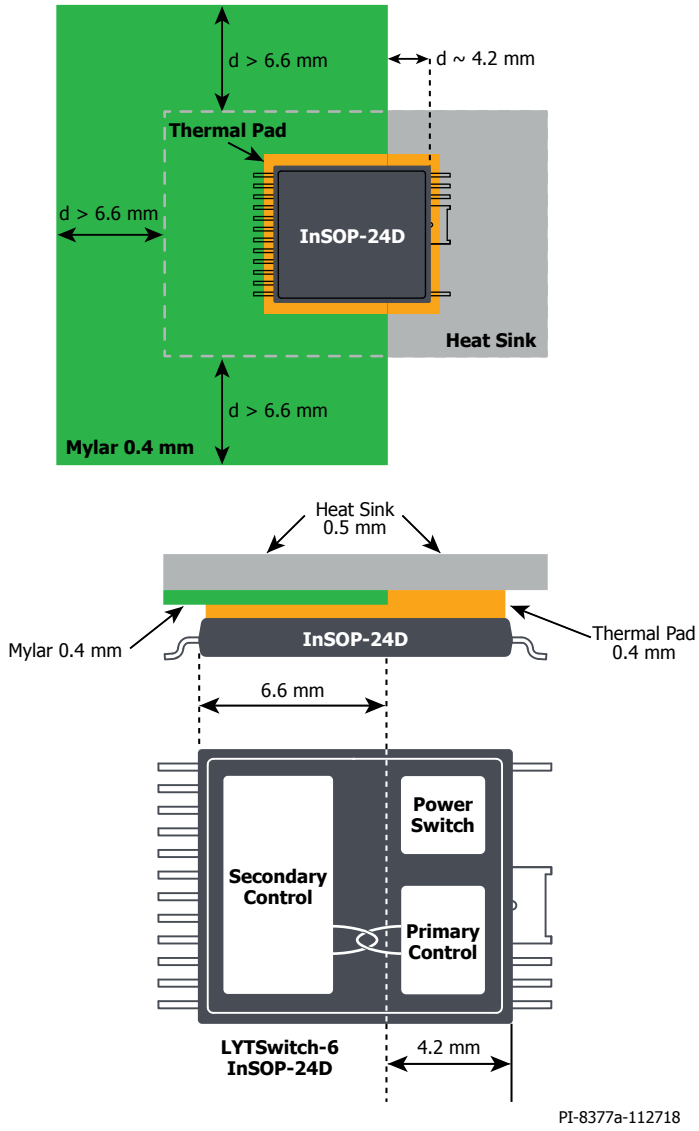

Figure 19. Simplified Diagram of Heat spreader Attachment to an InSOP-24D Package.

Recommended Position of InSOP-24D Package with Respect to Transformer

The PCB underneath the transformer and InSOP-24D should be rigid. If large transformers are used together with a thin PCB (<1.5 mm), it is recommended that the transformer be moved away from the InSOP package. Cutting a slot in the PCB that runs near-to or underneath the InSOP package is not generally recommended as this weakens the PCB. For long PCBs, the use of a mechanical support or post in the middle of the board or located near to the InSOP package is recommended.

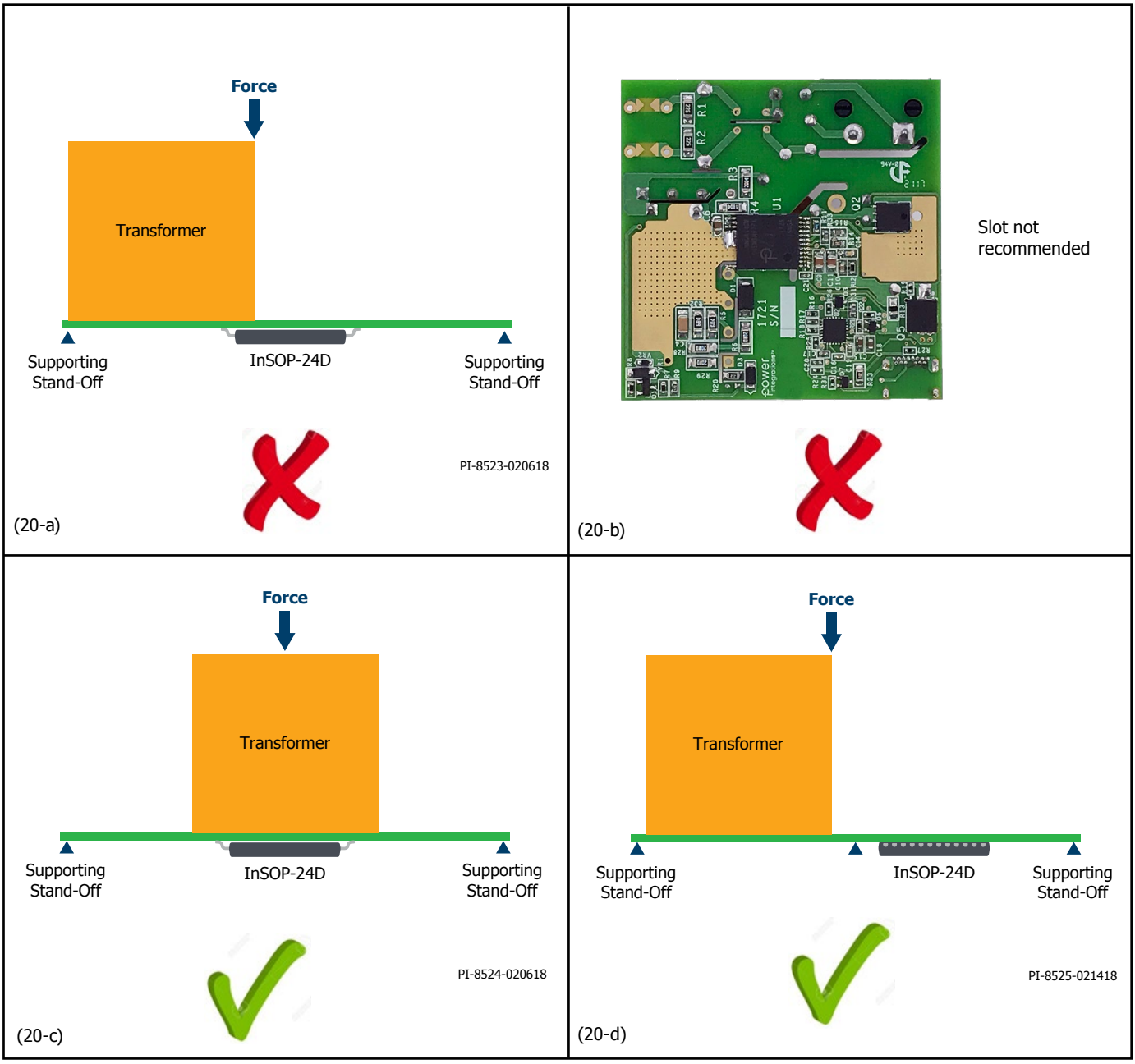

Figure 20. Recommended Position of InSOP-24D Package Shown with Check Mark.

Quick Design Checklist

As with any power supply, the performance of all LYTSwitch-6 designs should be measured on the bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage – Verify that the V_{DS} of the LYTSwitch-6 IC and the SR FET do not exceed 90% of their respective breakdown voltages at the highest input voltage and peak (overload) output power both during normal operation and at start-up.

Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum Drain current for the primary switch should be below the specified absolute maximum ratings.

Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature meets specified limits for the LYTSwitch-6 IC, transformer, output SR FET, and output capacitors. There should be sufficient thermal margin to account for part-to-part variation in the $R_{DS(ON)}$ of the LYTSwitch-6 IC. At low-line and full load it is recommended that the LYTSwitch-6 SOURCE pin temperature is limited to 110 °C to allow for these variations.

Design Considerations When Using PowiGaN Devices (LYT6078C, LYT6079C and LYT6070C)

Switching Frequency (f_{sw})

It is a unique feature in LYT6078C, LYT6079C and LYT6070C that for full load, the designer can set the switching frequency to between 25 kHz to 95 kHz. For lowest temperature, the switching frequency should be set to around 60 kHz. For a smaller transformer, the full load switching frequency needs to be set to 95 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection. The following table provides a guide to frequency selection based on device size. This represents the best compromise between overall device losses (conduction losses and switching losses) based on the size of the integrated high-voltage switch.

PowiGaN device LYT6078C	65 kHz
PowiGaN device LYT6079C	65 kHz
PowiGaN device LYT6070C	60 kHz

Drain Voltage and Reflected Output Voltage, V_{OR} (V)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 21.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 21 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (VOR) to maintain K_P = 0.8 at minimum input voltage for universal input and $K_P \geq 1$ for high-line-only conditions.

Consider the following for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given LYT6078C, LYT6079C and LYT6070C device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

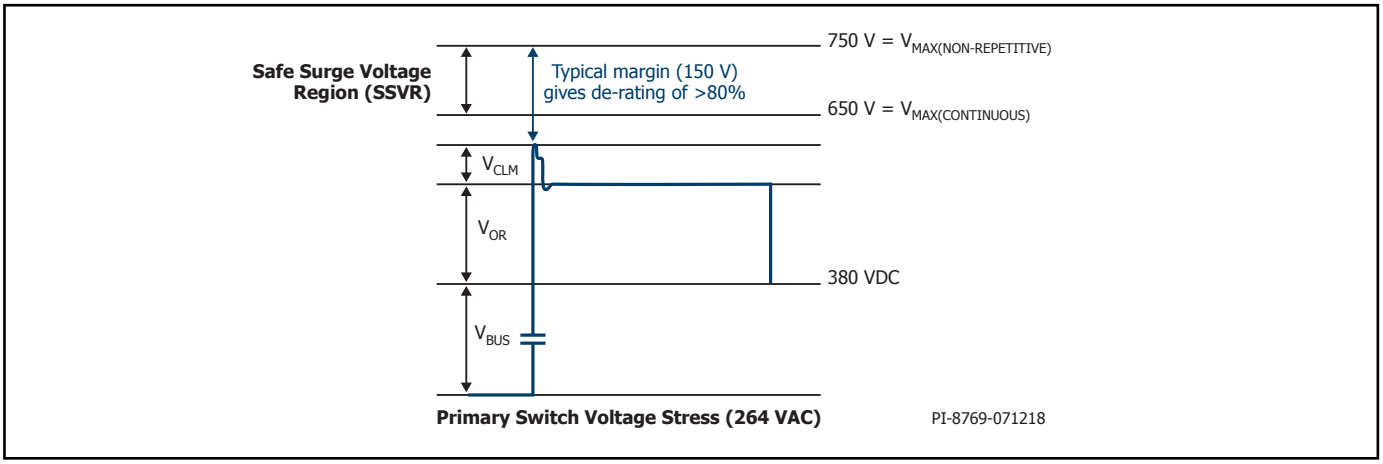

Figure 21. Peak Drain Voltage for 264 VAC Input Voltage (Applicable for LYT6078C, LYT6079C and LYT6070C).

There are some exceptions to this. For very high output currents the VOR should be reduced to get highest efficiency. For output voltages above 15 V, VOR should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

Thermal Management Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main heat removal path for the device. The SOURCE pin should therefore be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area can be maximized for good heat sinking without increasing EMI. Similarly for the output SR FET, maximize the PCB area connected to the pins of the SR FET.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered be sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Thermal Resistance Test Conditions for PowiGaN Devices (LYT6078C, LYT6079C and LYT6070C)

Thermal resistance value is for primary power device junction to ambient only.

Testing performed on custom thermal test PCB as shown in Figure 22. The test board consists of 2 layers of 2 oz. Cu with the InSOP package mounted to the top surface and connected to a bottom layer Cu heat sinking area of 550 mm^2.

Connection between the two layers was made by 82 vias in a 5 x 17 matrix outside the package mounting area. Vias are spaced at 40 mils, with 12 mil diameter and plated through holes are not filled.

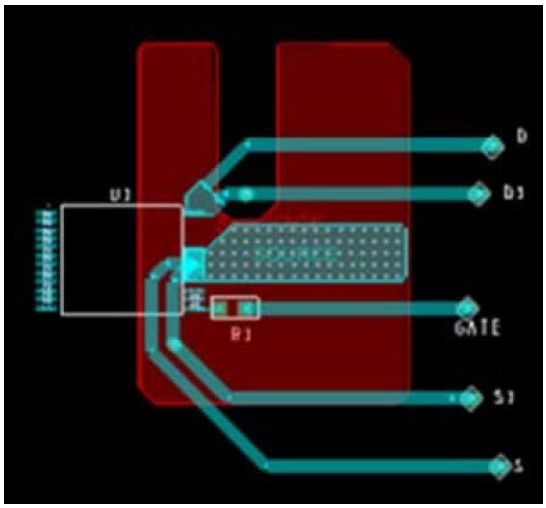

Figure 22. Thermal Resistance Test Conditions for PowiGaN Devices (LYT6078C, LYT6079C and LYT6070C.)

Second Applications Design Example

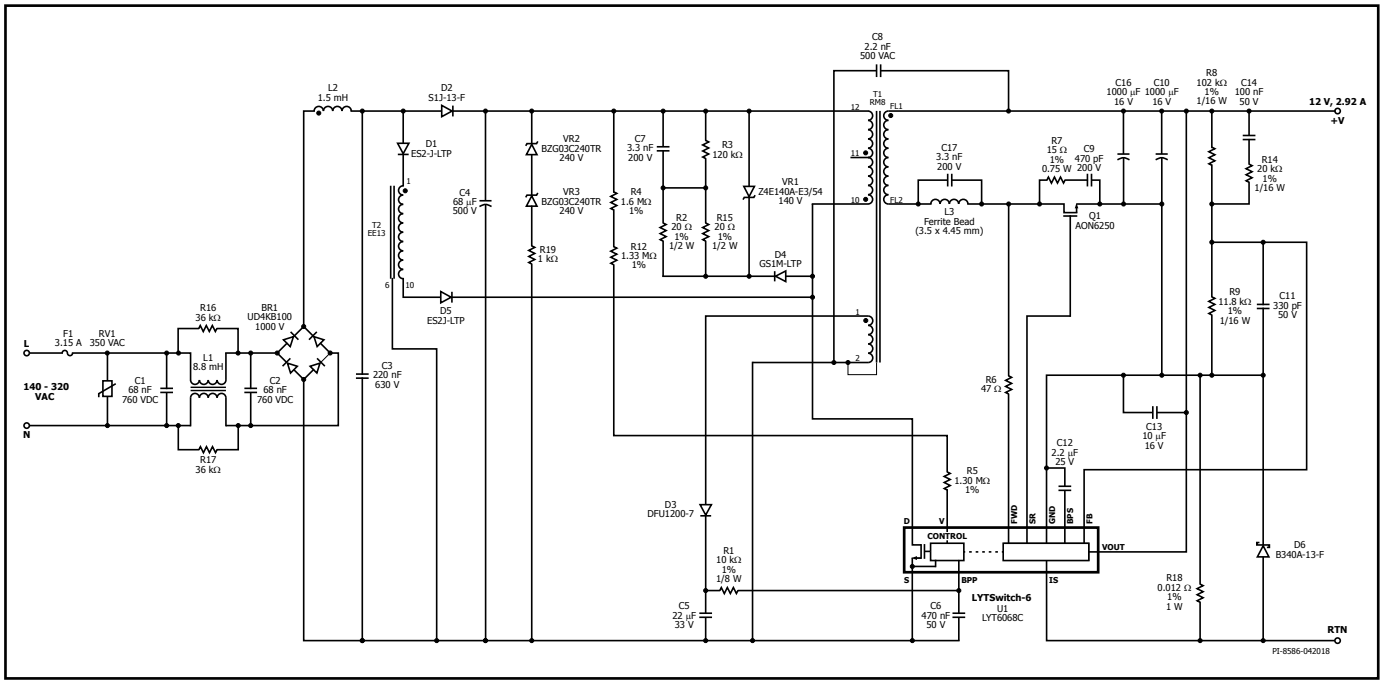

Figure 23. Schematic of DER-637, 35 W, 12 V, 2.92 A, 140 VAC – 320 VAC using LYSwitch-6 LYT6068C with Synchronous Rectification.

A High Efficiency, 35 W, 12 V Universal Input LED Ballast – with Synchronous Rectification

The circuit shown on Figure 23 is a 35 W isolated flyback power supply with a single-stage power factor correction circuit for LED lighting applications. It provides a constant voltage output of 12 V with accurate voltage regulation and an output current of up to 2.92 A. The power supply is intended for applications where a post regulators are used to independently regulate multiple LED strings design such as in RGBW smart lighting. The power supply is also ideal for single-LED string applications as it delivers the same maximum constant output current with accurate regulation and no line-induced ripple from 12 V to 3 V output. The circuit is highly efficient and provides excellent line and load regulation across an input voltage range of 140 VAC to 320 VAC. The power supply also provides a PF of greater than 0.9 PF and less than 20% A-THD at 230 VAC.

Input Stage

Fuse F1 provides protection, and isolates the circuit from the input line in the event of catastrophic component failure. Varistor RV1 is connected after the fuse and acts as a voltage clamp – limiting the voltage to a safe level in the event of a line transient or surge. Bridge diode BR1 rectifies the AC line voltage to provide a full-wave rectified DC voltage to the input film capacitors C3 and C4. The circuit employs a 2-stage EMI filter consisting of C1, L1, C2, L2, and C3.

Primary Flyback Stage

The bulk capacitor C4 filters the line ripple voltage and provides A DC voltage to the flyback stage. Capacitor C4 also filters differential current which reduces conducted EMI noise. The voltage across the bulk capacitor (C4) monitored via the INPUT OVERVOLTAGE pin resistors (R4 and R12) to provide line overvoltage and brown-in protection. The overvoltage threshold (I_{OV+}) determines the overvoltage threshold, while (I_{UV+}) determines the line turn-on voltage. In the event of a line surge or transient, an input overvoltage shutdown will be triggered by a line voltage exceeding 490 V_{PK}.

One end of the transformer (T1) primary winding is connected to the positive terminal of the bulk capacitor (C4) while the other side is connected to the Drain of the LYTSwitch-6 (U1) IC's the integrated 650 V power switch. A low cost RCD primary clamp, D4, R2, R15, R3 and C7 limits the voltage spike seen by the power switch. The spike is caused by transformer leakage inductance. The RCD primary clamp also reduces radiated and conducted EMI. Clamping Zener VR1 limits the drain voltage spike during start-up into full load at 320 VAC.

The LYTSwitch-6 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C6) when line voltage is first applied. During normal operation the primary-side is powered from an auxiliary winding on transformer T1. Output of the auxiliary winding is rectified by diode D3 and filtered by capacitor C5. Resistor R1 limits the current supplied to the PRIMARY BYPASS pin. The value of the PRIMARY BYPASS pin capacitor C6 used is 470 nF which sets normal current limit.

Power Factor Correction Stage

The PFC stage comprises inductor (T2) in series with blocking diode (D1 and D5) and is connected to the DRAIN pin of the LYTSwitch-6 IC. High power factor correction is achieved using a Switched Valley-Fill Single Stage PFC (SVF S^2PFC) technique, operating in discontinuous conduction mode (DCM). The DCM switched current from inductor T2 shapes the input current into a quasi-sinusoid when the rectified voltage on C3 is less than the DC voltage on C4 resulting in a high power factor.

During switch on-time, energy is stored in the PFC inductor (T2) and flyback transformer (T1). During switch off-time, the energy from both the PFC and flyback inductors is transferred to the secondary-side through the flyback transformer.

Diode D2 isolates capacitor C3 from the rectified AC input. It also provides a current path for charging of the bulk capacitor C4, especially at low-line which improves efficiency. Free-wheel diodes D1 and D5 provide a path for the energy stored in the PFC inductor to

transfer to the secondary-side during switch off-time. Diode D1 and D5 are connected in series to withstand the resonant ring induced on the PFC inductor when the switch turns off.

During no-load or under light load (<10% load) the energy stored in the PFC inductor (T2) may be more than the secondary load requires, the excess energy from the PFC inductor is recycled to the bulk capacitor C4 and boosts the bulk voltage. A Zener-resistor clamp, (VR2 and VR3 in series with R19) is connected across the bulk capacitor C4 to limit the voltage rise to safe levels. The Zener clamp voltage is restricted to less than the 500 V rating of the bulk capacitor C4.

Secondary Stage

The secondary-side control provided by the LYTSwitch-6 IC provides constant output voltage and constant output current. The output from the secondary winding of the transformer is rectified by SR FET Q1 and filtered by output capacitors C10 and C16. Adding an RC snubber (R7 and C9) across the SR FET reduces voltage stress.

The secondary-side of the IC is self-powered using either the secondary winding forward voltage via the FORWARD pin or the output voltage via the OUTPUT VOLTAGE pin. Capacitor C13 connected to the SECONDARY BYPASS pin of LYTSwitch-6 IC (U1) provides decoupling for the internal circuitry.

During constant voltage operation, output voltage regulation is achieved by sensing the output voltage via a potential divider formed by resistors R8 and R9. The voltage across R9 is monitored by the FEEDBACK pin and compared to an internal reference voltage of 1.265 V to maintain accurate regulation. Bypass capacitor C11 is placed across FEEDBACK and SECONDARY GROUND pins to filter high frequency noise preventing interference with the feedback signal.

During constant current operation, the output current is set by the sense resistor R18. The voltage across the sense resistor is compared to the ISENSE pin's internal reference threshold of 35 mV in order to maintain constant current regulation. Diode D6 in parallel with the current sense resistor R18 clamps the voltage across the ISENSE pin and SECONDARY GROUND pin to protect the IC from the high current surge from the output capacitor induced by an output short-circuit.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage ..... -0.3 V to 650 V / 725 V / 750 V[8]
DRAIN Pin Peak Current: LYT6063C .....2.24 A[4]
LYT6065C ..... 3.87 A[4]
LYT6067C ..... 5.57 A[4]
LYT6068C ..... 6.24 A[4]
LYT6073C ..... 2.38 A[5]
LYT6075C ..... 4.11 A[5]
LYT6077C ..... 5.92 A[5]
PowiGaN device LYT6078C .....6.5 A[3]
PowiGaN device LYT6079C ..... 10 A[3]
PowiGaN device LYT6070C ..... 14 A[3]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Current .....100 mA
FW Pin Voltage .....-1.5 V to 150 V
FB Pin Voltage ..... -0.3 V to 6 V
SR Pin Voltage ..... -0.3 V to 6 V
V Pin Voltage (LYT606xC) .....-0.3 V to 650 V
V Pin Voltage (LYT607xC) .....-0.3 V to 725 V
IS Pin Voltage[9] ..... -0.3 V to 0.3 V
VOUT Pin Voltage .....-0.3 V to 27 V
Storage Temperature .....-65 to 150 °C
Operating Junction Temperature[6] .....-40 to 150 °C
Ambient Temperature .....-40 to 105 °C
Lead Temperature[7] .....260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 33 about maximum allowable voltage and current combinations.
4. Please refer to Figure 24 about maximum allowable voltage and current combinations.
5. Please refer to Figure 34 about maximum allowable voltage and current combinations.
6. Normally limited by internal circuitry.
7. 1/16” from case for 5 seconds.
8. PowiGaN devices:
   Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V
   Maximum continuous drain voltage ..... -0.3 V to 650 V
9. Absolutely maximum voltage for less than 500 µsec is 3 V.

Thermal Resistance

Thermal Resistance:
(θ_{JA}) ..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC}) .....8 °C/W[3]
PowiGaN devices LYT6079C and LYT6070C
(θ_{JA}) ..... 50 °C/W[4]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.
4. Please see Figure 22.`

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C	22	25	27	kHz
Jitter Frequency	f_M	T_J = 25 °C, f_{SW} = 100 kHz	0.80	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C	12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}				$t_{OFF(MIN)}$	µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C	LYT606xC LYT607xC	145	200	300	µA
			LYT6078C LYT6079C LYT6070C	145	266	425	
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz) T_J = 25 °C	LYT6063C	0.32	0.43	0.61	mA
			LYT6065C	0.49	0.65	1.03	
			LYT6067C	0.77	1.03	1.38	
			LYT6068C	0.90	1.20	1.75	
			LYT6073C	0.36	0.48	0.65	
			LYT6075C	0.59	0.79	1.10	
			LYT6077C	0.90	1.20	1.73	
			LYT6078C	0.93	1.24	1.79	
			LYT6079C LYT6070C	1.46	1.95	2.81	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}			4.65	4.90	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.80	3.15	3.50	V
OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	LYT606xC LYT607xC	106	115	118	µA
			LYT6079C LYT6070C	106	112	118	
OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C	LYT606xC LYT607xC		7		µA
			LYT6078C LYT6079C LYT6070C		8		
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100			µA
OV Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
UV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	LYT606xC LYT607xC	23.9	26.1	28.2	µA
			LYT6078C LYT6079C LYT6070C	22.4	24.4	26.7	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Line Fault Protection							
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT}	di/dt = 163 mA/µs T_J = 25 °C	LYT60x3C	511	550	589	mA
		di/dt = 213 mA/µs T_J = 25 °C	LYT60x5C	883	950	1017	
		di/dt = 300 mA/µs T_J = 25 °C	LYT60x7C	1348	1450	1552	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6068C	1534	1650	1766	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6078C	1581	1700	1819	
		di/dt = 425 mA/µs T_J = 25 °C	LYT6079C	1767	1900	2033	
		di/dt = 525 mA/µs T_J = 25 °C	LYT6070C	2139	2300	2461	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$	di/dt = 163 mA/µs T_J = 25 °C	LYT60x3C	591	650	709	mA
		di/dt = 213 mA/µs T_J = 25 °C	LYT60x5C	1046	1150	1254	
		di/dt = 300 mA/µs T_J = 25 °C	LYT60x7C	1501	1650	1799	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6068C	1683	1850	2017	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6078C	1767	1900	2033	
		di/dt = 425 mA/µs T_J = 25 °C	LYT6079C	1980	2130	2279	
		di/dt = 525 mA/µs T_J = 25 °C	LYT6070C	2395	2576	2756	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		102	110	118	kHz
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
BYPASS Pin Fault Detection Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5	11.3	mA
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C		0.17	0.20	0.23	sec

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LYT6063C $I_D = I_{LIMIT+1}$	T_J = 25 °C		4.90	5.64	Ω
			T_J = 100 °C		7.60	8.74	
		LYT6065C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		LYT6067C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.02	1.17	
			T_J = 100 °C		1.58	1.82	
		LYT6068C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.86	0.99	
			T_J = 100 °C		1.34	1.54	
		LYT6073C $I_D = I_{LIMIT+1}$	T_J = 25 °C		4.42	5.08	
			T_J = 100 °C		6.85	7.88	
		LYT6075C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		LYT6077C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
		LYT6078C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		LYT6079C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		LYT6070C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C	1.250	1.265	1.280	V
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C	118	132	145	kHz
OUTPUT VOLTAGE Pin Auto-Restart Threshold	$V_{VO(AR)}$			3.45		V
OUTPUT VOLTAGE Pin Auto-Restart Timer	$t_{VOUT(AR)}$	T_J = 25 °C		49.5		ms
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C		325	485	µA
BPS Pin Voltage	V_{BPS}		4.20	4.40	4.60	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$		3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$			0.65		V
Current Limit Voltage Threshold	$I_{SV(TH)}$	Set by External Resistor T_J = 25 °C	35.17	35.90	36.62	mV
FWD Pin Breakdown Voltage	V_{FWD}		150			V
Minimum Off-Time	$t_{OFF(MIN)}$		2.48	3.38	4.37	µs
Soft-Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C	7.5	11.75	19	ms
BPS Pin Fault Detection Threshold Current	$I_{BPS(SD)}$		5.2	8.9	12	mA
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$	T_J = 25 °C		112	135	mV
Thermal Foldback	T_{JB}			124		°C
Thermal Foldback Hysteresis	$T_{JB(H)}$			15		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}		4.2	4.4	4.6	V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-2.5	0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	125	165	195	mA
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz	87	97	115	mA
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF See Note B 10-90%		50		ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF See Note B 90-10%		80		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	7.2	8.3	12	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA	10.0	12.1	13.4	Ω

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. See Absolute Maximum Ratings "DRAIN Pin Voltage" for details.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

Typical Performance Curves

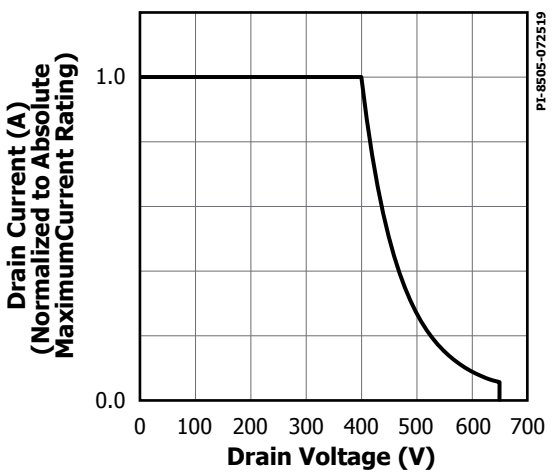

Figure 24. Maximum Allowable Drain Current vs. Drain Voltage (LYT606xC).

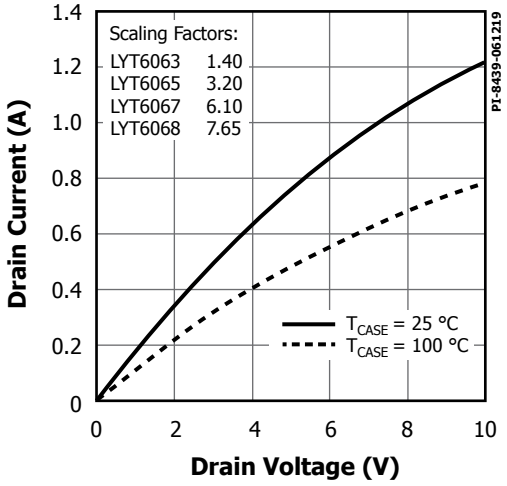

Figure 25. Output Characteristics.

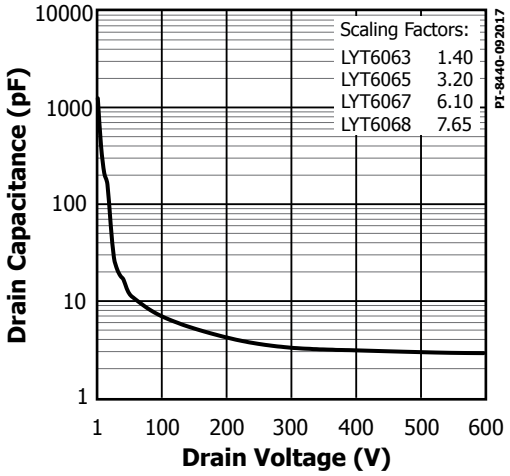

Figure 26. C_{OSS} vs. Drain Voltage.

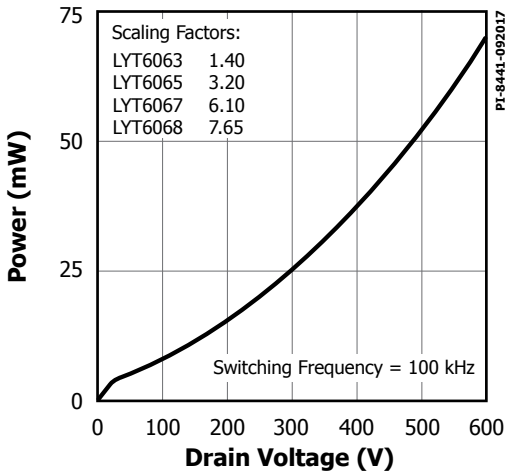

Figure 27. Drain Capacitance Power.

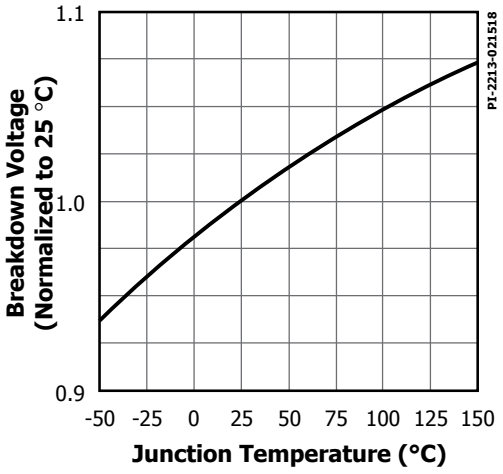

Figure 28. Breakdown vs. Temperature.

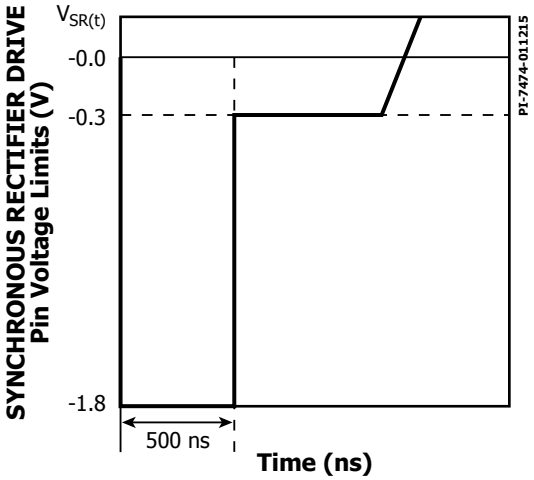

Figure 29. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

Typical Performance Curves

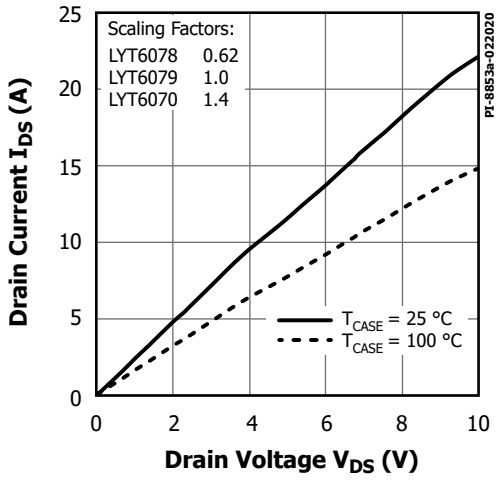

Figure 30. Output Characteristics.

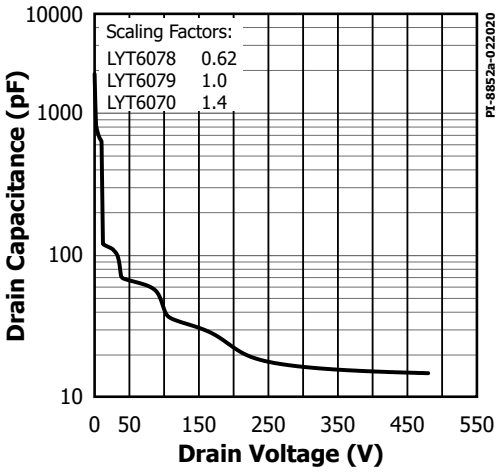

Figure 31. C_{OSS} vs. Drain Voltage.

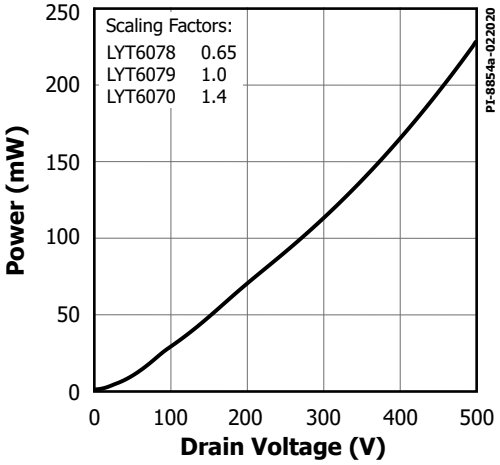

Figure 32. Drain Capacitance Power.

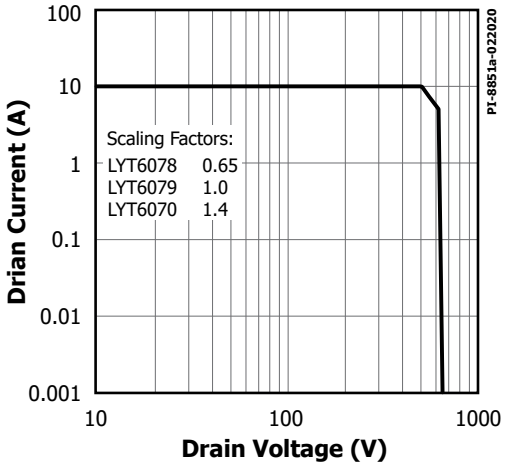

Figure 33. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices LYT6078, LYT6079, LYT6070).

Typical Performance Curves

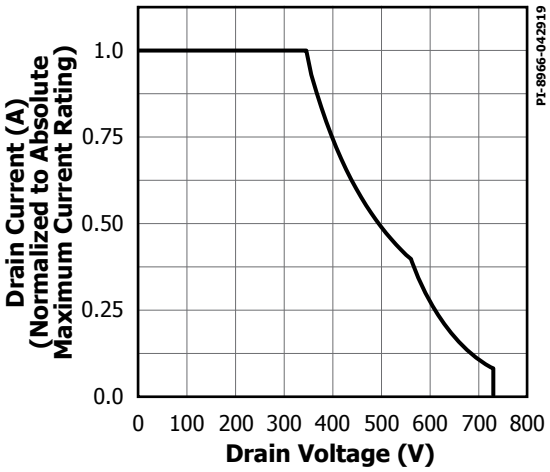

Figure 34. Maximum Allowable Drain Current vs. Drain Voltage (LYT607x).

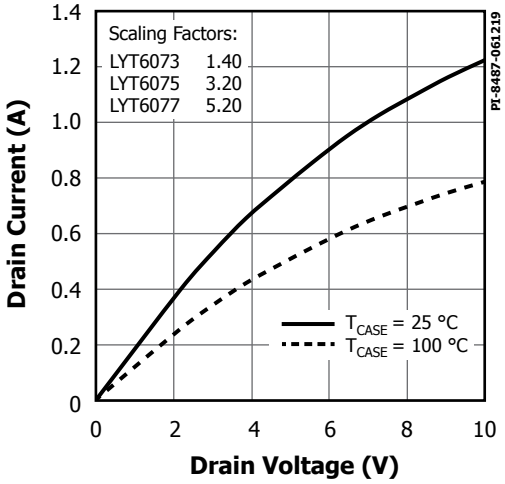

Figure 35. Output Characteristics.

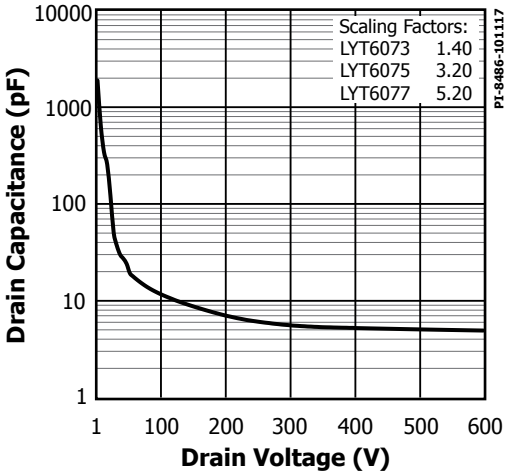

Figure 36. C_{OSS} vs. Drain Voltage.

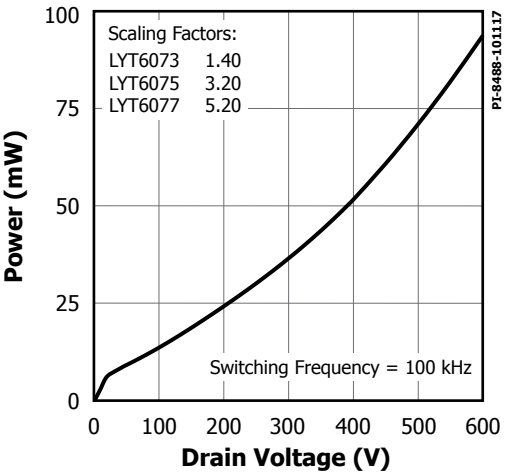

Figure 37. Drain Capacitance Power.

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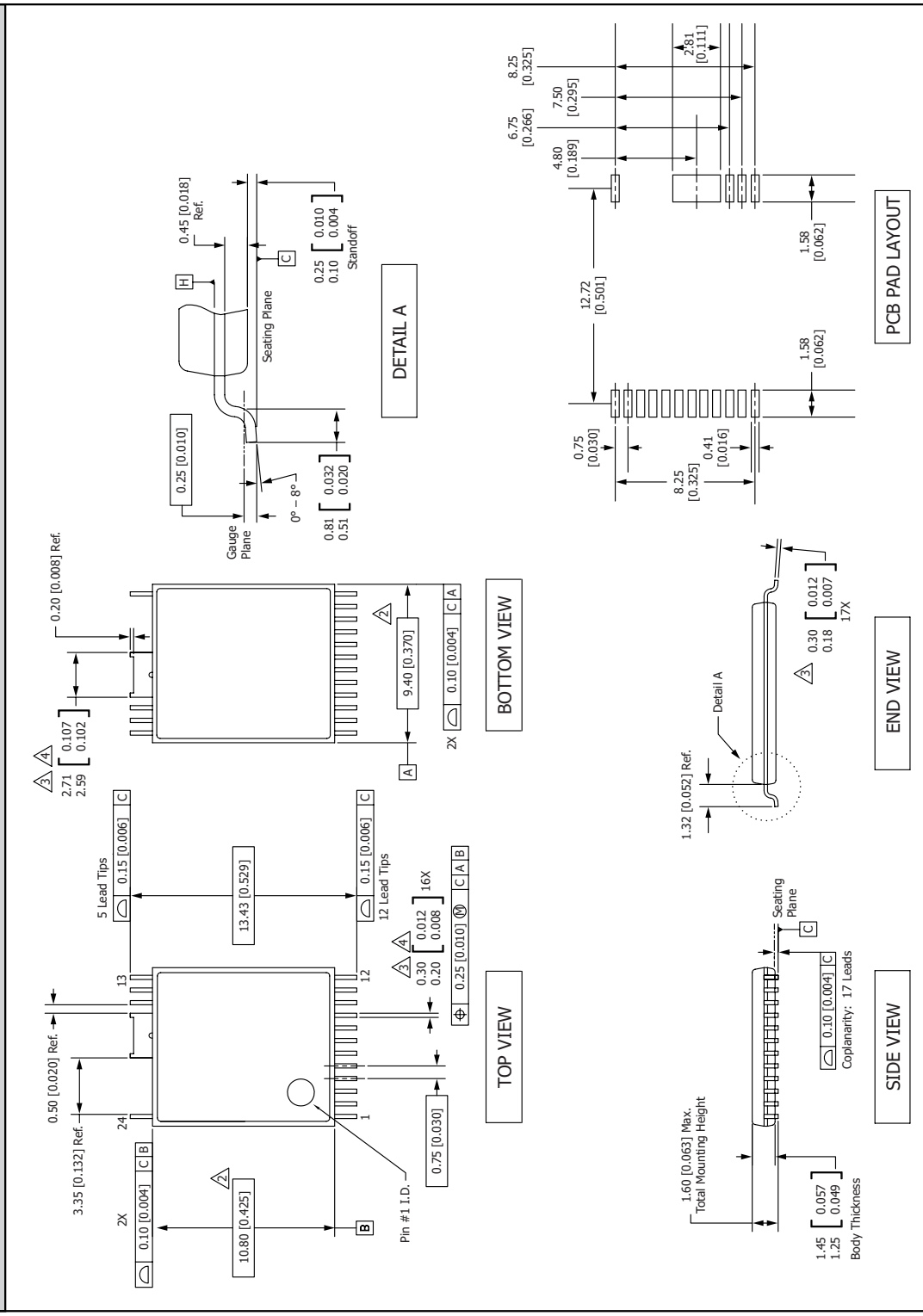

Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

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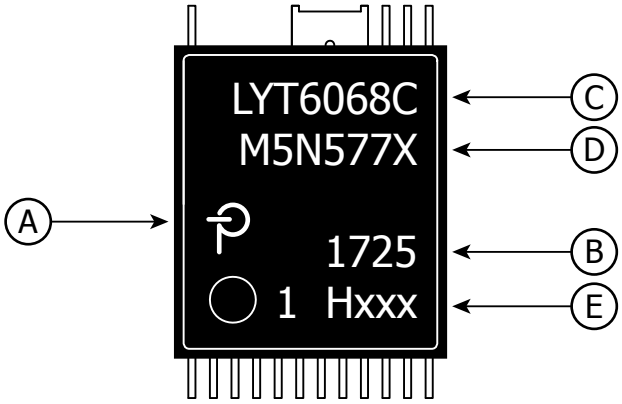
POD-InSOP-24D Rev B

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8881-112718

Feature Code Table

Feature Code	I_{LIM}	I_{LIM+1}	I_{UV+}	I_{UV-}
H125	3.1 A	3.472 A	80 µA	70 µA
H127	3.8 A	4.26 A	80 µA	70 µA
H129	3.1 A	3.472 A	24.4 µA	10 µA
H131	3.8 A	4.26 A	24.4 µA	10 µA

	Common Feature Code			
Part	**H125**	**H127**	**H129**	**H131**
LYT6079C-H1XX	✓	✓	✓	✓
LYT6070C-H1XX	✓	✓	✓	✓

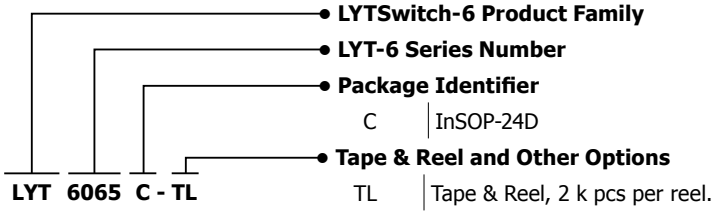
MSL Table

Part Number	MSL Rating
LYT60xxC	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
E	Code L. Added Applications section.	02/18
E	Fixed error in equation on page 14.	06/18
F	Added LYT6079C and LYT6070C parts.	08/18
G	Code A release of LYT6079C and LYT6070C parts. Changed I_{OV-} to I_{OV+} and updated I_{OV+} and $I_{OV(H)}$ Condition, Min, Typ and Max parameter values; updated V_V Condtion. Updated I_{LIMIT} Typ parameter value, deleted BV_{DSS} parameter, added Note A to T_{SD} and $T_{SD(H)}$ Condition parameters. Updated t_R, t_F, R_{PU} and R_{PD} Condition, Min, Typ and Max parameter values. Added Notes B and C. Updated wording on pages 3, 4, 6, 22 and added Note 6 reference in Abs Max Ratings table. Updated $I_{DSS}1$ and I_{DSS2} parameters and Typical Performance Curve Figures 23 and 33.	08/19
H	PCN-19281 – Updated text in PRIMARY BYPASS Pin Capacitor (C_{BPP}) and SECONDARY BYPASS Pin Capacitor (C_{BPS}) sections. Updated parameters V_V, V_{SR} and $I_{BPS(SD)}$.	10/19
I	Added Feature Code and Common Feature Code tables.	11/19
J	Code A release. Added LYT6078C part.	02/20
K	Updated safety information on page 1 and corrected typo in Package drawing on page 33.	06/20
L	Updated Parameter name for V_{FWD}.	03/23

Notes

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