WINSOURCE ELECTRONICS

THE DATASHEET OF

LTM8064IY

58V_{IN}, 6A CVCC Step-Down µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **CVCC: Constant-Voltage, Constant-Current**
- **2-Quadrant: Sources and Sinks Output Current**
- **Parallelable for Increased Output Current, Even from Different Voltage Sources**
- **Adjustable Output Current Up to 7A When Sourcing or 9.1A When Sinking**
- **Wide Input Voltage Range: 6V to 58V**
- **1.2V to 36V Output Voltage**
- Selectable Switching Frequency: 100kHz to 1MHz
- (e1) RoHS Compliant Package
- Programmable Soft-Start
- Tiny (16mm × 11.9mm × 4.92mm) Surface Mount BGA Package

APPLICATIONS

- Short-Circuit Protection or Accurate Output Current Limit
- High Power LED Drive
- Peltier Driver
- Motor Drive
- Battery/Supercap Charging and Cell Balancing

DESCRIPTION

The LTM®8064 is a 58V_{IN}, 6A, constant-voltage, constant-current (CVCC), step-down µModule® (power module) regulator. Included in the package are the switching controller, power switches, inductor and support components. Operating over an input voltage range of 6V to 58V, the LTM8064 supports an output voltage range of 1.2V to 36V. CVCC operation allows the LTM8064 to accurately regulate its output current up to 7A when sourcing and 9.1A when sinking over the entire output range. The output current can be set by a control voltage, a single resistor or a thermistor. To set the switching frequency, simply place a resistor from the RT pin to ground. A resistor from FB to ground will set the output voltage. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8064 is packaged in a thermally enhanced, compact (16mm × 11.9mm × 4.92mm) over-molded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8064 is RoHS compliant.

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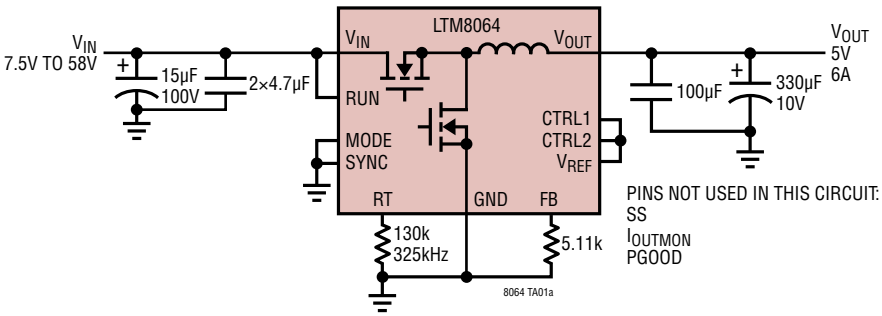
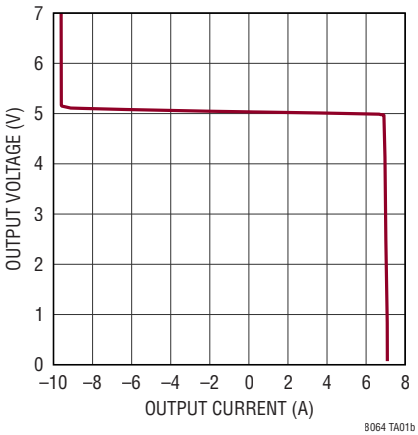
TYPICAL APPLICATION

58V_{IN}, 5V_{OUT} Step-Down CVCC Converter



Output Voltage vs Output Current
V_{IN} = 12V

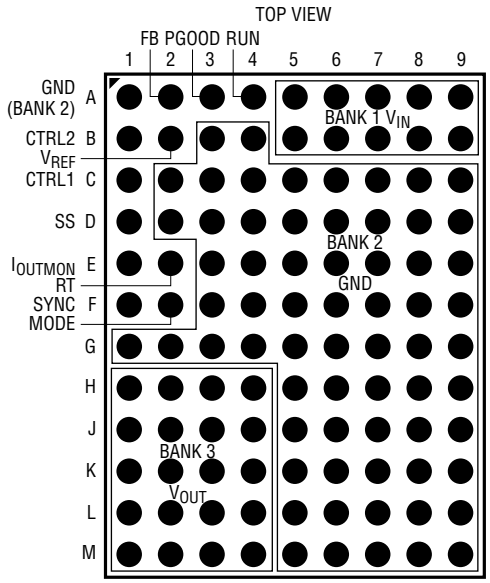


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN 60V
FB, CTRL1, CTRL2, I_{OUTMON} 3V
V_{OUT}.....40V
MODE, SYNC, PGOOD.....6V
Internal Operating Temperature Range .. –40°C to 125°C
Peak Solder Reflow Temperature ..... 245°C
Storage Temperature..... –55°C to 125°C

PIN CONFIGURATION



BGA PACKAGE
108-LEAD (16mm × 11.9mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 6.9°C/W, $\theta_{JCbottom}$ = 2.2°C/W, θ_{JCTOP} = 8.1°C/W, θ_{JB} = 6.0°C/W
WEIGHT = 2.44g, θ VALUES DETERMINED PER JEDEC JESD51-9, 51-12

ORDER INFORMATION

http://www.linear.com/product/LTM8064#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (NOTE 2)
		DEVICE	FINISH CODE			
LTM8064EY#PBF	SAC305 (RoHS)	LTM8064Y	e1	BGA	3	–40°C to 125°C
LTM8064IY#PBF	SAC305 (RoHS)	LTM8064Y	e1	BGA	3	–40°C to 125°C
LTM8064IY	SnPb (63/37)	LTM8064Y	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: http://www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating internal temperature range, otherwise specifications are at T_A = 25°C. RUN = 3V unless otherwise noted (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN} Falling	●			6	V
Output DC Voltage	R_{FB} Open R_{FB} = 562Ω			1.2 36		V V
Output DC Sourcing Current	CTRL1, CTRL2 = 1.5V				6	A
Quiescent Current Into V_{IN}	V_{IN} = 24V, RUN = 0V V_{IN} = 24V, No Load, MODE = 0V			0.2 2.5	6 5	µA mA
Line Regulation	6V < V_{IN} < 58V, I_{OUT} = 1A			0.1		%
Load Regulation	V_{IN} = 24V, 0A < I_{OUT} < 6A			0.5		%
Output RMS Voltage Ripple	V_{IN} = 24V, I_{OUT} = 4.5A			10		mV
Switching Frequency	R_T = 40.2k R_T = 453k			1000 100		kHz kHz
Voltage at FB Pin		●	1.176	1.20	1.224	V
Current Out of FB Pin	FB = 0V, V_{OUT} = 1V			61.75		µA
RUN Pin Current	RUN = 1.4V			5		µA
RUN Threshold Voltage (Falling)			1.46	1.52	1.58	V
RUN Input Hysteresis				185		mV
CTRL1 Control Range			0		1.5	V
CTRL1 Pin Current				20		nA
CTRL1 Sourcing Current Limit	CTRL1 = 1.5V CTRL1 = 0.75V		6.3 2.85	7.0 3.55	7.7 4.25	A A
CTRL1 Sinking Current Limit	CTRL1 = 1.5V CTRL1 = 0.75V		8.2 4.5	9.1 5.75	10.0 6.9	A A
CTRL2 Control Range			0		1.5	V
CTRL2 Pin Current				100		nA
CTRL2 Sourcing Current Limit	CTRL2 = 1.5V CTRL2 = 0.75V		6.3 2.85	7.0 3.55	7.7 4.25	A A
CTRL2 Sinking Current Limit	CTRL2 = 1.5V CTRL2 = 0.75V		8.2 4.5	9.1 5.75	10.0 6.9	A A
V_{REF} Voltage	0.5mA Load		1.89		2.06	V
SS Pin Current				11		µA
SYNC Input Low Threshold	f_{SYNC} = 600kHz				1.4	V
SYNC Input High Threshold	f_{SYNC} = 600kHz		2.3			V
SYNC Bias Current	SYNC = 0V SYNC = 5V				1 1	µA µA
MODE Low Threshold Voltage					2	V
MODE High Threshold Voltage			3			V
MODE Bias Current	MODE = 0V			50		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating internal temperature range, otherwise specifications are at T_A = 25°C. RUN = 3V unless otherwise noted (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Upper Threshold Voltage	FB Rising			1.36		V
PGOOD Upper Threshold Hysteresis				40		mV
PGOOD Lower Threshold Voltage	FB Falling			1.06		V
PGOOD Lower Threshold Hysteresis				40		mV
PGOOD Sink Current	PGOOD = 2V			8		mA
PGOOD Leakage Current	PGOOD = 6V				1	µA
I_{OUTMON} Voltage	I_{OUT} = 7.1A I_{OUT} = 3.55A		1.27 0.57		1.68 0.96	V V

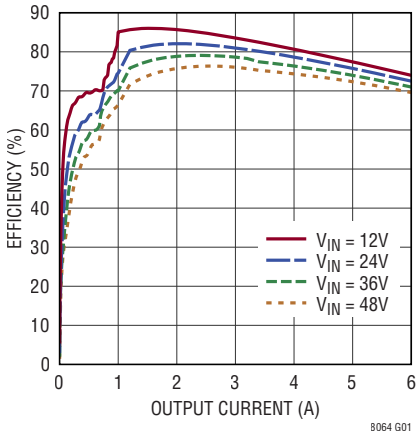
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This µModule regulator includes overtemperature protection that is intended to protect the device during momentary overload conditions. Internal temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum internal temperature may impair device reliability.

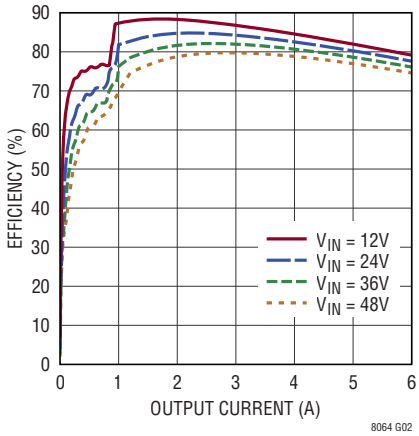
Note 3: The LTM8064E is guaranteed to meet performance specifications from 0°C to 125°C internal operating temperature. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8064I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

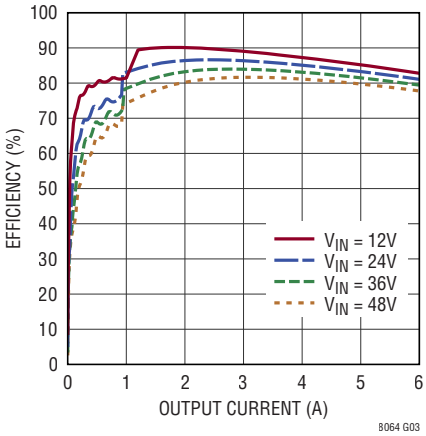
Efficiency vs Output Current
V_{OUT} = 1.8V



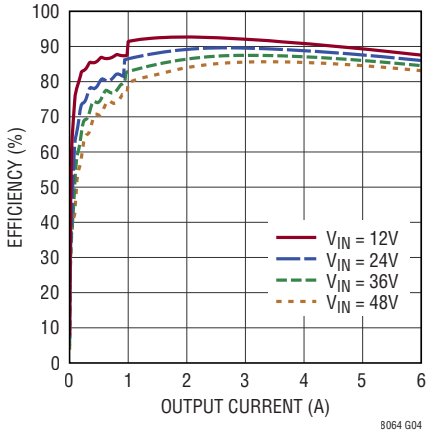
Efficiency vs Output Current
V_{OUT} = 2.5V



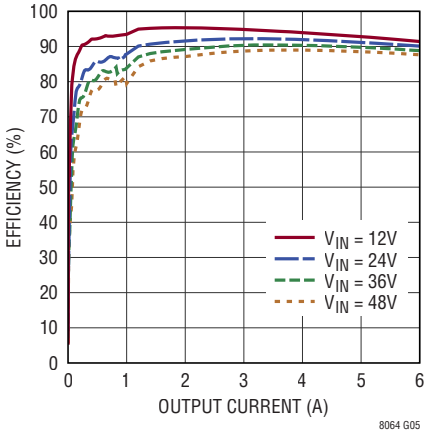
Efficiency vs Output Current
V_{OUT} = 3.3V



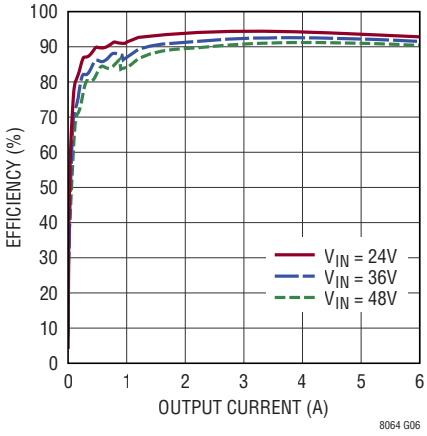
Efficiency vs Output Current
V_{OUT} = 5V



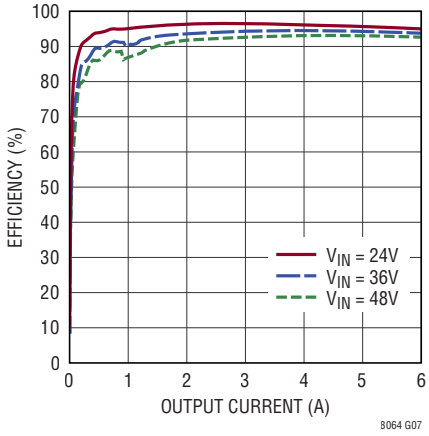
Efficiency vs Output Current
V_{OUT} = 8V



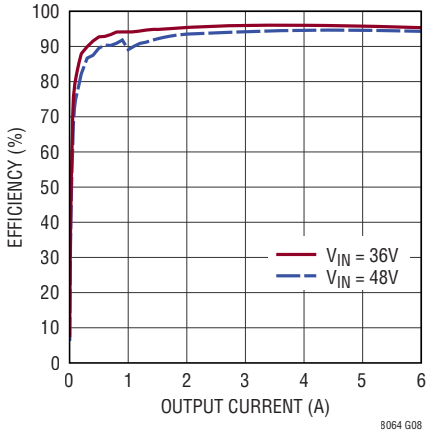
Efficiency vs Output Current
V_{OUT} = 12V



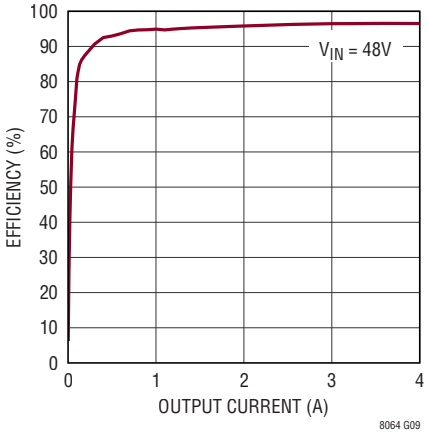
Efficiency vs Output Current
V_{OUT} = 18V



Efficiency vs Output Current
V_{OUT} = 24V

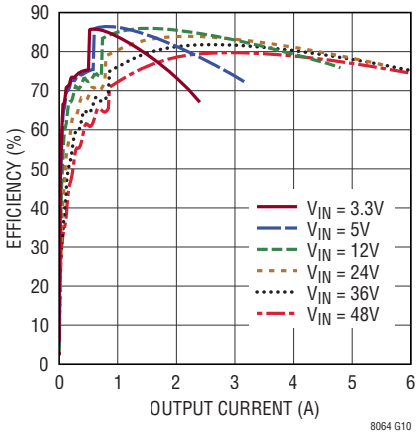


Efficiency vs Output Current
V_{OUT} = 36V

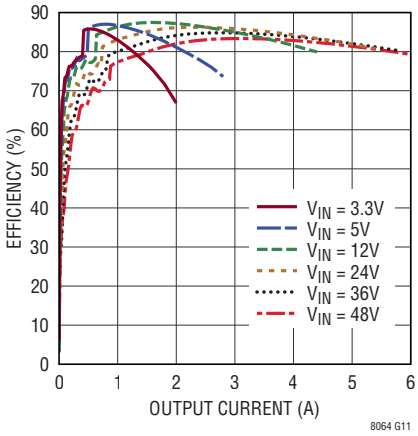


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

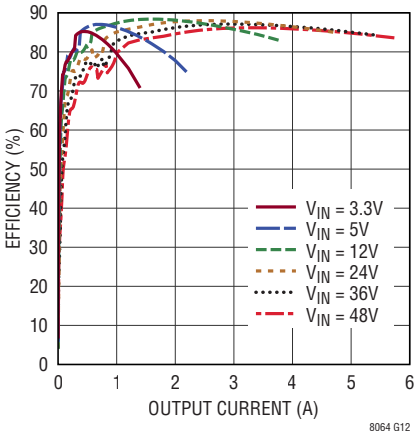
Efficiency vs Output Current
V_{OUT} = –3.3V



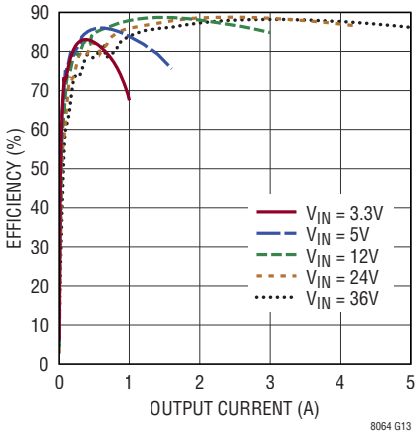
Efficiency vs Output Current
V_{OUT} = –5V



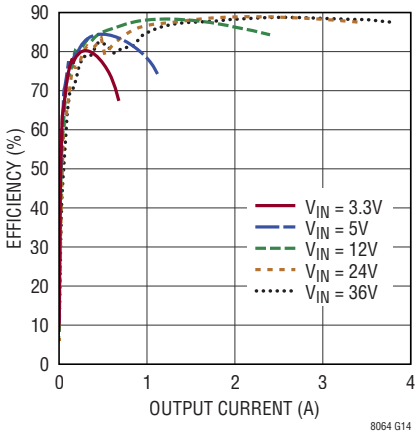
Efficiency vs Output Current
V_{OUT} = –8V



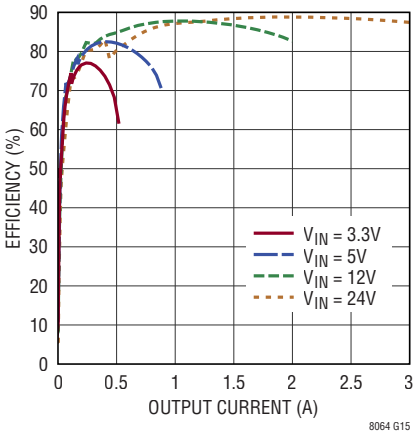
Efficiency vs Output Current
V_{OUT} = –12V



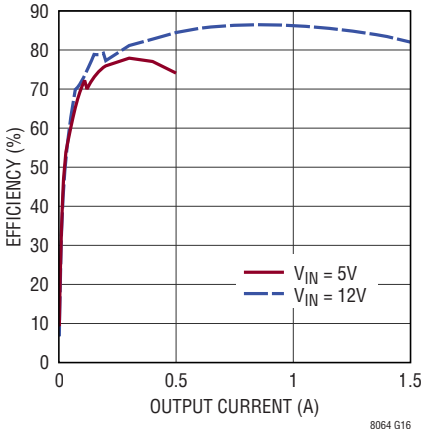
Efficiency vs Output Current
V_{OUT} = –18V



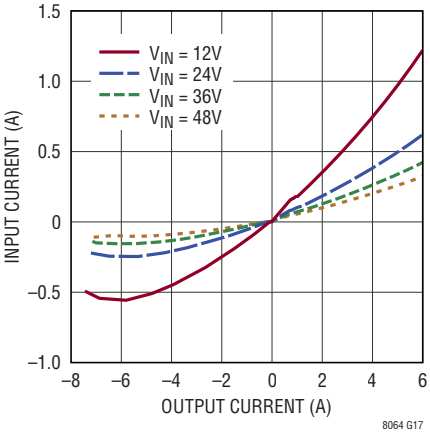
Efficiency vs Output Current
V_{OUT} = –24V



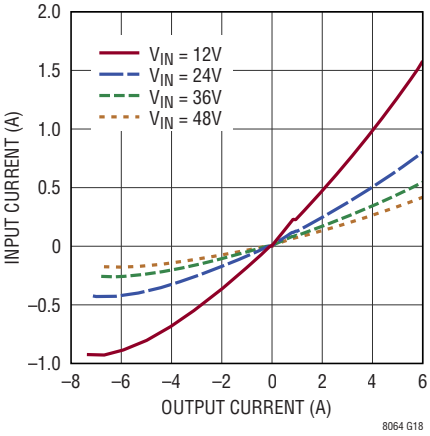
Efficiency vs Output Current
V_{OUT} = –36V



Input Current vs Output Current
V_{OUT} = 1.8V

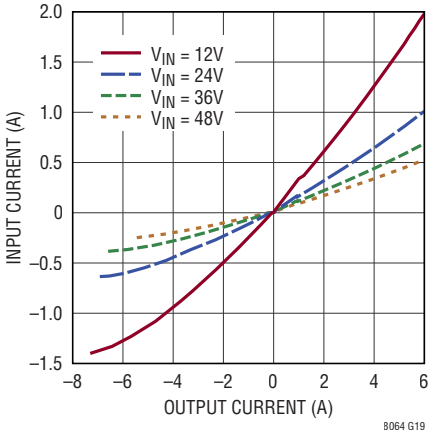


Input Current vs Output Current
V_{OUT} = 2.5V

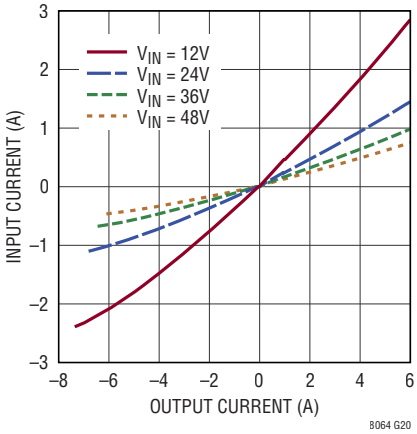


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

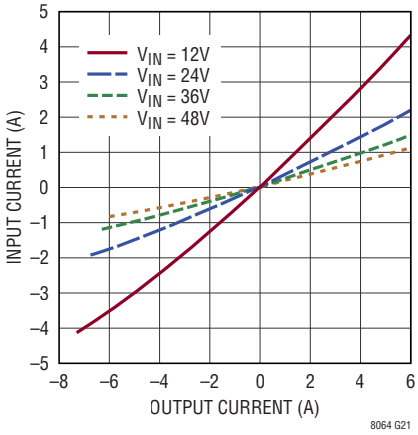
Input Current vs Output Current V_{OUT} = 3.3V



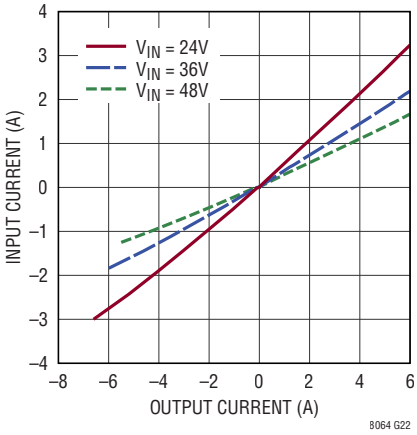
Input Current vs Output Current V_{OUT} = 5V



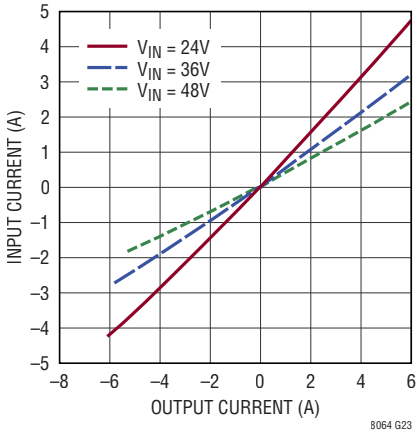
Input Current vs Output Current V_{OUT} = 8V



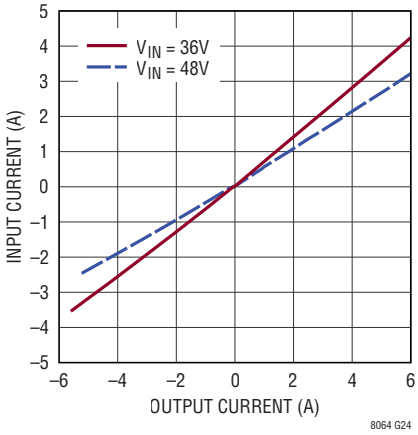
Input Current vs Output Current V_{OUT} = 12V



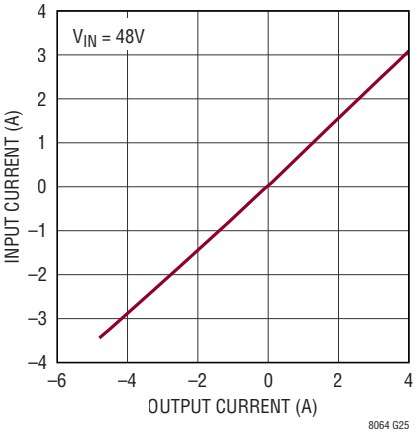
Input Current vs Output Current V_{OUT} = 18V



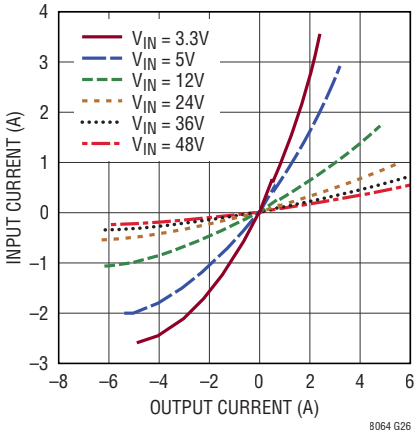
Input Current vs Output Current V_{OUT} = 24V



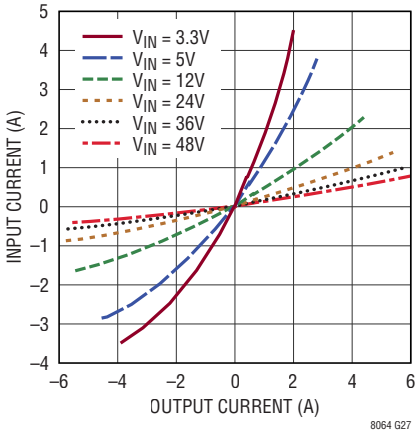
Input Current vs Output Current V_{OUT} = 36V



Input Current vs Output Current V_{OUT} = −3.3V

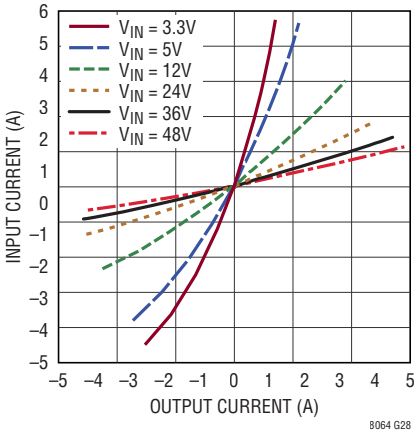


Input Current vs Output Current V_{OUT} = −5V

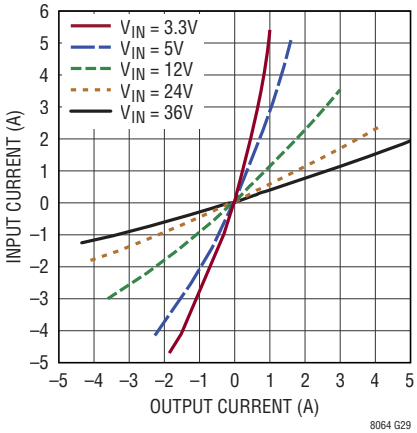


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

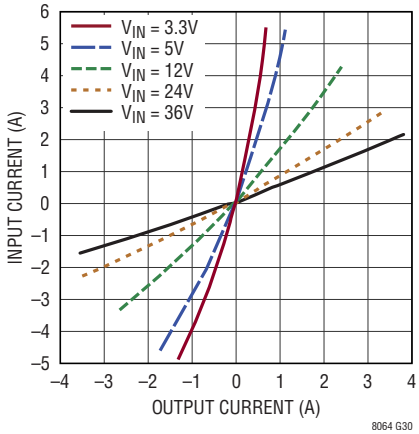
Input Current vs Output Current
V_{OUT} = –8V



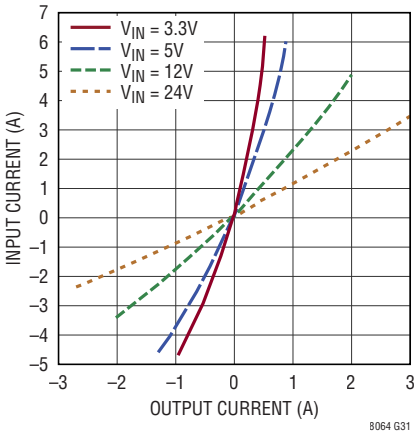
Input Current vs Output Current
V_{OUT} = –12V



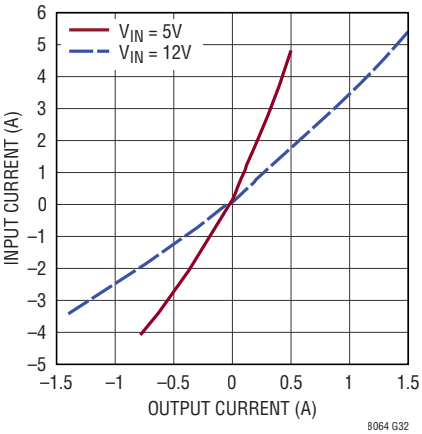
Input Current vs Output Current
V_{OUT} = –18V



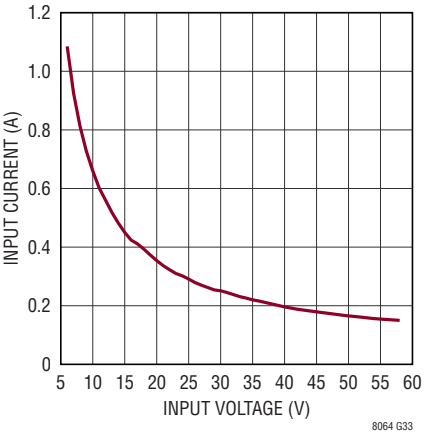
Input Current vs Output Current
V_{OUT} = –24V



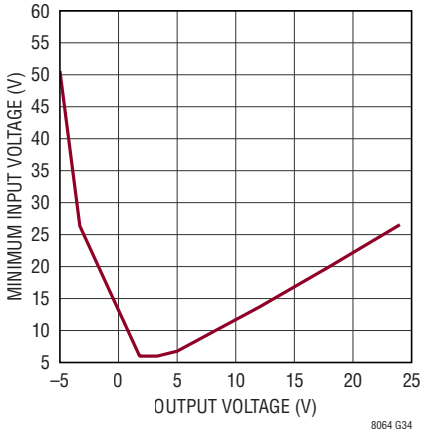
Input Current vs Output Current
V_{OUT} = –36V



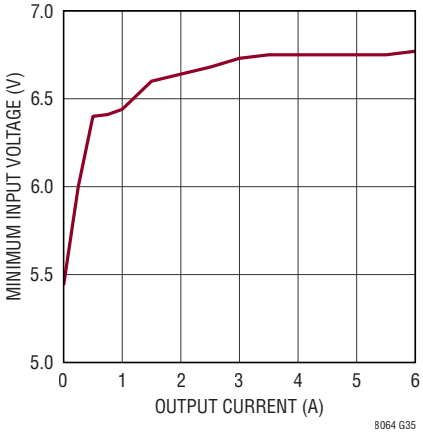
Input Current vs Input Voltage
Output Shorted



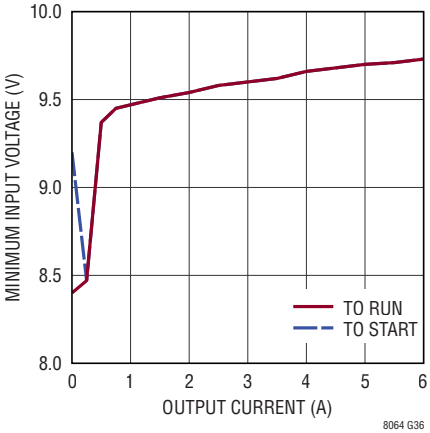
Minimum Input Voltage
vs Output Voltage, I_{OUT} = 6A



Minimum Input Voltage
vs Output Voltage, V_{OUT} = 5V

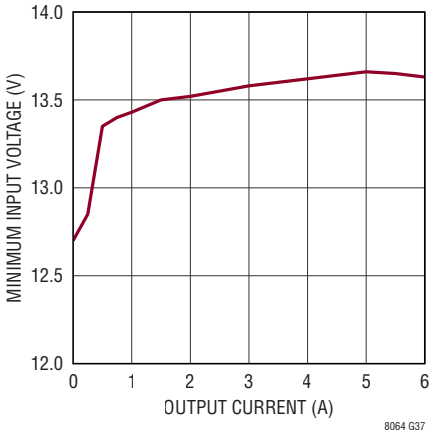


Minimum Input Voltage
vs Output Current, V_{OUT} = 8V

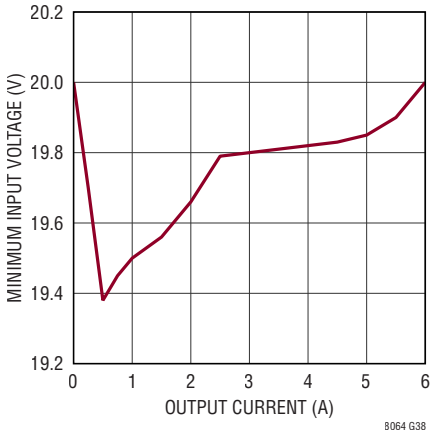


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

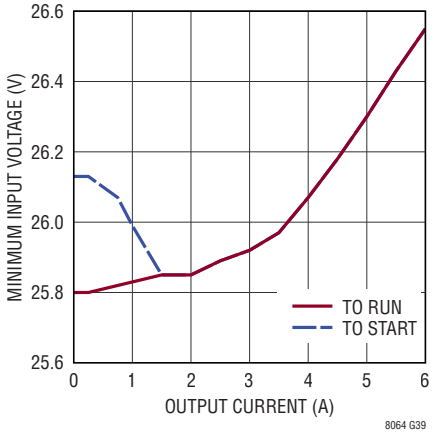
Minimum Input Voltage vs Output Current, V_{OUT} = 12V



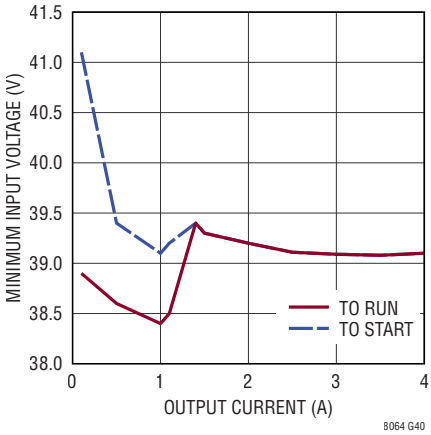
Minimum Input Voltage vs Output Current, V_{OUT} = 18V



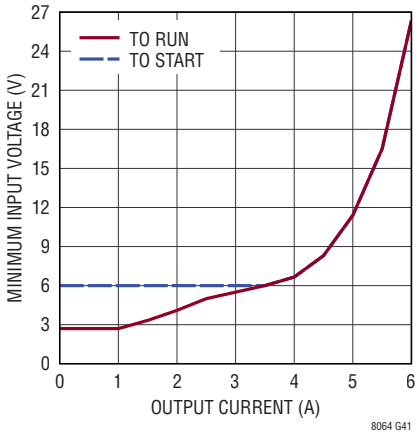
Minimum Input Voltage vs Output Current, V_{OUT} = 24V



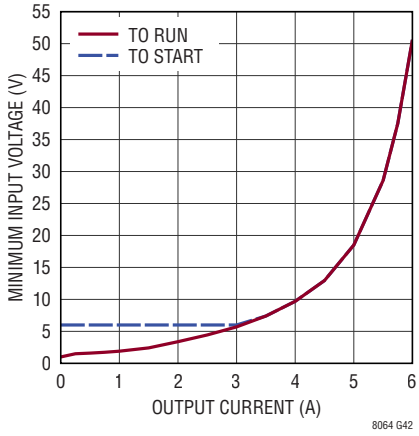
Minimum Input Voltage vs Output Current, V_{OUT} = 36V



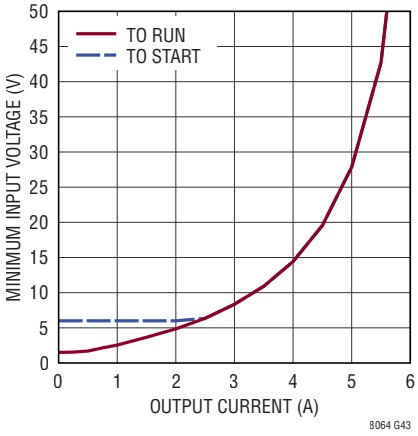
Minimum Input Voltage vs Output Current, V_{OUT} = –3.3V



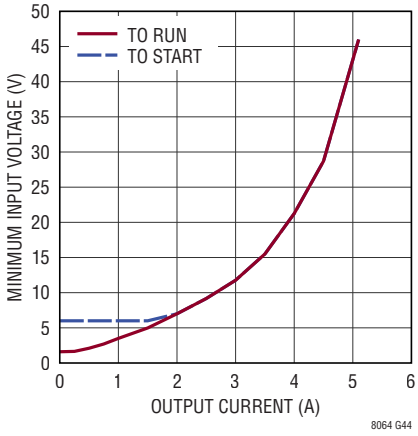
Minimum Input Voltage vs Output Current, V_{OUT} = –5V



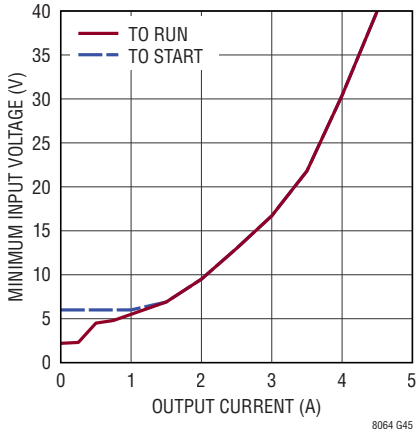
Minimum Input Voltage vs Output Current, V_{OUT} = –8V



Minimum Input Voltage vs Output Current, V_{OUT} = –12V

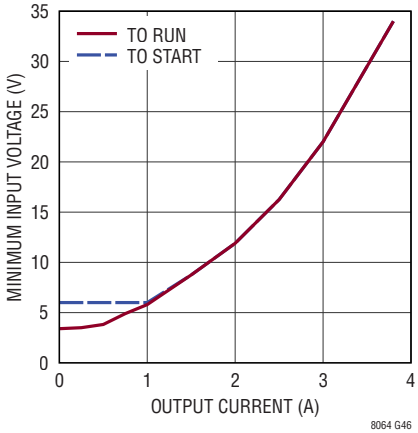


Minimum Input Voltage vs Output Current, V_{OUT} = –18V

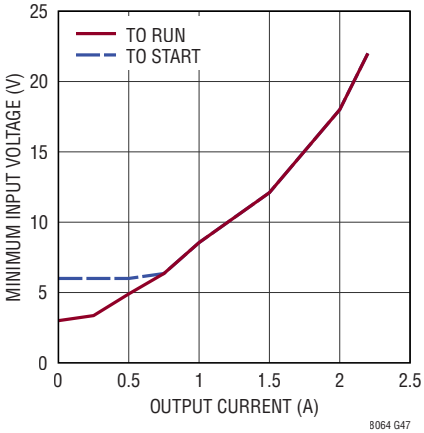


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

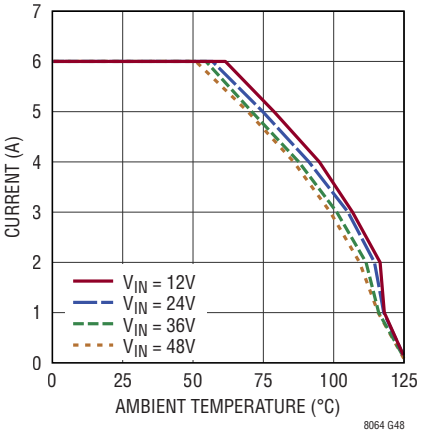
Minimum Input Voltage vs Output Current, V_{OUT} = –24V



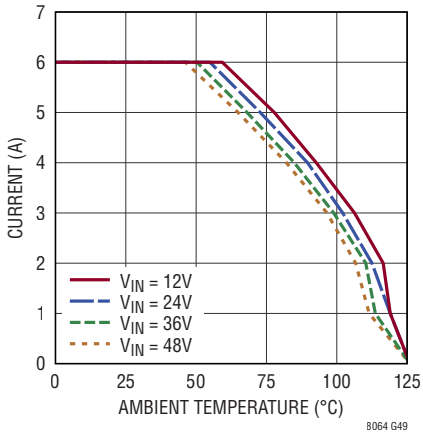
Minimum Input Voltage vs Output Current, V_{OUT} = –36V



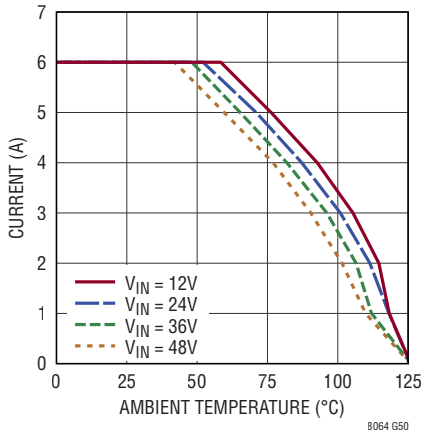
Derating Curve V_{OUT} = 1.8V



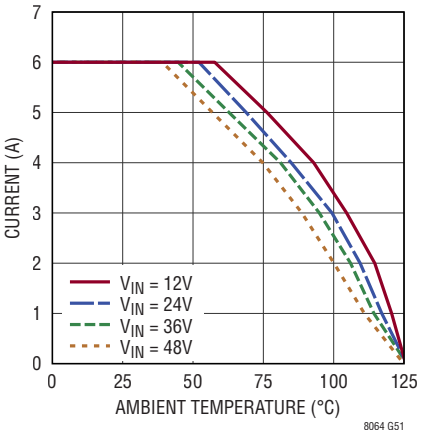
Derating Curve V_{OUT} = 2.5V



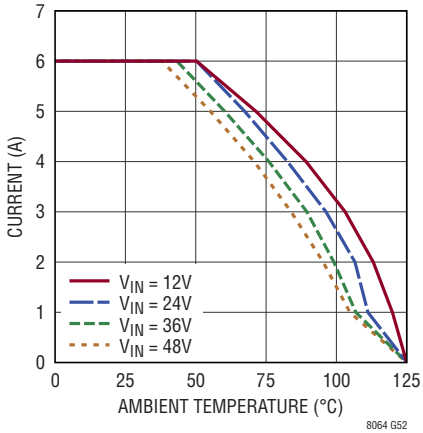
Derating Curve V_{OUT} = 3.3V



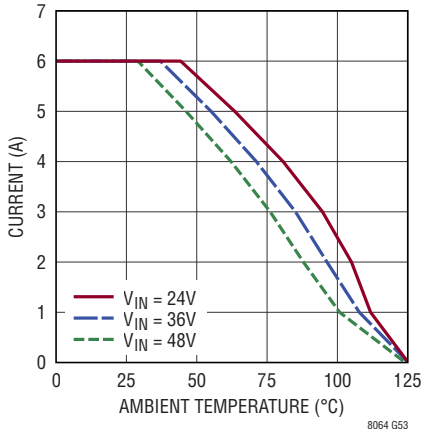
Derating Curve V_{OUT} = 5V



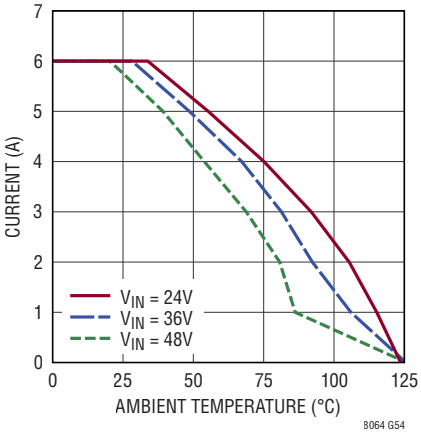
Derating Curve V_{OUT} = 8V



Derating Curve V_{OUT} = 12V

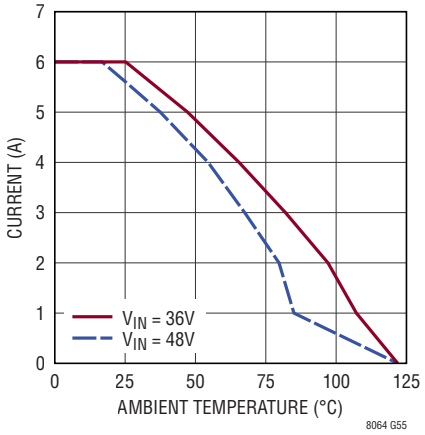


Derating Curve V_{OUT} = 18V

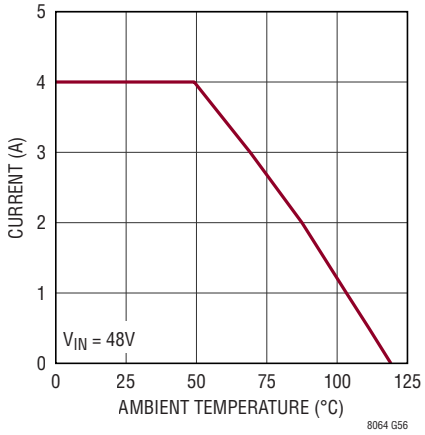


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

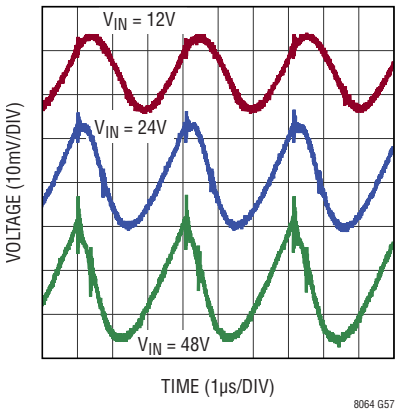
Derating Curve
V_{OUT} = 24V



Derating Curve
V_{OUT} = 36V

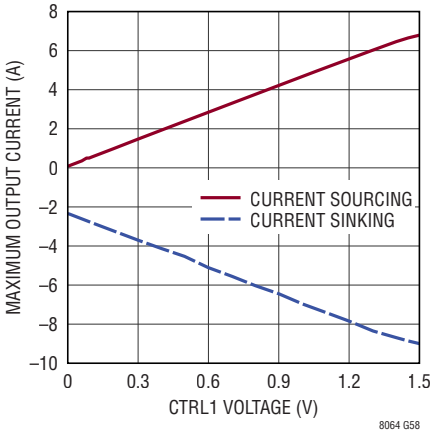


Output Voltage Ripple
V_{OUT} = 5V, I_{OUT} = 6A

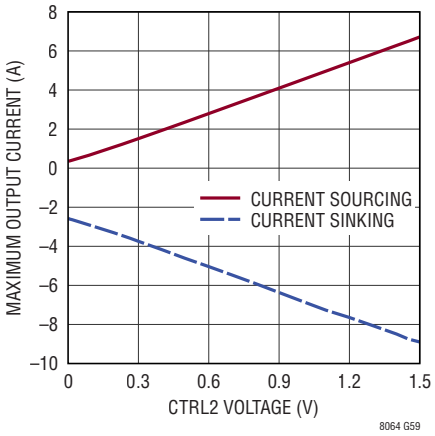


MEASURED WITH HP461N, 150MHz AMPLIFIER

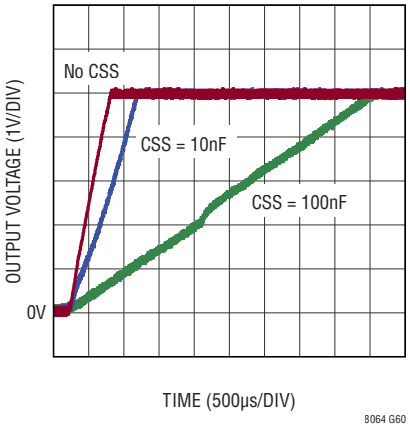
Maximum Output Current vs
CTRL1 Voltage (CTRL2 = 2V)



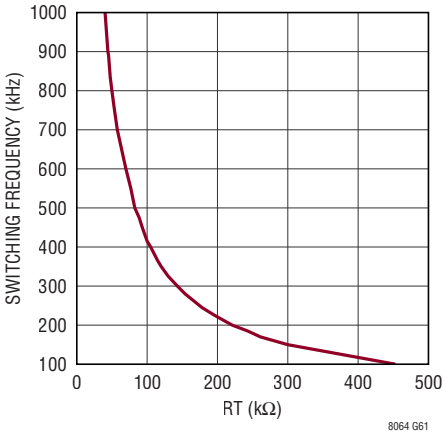
Maximum Output Current vs
CTRL2 Voltage (CTRL1 = 2V)



Start-Up Waveform Using Various
SS Capacitors, V_{IN} = 12V, I_{OUT} = 2A



Switching Frequency vs RT Value



PIN FUNCTIONS

V_{IN} (Bank 1): The V_{IN} pin supplies current to the LTM8064's internal regulator and to the internal power switches. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8064 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8064 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{FB}) to this net.

V_{OUT} (Bank 3): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

FB (Pin A2): The LTM8064 regulates its FB pin to 1.2V (typical). Connect the feedback resistor from this pin to ground. The value of R_{FB} is given by the equation:

$$R_{FB} = \frac{19.44}{(V_{OUT} - 1.2)}$$

where R_{FB} is in kΩ.

PGOOD (Pin A3): Power Good Pin. The PGOOD pin is the open-drain output of an internal comparator. PGOOD remains low unless the FB pin voltage is within the range in the Electrical Characteristics table. If this function is not used, float this pin.

RUN (Pin A4): The RUN pin acts as an enable pin and turns on the internal circuitry at 1.705V (typical). The pin does not have any pull-up or pull-down, requiring a voltage bias for normal part operation. Full shutdown occurs below about 0.5V. If unused, the RUN pin may be tied to V_{IN}. Drive with a source that has an impedance greater than 20Ω.

CTRL2 (Pin B1): Connect a resistor/NTC thermistor from the CTRL2 pin to GND to reduce the maximum regulated output current of the LTM8064 in response to temperature. The maximum control voltage is 1.5V (typical). If this function is not used, tie to V_{REF}.

V_{REF} (Pin B2): Buffered 2V reference capable of 0.5mA drive. If this function is not used, float this pin. Do not drive this pin with an external source.

CTRL1 (Pin C1): The CTRL1 pin reduces the maximum regulated output current of the LTM8064. The maximum control voltage is 1.5V (typical). If this function is not used, tie to V_{REF}.

SS (Pin D1): Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The soft-start pin has an 11µA (typical) charging current. When the voltage at this pin is lower than voltages at CTRL1 and CTRL2, it overrides both signals and determines the regulated current. See the Soft-Start section in the Applications Information for more information. Do not drive this pin with an external source. If this function is not used, float this pin.

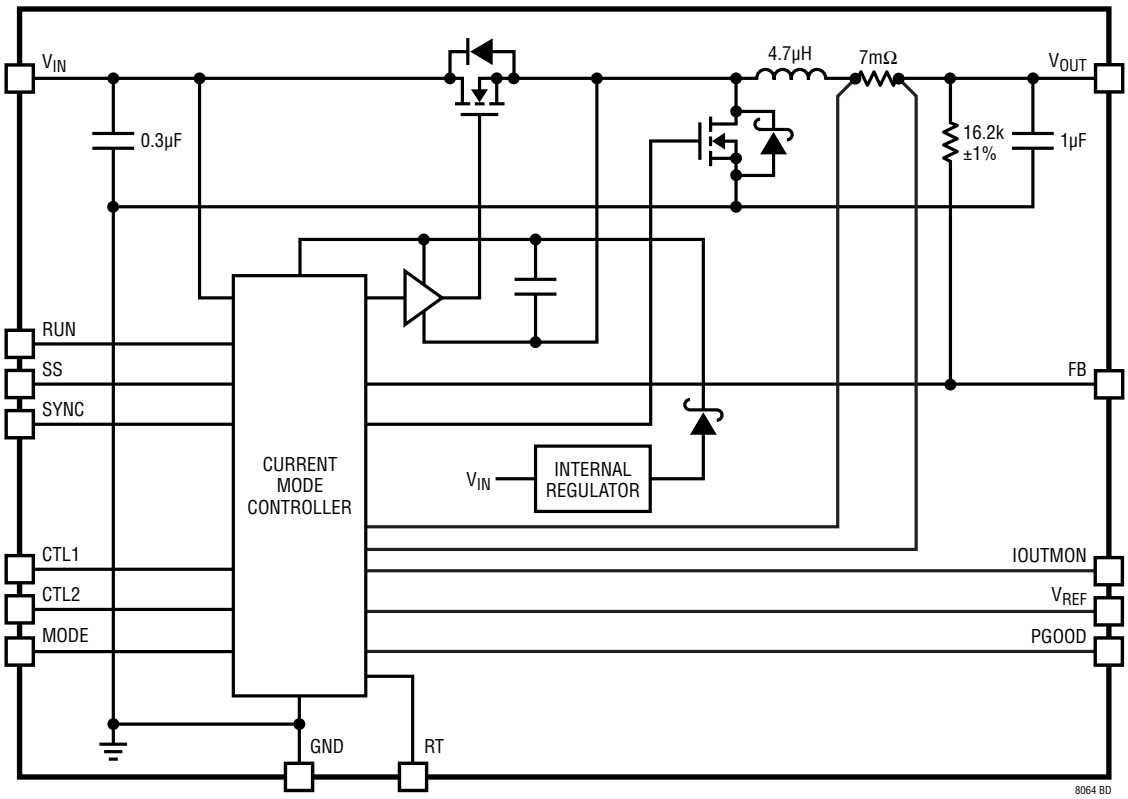
I_{OUTMON} (Pin E1): I_{OUTMON} is the buffered output of the output current sense amplifier. This voltage output enables monitoring the averaged output current of the load with a voltage of $V_{IOUTMON} = 0.211 \bullet I_{LOAD}$ at 25°C. The capacitive loading of this pin should be less than 1nF. This feature is disabled when the part is used to sink current. If this function is not used, float this pin.

RT (Pin E2): The RT pin is used to program the switching frequency of the LTM8064 by connecting a resistor from this pin to ground. The switching frequency is programmable from 100kHz to 1MHz. The Applications Information section of the data sheet includes a table (Table 2) to determine the resistance value based on the desired switching frequency. When using the SYNC function, set the frequency at least 20% lower than the SYNC pulse frequency. Do not leave this pin open or drive with an external source.

SYNC (Pin F1): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. This pin should be grounded when not in use. When laying out the board, avoid noise coupling to or from the SYNC trace. See the Synchronization section in Applications Information.

MODE (Pin F2): Float the MODE pin to operate the µModule in forced continuous mode (FCM). To operate in discontinuous mode (DCM), ground the MODE pin. By default, the MODE pin is pulled up to about 5V by an internal 100k resistor. See the Applications Information section for details about the different switching modes.

BLOCK DIAGRAM



OPERATION

The LTM8064 is a standalone, nonisolated, constant-voltage, constant-current, step-down, switching DC/DC power supply that can source up to 6A output current. This µModule provides a precisely regulated output voltage from 1.21V to 36V programmable via one external resistor. The input voltage range is 6V to 58V. Make sure the input voltage is high enough to support the desired output voltage and load current over the operating range and environment.

As shown in the Block Diagram, the LTM8064 contains a current mode controller, power switches, power inductor, and a modest amount of input and output capacitance. Add external components per Table 1 to achieve robust operation.

The LTM8064 utilizes fixed-frequency, average current mode control to accurately regulate the output current, independently from the output voltage. This is an ideal solution for applications requiring a regulated current source. Once the output has reached the regulation voltage determined by the resistor from the FB pin to ground, the output current will be reduced by the voltage regulation loop.

The LTM8064 is capable of operating as a 2-quadrant device, meaning it can either sink or source current in order to regulate its output voltage, when the MODE pin is floated. When the MODE pin is grounded, the µModule will operate as a 1-quadrant device, meaning it can only source current.

If the load forces current into the LTM8064 while in 1-quadrant mode, the output voltage will rise. While in 2-quadrant mode, the LTM8064 will sink current to keep the output voltage in regulation.

The LTM8064 will be able to maintain the output voltage at the target regulation point as long as the current from the load does not exceed its sinking current limit (9.1A typical). Exceeding this current limit will cause the output voltage to rise. If the output voltage of the LTM8064 rises above the input voltage, current will flow through an internal power diode and the output voltage will be clamped to a diode drop above the input voltage.

When the LTM8064 is sinking current, it maintains its output voltage regulation by power conversion, not power dissipation. This means that the energy provided to the LTM8064 is delivered to its input power bus. The power bus must be able to accept or use the energy, otherwise, the power bus's voltage will rise. This can raise the LTM8064 input voltage above the absolute maximum voltage. Please see the Input Precautions section for further details.

By floating or grounding the MODE pin, the LTM8064 can operate in either FCM (forced continuous mode) or DCM (discontinuous conduction mode), respectively. In FCM, the part will not skip cycles when the load approaches zero amps. This may be particularly useful in applications where the synchronization function is used, or any time discontinuous switching is undesirable. Do not load current share with all parts operating in FCM only. The part uses a master/slave relationship to current share, with the master operating in FCM and each slave operating in DCM. In DCM, the part may skip cycles during light-load conditions. In this operating mode, the part is capable of load current sharing with other LTM8064 µModules (or LTM8026s as slaves only).

The current control loop has two reference inputs, determined by the voltage at the analog control pins, CTRL1 and CTRL2. CTRL1 is typically used to set the maximum

OPERATION

allowable current output of the LTM8064, while CTRL2 is typically used with a NTC thermistor to reduce the output current in response to temperature. The lower of the two analog voltages on CTRL1 and CTRL2 determines the regulated output current. The analog control range of both the CTRL1 and CTRL2 pins are from 0V to 1.5V. As shown in the Typical Performance Characteristics section, the sourcing and sinking currents are not symmetric.

The RUN pin functions as a precision enable pin. When the voltage at the RUN pin is lower than 1.52V (typical), switching is terminated. Below the turn-on threshold, the RUN pin sinks 5µA (typical). This current can be used with a resistor between RUN and V_{IN} to set the hysteresis.

During start-up, the SS pin is held low until the part is enabled, after which the capacitor at the soft-start pin is charged with an 11µA (typical) current source. See the Soft-Start section in the Applications Information for more information.

The LTM8064 contains a power good comparator which trips when the FB pin is out of regulation. The PGOOD output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8064 is enabled and V_{IN} is above 6V.

The LTM8064 is equipped with a thermal shutdown to protect the device during momentary overload conditions. It is set above the 125°C absolute maximum internal temperature rating to avoid interfering with normal specified operation. Internal device temperatures will exceed the absolute maximum rating when the overtemperature protection is active. Continuous or repeated activation of the thermal shutdown may impair device reliability. During thermal shutdown, all switching is terminated and the SS pin is driven low.

The switching frequency is determined by a resistor from the RT pin to GND. The LTM8064 may also be synchronized to an external clock through the use of the SYNC pin.

APPLICATIONS INFORMATION

The design process is summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.

2. Apply the recommended C_{IN}, C_{OUT}, R_{FB} and R_T values.

While these component combinations have been tested for proper operation, it is necessary for the user to verify proper operation over the intended system's input voltage, load and environmental conditions. The maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8064 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values may yield improved dynamic response, but using values that are too large may also result in undesirable operation.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration (T_A = 25°C. See Typical Performance Characteristics for Load Conditions)

V_{IN} Range (V)	V_{OUT} (V)	C_{IN}*	C_{OUT}*	R_{FB} (Ω)	$f_{OPTIMAL}$ (kHz)	$RT_{OPTIMAL}$ (kΩ)	f_{MAX} (kHz)	RT_{MIN} (kΩ)
6V to 36V	1.2	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	Open	170	261	200	221
6V to 36V	1.5	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	64.9k	175	255	245	178
6V to 36V	1.8	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	32.4k	180	249	300	143
6V to 36V	2.2	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	19.1k	200	221	365	115
6V to 36V	2.5	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	15.0k	225	196	415	100
6V to 36V	3.3	2x10µF, 1210, 50V	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	9.31k	300	143	550	76.8
7.5V to 36V	5	2x10µF, 1210, 50V	330µF, 10V, 35mΩ, Tantalum 100µF, 1210, 6.3V, X5R, Ceramic	5.11k	325	130	835	47.5
10.5V to 36V	8	2x10µF, 1210, 50V	150µF, 16V, 30mΩ, Tantalum 100µF, 1210, 10V, X5R, Ceramic	2.87k	350	124	1000	40.2
14.5V to 36V	12	2x10µF, 1210, 50V	150µF, 16V, 30mΩ, Tantalum 47µF, 1210, 16V, X5R, Ceramic	1.78k	415	100	1000	40.2
21V to 36V	18	2x10µF, 1210, 50V	100µF, 25V, 100mΩ, Tantalum 22µF, 1210, 25V, X5R, Ceramic	1.15k	450	95.3	1000	40.2
27V to 36V	24	2x10µF, 1210, 50V	47µF, 35V, 200mΩ, Tantalum 22µF, 1210, 25V, X5R, Ceramic	845	475	88.7	1000	40.2
6V to 58V	1.2	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	open	170	261	180	249
6V to 58V	1.5	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	64.9k	175	255	185	243
6V to 58V	1.8	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	32.4k	180	249	200	221
6V to 58V	2.2	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	19.1k	200	221	245	178
6V to 58V	2.5	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	15.0k	225	196	280	154
6V to 58V	3.3	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	470µF, 6.3V, 45mΩ, Tantalum 220µF, 1206, 4V, X5R, Ceramic	9.31k	300	143	365	115
7.5V to 58V	5	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	330µF, 10V, 35mΩ, Tantalum 100µF, 1210, 6.3V, X5R, Ceramic	5.11k	325	130	550	76.8
10.5V to 58V	8	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	150µF, 16V, 30mΩ, Tantalum 100µF, 1210, 10V, X5R, Ceramic	2.87k	350	124	890	45.2
14.5V to 58V	12	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	150µF, 16V, 30mΩ, Tantalum 47µF, 1210, 16V, X5R, Ceramic	1.78k	415	100	1000	40.2
21V to 58V	18	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	100µF, 25V, 100mΩ, Tantalum 22µF, 1210, 25V, X5R, Ceramic	1.15k	450	95.3	1000	40.2
27V to 58V	24	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	47µF, 35V, 200mΩ, Tantalum 22µF, 1210, 25V, X5R, Ceramic	845	475	88.7	1000	40.2
40V to 58V	36	15µF, 100V, OS-CON 2x4.7µF, 1206, 100V, X7S, Ceramic	10µF, 50V, 400mΩ, Tantalum 2x10µF, 1210, 50V, X7R, Ceramic	562	525	80.6	1000	40.2

Note: An input bulk capacitor is required. *For each application, all capacitors are required.

APPLICATIONS INFORMATION

Many of the output capacitances given in Table 1 specify an electrolytic capacitor. Ceramic capacitors may also be used in the application, but it may be necessary to use more of them. Many high value ceramic capacitors have a large voltage coefficient, so the actual capacitance of the component at the desired operating voltage may be only a fraction of the specified value. Very low ESR of ceramic capacitors may necessitate additional capacitors for acceptable stability margin. For a more detailed explanation of this, see Applications Note 104.

A ceramic capacitor at the input of the LTM8064 combined with input trace or cable inductance can form a high Q (underdamped) tank circuit. If the LTM8064 circuit is hot-plugged into a supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Programming Switching Frequency

The LTM8064 has an operational switching frequency range between 100kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open. See Table 2 for resistor values and the corresponding switching frequencies.

The Typical Performance Characteristics section contains a graph that shows the switching frequency versus R_T value.

Table 2. R_T Resistor Values and Their Resultant Switching Frequencies

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	453
200	221
300	143
400	105
500	82.5
600	69.8
700	57.6
800	49.9
900	44.2
1000	40.2

Switching Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8064 is flexible enough to accommodate a wide range of operating frequencies, a frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8064 in some fault conditions. A frequency that is too low can result in too much output ripple or too much output capacitance.

Switching Frequency Synchronization

The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 1.4V and a logic high greater than 2.3V. The input frequency must be about 20% higher than the frequency determined by the resistor at the RT pin. Input signals outside of these specified parameters may cause erratic switching behavior and subharmonic oscillations. The SYNC pin must be tied to GND if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Soft-Start

The LTM8064 utilizes the soft-start function to control the regulated output current instead of the output voltage. A controlled output current ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor connected from the SS pin to GND programs the slew rate. The charging current is 11µA and reduces the set current as long as the SS pin voltage is lower than the CTRL1 and CTRL2 voltages. An example of the start-up waveforms are shown for various SS capacitances in the Typical Performance Characteristics section.

Power Good

The PGOOD pin is the open-drain output of an internal comparator. PGOOD remains low unless the FB pin voltage is within ±12.5%. When the FB pin voltage is within this range, the PGOOD MOSFET is turned off and the pin is

APPLICATIONS INFORMATION

allowed to be pulled up by an external resistor to a source no greater than 6V. The V_{REF} pin can be used as this source provided a resistance ≥10k is used as the pull-up. The PGOOD output is valid when V_{IN} is above 6V (typical) and RUN is high. If this function is not used, float this pin.

Switching Modes

By default, the LTM8064 operates in FCM. This means that the part will not skip cycles when the load approaches zero amps. This may be particularly useful in applications where the synchronization function is used, or any time discontinuous switching is undesirable. The LTM8064 will not operate in FCM when an input UVLO or minimum duty cycle violation occurs.

Also while operating in FCM, the LTM8064 is capable of functioning as a 2-quadrant device, meaning it can both source and sink current. Please see the Input Precautions section for further details.

If DCM is desired, whether for light-load efficiency increases or load current sharing, the MODE pin voltage must be grounded. During extremely light load conditions while operating in DCM, pulse skipping may occur which may result in higher than desired output voltage ripple. If this behavior cannot be tolerated, operate the part in FCM or use a minimum load of approximately 100mA. See the Load Sharing section for more details.

Maximum Output Current Adjust

To adjust the regulated load current, an analog voltage is applied to the CTRL1 or CTRL2 pins. Varying the voltage between 0V and 1.5V reduces the output current from the part's maximum, typically 7A sourcing and 9.1A sinking. Above 1.5V, the control voltage has no effect on the output current. Graphs of the output current vs CTRL1 and CTRL2 voltages are given in the Typical Performance Characteristics section. The LTM8064 provides a 2V (typical) reference voltage for use with resistive dividers to set the output current limit. The following equations can be used to calculate the current limit:

$$I_{MAX} = \frac{9.31 \bullet R2}{R1+R2} \text{ Amps (Sourcing Current)}$$

$$I_{MAX} = \frac{9.31 \bullet R2}{R1+R2} + 2.1A \text{ (Sinking Current)}$$

where R1 and R2 are in kΩ.

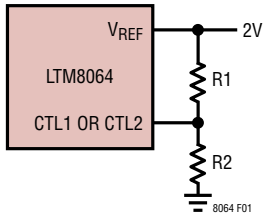


Figure 1. Setting the Output Current Limit

Load Current Derating Using the CTRL2 Pin

In high current applications, derating the maximum current based on operating temperature prevents damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on load/board temperature. To achieve this, the LTM8064 uses the CTRL2 pin to reduce the effective regulated current in the load. While CTRL1 programs the regulated current in the load, CTRL2 can be configured to reduce this regulated current based on the analog voltage at the CTRL2 pin. The load/board temperature derating is programmed using a resistor divider with a temperature dependent resistance (Figure 2). When the load/board temperature rises, the CTRL2 voltage will decrease. To reduce the regulated current, the CTRL2 voltage must be lower than the voltage at the CTRL1 pin. CTRL2 may be higher than CTRL1, but then it will have no effect.

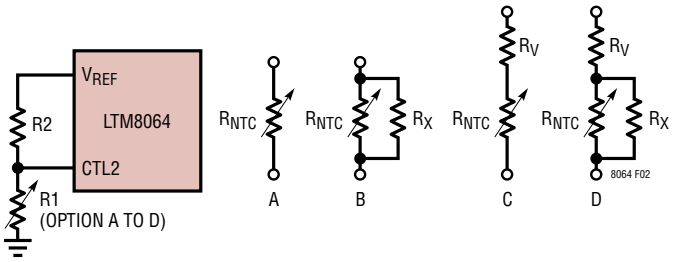


Figure 2. Load Current Derating vs Temperature Using NTC Resistor

APPLICATIONS INFORMATION

Voltage Regulation

In situations where the output of the LTM8064 is required to sink current (that is, the load is driving current into the LTM8064 output), the µModule regulator will maintain voltage regulation as long as the sinking current limit is not exceeded. If the current limit is exceeded, the output voltage may begin to rise.

The LTM8064 does not have output overvoltage protection, making it ideal for applications where the current must remain in regulation even if the output current reverses. For example, in a thermoelectric cooling (TEC) application, the voltage is not particularly important and an output overvoltage cutoff function could be more of a nuisance than a benefit, so the LTM8064 is a good choice.

If the output voltage of the LTM8064 rises above the input, current will flow through an internal power diode to the input bus. The output will be clamped to a diode drop above the input, and current regulation will be lost.

Negative Output

The LTM8064 is capable of generating a negative output voltage by connecting its V_{OUT} to system GND and the LTM8064 GND to the negative voltage rail. An example of this is shown in the Typical Applications section. The most versatile way to generate a negative output is to use a dedicated regulator that was designed to generate a negative voltage, but using a buck regulator like the LTM8064 to generate a negative voltage is a simple and cost effective solution, as long as certain design considerations are taken into account.

Figure 3a shows a typical negative output voltage application. Note that LTM8064 V_{OUT} is tied to system GND and input power is applied from V_{IN} to LTM8064 V_{OUT}. As a result, the LTM8064 is not behaving as a true buck regulator, and the maximum output current is dependent upon the input voltage. In the example shown in the Typical Applications section, there is an attending graph that shows how much current the LTM8064 can deliver for given input voltages.

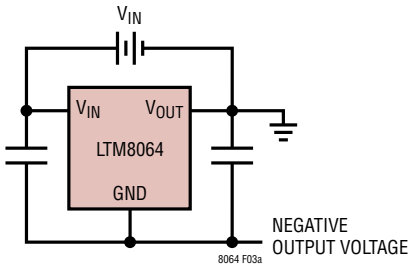


Figure 3a. The LTM8064 Can Be Used to Generate A Negative Voltage

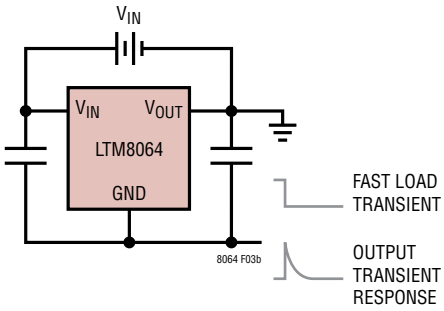


Figure 3b. Any Output Voltage Transient Appears on LTM8064 GND

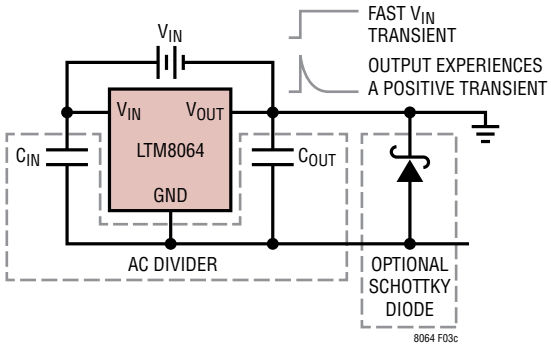


Figure 3c. A Schottky Diode Can Limit the Transient Caused by A Fast Rising V_{IN} to Safe Levels

Note that this configuration requires that any load current transient will directly impress the transient voltage onto the LTM8064 GND, as shown in figure 3b, so fast load transients can disrupt the LTM8064's operation or even cause damage. Carefully evaluate whether the negative buck configuration is suitable for the application.

APPLICATIONS INFORMATION

The C_{IN} and C_{OUT} capacitors in figure 3c form an AC divider at the negative output voltage node. If V_{IN} is hot-plugged or rises quickly, the resultant V_{OUT} will be a positive transient, which may be unhealthy for the application load. An anti-parallel Schottky diode may be able to prevent this positive transient from damaging the load. The location of this Schottky diode is important. For example, in a system where the LTM8064 is far away from the load, placing the Schottky diode closest to the most sensitive load component may be the best design choice. Carefully evaluate whether the negative buck configuration is suitable for the application.

Thermal Shutdown

If the part is too hot, the LTM8064 engages its thermal shutdown, terminates switching and discharges the soft-start capacitor. This thermal shutdown threshold is higher than the 125°C absolute maximum rating. This results in internal temperatures that will exceed the 125°C absolute maximum rating when the thermal shutdown is active, possibly impairing the device's reliability. When the part has cooled, the part automatically re-starts.

UVLO and Shutdown

The LTM8064 has an internal UVLO that terminates switching, resets all synchronous logic, and discharges the soft-start capacitor for input voltages below 4V. The LTM8064 also has a precision RUN function that enables switching when the voltage at the RUN pin rises to 1.705V (typical) and shuts down the LTM8064 when the RUN voltage falls to 1.52V (typical). There is also an internal current source that provides 5µA (typical) of pull-down current to program additional UVLO hysteresis. For RUN rising, the current source is sinking 5µA until RUN = 1.705V, after which the current source turns off. For RUN falling, the current source is off until RUN = 1.52V, after which it sinks 5µA. The following equations determine the voltage divider resistors for programming the falling UVLO voltage and rising enable voltage (V_{ENA}) as configured in Figure 4.

$$R1 = \frac{1.52V \bullet R2}{UVLO - 1.52V}$$

$$R2 = \frac{V_{ENA} - 1.122 \bullet UVLO}{5\mu A}$$

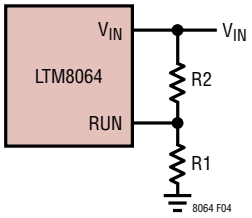


Figure 4. UVLO Configuration

Load Sharing

Two or more LTM8064s can share load current equally by making the following connections:

1. Connect I_{OUTMON} of the master to each of the slave's CTRL1 pins.
2. Tie the V_{OUT}, SS and RUN pins of the master to the corresponding pins of the slave.
3. Ground the MODE pin of all the slave parts.
4. Float the MODE pin of the master part.
5. The value of the master's FB resistor is determined by the equation given in the Pin Functions section.
6. The value of each slave's FB resistor should be one standard 1% resistor value (or EIA, E96) less than the master's FB resistor or roughly 0.98 • R_{FB_MASTER}.

Given the LTM8064's accurate current limit and CVCC operation, each paralleled unit will contribute a portion of the output current, up to the amount determined by the CTRL1 and CTRL2 pins. An example of this is given in the Typical Applications section.

APPLICATIONS INFORMATION

Input Current Tracking from Multiple Input Rails While Load Sharing

When load sharing using multiple fixed input rails, the system can be configured to force the input current of each LTM8064 to track one another. An example of this is shown in the Typical Applications section; please refer to the schematic while reading this discussion.

Suppose the application powers 3.3V at 12A and the system under consideration has regulated 24V and 12V input rails available with no restrictions of the power budget. Connect each slave µModule to its own 12V input rail and the master to the 24V input rail.

The input and output ceramic capacitors and the R_T and FB resistors for the master are chosen by the appropriate line in Table 1. Additionally, the input and output ceramic capacitors and the R_T resistors for the slave devices are also chosen by the appropriate line in Table 1. The FB resistors for the slave devices should be one standard 1% resistor value less than the master's FB resistor or roughly 0.98 • R_{FB_MASTER}. The final value of the slave's FB resistor may need to be adjusted to compensate for layout differences or parasitics.

Because the slave devices' input rail voltage is exactly half that of the master's input rail voltage, the input current drawn by the slave devices will be the same as the input current drawn by the master µModule if the slave devices' current supplied to the load is limited to half of the master's output current to the load. Therefore, the voltage at the CTRL1 pin on the slave devices must be half that of the I_{OUTMON} voltage of the master device. The 100k/100k resistor divider from the I_{OUTMON} pin of the master to ground is used to set the current supplied to the load by both of the slave µModules.

The previous discussion is for a specific application. This same process can be used for other fixed input rails as long as the input rail of the master is greater than the input rail of the slave device.

PCB Layout

Most of the difficulties associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8064. The LTM8064 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 5 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8064.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8064.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the LTM8064.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8064.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 5. The LTM8064 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

APPLICATIONS INFORMATION

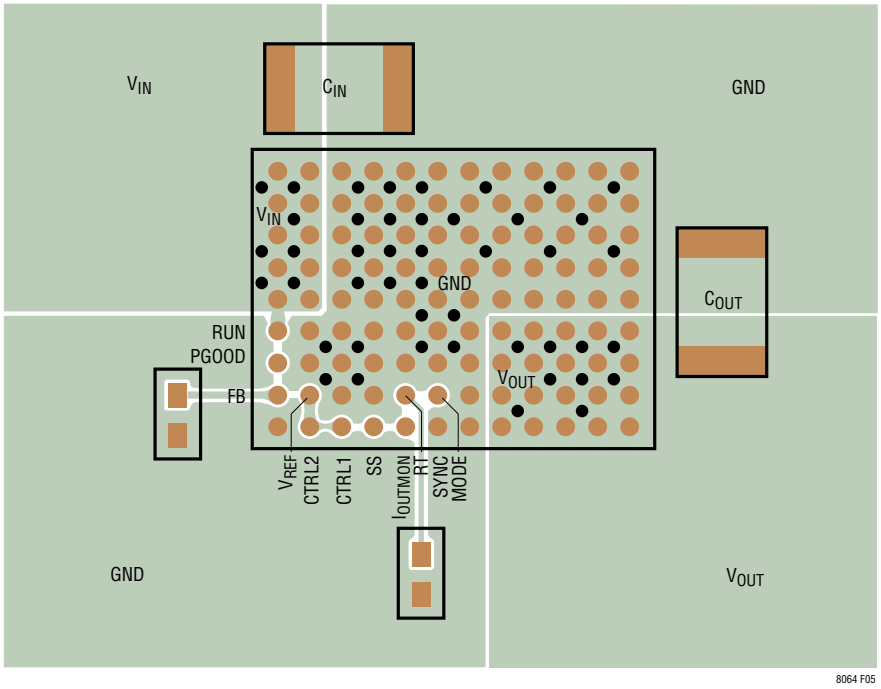


Figure 5. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Input Precautions

When the LTM8064 is sinking current, it maintains its output voltage regulation by power conversion, not power dissipation. This means that the energy provided to the LTM8064 is delivered to its input power bus. This power bus must be able to accept or use the energy, otherwise the power bus's voltage will rise. This can raise the LTM8064 input voltage above the absolute maximum voltage.

In many cases, the system load on the LTM8064 input bus will be sufficient enough to absorb the energy delivered by the µModule regulator. In cases where the LTM8064 is the largest or only power converter, this may not be true and some method must be devised to prevent the LTM8064's input voltage from rising too high. Figure 6a shows a passive crowbar circuit that will dissipate energy during momentary input overvoltage conditions. The breakdown voltage of the Zener diode is chosen in conjunction with the resistor, R, to set the circuit's trip point. The trip point is typically set well above the maximum V_{IN} voltage under normal operating conditions. This circuit does not have a precision threshold, and is subject to both part-to-part and temperature variations, so it is not suitable for applications where high accuracy is required or large voltage margins are not available.

The circuit in Figure 6b also dissipates energy during momentary overvoltage conditions, but is more precise than that in Figure 6a. It uses an inexpensive comparator and the V_{REF} output of the LTM8064 to establish a reference voltage. The optional hysteresis resistor in the comparator circuit avoids MOSFET chatter. Figure 6c shows a circuit that latches on and crowbars the input in an overvoltage event. The SCR latches when the input voltage threshold is exceeded, so this circuit should be used with a fuse, as shown, or employ some other method to interrupt current from the load.

APPLICATIONS INFORMATION

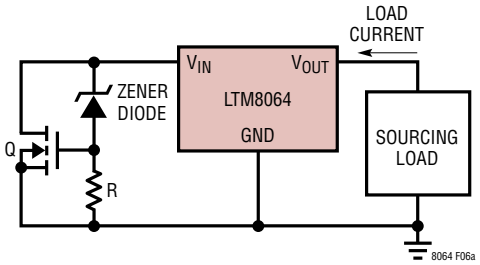


Figure 6a. The MOSFET Q Dissipates Momentary Energy to GND. The Zener Diode and Resistor Are Chosen to Ensure That the MOSFET Turns On Above the Maximum V_{IN} Voltage Under Normal Operation

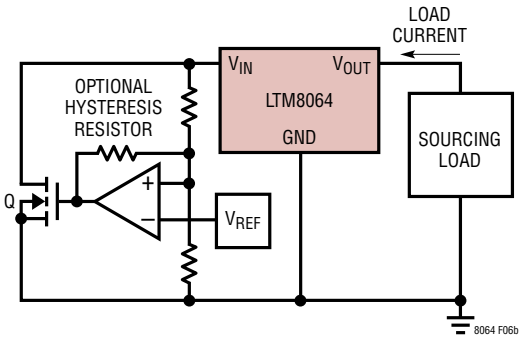


Figure 6b. The Comparator in This Circuit Activates the Q MOSFET at a More Precise Voltage Than the One Shown in Figure 5a

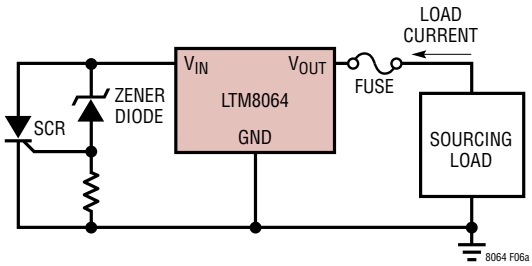


Figure 6c. The SCR Latches On When the Activation Threshold Is Reached, So a Fuse or Some Other Method of Disconnecting the Load Should be Used

As mentioned, the LTM8064 sinks current by energy conversion and not dissipation. Thus, no matter the protection circuit used, the amount of power that the protection circuit must absorb depends upon the amount of power at the input. For example, if the output voltage is 2.5V and can sink 5A, the input protection circuit should be designed to absorb at least 7.5W. In Figures 6a and 6b, let us say that the protection activation threshold is 50V. Then the circuit must be designed to be able to dissipate 7.5W and accept 7.5W/50V = 150mA.

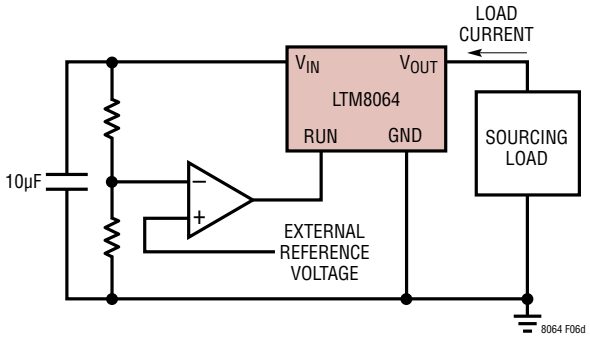


Figure 6d. This Comparator Circuit Turns Off the LTM8064 if the Input Rises Above a Predetermined Threshold. When the LTM8064 Turns Off, the Energy Stored in the Internal Inductor Will Raise V_{IN} a Small Amount Above the Threshold

Figures 6a through 6c are crowbar circuits, which attempt to prevent the input voltage from rising above some level by clamping the input to GND through a power device. In some cases, it is possible to simply turn off the LTM8064 when the input voltage exceeds some threshold. This is possible when the voltage power source that drives current into V_{OUT} never exceeds V_{IN}. An example of this circuit is shown in Figure 6d. When the power source on the output drives V_{IN} above a predetermined threshold, the comparator pulls down on the RUN pin and disables the LTM8064. When this happens, the input capacitance needs to absorb the energy stored within the LTM8064's internal inductor, resulting in an additional voltage rise. As shown in the Block Diagram, the internal inductor value is 4.7µH. If the LTM8064 sinking current limit is set to 6A, for example, the energy that the input capacitance must absorb is $1/2\ LI^2 = 58.75\mu J$. Suppose the comparator circuit in Figure 6d is set to pull the RUN pin down when V_{TRIP} = 15V. The input voltage will rise according to the capacitor energy equation:

$$1/2 \bullet C(V_{IN}^2 - V_{TRIP}^2) = 58.75\mu J$$

If the total input capacitance is 10µF, the input voltage will rise to:

$$58.75\mu J = 1/2 \bullet 10\mu F(V_{IN}^2 - 15V^2)$$

$$V_{IN} = 15.39V$$

APPLICATIONS INFORMATION

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8064. However, these capacitors can cause problems if the LTM8064 is plugged into a live input supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8064 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8064's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8064 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is physically large.

Thermal Considerations

The LTM8064 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8064 mounted to a 79cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JBoard} – Thermal resistance from junction to the printed circuit board

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of

APPLICATIONS INFORMATION

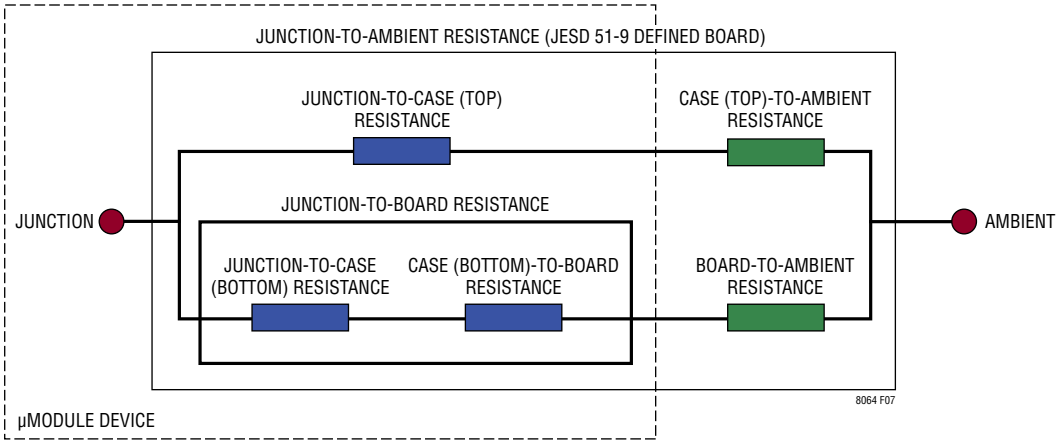


Figure 7. Thermal Resistances Among µModule Device, Printed Circuit Board and Environment

the board. The board temperature is measured a specified distance from the package, using a 2-sided, 2-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

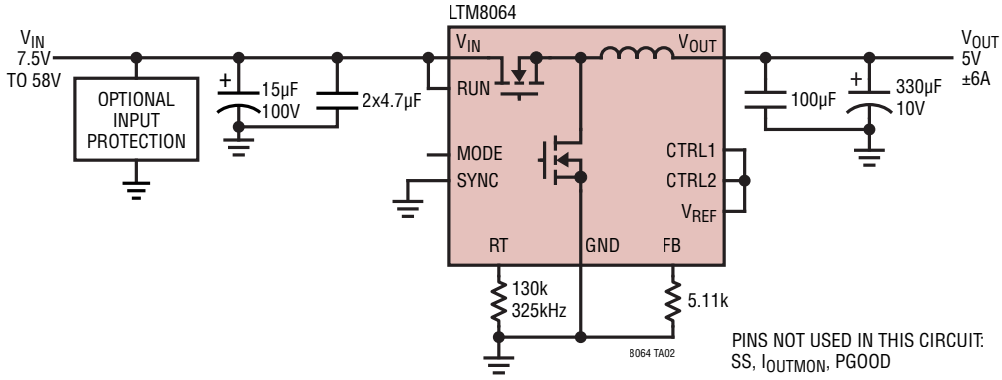
A graphical representation of these thermal resistances is given in Figure 7.

The blue resistances are contained within the µModule, and the green are outside.

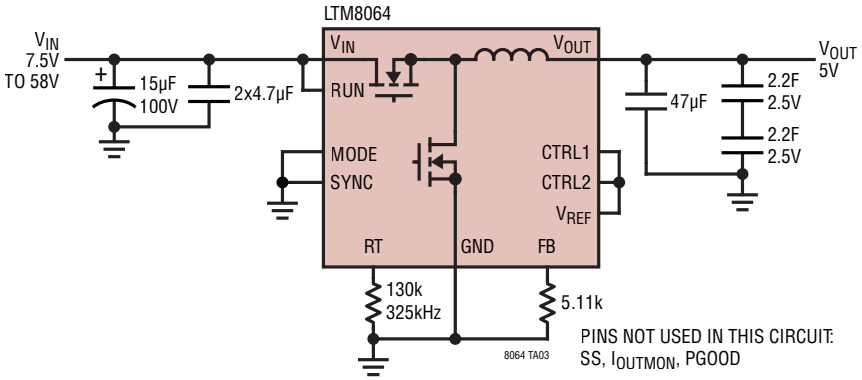
The die temperature of the LTM8064 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8064. The bulk of the heat flow out of the LTM8064 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

TYPICAL APPLICATIONS

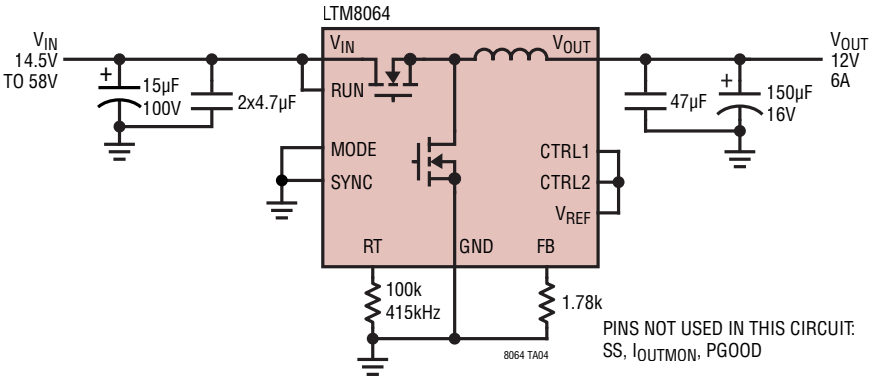
±6A, 5V (2-Quadrant) µModule Voltage Regulator



58V_{IN}, LTM8064 Charges Two 2.5V Series Supercapacitors at 7A

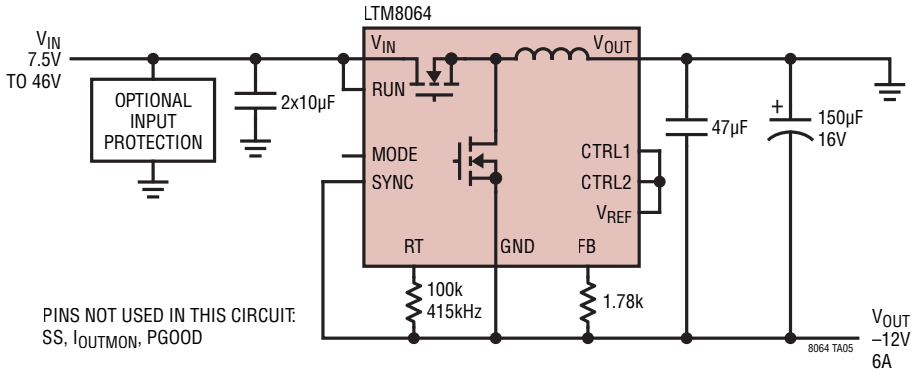


58V_{IN}, 12V_{OUT} Step-Down CVCC Converter

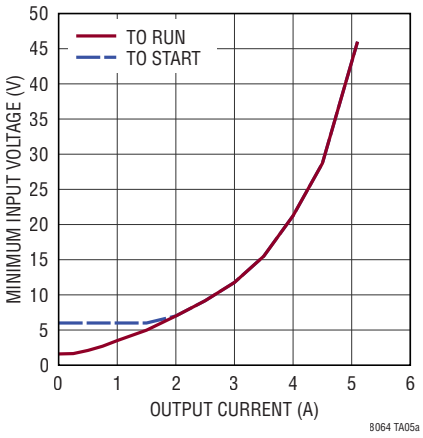


TYPICAL APPLICATIONS

46V_{IN}, –12V_{OUT} Negative Converter

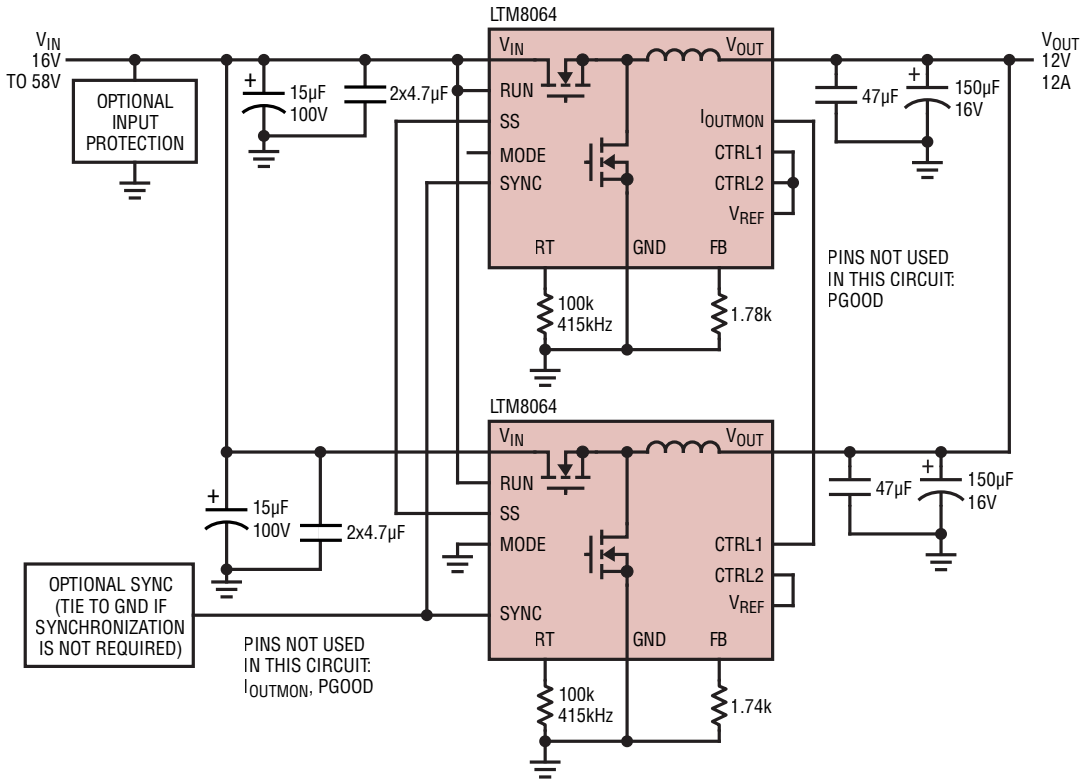


Minimum Input Voltage vs Output Current, V_{OUT} = –12V

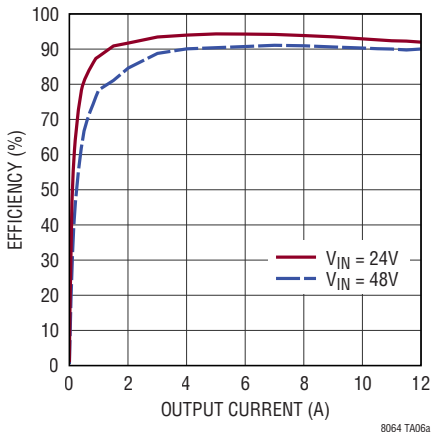


TYPICAL APPLICATIONS

Two LTM8064s Operating in Parallel to Produce 12V$_{OUT}$ at 12A

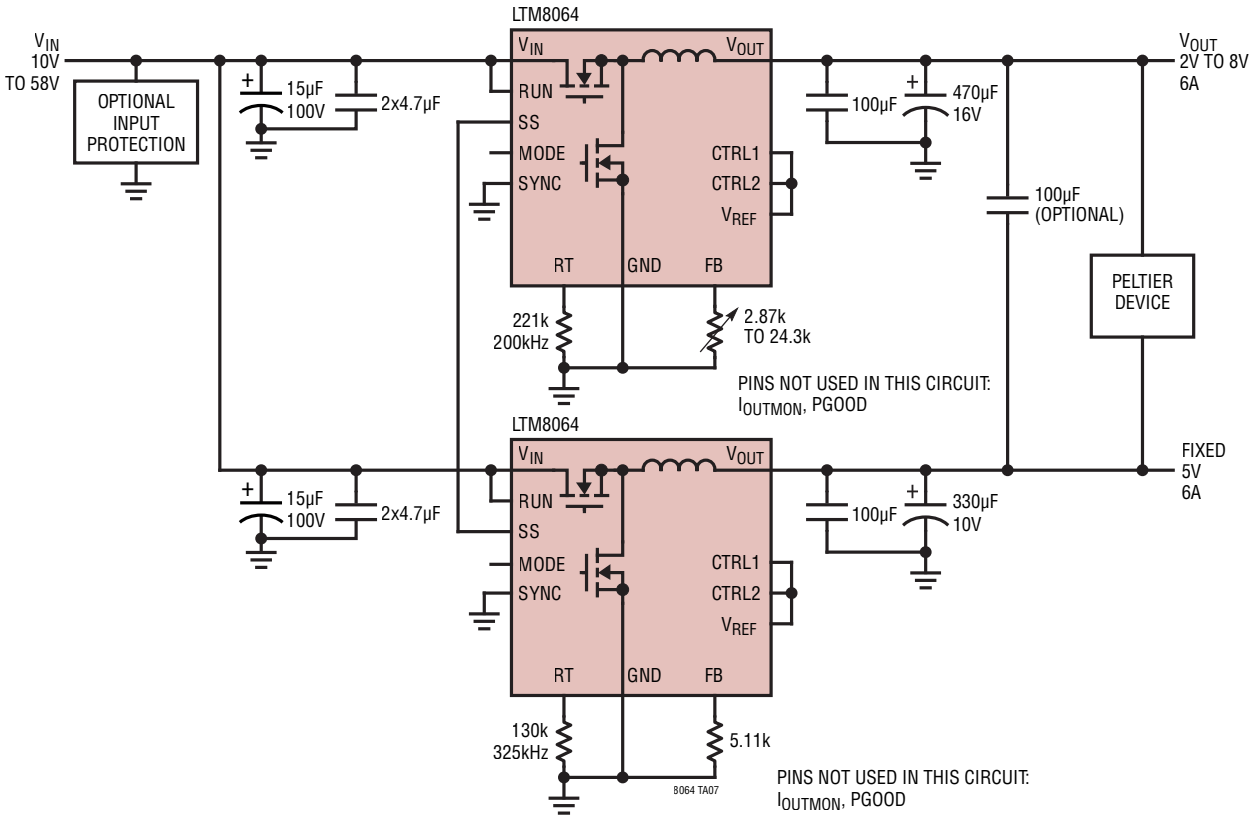


Efficiency vs Output Current
V$_{OUT}$ = 12V

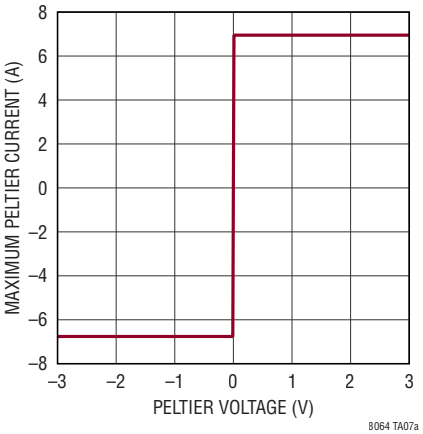


TYPICAL APPLICATIONS

Two LTM8064s Used to Regulate Positive or Negative Voltage (and Current) Across a Peltier Device

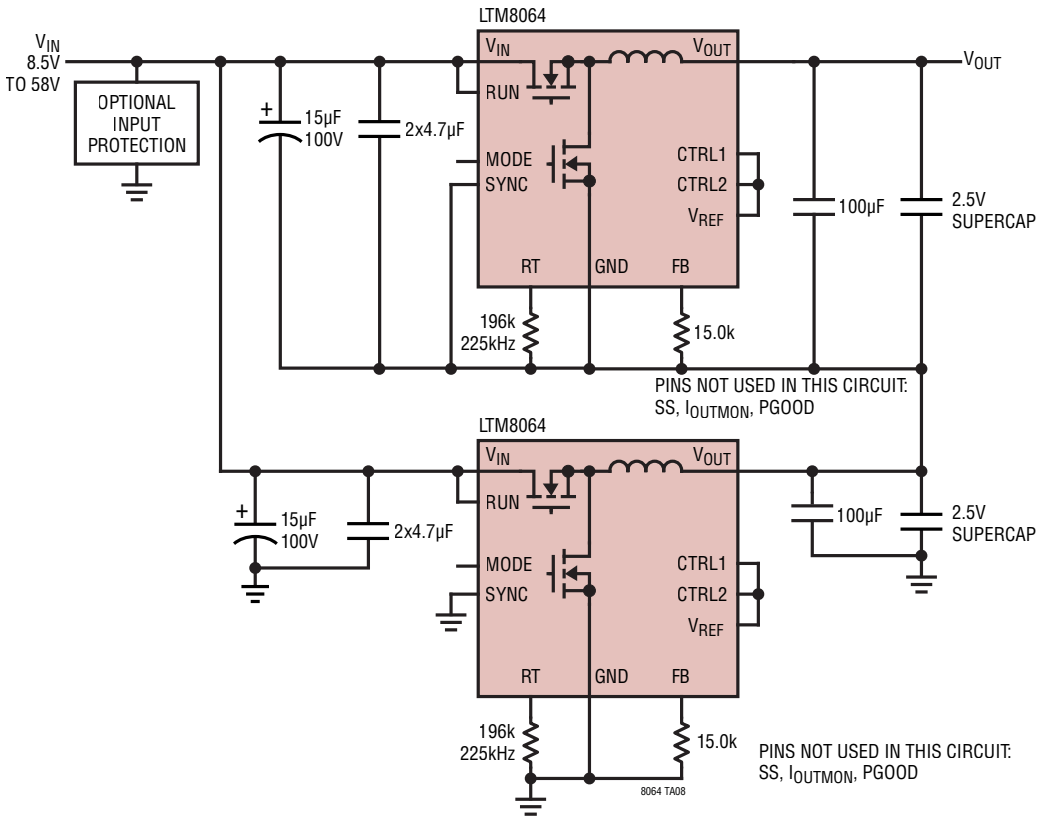


Maximum Peltier Current vs Peltier Voltage

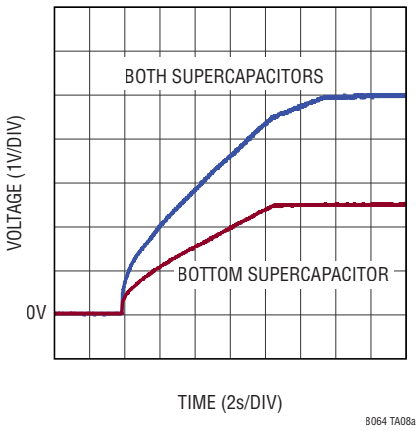


TYPICAL APPLICATIONS

Stack Two LTM8064s to Charge and Actively Balance Supercapacitors (or Batteries)

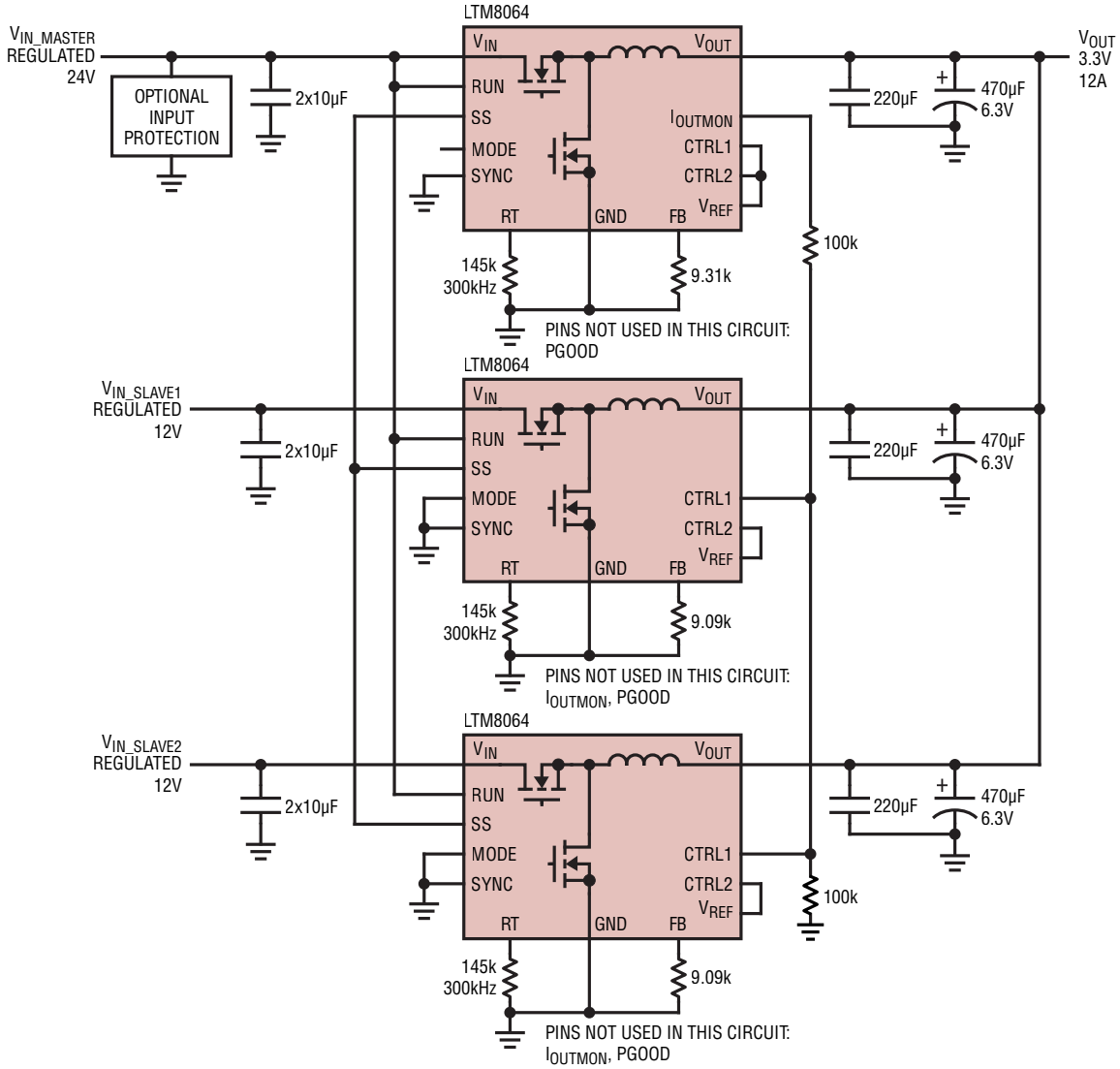


Complete Charging Time of Supercapcitors

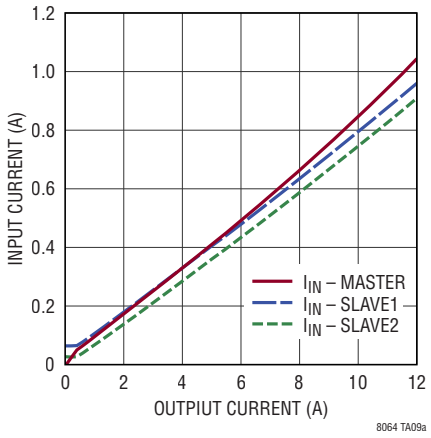


TYPICAL APPLICATIONS

Input Current Tracking from Multiple Input Rails While Load Sharing



The Input Current of Each Slave Supply Tracks the Input Current of the Master

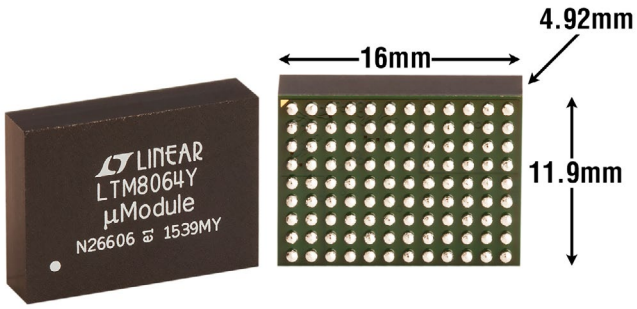


PACKAGE DESCRIPTION

Table 3. Pin Assignment Table (Arranged by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	CTRL2	C1	CTRL1	D1	SS	E1	I_{OUTMON}	F1	SYNC
A2	FB	B2	V_{REF}	C2	GND	D2	GND	E2	RT	F2	MODE
A3	PGOOD	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A4	RUN	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	V_{IN}	B5	V_{IN}	C5	GND	D5	GND	E5	GND	F5	GND
A6	V_{IN}	B6	V_{IN}	C6	GND	D6	GND	E6	GND	F6	GND
A7	V_{IN}	B7	V_{IN}	C7	GND	D7	GND	E7	GND	F7	GND
A8	V_{IN}	B8	V_{IN}	C8	GND	D8	GND	E8	GND	F8	GND
A9	V_{IN}	B9	V_{IN}	C9	GND	D9	GND	E9	GND	F9	GND

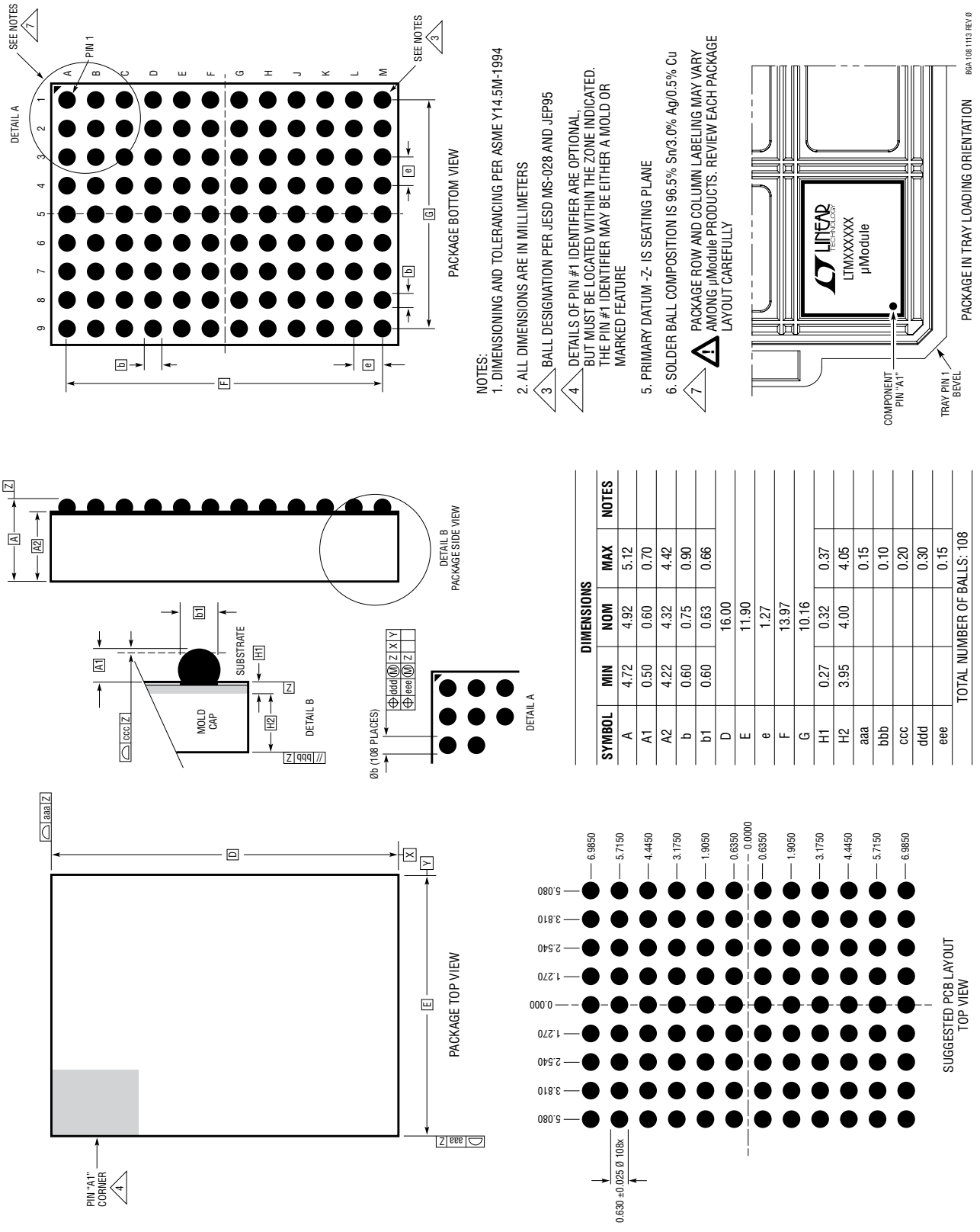
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	V_{OUT}	J1	V_{OUT}	K1	V_{OUT}	L1	V_{OUT}	M1	V_{OUT}
G2	GND	H2	V_{OUT}	J2	V_{OUT}	K2	V_{OUT}	L2	V_{OUT}	M2	V_{OUT}
G3	GND	H3	V_{OUT}	J3	V_{OUT}	K3	V_{OUT}	L3	V_{OUT}	M3	V_{OUT}
G4	GND	H4	V_{OUT}	J4	V_{OUT}	K4	V_{OUT}	L4	V_{OUT}	M4	V_{OUT}
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND	M5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	GND	H7	GND	J7	GND	K7	GND	L7	GND	M7	GND
G8	GND	H8	GND	J8	GND	K8	GND	L8	GND	M8	GND
G9	GND	H9	GND	J9	GND	K9	GND	L9	GND	M9	GND



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM8064#packaging for the most recent package drawings.

BGA Package
108-Lead (16mm × 11.9mm × 4.92mm)
(Reference LTC DWG # 05-08-1965 Rev Ø)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		16.00		
E		11.90		
e		1.27		
F		13.97		
G		10.16		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 108				

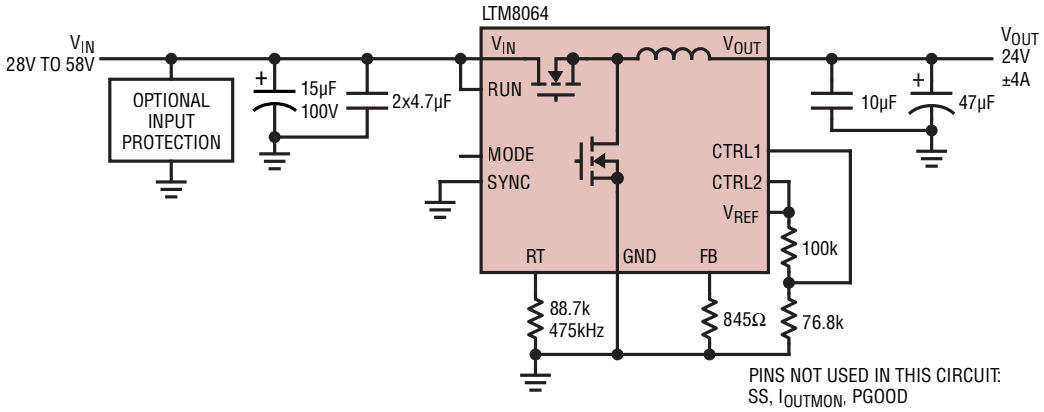
8064fa

REVISION HISTORY

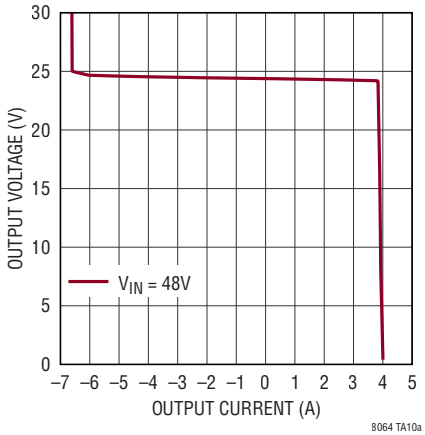
REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/16	Corrected Typical Application circuit, removed extra ground symbol	31

TYPICAL APPLICATION

58V_{IN}, 24V_{OUT} Step-Down Converter with 4A Accurate Current Limit



Output Voltage vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8026	36V_{IN}, 5A Step-Down µModule Regulator with Adjustable Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, Adjustable Current Limit, Parallelable Outputs, CLK Input, 11.25mm × 15mm × 2.82mm LGA Package
LTM8052/LTM8052A	36V_{IN}, ±5A µModule Regulator with Adjustable Accurate Current Limit	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V, –5V ≤ I_{OUT} ≤ 5A, Synchronizable, Pin Compatible with LTM8026, 11.25mm × 15mm × 2.82mm LGA Package
LTM8027	60V_{IN}, 4A DC/DC Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 60V, 2.5V ≤ V_{OUT} ≤ 24V, 15mm × 15mm × 4.32mm LGA Package
LTM8050	60V_{IN}, 2A DC/DC Step-Down µModule Regulator	3.6V ≤ V_{IN} ≤ 58V, 0.8V ≤ V_{OUT} ≤ 24V, 9mm × 15 × 4.92mm BGA Package

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