WINSOURCE ELECTRONICS

THE DATASHEET OF

LTC2946MPMS#PBF

Wide Range I²C Power, Charge and Energy Monitor

FEATURES

- **Rail-to-Rail Input Range: 0V to 100V**
- **Wide Input Supply Range: 2.7V to 100V**
- **Shunt Regulator for Supplies >100V**
- **ΔΣ ADC with Less Than ±0.4% Total Unadjusted Error**
- 12-Bit Resolution for Current and Voltages
- ±1% Accurate Power and Energy Measurements
- ±0.6% Accurate Current and Charge Measurements
- Additional ADC Input Monitors an External Voltage
- Internal ±5% or External Time Bases
- Continuous Scan and Snapshot Modes
- Stores Minimum and Maximum Values
- Alerts When Limits Exceeded
- Split SDA Pin Eases Opto-Isolation
- Shutdown Mode with I_Q < 40µA
- Available in 4mm × 3mm DFN and 16-Lead MSOP Packages

APPLICATIONS

- Telecom Infrastructure
- Industrial Equipment
- General Purpose Energy Measurement

DESCRIPTION

The LTC®2946 is a rail-to-rail system monitor that measures current, voltage, power, charge and energy. It features an operating range of 2.7V to 100V and includes a shunt regulator for supplies above 100V. The current measurement common mode range of 0V to 100V is independent of the input supply. A 12-bit ADC measures load current, input voltage and an auxiliary external voltage. Load current and internally calculated power are integrated over an external clock or crystal or internal oscillator time base for charge and energy. An accurate time base allows the LTC2946 to provide measurement accuracy of better than ±0.6% for charge and ±1% for power and energy. Minimum and maximum values are stored and an overrange alert with programmable thresholds minimizes the need for software polling. Data is reported via a standard I²C interface.

The LTC2946 I²C interface includes separate data input and output pins for use with standard or opto-isolated I²C connections. The LTC2946-1 has an inverted data output for use with inverting opto-isolator configurations.

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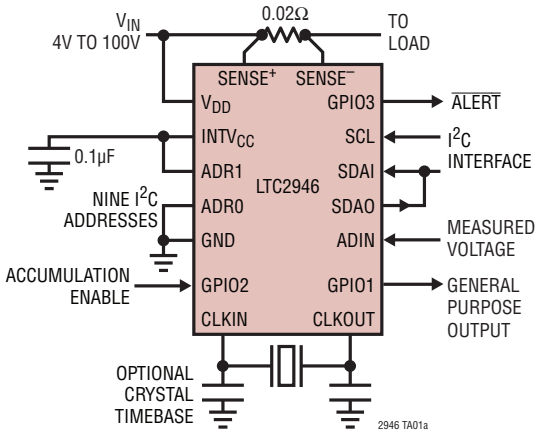
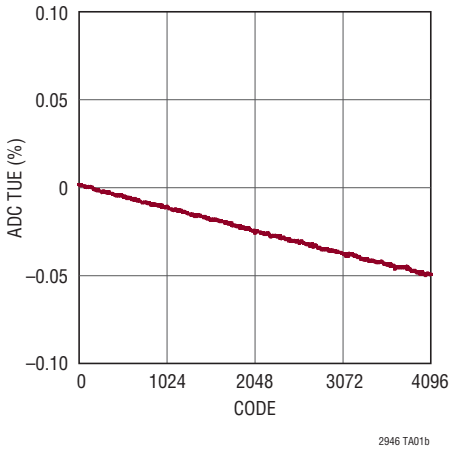
TYPICAL APPLICATION

Wide Range Power, Charge and Energy Monitor with Onboard ADC and I²C



ADC Total Unadjusted Error (ADIN)

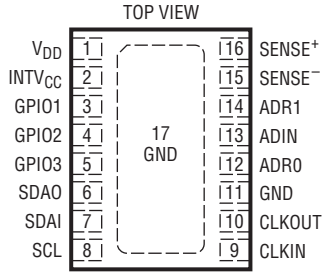


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

V_{DD} Voltage ..... –0.3V to 100V
$SENSE^+$ Voltage ..... –1V to 100V
$SENSE^-$ Voltage .....–1V or $SENSE^+$ – 1V to $SENSE^+$ + 1V
$INTV_{CC}$ Voltage
(Note 3).....–0.3V to Lesser of 5.8V, V_{DD} + 0.3V
ADR1, ADR0, ADIN, SDAO, $\overline{SDAO}$, GPIO1 TO GPIO3
Voltages ..... –0.3V to 7V
CLKOUT Voltage .....–0.3V to $INTV_{CC}$ + 0.3V
CLKIN Voltage..... –0.3V to 5.5V
$INTV_{CC}$ Clamp Current 35mA
SCL, SDAI Voltages (Note 4)..... –0.3V to 5.9V
SCL, SDAI Clamp Current 5mA
Operating Temperature Range
LTC2946C..... 0°C to 70°C
LTC2946I .....–40°C to 85°C
LTC2946H..... –40°C to 125°C
LTC2946MP..... –55°C TO 125°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS Package Only.....300°C

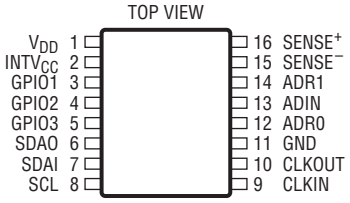
PIN CONFIGURATION

LTC2946



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN

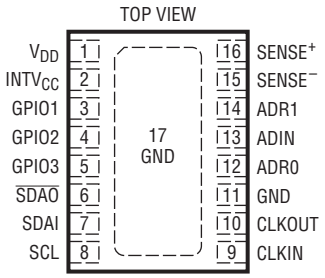
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, E PAD GND SOLDERED DOWN
EXPOSED PAD (PIN 17) IS GND, PCB GND CONNECTION IS OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP

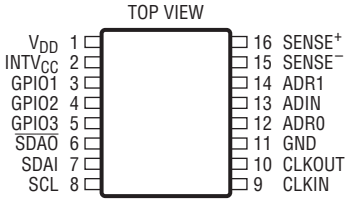
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

LTC2946-1



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, E PAD GND SOLDERED DOWN
EXPOSED PAD (PIN 17) IS GND, PCB GND CONNECTION IS OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2946CDE#PBF	LTC2946CDE#TRPBF	2946	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2946IDE#PBF	LTC2946IDE#TRPBF	2946	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2946HDE#PBF	LTC2946HDE#TRPBF	2946	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2946CDE-1#PBF	LTC2946CDE-1#TRPBF	29461	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2946IDE-1#PBF	LTC2946IDE-1#TRPBF	29461	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2946HDE-1#PBF	LTC2946HDE-1#TRPBF	29461	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2946CMS#PBF	LTC2946CMS#TRPBF	2946	16-Lead Plastic MSOP	0°C to 70°C
LTC2946IMS#PBF	LTC2946IMS#TRPBF	2946	16-Lead Plastic MSOP	–40°C to 85°C
LTC2946HMS#PBF	LTC2946HMS#TRPBF	2946	16-Lead Plastic MSOP	–40°C to 125°C
LTC2946MPMS#PBF	LTC2946MPMS#TRPBF	2946	16-Lead Plastic MSOP	–55°C to 125°C
LTC2946CMS-1#PBF	LTC2946CMS-1#TRPBF	29461	16-Lead Plastic MSOP	0°C to 70°C
LTC2946IMS-1#PBF	LTC2946IMS-1#TRPBF	29461	16-Lead Plastic MSOP	–40°C to 85°C
LTC2946HMS-1#PBF	LTC2946HMS-1#TRPBF	29461	16-Lead Plastic MSOP	–40°C to 125°C
LTC2946MPMS-1#PBF	LTC2946MPMS-1#TRPBF	29461	16-Lead Plastic MSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 4V to 100V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{DD}	V_{DD} Input Supply Voltage		●	4		100	V
V_{CC}	$INTV_{CC}$ Input Supply Voltage		●	2.7		5.8	V
I_{DD}	V_{DD} Supply Current	V_{DD} = 48V, $INTV_{CC}$ Open Shutdown	● ●		0.9 15	1.3 40	mA µA
I_{CC}	$INTV_{CC}$ Supply Current	$INTV_{CC}$ = V_{DD} = 5V Shutdown	● ●		0.7 15	1.0 40	mA µA
$V_{CC(LDO)}$	$INTV_{CC}$ Linear Regulator Voltage	8V < V_{DD} < 100V, I_{LOAD} = 0mA	●	4.4	5	5.4	V
$\Delta V_{CC(LDO)}$	$INTV_{CC}$ Linear Regulator Load Regulation	8V < V_{DD} < 100V, I_{LOAD} = 0mA to 10mA	●		100	200	mV
V_{CCZ}	Shunt Regulator Voltage at $INTV_{CC}$	V_{DD} = 48V, I_{CC} = 1mA	●	5.8	6.3	6.7	V
ΔV_{CCZ}	Shunt Regulator Load Regulation	V_{DD} = 48V, I_{CC} = 1mA to 35mA	●			250	mV
$V_{CC(UVL)}$	$INTV_{CC}$ Supply Undervoltage Lockout	$INTV_{CC}$ Rising, V_{DD} = $INTV_{CC}$	●	2.3	2.6	2.69	V
$V_{DD(UVL)}$	V_{DD} Supply Undervoltage Lockout	V_{DD} Rising, $INTV_{CC}$ Open	●	2.4	2.8	3	V
$V_{DDI2C(RST)}$	V_{DD} I^2C Logic Reset	V_{DD} Falling, $INTV_{CC}$ Open	●	1.7	2.1		V
$V_{CCI2C(RST)}$	$INTV_{CC}$ I^2C Logic Reset	$INTV_{CC}$ Falling, V_{DD} = $INTV_{CC}$	●	1.7	2.1		V
SENSE Inputs							
$I_{SENSE^+(HI)}$	48V $SENSE^+$ Input Current	$SENSE^+$, $SENSE^-$, V_{DD} = 48V Shutdown	● ●		100	150 1	µA µA
$I_{SENSE^-(HI)}$	48V $SENSE^-$ Input Current	$SENSE^+$, $SENSE^-$, V_{DD} = 48V Shutdown	● ●			20 1	µA µA
$I_{SENSE^+(LO)}$	0V $SENSE^+$ Source Current	$SENSE^+$, $SENSE^-$ = 0V, V_{DD} = 48V Shutdown	● ●			–10 –1	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 4V to 100V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SENSE(LO)}^-$	0V SENSE⁻ Source Current	SENSE⁺, SENSE⁻ = 0V, V_{DD} = 48V	●			–5	µA
		Shutdown	●			–1	µA
ADC (SENSE⁺, SENSE⁻ = 0V, 100V) (Note 5)							
RES	Resolution (No missing codes)	(Note 7)	●	12			Bits
TUE	Total Unadjusted Error (Note 6)	ΔSENSE (C-, I-Grade)	●			±0.6	%
		ΔSENSE (H-, MP-Grade)	●			±0.7	%
		SENSE⁺, V_{DD} (C-, I-Grade)	●			±0.4	%
		SENSE⁺, V_{DD} (H-, MP-Grade)	●			±0.5	%
		ADIN (C-, I-Grade)	●			±0.3	%
		ADIN (H-, MP-Grade)	●			±0.4	%
V_{FS}	Full-Scale Voltage	ΔSENSE (C-, I-Grade)	●	101.8	102.4	103	mV
		ΔSENSE (H-, MP-Grade)	●	101.7	102.4	103.1	mV
		SENSE⁺, V_{DD} (C-, I-Grade)	●	102	102.4	102.8	V
		SENSE⁺, V_{DD} (H-, MP-Grade)	●	101.9	102.4	102.9	V
		ADIN (C-, I-Grade)	●	2.042	2.048	2.054	V
		ADIN (H-, MP-Grade)	●	2.04	2.048	2.056	V
LSB	LSB Step Size	ΔSENSE			25		µV
		SENSE⁺, V_{DD}			25		mV
		ADIN			0.5		mV
V_{OS}	Offset Error	ΔSENSE (C-, I-Grade)	●			±2.1	LSB
		ΔSENSE (H-, MP-Grade)	●			±3.1	LSB
		SENSE⁺, V_{DD}	●			±1.5	LSB
		ADIN	●			±1.1	LSB
INL	Integral Nonlinearity	ΔSENSE	●			±2.5	LSB
		SENSE⁺, V_{DD}	●			±2	LSB
		ADIN	●			±2	LSB
σ_τ	Transition Noise (Note 7)	ΔSENSE			1.2		μV_{RMS}
		SENSE⁺, V_{DD}			0.3		mV_{RMS}
		ADIN			10		μV_{RMS}
t_{CONV}	Conversion Time (Snapshot Mode)	ΔSENSE	●	62.4	65.6	68.8	ms
		SENSE⁺, V_{DD}, ADIN	●	31.2	32.8	34.4	ms
R_{ADIN}	ADIN Input Resistance	V_{DD} = 48V, ADIN = 3V	●	3	10		MΩ
CLKIN, CLKOUT, GPIO							
$V_{CLKIN(TH)}$	CLKIN Input Threshold		●	0.7	1	1.3	V
$f_{CLKIN(MAX)}$	Maximum CLKIN Frequency		●	25			MHz
$I_{CLKIN(IN)}$	CLKIN Input Current	V_{CLKIN} = 5V	●		5	10	µA
I_{CLKOUT}	CLKOUT Output Current	V_{CLKIN} = 0V, V_{CLKOUT} = 0V	●	–70	–100	–130	µA
$V_{GPIO(TH)}$	GPIO Input Threshold	V_{GPIO} Rising	●	1.06	1.22	1.32	V
$V_{GPIO(HYST)}$	GPIO Input Hysteresis				36		mV
$V_{GPIO(OL)}$	GPIO Output Low Voltage	I_{GPIO} = 8mA	●		0.15	0.4	V
$I_{GPIO(IN)}$	GPIO Input Leakage Current	V_{GPIO} = 5V	●		0	±1	µA
I²C Interface (V_{DD} = 48V)							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	1.9	2.4	2.7	V
$V_{ADR(L)}$	ADR0, ADR1 Input Low Threshold		●	0.3	0.6	0.9	V
$I_{ADR(IN)}$	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, 3V	●			±13	µA
$I_{ADR(IN,Z)}$	Allowable Leakage When Open		●			±7	µA
$V_{OD(OL)}$	SDAO, $\overline{SDAO}$, Output Low Voltage	I_{SDAO}, $I_{\overline{SDAO}}$ = 8mA	●		0.15	0.4	V
$I_{SDA,SCL(IN)}$	SDAI, SDAO, $\overline{SDAO}$, SCL Input Current	SDAI, SDAO, $\overline{SDAO}$, SCL = 5V	●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 4V to 100V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SDA,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.5	1.8	2.1	V
$V_{SDA,SCL(CL)}$	SDAI, SCL Clamp Voltage	I_{SDAI}, I_{SCL} = 3mA	●	5.9	6.4	6.9	V
I²C Interface Timing							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400			kHz
t_{LOW}	SCL LOW Period		●		0.65	1.3	µs
t_{HIGH}	SCL HIGH Period		●		50	600	ns
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START Condition		●		0.12	1.3	µs
$t_{HD,STA(MIN)}$	Hold Time After (Repeated) START Condition		●		140	600	ns
$t_{SU,STA(MIN)}$	Repeated START Condition Setup Time		●		30	600	ns
$t_{SU,STO(MIN)}$	STOP Condition Setup Time		●		30	600	ns
$t_{HD,DATI(MIN)}$	Data Hold Time Input		●		–100	0	ns
$t_{HD,DATO(MIN)}$	Data Hold Time Output		●	300	600	900	ns
$t_{SU,DAT(MIN)}$	Data Setup Time		●		30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width		●	50	110	250	ns
t_{RST}	Stuck Bus Reset Time	SCL or SDAI Held Low	●	25	33		ms
C_X	SCL, SDAI Input Capacitance (Note 7)				5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to ground, unless otherwise noted.

Note 3: An internal shunt regulator limits the $INTV_{CC}$ pin to a minimum of 5.8V. Driving this pin to voltages beyond 5.8V may damage the part. This pin can be safely tied to higher voltages through a resistor that limits the current below 35mA.

Note 4: Internal clamps limit the SCL and SDAI pins to a minimum of 5.9V. Driving these pins to voltages beyond the clamp may damage the part. The pins can be safely tied to higher voltages through resistors that limit the current below 5mA.

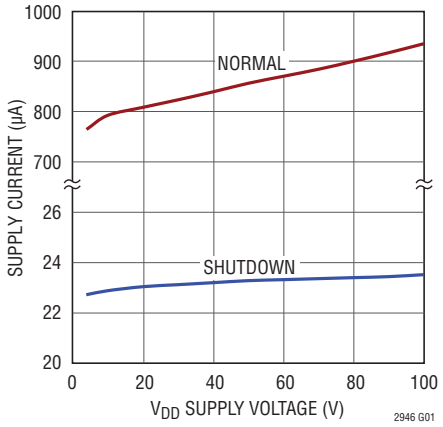
Note 5: ΔSENSE is defined as $V_{SENSE}^+ - V_{SENSE}^-$

Note 6: TUE = (ACTUAL CODE – IDEAL CODE)/4096 • 100% where IDEAL CODE is derived from a straight line passing through Code 0 at 0V and theoretical code of 4096 at V_{FS}.

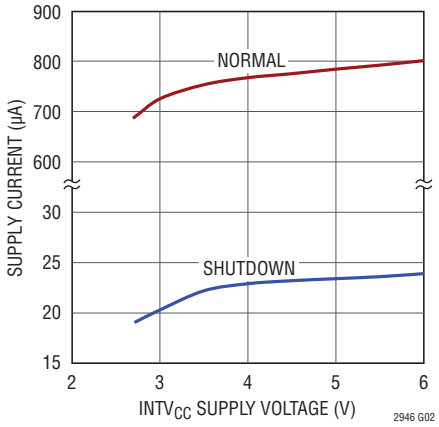
Note 7: Guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

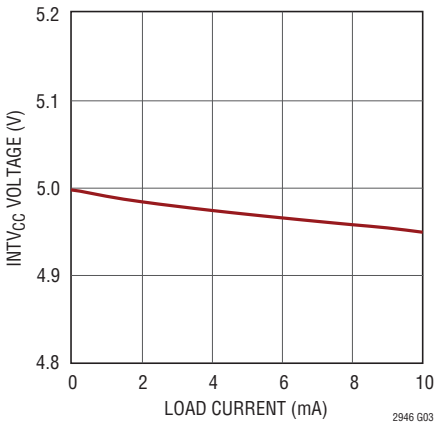
V_{DD} Supply Current



$INTV_{CC}$ Supply Current

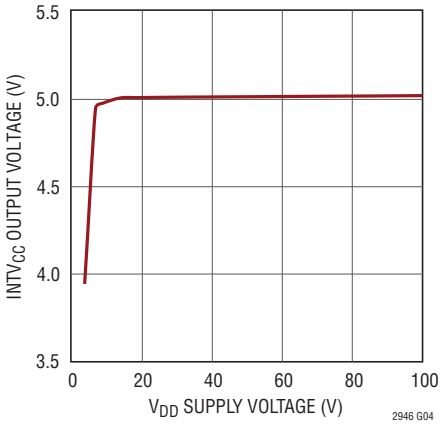


$INTV_{CC}$ Load Regulation

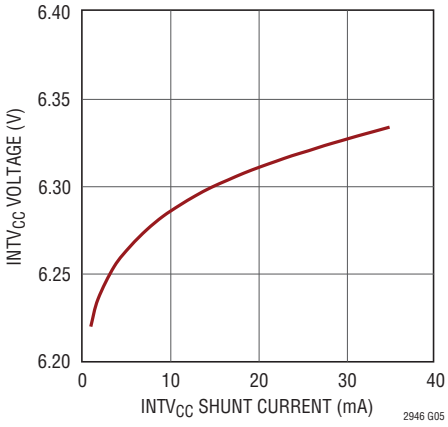


TYPICAL PERFORMANCE CHARACTERISTICS

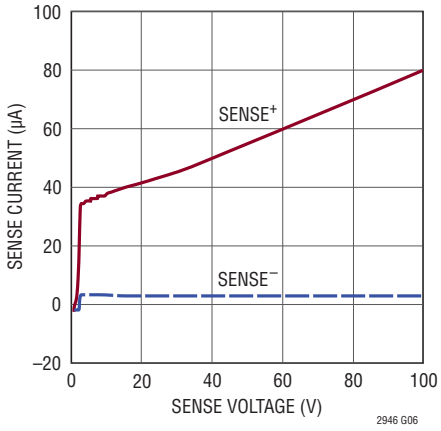
$INTV_{CC}$ Line Regulation



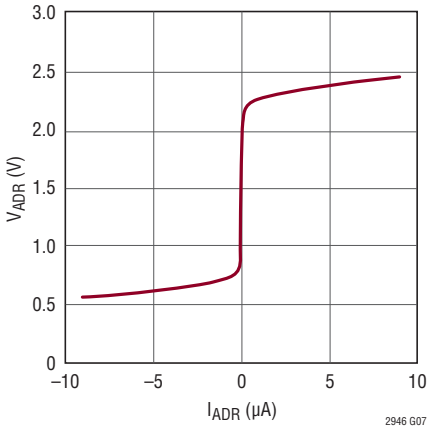
$INTV_{CC}$ Shunt Regulator Load Regulation



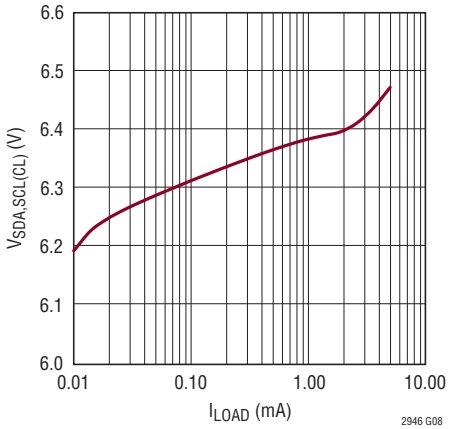
SENSE Input Current



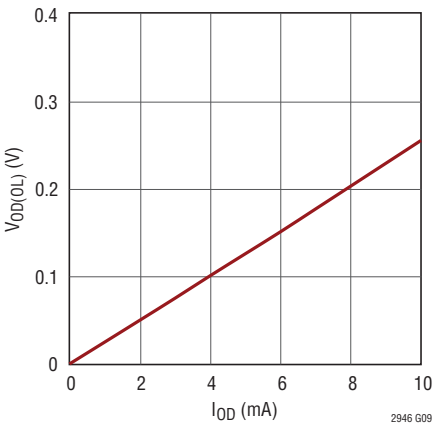
ADR Voltage with Current Source or Sink



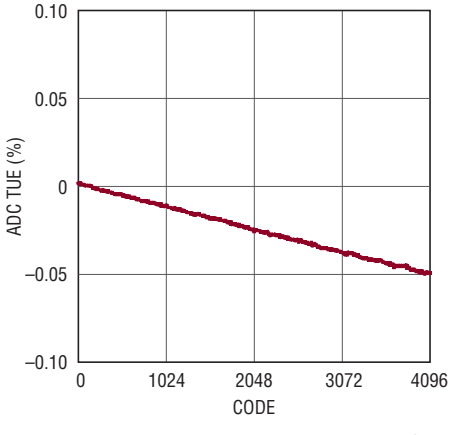
SCL/SDAI Loaded Clamp Voltage vs Load Current



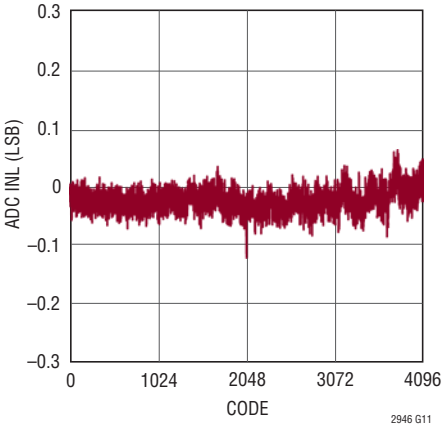
GPIO, SDAO, $\overline{SDAO}$ Loaded Output Low Voltage vs Load Current



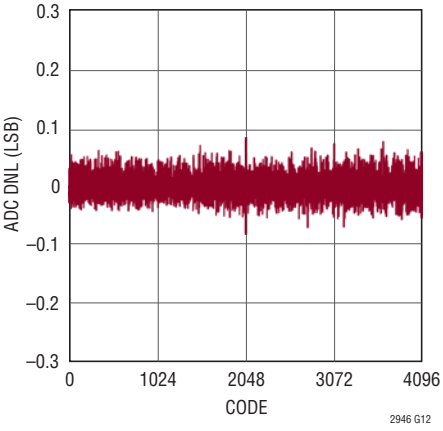
ADC Total Unadjusted Error (ADIN)



ADC Integral Nonlinearity (ADIN)

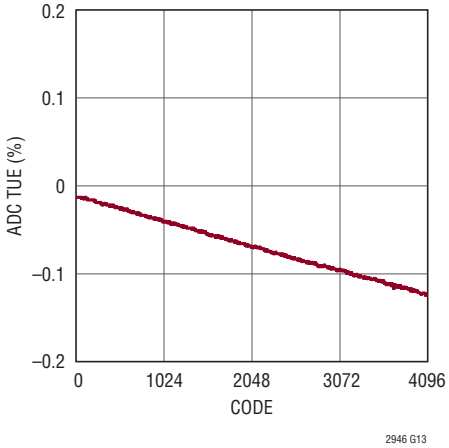


ADC Differential Nonlinearity (ADIN)

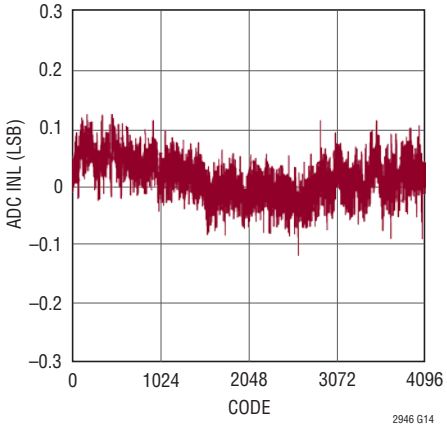


TYPICAL PERFORMANCE CHARACTERISTICS

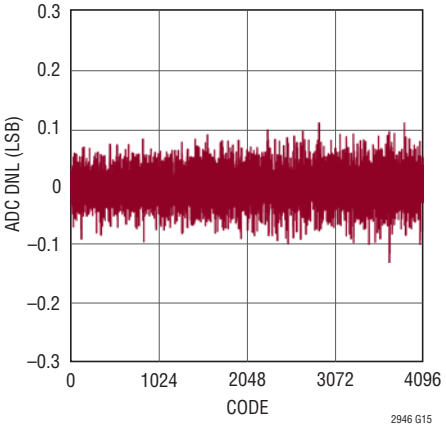
ADC Total Unadjusted Error (ΔSENSE)



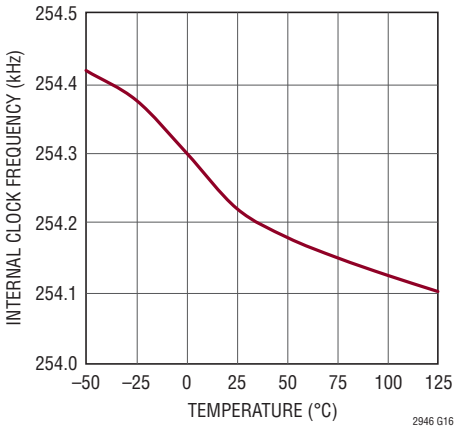
ADC Integral Nonlinearity (ΔSENSE)



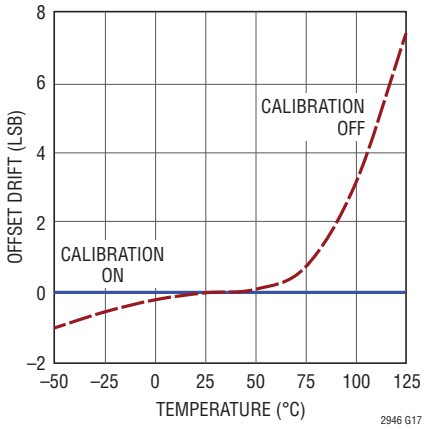
ADC Differential Nonlinearity (ΔSENSE)



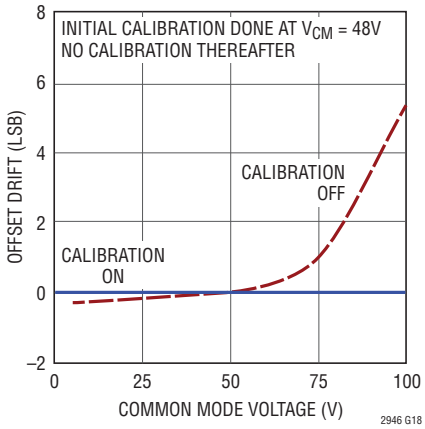
Internal Clock Frequency Over Temperature



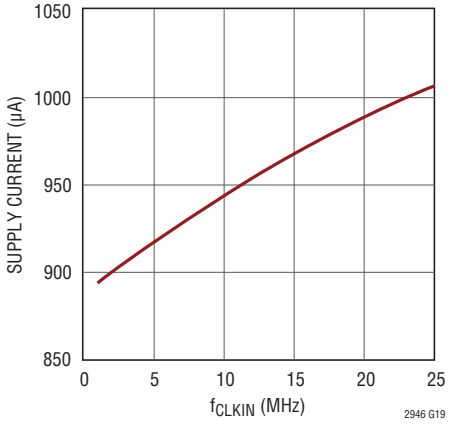
Current Sense Amplifier Offset Drift Over Temperature



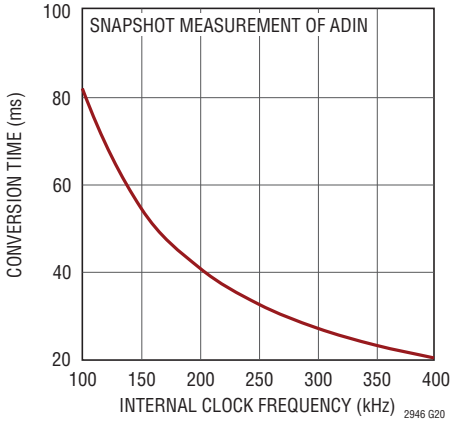
Current Sense Amplifier Offset Drift Over Input Common Mode



V_{DD} Supply Current over CLKIN Frequency



ADC Conversion Time over Internal Clock Frequency



PIN FUNCTIONS

ADIN: ADC Input. The onboard ADC measures voltages between 0V and 2.048V with respect to GND or $INTV_{CC}$. Tie to ground if unused. See Table 3 in the Applications Information section for details.

ADR1, ADR0: I^2C Device Address Inputs. Connecting these pins to $INTV_{CC}$, GND, or leaving the pins open configures one of nine possible addresses. See Table 1 in the Applications Information section for details.

CLKIN: Clock Input. Connect to ground to use the internal ±5% clock. For improved accuracy, connect to an external crystal oscillator circuit or drive with an external clock.

CLKOUT: Clock Output. Connect to an external crystal oscillator circuit. Leave open if unused.

EXPOSED PAD: Exposed Pad may be left open or connected to device ground. For best thermal performance, connect to a large PCB area.

GND: Device Ground.

GPIO1: General Purpose Input/Output (Open Drain). Configurable to general purpose output or input. Tie to ground if unused. See Table 9 in the Applications Information section for details.

GPIO2: General Purpose Input/Output (Open Drain). Configurable to general purpose output, input or accumulation enable (ACC) to gate internal accumulators. Tie to ground if unused. See Table 9 in the Applications Information section for details.

GPIO3: General Purpose Input/Output (Open Drain). Configurable to general purpose output, input or $\overline{ALERT}$. As $\overline{ALERT}$, it is pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by setting the corresponding bit in the ALERT registers, as shown in Tables 5 and 8. Tie to ground if unused. See Table 9 in the Applications Information section for details.

$INTV_{CC}$: Internal Low Voltage Supply Input/Output. This pin is used to power internal circuitry. It can be configured as a direct input for a low voltage supply, as a linear regulator from a higher voltage supply connected to V_{DD}, or as a shunt regulator. Connect this pin directly to a 2.7V to 5.8V supply if available. When $INTV_{CC}$ is powered from an external supply, short the V_{DD} pin to $INTV_{CC}$. If V_{DD} is connected to a 4V to 100V supply, $INTV_{CC}$ becomes the 5V output of an internal series regulator that can supply up to 10mA to external circuitry. For even higher supply voltages, or if a floating topology is desired, $INTV_{CC}$ can be used as a 6.3V shunt regulator. Connect the supply to $INTV_{CC}$ through a resistor or current source that limits the shunt regulator current to less than 35mA. An undervoltage lockout circuit disables the ADC when the voltage at this pin drops below 2.5V. Connect a bypass capacitor of 0.1µF or greater from this pin to ground. If an external load is present, for loop stability use a bypass capacitor of 0.22µF or greater.

SCL: I^2C Bus Clock Input. Data at the SDAI pin is shifted in or out on rising edges of SCL. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SCL and V_{DD} or $INTV_{CC}$. The voltage at SCL is internally clamped to 6.4V typically.

PIN FUNCTIONS

SDAI: I^2C Bus Data Input. Used for shifting in address, command or data bits. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SDAI and V_{DD} or $INTV_{CC}$. The voltage at SDAI is internally clamped to 6.4V typically. Tie to SDAO for normal I^2C operation.

SDAO: LTC2946 Only. I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required. Tie to SDAI for normal I^2C operation.

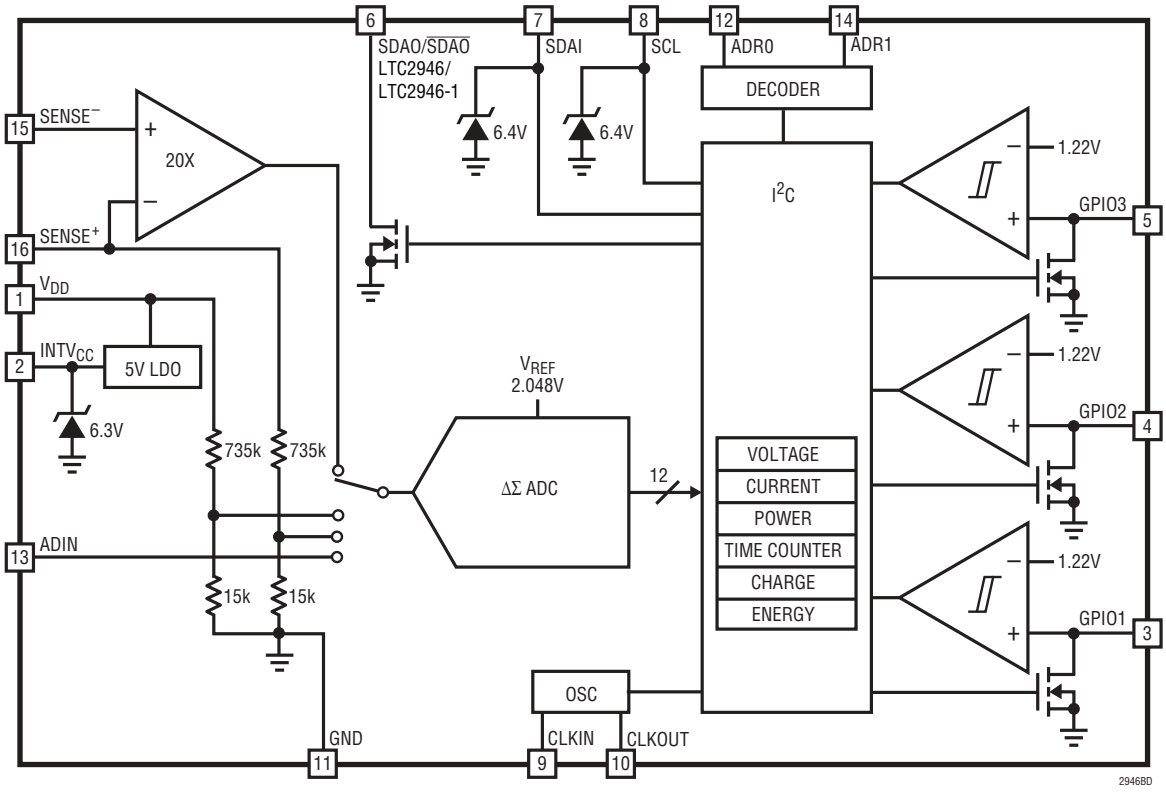
$\overline{\text{SDAO}}$: LTC2946-1 Only. Inverted I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Data is inverted for convenience of opto-isolation. An external pull-up resistor or current source is required. The LTC2946-1 cannot be used in nonisolated I^2C applications without additional components.

$SENSE^+$: Supply Voltage and Current Sense Input. Used as a supply and current sense input for internal current sense amplifier. The voltage at this pin is monitored by the onboard ADC with a full-scale input range of 102.4V. See Figure 20 for recommended Kelvin connection.

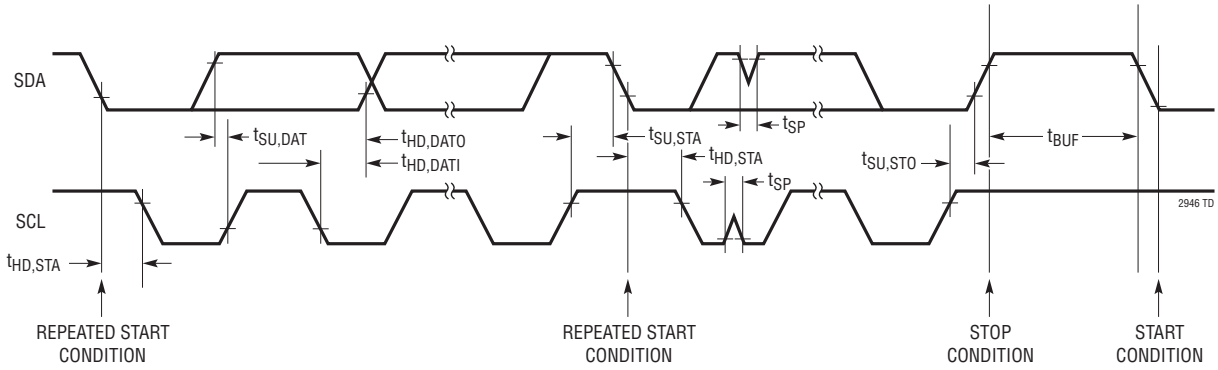
$SENSE^-$: Current Sense Input. Connect an external sense resistor between $SENSE^+$ and $SENSE^-$. The differential voltage between $SENSE^+$ and $SENSE^-$ is monitored by the onboard ADC with a full-scale sense voltage of 102.4mV.

V_{DD}: High Voltage Supply Input. This pin powers an internal series regulator with input voltages ranging from 4V to 100V and produces 5V at $INTV_{CC}$ when V_{DD} is above 8V. Connect a bypass capacitor of 0.1µF or greater from this pin to ground if an external load is present on the $INTV_{CC}$ pin. The onboard 12-bit ADC can be configured to monitor the voltage at V_{DD} with a full-scale input range of 102.4V.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC2946 accurately monitors current, voltage and power of any supply rail from 0V to 100V. An internal linear regulator allows the LTC2946 to operate directly from a 4V to 100V rail, or from an external supply voltage between 2.7V and 5.8V. Quiescent current is less than 1.3mA in normal operation. Enabling shutdown mode via the I²C interface reduces the quiescent current to below 40µA.

The onboard 12-bit analog-to-digital converter (ADC) runs either continuously or on demand using snapshot mode. There are seven continuous scan modes that can be selected via I²C. These modes configure the ADC to repeatedly measure the differential voltage between SENSE⁺ and SENSE⁻ (full-scale 102.4mV), the voltage at SENSE⁺ or V_{DD} pin (full-scale 102.4V) and the voltage applied to ADIN pin (full-scale 2.048V) at internally set duty cycles. See the Applications Information section for more details. The conversion results are stored in onboard registers.

In snapshot mode, the LTC2946 performs a single measurement of one selected voltage or current. A status bit in the STATUS2 register monitors the ADC's conversion progress; when complete, the conversion result is stored in the corresponding data registers.

The GPIO1 to GPIO3 pins are general purpose inputs or general purpose open-drain outputs. GPIO2 may also be configured as an enabling input for the accumulators. Similarly, GPIO3 may be configured as an $\overline{\text{ALERT}}$ output.

Onboard logic stores the minimum and maximum values for each ADC measurement, calculates power data by digitally multiplying the stored current and voltage data, and optionally triggers an alert by pulling the GPIO3 pin low when the ADC measured value falls outside the programmed window thresholds. The LTC2946 includes accumulators that integrate the measured current and power over time to produce charge and energy values. The accumulators integrate at a rate determined either with an internal trimmed ±5% clock, a precision clock generated from an external crystal, or an external clock. The accumulators can be preset with a value and optionally generate an alert when they overflow.

The LTC2946 includes an I²C interface to access the onboard data registers and to program the alert threshold, configuration and control registers. Two three-state pins, ADR1 and ADR0, are decoded to allow nine device addresses (see Table 1). The SDA pin is split into SDAI (input) and SDAO (output, LTC2946) or $\overline{\text{SDAO}}$ (output, LTC2946-1) to facilitate opto-isolation. Tie SDAI and SDAO together for normal, nonisolated I²C operation.

APPLICATIONS INFORMATION

The LTC2946 offers a compact and complete solution for high and low side power monitoring with integrated energy and charge accumulators. With an input common mode range of 0V to 100V and a wide input supply operating voltage range from 2.7V to 100V, this device is ideal for a wide variety of power management applications including automotive, industrial and telecom infrastructure. The basic application circuit shown in Figure 1 provides monitoring of high side current with a 0.02Ω resistor (5.12A full-scale), input voltage (102.4V full-scale) and an external voltage (2.048V full-scale), all using an internal 12-bit ADC.

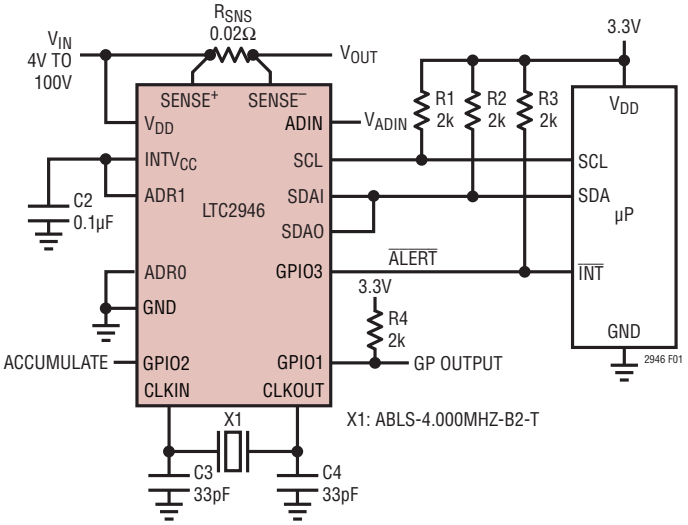


Figure 1. High Side Power, Energy and Charge Monitor Using the LTC2946

APPLICATIONS INFORMATION

Data Converter, Multiplier and Accumulator

The LTC2946 features an onboard, 12-bit ΔΣ ADC that inherently averages input signal and noise over the conversion time window. The differential voltage between SENSE+ and SENSE– (ΔSENSE) is monitored with 25µV/LSB resolution (102.4mV full-scale) to allow accurate measurement of the load current across very low value shunt resistors. The supply voltage at V_{DD} or SENSE+ is directly measured with 25mV/LSB resolution (102.4V full-scale). The voltage at the uncommitted ADIN pin can also be measured with 0.5mV/LSB resolution (2.048V full-scale) to allow monitoring of an arbitrary external voltage.

The supply voltage data is derived from V_{DD}, SENSE+ or ADIN depending on the external application circuit. SENSE+ is selected by default as it is normally connected to the supply voltage as shown in Figure 4 (4a to 4c) and Figure 5b. In negative supply voltage systems, such as shown in Figure 5d, V_{DD} is used to measure the supply voltage at GND with respect to the device ground. For positive and negative supply voltages of more than 100V, as shown in Figure 5a and Figure 5c, external resistors can be used to divide down the voltage for ADIN to measure the supply voltage. CA[4:3] in the CTRLA register select between V_{DD}, SENSE+ and ADIN for supply voltage data. More details can be found in Table 3. A 24-bit power value is generated by digitally multiplying the 12-bit load current data with the 12-bit supply voltage data. 1LSB of power is 1LSB of voltage multiplied by 1LSB of ΔSENSE (current). The result is held in the three adjacent POWER registers (Table 2).

During conversions, the data converter's input is multiplexed to measure four voltages: ΔSENSE, the current sense amplifier's offset, V_{DD} or V_{SENSE}^+, and V_{ADIN} at various duty cycle by configuring CA[6:5] and CA[2:0] in the CTRLA register (Table 3). Some configurations are shown in Figure 2 (2a to 2c) to illustrate the various conversion timing sequences. In Figure 2a, it is shown that upon power-up or after an I^2C write transaction to the CTRLA register the ADC will first measure the current sense amplifier's offset (calibration) and again after every other conversion which can be either V_{ADIN}, the supply voltage (V_{DD} or V_{SENSE}^+) or the load current (ΔSENSE). Figure 2b shows periodic calibration performed every 16 conversions. In Figure 2c a more specific configuration is shown where the ADC periodically calibrates the current sense amplifier with other voltages sequenced for conversions in between.

Two factors need to be considered when selecting between these configurations:

1. Presence of load current harmonics in sync with the windows when the ADC is not sampling the current. The user can improve measurement accuracy of the load current signal with such harmonics by selecting a higher duty cycle for ΔSENSE. For most complete coverage, the ADC can be configured to continuously measure the current by setting CA[2:0] to 110.
2. Increasing the duty cycle for current measurement will result in less frequent updates of the current sense amplifier's offset and the supply voltage values, hence the amount they drift with respect to time and temperature determines the best configuration to use. An on-demand update can also be done with a single I^2C write transaction to the CTRLA register, which will command new measurements of the current sense amplifier's offset and the supply voltage. The results will be used for offset calibration and for providing the voltage value for the multiplier. For example, if CA[6:5] is set to code 11, and CA[2:0] is set to 110, a new offset and voltage values will be produced two ADC conversions after the I^2C write transaction. The ADC will continuously measure the current thereafter.

The timing diagram shown in Figure 2d illustrates the sequence in which the power and accumulator data are generated following conversions in the default configuration. At t_1, the ADC has just finished a conversion of the current (ΔSENSE) signal. The time counter is incremented by one count while the new current data at t_1 is added to the charge accumulator. A new power value is generated by multiplying $I_{(t1)}$ with the previous voltage (V_{IN}) data that is then added to the energy accumulator. From t_1 to t_3, the systematic offset of the current sense amplifier is measured and stored. The ADC then performs a conversion on V_{IN}. A calibration is done again at t_4 before the ADC converts ΔSENSE. The charge and energy accumulators are incremented at t_2, t_3, t_4, t_5, t_6 and t_7, with current and power data from time t_1. The timer counter will keep track

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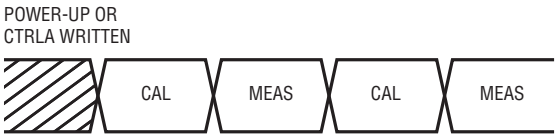
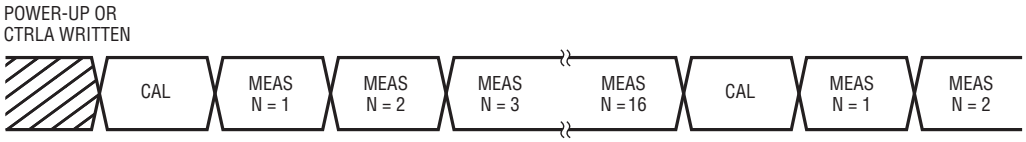
of the number of accumulations that have occurred. At t_8, new current and power data becomes available and these values are added to the charge and energy accumulators. For other CA configurations, the charge and energy accumulators behave similarly; during calibration and when not measuring current the last current value will be used for accumulation and calculation of power.

A 12-bit digital word corresponding to each measured voltage is stored in two adjacent registers out of the six total ADC data registers (ΔSENSE MSB/LSB, V_{IN} MSB/LSB, and ADIN MSB/LSB), with the eight MSBs in the first register and the four LSBs in the second (see Table 2). The lowest 4 bits in the LSB registers are set to 0. These data registers are updated immediately following the corresponding ADC conversion.

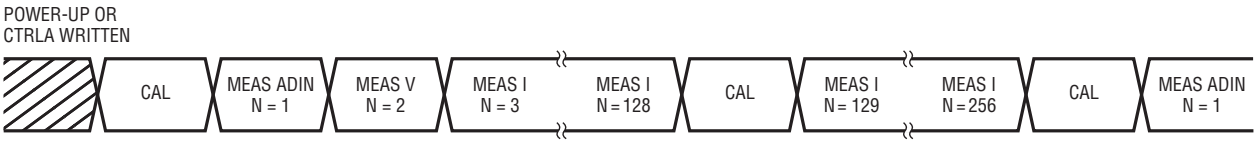
The 4-byte time counter keeps track of the elapsed time during which current and power measurements have been added to the charge and energy accumulators, respectively. At 16.395ms per count it will keep counts up to 2.23 years (see Table 15). Dividing the energy/charge by the time in the timer will yield the average power/current over the time interval in the timer. The charge accumulator is a 36-bit register with the most significant 32-bits accessible, hence one charge bit is equivalent to one timer tick of 16 (2^4) counts of current. Similarly, the energy accumulator is a 48-bit register with the most significant 32-bits accessible, hence one energy bit is equivalent to one timer tick of 65536 (2^{16}) counts of power. With current and power at full-scale the charge and energy accumulators are capable of storing 3.2 days of data which translates to several months at nominal current and power levels.



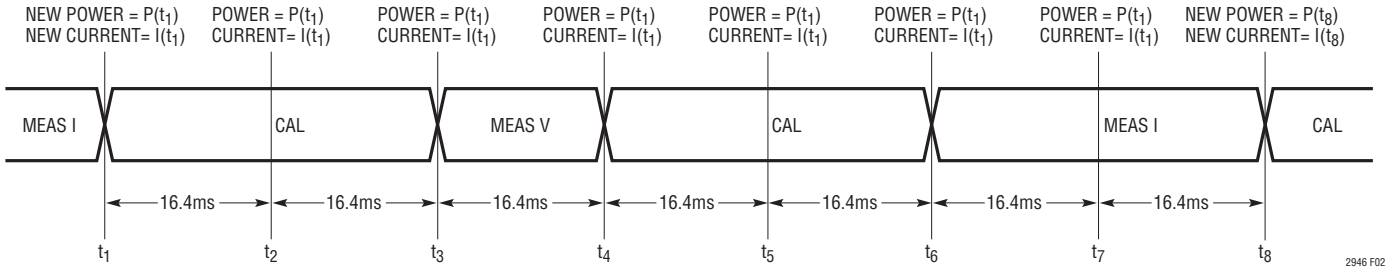
(2a) Current Sense Amplifier Calibrated Every Conversion, CA[6:5] = 00



(2b) Current Sense Amplifier Calibrated Every 16 Conversions, CA[6:5] = 01



(2c) The ADC Conversion Sequence for CA[6:5] = 10 and CA[2:0] = 101



(2d) Default ADC Conversion Sequence

Figure 2

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Since the accumulators contain multiple bytes of data, a single page read transaction of the accumulators is required to ensure the data is coherent. All the accumulators are writable, allowing them to be preloaded with given values. The LTC2946 can then be configured to generate an overflow alert after a specified amount of energy or charge has been delivered or when a preset amount of time has elapsed.

A snapshot mode is also included which makes a measurement of a single selected voltage (either ΔSENSE, V_{DD} or V_{SENSE}^+, or V_{ADIN}). To make a snapshot measurement, write the 2-bit code of the desired ADC channel to CA[4:3] and code 111 to CA[2:0] using a write byte command to the CTRLA register. When the write byte command is completed, the ADC converts the selected voltage and the busy bit S2[3] in the STATUS2 register (see Table 10) will be set to indicate that the conversion is in progress. After completing the conversion, the ADC will halt and the busy bit will reset to indicate that the data is ready. An alert may be generated at the end of a snapshot conversion by setting bit AL2[7] in the ALERT2 register (Table 8). To make another snapshot measurement, rewrite the CTRLA register. In snapshot mode, the POWER registers, time counters, charge and energy accumulators are not refreshed.

Crystal Oscillator/External Clock

Accurately measuring energy/charge by integrating power/current requires a precise integration period. The on-chip clock of the LTC2946 is trimmed to within ±5%. To enable timekeeping with the on-chip clock, tie CLKIN to GND and leave CLKOUT open. For better accuracy, a crystal oscillator or resonator may be connected to the CLKIN and CLKOUT pins, as shown in Figure 1. Alternately, an external clock between 1MHz and 25MHz may be applied to CLKIN with CLKOUT left unconnected. The clock frequency at CLKIN is divided by 4× the value in the CLK_DIV register (see Table 13) to generate an internal clock with targeted frequency of 250kHz for the data converter's delta-sigma modulator. With an external clock or crystal, the sampling frequency of the ADC can be adjusted by configuring the CLK_DIV register (Register 43h). Limit the sampling clock to between 100kHz and 400kHz and at least 20kHz above or below f_{IN}.

The delta-sigma ADC provides inherent averaging of the input signal such that an anti-aliasing filter is not required in most applications. However, noise ripple (f_{IN}) occurring at integer multiples of the modulator sampling frequency (f_S) can still pose problems. Figure 3 shows how the sampling frequency as a function of the input frequency affects the amount of error. When $f_S = f_{IN}$, in the worst case the input signal may be sampled entirely at its peak

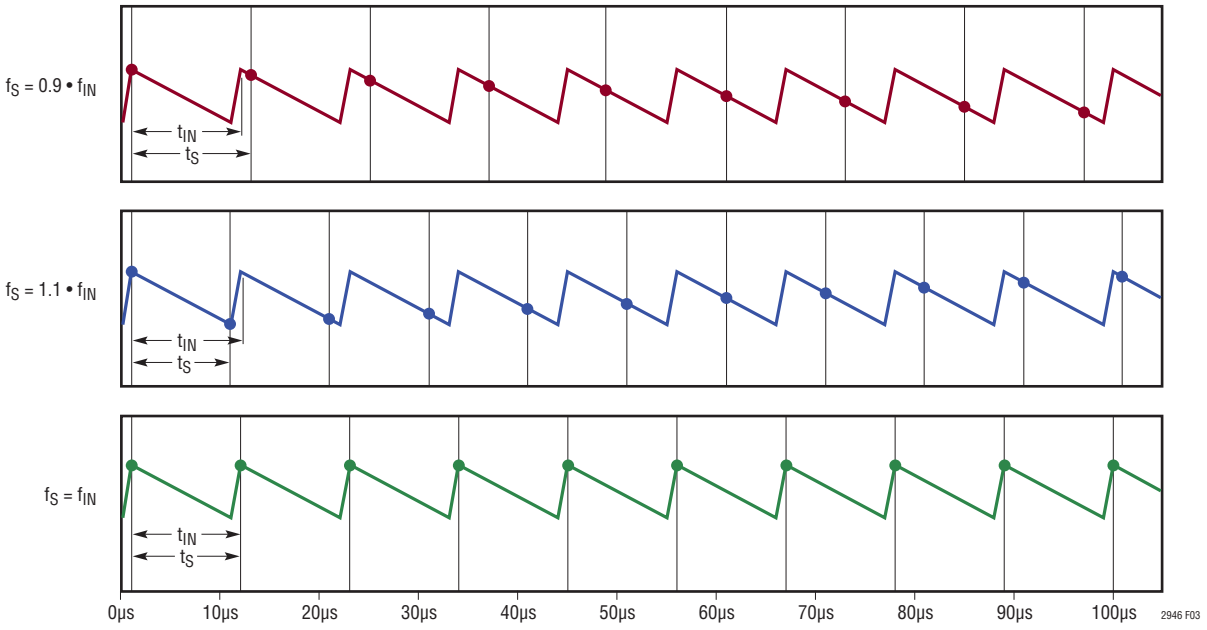

Figure 3. Waveforms Showing the Effect of Aliasing

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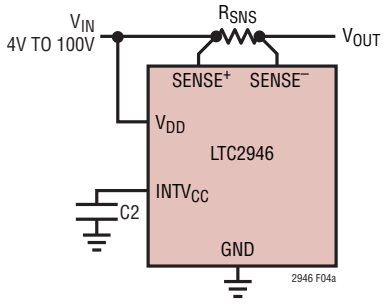
(or trough) resulting in an average output value of V_{PEAK} (or V_{TROUGH}). The actual average value of the input is ½ • (V_{PEAK} – V_{TROUGH}). Slightly adjusting the sampling frequency will remove the error as samples representative of the entire waveform are averaged over the conversion period. This is illustrated in the waveforms corresponding to $f_S = 0.9f_{IN}$ and $f_S = 1.1f_{IN}$. The input can be seen to get sampled at multiple instances between the peak and trough. Averaging sufficient number of samples will then yield the correct result.

Flexible Power Supply to LTC2946

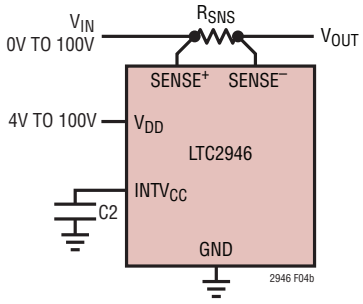
The LTC2946 can be externally configured to derive power from a wide range of supplies. The LTC2946 includes an onboard linear regulator to power the low voltage internal circuitry connected to the $INTV_{CC}$ pin from high V_{DD} voltages. The linear regulator operates with V_{DD} voltages from 4V to 100V, and a shunt regulator is available for voltages above 100V. The linear regulator produces a 5V output capable of supplying 10mA at the $INTV_{CC}$ pin when V_{DD} is greater than 8V. The regulator is disabled when the junction temperature rises above 150°C, and the output is protected against accidental shorts. Bypass capacitors of 0.1µF, or greater, at both the V_{DD} and $INTV_{CC}$ pins are recommended for optimal transient performance. Note that operation with high V_{DD} voltages can result in significant power dissipation, and care is required to ensure that the maximum operating junction temperature stays below 125°C. For improved thermal resistance, use the DFN package and solder the exposed pad to a large copper region on the PCB.

Figure 4a shows the LTC2946 being used to monitor an input supply that ranges from 4V to 100V. No secondary supply is needed since V_{DD} can be connected directly to the input supply. If the LTC2946 is used to monitor an input supply of 0V to 100V, it can derive power from a wide range secondary supply connected to the V_{DD} pin as shown in Figure 4b. The $SENSE^{+/-}$ pins can be biased independently of the part's supply voltage. Alternatively, if a low voltage supply is present it can be connected to the $INTV_{CC}$ pin, as shown in Figure 4c, to minimize on-chip power dissipation. When $INTV_{CC}$ is powered from a secondary supply, connect V_{DD} to $INTV_{CC}$.

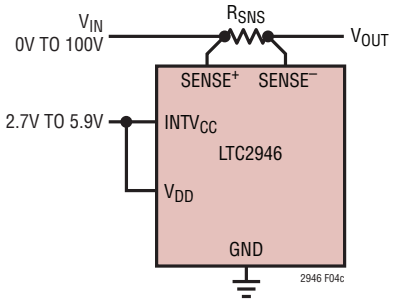
For supply voltages above 100V, the shunt regulator at $INTV_{CC}$ can be used in both high and low side configurations to provide power to the LTC2946 through an external shunt resistor, R_{SHUNT}. Figure 5a shows a high side power



(4a) LTC2946 Derives Power from the Supply Being Monitored



(4b) LTC2946 Derives Power from a Wide Range Secondary Supply



(4c) LTC2946 Derives Power from a Low Voltage Secondary Supply

Figure 4

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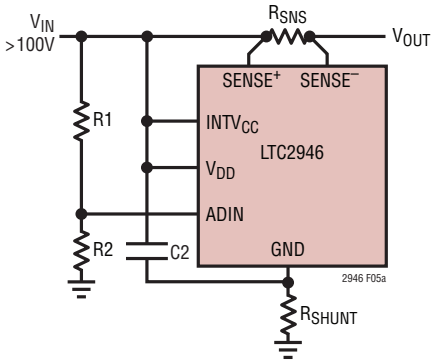
monitor with an input monitoring range beyond 100V in a high side shunt regulator configuration. The device ground is separated from ground through R_{SHUNT} and clamped at 6.3V below the input supply. Note that due to the different ground levels, the I^2C signals from the part need to be level shifted for communication with other ground referenced components. The bus voltage is measured with a resistor string connected to ADIN. Set CA[7] in the CTRLA register so that the ADC measures ADIN with reference to $INTV_{CC}$ instead of GND. The measurement range at ADIN is then from $INTV_{CC}$ to $INTV_{CC}$ – 2.048V.

Figure 5b shows a high side rail-to-rail power monitor which derives power from a secondary supply greater than 100V. The voltage at $INTV_{CC}$ is clamped at 6.3V above ground in a low side shunt regulator configuration to power the part. In low side power monitors, the device ground and the current sense inputs are connected to the negative terminal of the input supply as shown in Figure 5c. The low side shunt regulator configuration allows operation with input supplies above 100V by clamping the voltage at $INTV_{CC}$. R_{SHUNT} should be sized according to the following equation:

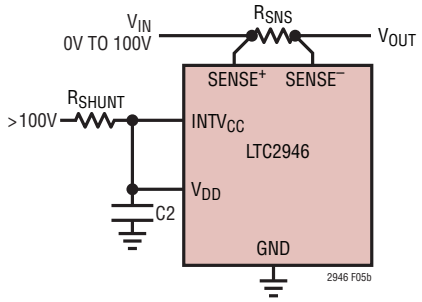
$$\frac{V_{S(MAX)} - V_{CCZ(MIN)}}{I_{CC(ABSMAX)}} \le R_{SHUNT} \le \frac{V_{S(MIN)} - V_{CCZ(MAX)}}{I_{CC(MAX)} + I_{LOAD(MAX)}} \quad (1)$$

$$\frac{V_{S(MAX)} - 5.8V}{35mA} \le R_{SHUNT} \le \frac{V_{S(MIN)} - 6.7V}{1mA + I_{LOAD(MAX)}}$$

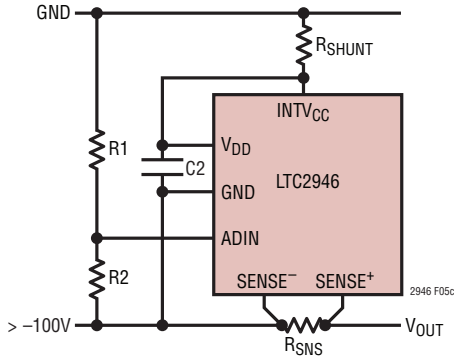
where $V_{S(MAX)}$ and $V_{S(MIN)}$ are the operating maximum and minimum limits of the supply. $I_{LOAD(MAX)}$ is the maximum external current load that is connected to the shunt regulator. The shunt resistor must also be rated to safely



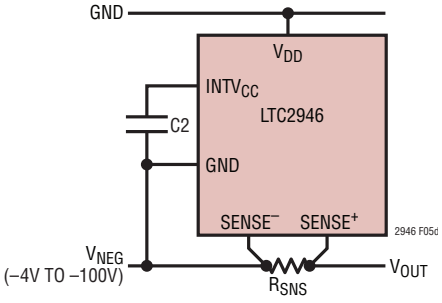
(5a) LTC2946 Derives Power Through a High Side Shunt Regulator



(5b) LTC2946 Derives Power Through a Low Side Shunt Regulator in a High Side Current Sense Topology



(5c) LTC2946 Derives Power Through a Low Side Shunt Regulator in a Low Side Current Sense Topology



(5d) LTC2946 Derives Power from the Supply Monitored in a Low Side Current Sense Topology

Figure 5

APPLICATIONS INFORMATION

dissipate the worst-case power. As an example, consider the –48V telecom system where the supply operates from –36V to –72V and the shunt regulator is used to supply an external load up to 4mA. R_{SHUNT} needs to be between 1.9k and 5.9k according to the previous equation, and for reduced power dissipation, a larger resistance is advantageous. The worst-case power dissipated in an R_{SHUNT} of 5.36k is calculated to be 0.8W. Three 0.5W rated 1.8k resistors in series would suffice for this example.

If the supply input is below 100V, the shunt resistor is not required and V_{DD} can be connected to GND of the supply as shown in Figure 5d.

Supply Undervoltage Lockout

During power-up, the internal I^2C logic and the ADC are enabled when either V_{DD} or $INTV_{CC}$ rises above its undervoltage lockout threshold. During power-down, the ADC is disabled when V_{DD} and $INTV_{CC}$ fall below their respective undervoltage lockout thresholds. The internal I^2C logic is reset when V_{DD} and $INTV_{CC}$ fall below their respective I^2C reset thresholds.

Shutdown Mode

The LTC2946 includes a low quiescent current shutdown mode, controlled by bit CB[6] in the CTRLB register (Table 4). Setting CB[6] puts the part in shutdown mode, powering down the ADC, internal reference and onboard linear regulator. The internal I^2C bus remains active, and although the ADR1 and ADR0 pins are disabled, the device will retain the most recently programmed I^2C bus address. All onboard registers retain their contents and can be accessed through the I^2C interface. To re-enable ADC conversions, reset bit CB[6] in the CTRLB register. The analog circuitry will power up and all registers will retain their contents.

The onboard linear regulator is disabled in shutdown mode to conserve power. If the onboard linear regulator is used to power external I^2C bus related circuitry such as optocouplers or pull-ups, I^2C communication will be lost when the part is shut down. The LTC2946 would then have to be reset by cycling its power to come out of shutdown. If low I_Q mode is not required, ensure bit CB[6] in the CTRLB register is masked off during software development. It is recommended that external regulators be used in such applications if powering down the LTC2946 is desirable. As an added layer of protection against this scenario, bit CB[4] in the CTRLB register can be set during system configuration to enable the LTC2946 to automatically exit shutdown mode when the I^2C lines are low for more than 33ms (which can be a result of accidental shutdown of the LTC2946's linear regulator powering the I^2C). The user can elect to be alerted of this event by setting bit AL2[3] in the ALERT2 register (Table 8). Quiescent current drops below 40µA in shutdown mode with the internal regulator disabled.

Configuring the GPIO Pins

The LTC2946 has three GPIO pins configurable through the GPIO_CFG register (Table 9) to be used as general purpose input/output pins. As general purpose inputs, GPIO1 through GPIO3 can be either active HIGH or LOW. In addition, GPIO2 can also be used as an accumulation enable input by writing bits CB[3:2] = [10] to allow integration of the time counter, charge and energy accumulators. GPIO1 through GPIO3 have comparators monitoring the voltage on these pins with a threshold of 1.22V, the results of which may be read from bits S2[6:4] in the STATUS2 register, as shown in Table 10. An alert may be generated when GPIO1 or GPIO2 are active as inputs by setting bits AL2[6] and AL2[5], respectively, in the ALERT2 register.

GPIO1-3 can be pulled low as general purpose outputs, which are otherwise high impedance. GPIO3 is by default an $\overline{\text{ALERT}}$ output that pulls low when an alert event is present. To pull GPIO3 ($\overline{\text{ALERT}}$) low in the absence of an alert event, set GC[7] of the GPIO3_CTRL register (Table 12). Clearing this bit will release the GPIO3 ($\overline{\text{ALERT}}$). GC[7] does not have an effect on GPIO3 if it is not configured as an $\overline{\text{ALERT}}$ output. Likewise, GC[6] does not affect GPIO3 if it is not configured as a general purpose output. GC[7] is set whenever an alert event occurs irrespective of GPIO3's configuration. Reset GC[7] before reconfiguring GPIO3 to $\overline{\text{ALERT}}$.

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I²C Reset

The accumulators can be programmed to reset themselves after the host reads the last byte (3Fh) of the accumulator data by writing bits CB[1:0] to [01] in the CTRLB register (Table 4). This feature removes the need to issue a reset command after polling the LTC2946 for accumulated data. The accumulators will continue to accumulate after the reset. To reset the accumulators without such read command, write bits CB[1:0] to [10]. The accumulators will stay reset if CB[1:0] = [10]. All registers are reset when CB[1:0] = [11], and these bits will then auto-reset to [00].

The ADC sequencing configuration is preserved through the I²C reset, regardless of the CTRLA register having reset. To change the sequencing configuration after such resets, rewrite the CTRLA register.

Storing Minimum and Maximum Values

The LTC2946 compares each measurement including the calculated power with the stored values in the respective MIN and MAX registers for each parameter (Table 2). If the new conversion is beyond the stored minimum or maximum values, the MIN or MAX registers are updated with the new values. The MIN and MAX of the registers are refreshed at the end of their respective ADC conversions in continuous scan modes and snapshot mode. They are also refreshed if the ADC registers are written via the I²C bus with values beyond the stored values. To initiate a new peak hold cycle, write all 1's to the MIN registers and all 0's to the MAX registers via the I²C bus. These registers will be updated when the next respective ADC conversion is done.

The LTC2946 also includes MIN and MAX threshold registers (Table 2) for the measured parameters including the calculated power. At power-up, the maximum thresholds are set to all 1's, and minimum thresholds are set to all 0's, effectively disabling them. The thresholds can be reprogrammed to any desired value via the I²C bus.

Fault Alert and Resetting Faults

As soon as a measured quantity falls below the minimum threshold or exceeds the maximum threshold, the LTC2946 sets the corresponding flag in the STATUS1 (Table 6) register and latches it into the FAULT1 (Table 7) register (see Figure 6). Other events such as GPIO state change, stuck bus wake-up and accumulator overflow have their present status in the STATUS2 (Table 10) register and any fault is latched in the FAULT2 (Table 11) register. The GPIO3 pin is pulled low if the appropriate bit in the ALERT1 (Table 5) and ALERT2 (Table 8) registers is set and it is configured as $\overline{\text{ALERT}}$ output. More details on the alert behavior can be found in the Alert Response Protocol section.

An active fault indication can be reset by writing zeros to the corresponding FAULT register bits or setting bit CB[5] in the CTRLB register. If bit CB[5] is set, reading the FAULT1 or FAULT2 register will cause the corresponding register to reset. All FAULT register bits are also cleared if the V_{DD} and $INTV_{CC}$ fall below their respective I²C logic reset threshold. Note that faults that are still present, as indicated in the STATUS1 and STATUS2 registers, will immediately reappear.

When accumulators (time, charge and energy) overflow, the corresponding bits in the STATUS2 register are set and will stay set. The accumulator overflow bits in the FAULT2 register will reappear after they have been cleared via I²C since the STATUS2 register continues to indicate overflow faults.

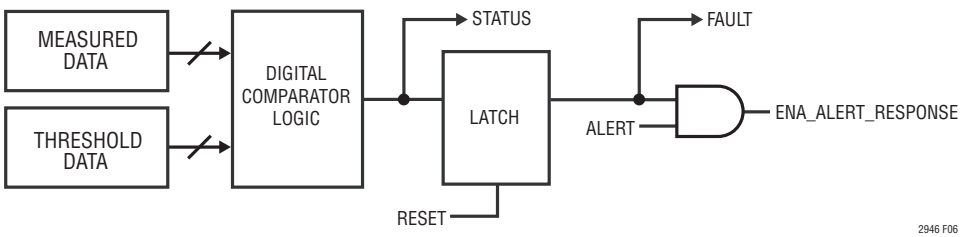

Figure 6. LTC2946 Fault Alert Generation Blocks

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If it is necessary to clear accumulator overflow fault(s), the recommended procedure is:

1. Read the accumulators
2. Store these values in an external memory
3. Issue a reset to the accumulators by writing bits CB[1:0] to [10]. Then disable reset by writing bits CB[1:0] to [00].
4. Write the stored values back to the accumulators

Steps 2 and 4 can be skipped if there is no need to continue the accumulation from present values.

I²C Interface

The LTC2946 includes an I²C/SMBus-compatible interface to provide access to the onboard registers. Figure 6 shows a general data transfer format using the I²C bus.

The LTC2946 is a read/write slave device and supports the SMBus read byte, write byte, read word and write word protocols. The LTC2946 also supports extended read and write commands that allow reading or writing more than two bytes of data. When using the read/write word or extended read and write commands, the bus master issues an initial register address and the internal register address

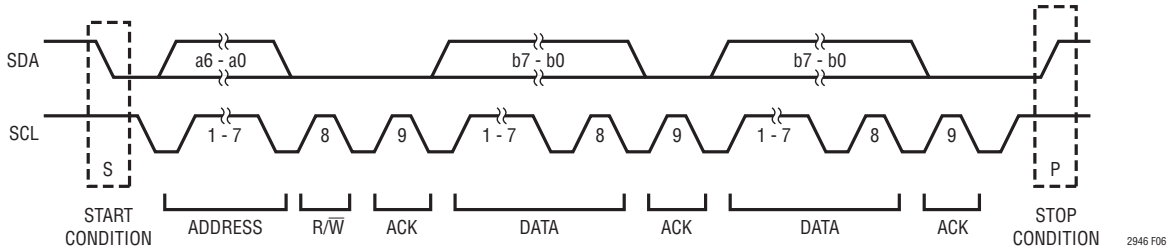

Figure 7. General Data Transfer Over I²C

S	ADDRESS	W	A	COMMAND	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	

2946 F08

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
Ā: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
W: WRITE BIT (LOW
S: START CONDITIOI
P: STOP CONDITION

Figure 8. LTC2946 Serial Bus SDA Write Byte Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	b7:b0	0	

2946 F09

Figure 9. LTC2946 Serial Bus SDA Write Word Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	...	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	b7:b0	0	...	b7:b0	0	

2946 F10

Figure 10. LTC2946 Serial Bus SDA Write Page Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	1	

2946 F11

Figure 11. LTC2946 Serial Bus SDA Read Byte Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	1	

2946 F12

Figure 12. LTC2946 Serial Bus SDA Read Word Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	...	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	...	b7:b0	1	

2946 F13

Figure 13. LTC2946 Serial Bus SDA Read Page Protocol Protocol

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pointer automatically increments by 1 after each byte of data is read or written. After the register address reaches 43h, it will roll over to 00h and continue incrementing. A STOP condition resets the register address pointer to 00h. The data formats for the above commands are shown in Figure 7 through Figure 13. Note that only the read byte command is available to the E7 and E8 (MFR_SPECIAL_ID) registers (Table 2).

I²C Device Addressing

Nine distinct I²C bus addresses are configurable using the three-state pins ADR0 and ADR1, as shown in Table 1.

ADR0 and ADR1 should be tied to $INTV_{CC}$, to GND, or left floating (NC) to configure the lower four address bits. During low power shutdown, the address select state is latched into memory powered from standby supply. Address bits a6, a5 and a4 are permanently set to 110b and the least significant bit is the R/$\overline{W}$ bit. In addition, all LTC2946 devices will respond to a common mass write address 1100_110b; this allows the bus master to write to several LTC2946s simultaneously, regardless of their individual address settings. The LTC2946 will also respond to the standard ARA address 0001_100b if the GPIO3 ($\overline{ALERT}$) pin is asserted. See the Alert Response Protocol section for more details. The LTC2946 will not respond to the ARA address if no alerts are pending.

START and STOP Conditions

When the I²C bus is idle, both SCL and SDA are in the HIGH state. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL stays high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to high while SCL stays high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTC2946 I²C interface features a stuck-bus reset timer to prevent it from holding the bus lines low indefinitely if the SCL signal is interrupted during a transfer. The timer starts when either SCL or SDAI is low, and resets when both SCL and SDAI are pulled high. If either SCL or SDAI are low for over 33ms, the stuck-bus timer will expire, and the internal I²C interface and the SDAO pin pull-down logic will be reset to release the bus. Normal communication will resume at the next START command.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave to indicate that the last byte of data was received. The master always releases the SDA line during the acknowledge clock pulse. The LTC2946 will pull the SDA line low on the 9th clock cycle to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must acknowledge the slave by pulling down the SDA line during the 9th clock pulse to indicate receipt of a data byte. After the last byte has been received by the master, it will leave the SDA line high (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins a write operation with a START condition followed by the seven-bit slave address and the R/$\overline{W}$ bit set to zero. After the addressed LTC2946 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to write. The LTC2946 acknowledges this and then latches the lower six bits of the command byte into its internal register address pointer. The master then delivers the data byte and the LTC2946 acknowledges once more and writes the data into the internal register pointed to by the register address pointer. If the master continues sending additional data bytes with a write word or extended write command, the additional data bytes will be acknowledged by the LTC2946, the register address pointer will automatically increment by one, and data will be written as previously stated. The write operation terminates and the register address pointer resets to 00h when the master sends a STOP condition.

Read Protocol

The master begins a read operation with a START condition followed by the 7-bit slave address and the R/W bit set to zero. After the addressed LTC2946 acknowledges

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the address byte, the master then sends a command byte that indicates which internal register the master wishes to read. The LTC2946 acknowledges this and then latches the lower six bits of the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same 7-bit address with the R/W bit now set to 1. The LTC2946 acknowledges and sends the contents of the requested register. The transmission terminates when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a read word command, the LTC2946 will send the contents of the next register. If the master keeps acknowledging, the LTC2946 will keep incrementing the register address pointer and sending out data bytes. The read operation terminates and the register address pointer resets to 00h when the master sends a STOP condition.

Alert Response Protocol

When any of the fault bits in the FAULT1 and FAULT2 register are set, a bus alert is generated if the appropriate bit in the ALERT1 or ALERT2 register has been set and GPIO3 is configured as an $\overline{\text{ALERT}}$ output. This allows the bus master to select which faults will generate alerts. At power-up, both ALERT registers are cleared (no alerts enabled) and the GPIO3 ($\overline{\text{ALERT}}$) pin is high. If an alert is enabled, the corresponding fault causes the GPIO3 ($\overline{\text{ALERT}}$) pin to pull low. The bus master responds to the alert in accordance with the SMBus alert response protocol by broadcasting the alert response address 0001_100b, and the LTC2946 replies with its own address and releases its GPIO3 ($\overline{\text{ALERT}}$) pin, as shown in Figure 14. The GPIO3 ($\overline{\text{ALERT}}$) line is also released if CB[7] is set and the LTC2946 is addressed (see Table 4) by any message. The GPIO3 ($\overline{\text{ALERT}}$) signal is not pulled low again until the FLT registers indicate a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate additional alerts until the associated FLT register bits have been cleared.

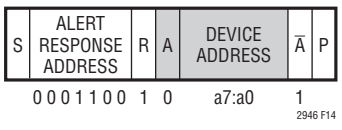

Figure 14. LTC2946 Serial Bus SDA Alert Response Protocol

If two or more LTC2946s on the same bus are generating alerts when the ARA is broadcast, the bus master will repeat the alert response protocol until the GPIO3 ($\overline{\text{ALERT}}$) line is released. Standard I^2C arbitration causes the device with the highest priority (lowest address) to reply first and the device with the lowest priority (highest address) to reply last.

Opto-Isolating the I^2C Bus

Opto-isolating a standard I^2C device is complicated by the bidirectional SDA pin. The LTC2946/LTC2946-1 minimize this problem by splitting the standard I^2C SDA line into SDAI (input) and SDAO (output, LTC2946) or $\overline{\text{SDAO}}$ (inverted output, LTC2946-1). The SCL is an input-only pin and does not require special circuitry to isolate. For conventional nonisolated I^2C applications, use the LTC2946 and tie the SDAI and SDAO pins together to form a standard I^2C SDA pin.

Low speed isolated interfaces that use standard open-drain opto-isolators can use the LTC2946 with the SDAI and SDAO pins separated, as shown in Figure 15. Connect SDAI to the output of the incoming opto-isolator with a pull-up resistor to $INTV_{CC}$ or a local 5V supply; connect SDAO to the cathode of the outgoing opto-isolator with a current-limiting resistor in series with the anode. The input and output must be connected together on the isolated side of the bus to allow the LTC2946 to participate in I^2C arbitration. Note that maximum I^2C bus speed will generally be limited by the speed of the opto-couplers used in this application.

The shunt regulators can supply up to 34mA of current to drive opto-isolator and pull-up resistors, as shown in Figure 16 and Figure 17. For identical SDAI/SCL pull-up resistors the maximum load is:

$$I_{LOAD(MAX)} = V_{CCZ(MAX)} \bullet \left(\frac{2}{R5} + \frac{1}{R4}\right) \quad (2)$$

$$I_{LOAD(MAX)} = 6.7V \bullet \left(\frac{2}{R5} + \frac{1}{R4}\right)$$

R_{SHUNT} can then be calculated using Equation 1. Note that both LTC2946 and LTC2946-1 can be used in the shunt

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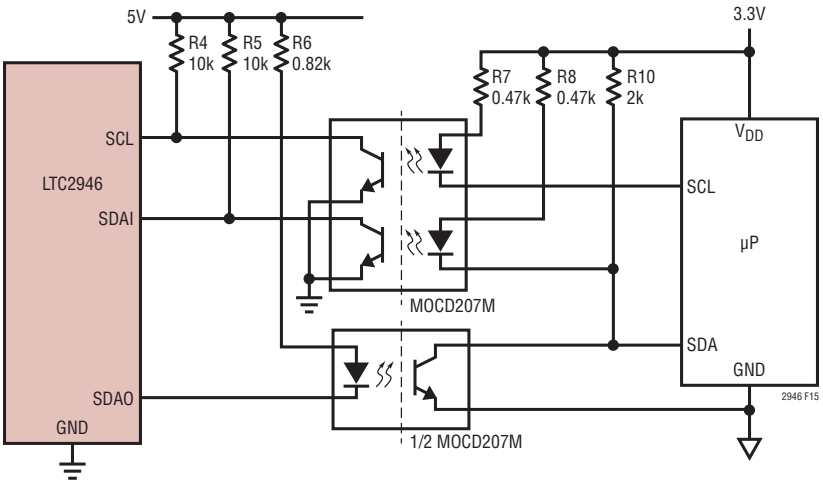

Figure 15. Opto-Isolation of a 10kHz I²C Interface Between LTC2946 and Microcontroller

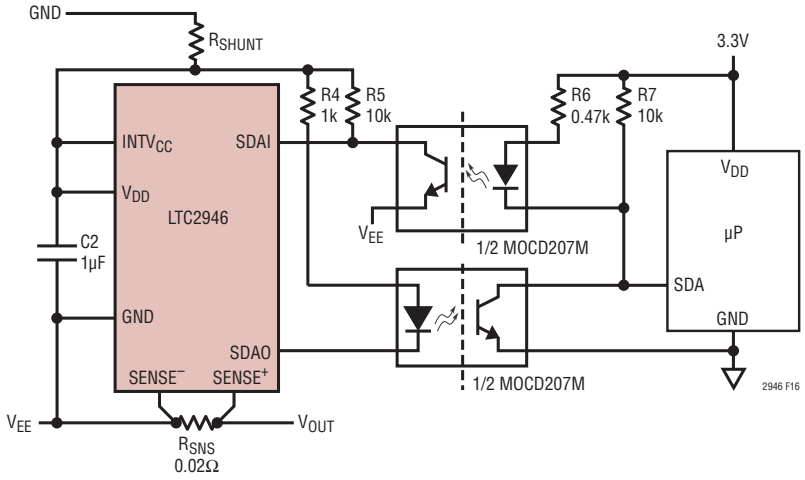

Figure 16. Low Speed 10kHz Opto-Isolators Powered from Low Side Shunt Regulator (SCL Omitted for Clarity)

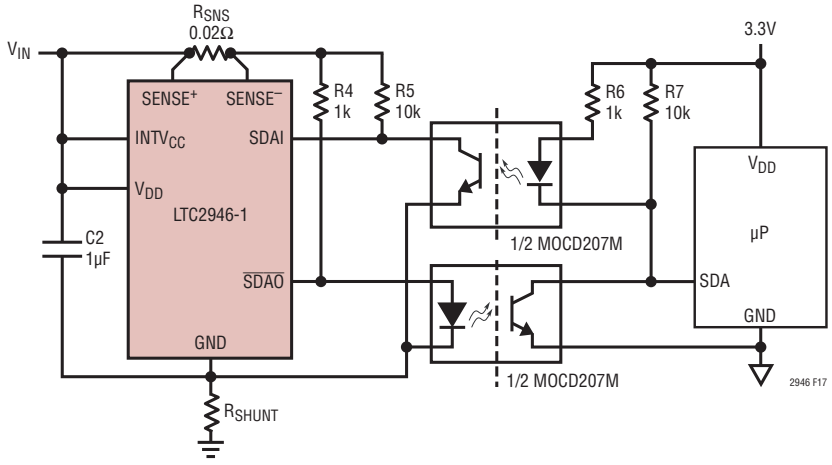

Figure 17. Low Speed 10kHz Opto-Isolators Powered from High Side Shunt Regulator (SCL Omitted for Clarity)

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regulator applications mentioned. Figure 18 shows an alternate connection for use with low speed opto-couplers and the LTC2946-1. This circuit uses a limited-current pull-up on the internally clamped SDAI pin and clamps the $\overline{SDAO}$ pin with the input diode of the outgoing opto-isolator, removing the need to use $INTV_{CC}$ for biasing in the absence of an auxiliary low voltage supply. For proper clamping:

$$\frac{V_{S(MAX)} - V_{SDA,SCL(MIN)}}{I_{SDA,SCL(MAX)}} \leq R4 \leq \frac{V_{S(MAX)} - V_{SDA,SCL(MAX)}}{I_{SDA,SCL(MIN)}} \quad (3)$$

$$\frac{V_{S(MAX)} - 5.9V}{5mA} \leq R4 \leq \frac{V_{S(MAX)} - 6.9V}{0.5mA}$$

As an example, a supply that operates from 36V to 72V would require the value of R4 to be between 13k and 58k.

The LTC2946-1 must be used in this application to ensure that the $\overline{SDAO}$ signal polarity is correct.

The LTC2946-1 can also be used with high speed opto-couplers with push-pull outputs and inverted logic as shown in Figure 19. The incoming opto-isolator draws power from the $INTV_{CC}$, and the data output is connected directly to the SDAI pin with no pull-up required. Ensure the current drawn does not exceed the 10mA maximum capability of the $INTV_{CC}$ pin. The $\overline{SDAO}$ pin is connected to the cathode of the outgoing opto-coupler with a current limiting resistor connected back to $INTV_{CC}$. An additional discrete N-channel MOSFET is required at the output of the outgoing opto-coupler to provide the open-drain pull-down that the I^2C bus requires. Finally, the input of the incoming opto-isolator is connected back to the output as in the low speed case.

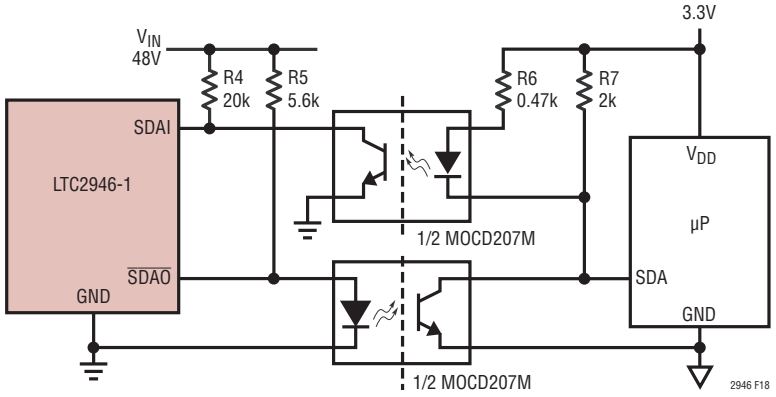

Figure 18. Opto-Isolation of a 1.5kHz I^2C Interface Between LTC2946-1 and Microcontroller (SCL Omitted for Clarity)

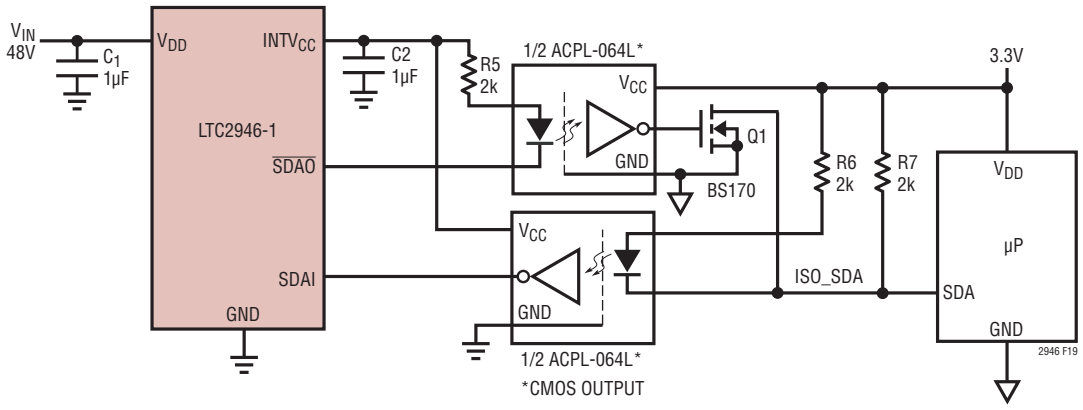

Figure 19. Opto-Isolation of a I^2C Interface with Low Power, High Speed Opto-Couplers (SCL Omitted for Clarity)

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Layout Considerations

A Kelvin connection between the sense resistor R_{SNS} and the LTC2946 is recommended to achieve accurate current sensing (Figure 20). The recommended minimum trace width for 1oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is preferred. Note that 1oz copper exhibits a sheet resistance of about 530µΩ per square. In very high current applications where the sense resistor can dissipate significant power, the PCB layout should include good thermal management techniques such as extra vias and wide metal area.

The crystal oscillator's clock amplitude is sensitive to parasitics such as stray capacitance on the CLKOUT pin and coupling between the CLKIN and CLKOUT pins. It is recommended that the CLKIN and CLKOUT traces from the LTC2946 to the crystal oscillator network be as short as practical with the load capacitors placed next to the crystal, as shown in Figure 21. To minimize stray capacitances, avoid large ground planes and digital signals near the crystal network.

Design Example

Given a 20mΩ sense resistor, calculate the weight value per LSB for the current, power, charge and energy registers:

Current = 25µV/LSB/R_{SNS}
= 1.25mA/LSB

Voltage = 25mV/LSB
($SENSE^+$/V_{DD} is sensing the voltage)

Power = 1.25mA/LSB • 25mV/LSB
= 31.25µW/LSB

Time = 16.39543ms/LSB (default configuration 250kHz target frequency)

Charge = 1.25mA/LSB • 16 • 16.384ms/LSB
= 327.9086µC/LSB

Energy = 31.25µW • 65536 • 16.39543ms
= 33.578mJ/LSB

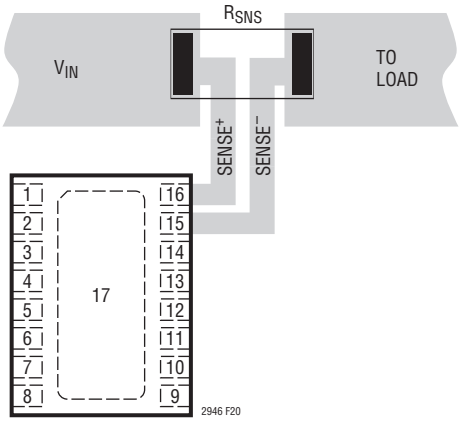

Figure 20. Recommended Layout for Kelvin Connection

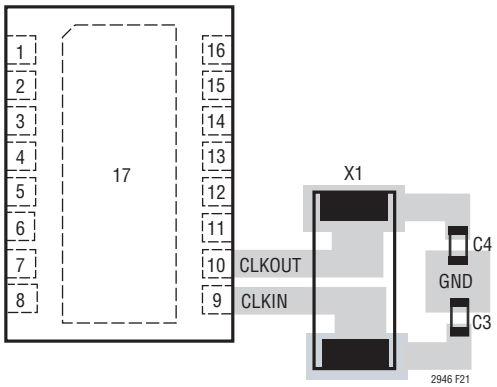

Figure 21. Recommended Layout for Crystal Oscillator

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Table 1. LTC2946 Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC2946 ADDRESS PINS	
	h	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$	ADR1	ADR0
Mass Write	CC	1	1	0	0	1	1	0	0	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X
0	CE	1	1	0	0	1	1	1	X	H	L
1	D0	1	1	0	1	0	0	0	X	NC	H
2	D2	1	1	0	1	0	0	1	X	H	H
3	D4	1	1	0	1	0	1	0	X	NC	NC
4	D6	1	1	0	1	0	1	1	X	NC	L
5	D8	1	1	0	1	1	0	0	X	L	H
6	DA	1	1	0	1	1	0	1	X	H	NC
7	DC	1	1	0	1	1	1	0	X	L	NC
8	DE	1	1	0	1	1	1	1	X	L	L

Table 2. LTC2946 Register Addresses and Contents

REGISTER ADDR	REGISTER NAME	READ/WRITE	DESCRIPTION	DEFAULT
00h	CTRLA	R/W	Operation Control Register A	18h
01h	CTRLB	R/W	Operation Control Register B	00h
02h	ALERT1	R/W	Selects Which Primary Faults Generate Alerts	00h
03h	STATUS1	R	Primary Status Information	00h
04h	FAULT1	R/W	Primary Fault Log	00h
05h	POWER MSB2	R/W	Power MSB2 Data	XXh
06h	POWER MSB1	R/W	Power MSB1 Data	XXh
07h	POWER LSB	R/W	Power LSB Data	XXh
08h	MAX POWER MSB2	R/W	Maximum Power MSB2 Data	00h
09h	MAX POWER MSB1	R/W	Maximum Power MSB1 Data	00h
0Ah	MAX POWER LSB	R/W	Maximum Power LSB Data	00h
0Bh	MIN POWER MSB2	R/W	Minimum Power MSB2 Data	FFh
0Ch	MIN POWER MSB1	R/W	Minimum Power MSB1 Data	FFh
0Dh	MIN POWER LSB	R/W	Minimum Power LSB Data	FFh
0Eh	MAX POWER THRESHOLD MSB2	R/W	Maximum POWER Threshold MSB2 to Generate Alert	FFh
0Fh	MAX POWER THRESHOLD MSB1	R/W	Maximum POWER Threshold MSB1 to Generate Alert	FFh
10h	MAX POWER THRESHOLD LSB	R/W	Maximum POWER Threshold LSB to Generate Alert	FFh
11h	MIN POWER THRESHOLD MSB2	R/W	Minimum POWER Threshold MSB2 to Generate Alert	00h
12h	MIN POWER THRESHOLD MSB1	R/W	Minimum POWER Threshold MSB1 to Generate Alert	00h
13h	MIN POWER THRESHOLD LSB	R/W	Minimum POWER Threshold LSB to Generate Alert	00h
14h	ΔSENSE MSB	R/W	ΔSENSE MSB Data	XXh
15h	ΔSENSE LSB	R/W	ΔSENSE LSB Data	X0h
16h	MAX ΔSENSE MSB	R/W	Maximum ΔSENSE MSB Data	00h
17h	MAX ΔSENSE LSB	R/W	Maximum ΔSENSE LSB Data	00h
18h	MIN ΔSENSE MSB	R/W	Minimum ΔSENSE MSB Data	FFh
19h	MIN ΔSENSE LSB	R/W	Minimum ΔSENSE LSB Data	F0h
1Ah	MAX ΔSENSE THRESHOLD MSB	R/W	Maximum ΔSENSE Threshold MSB to Generate Alert	FFh

APPLICATIONS INFORMATION

1Bh	MAX ΔSENSE THRESHOLD LSB	R/W	Maximum ΔSENSE Threshold LSB to Generate Alert	F0h
1Ch	MIN ΔSENSE THRESHOLD MSB	R/W	Minimum ΔSENSE Threshold MSB to Generate Alert	00h
1Dh	MIN ΔSENSE THRESHOLD LSB	R/W	Minimum ΔSENSE Threshold LSB to Generate Alert	00h
1Eh	V_{IN} MSB	R/W	ADC V_{IN} MSB Data	XXh
1Fh	V_{IN} LSB	R/W	ADC V_{IN} LSB Data	X0h
20h	MAX V_{IN} MSB	R/W	Maximum V_{IN} MSB Data	00h
21h	MAX V_{IN} LSB	R/W	Maximum V_{IN} LSB Data	00h
22h	MIN V_{IN} MSB	R/W	Minimum V_{IN} MSB Data	FFh
23h	MIN V_{IN} LSB	R/W	Minimum V_{IN} LSB Data	F0h
24h	MAX V_{IN} THRESHOLD MSB	R/W	Maximum V_{IN} Threshold MSB to Generate Alert	FFh
25h	MAX V_{IN} THRESHOLD LSB	R/W	Maximum V_{IN} Threshold LSB to Generate Alert	F0h
26h	MIN V_{IN} THRESHOLD MSB	R/W	Minimum V_{IN} Threshold MSB to Generate Alert	00h
27h	MIN V_{IN} THRESHOLD LSB	R/W	Minimum V_{IN} Threshold LSB to Generate Alert	00h
28h	ADIN MSB	R/W	ADIN MSB Data	XXh
29h	ADIN LSB	R/W	ADIN LSB Data	X0h
2Ah	MAX ADIN MSB	R/W	Maximum ADIN MSB Data	00h
2Bh	MAX ADIN LSB	R/W	Maximum ADIN LSB Data	00h
2Ch	MIN ADIN MSB	R/W	Minimum ADIN MSB Data	FFh
2Dh	MIN ADIN LSB	R/W	Minimum ADIN LSB Data	F0h
2Eh	MAX ADIN THRESHOLD MSB	R/W	Maximum ADIN Threshold MSB to Generate Alert	FFh
2Fh	MAX ADIN THRESHOLD LSB	R/W	Maximum ADIN Threshold LSB to Generate Alert	F0h
30h	MIN ADIN THRESHOLD MSB	R/W	Minimum ADIN Threshold MSB to Generate Alert	00h
31h	MIN ADIN THRESHOLD LSB	R/W	Minimum ADIN Threshold LSB to Generate Alert	00h
32h	ALERT2	R/W	Selects Which Secondary Faults Generate Alerts	00h
33h	GPIO_CFG	R/W	GPIO Configuration	00h
34h	TIME COUNTER MSB3	R/W	Time Counter MSB Data3	XXh
35h	TIME COUNTER MSB2	R/W	Time Counter MSB Data2	XXh
36h	TIME COUNTER MSB1	R/W	Time Counter MSB Data1	XXh
37h	TIME COUNTER LSB	R/W	Time Counter LSB Data	XXh
38h	CHARGE MSB3	R/W	Charge MSB Data3	XXh
39h	CHARGE MSB2	R/W	Charge MSB Data2	XXh
3Ah	CHARGE MSB1	R/W	Charge MSB Data1	XXh
3Bh	CHARGE LSB	R/W	Charge LSB Data	XXh
3Ch	ENERGY MSB3	R/W	Energy MSB Data3	XXh
3Dh	ENERGY MSB2	R/W	Energy MSB Data2	XXh
3Eh	ENERGY MSB1	R/W	Energy MSB Data1	XXh
3Fh	ENERGY LSB	R/W	Energy LSB Data	XXh
40h	STATUS2	R	Secondary Status Information	00h
41h	FAULT2	R/W	Secondary Fault Log	00h
42h	GPIO3_CTRL	R/W	GPIO3 Control Command	00h
43h	CLK_DIV	R/W	Clock Divider Command	04h
E7h	MFR_SPECIAL_ ID MSB	R	Manufacturer Special ID MSB Data	60h
E8h	MFR_SPECIAL_ID LSB	R	Manufacturer Special ID LSB Data	01h

APPLICATIONS INFORMATION

Table 3. CTRLA Register (00h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
CA[7]	ADIN Configuration	[1] = ADIN Measured with Respect to $INTV_{CC}$ [0] = ADIN Measured with Respect to GND	0
CA[6:5]	Offset Calibration Configuration	Offset Calibration [11] = 1st Power-Up or Use Last Calibrated Result [10] = Once Every 128 Conversions [01] = Once Every 16 Conversions [00] = Every Conversion	00
CA[4 :3]	Voltage Selection	[11] = $SENSE^+$ [10] = ADIN [01] = V_{DD} [00] = ΔSENSE**	11
CA[2 :0]	Channel Configuration	[111] = Snapshot Mode (Channel Defined by CA[4:3]). No Power, Energy or Charge Data Generated [110] = Voltage Measurement Once Followed by Current Measurement Indefinitely* [101] = ADIN, Voltage, Current Measurement at 1/256, 1/256 and 254/256 Duty Cycle, Respectively* [100] = ADIN, Voltage, Current Measurement at 1/32, 1/32 and 30/32 Duty Cycle, Respectively* [011] = Alternate ADIN, Voltage and Current Measurement* [010] = Voltage, Current Measurement at 1/128 and 127/128 Duty Cycle, Respectively* [001] = Voltage, Current Measurement at 1/16 and 15/16 Duty Cycle, Respectively* [000] = Alternate Voltage, Current Measurement*	000

*Voltage defined by CA[4:3] in polling modes.

**If ΔSENSE (00) is selected and the channel configuration is other than snapshot mode (111) the voltage data is always the value in the V_{IN} register prior to the mode change. It is recommended that ΔSENSE be avoided when polling modes are used.

Table 4. CTRLB Register (01h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
CB[7]	$\overline{ALERT}$ Clear Enable	Clear $\overline{ALERT}$ if Device is Addressed by the Master [1] = Enable [0] = Disable	0
CB[6]	Shutdown	[1] = Shutdown [0] = Power-Up	0
CB[5]	Cleared on Read Control	FAULT Registers Cleared on Read [1] = Cleared on Read [0] = Registers Not Affected by Reading	0
CB[4]	Stuck Bus Timeout Auto Wake-Up	Allows Part to Exit Shutdown Mode When Stuck-Bus Timer Is Reached [1] = Enable [0] = Disable	0
CB[3:2]	Enable Accumulation	[11] = Reserved [10] = Follows ACC State (GPIO2, See Table 9) ACC High, Accumulate ACC Low, No Accumulate [01] = No Accumulate [00] = Accumulate	00
CB[1:0]	Auto-Reset Mode/Reset	[11] = Reset All Registers [10] = Reset Accumulator (Time Counter, Charge and Energy) Registers [01] = Enable Auto-Reset [00] = Disable Auto-Reset	00

APPLICATIONS INFORMATION

Table 5. ALERT1 Register (02h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
AL1[7]	Maximum POWER Alert	Enables Alert When POWER > Maximum POWER Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[6]	Minimum POWER Alert	Enables Alert When POWER < Minimum POWER Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[5]	Maximum I_{SENSE} Alert	Enables Alert When I_{SENSE} > Maximum I_{SENSE} Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[4]	Minimum I_{SENSE} Alert	Enables Alert When I_{SENSE} < Minimum I_{SENSE} Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[3]	Maximum V_{IN} Alert	Enables Alert When V_{IN} > Maximum V_{IN} Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[2]	Minimum V_{IN} Alert	Enables Alert When V_{IN} < Minimum V_{IN} Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[1]	Maximum ADIN Alert	Enables Alert When ADIN > Maximum ADIN Threshold [1] = Enable Alert [0] = Disable Alert	0
AL1[0]	Minimum ADIN Alert	Enables Alert When ADIN < Minimum ADIN Threshold [1] = Enable Alert [0] = Disable Alert	0

Table 6. STATUS1 Register (03h): Read

BIT	REGISTER NAME	OPERATION	DEFAULT
S1[7]	POWER Overvalue	POWER > Maximum POWER Threshold [1] = POWER Overvalue [0] = POWER Not Overvalue	0
S1[6]	POWER Undervalue	POWER < Minimum POWER Threshold [1] = POWER Undervalue [0] = POWER Not Undervalue	0
S1[5]	I_{SENSE} Overvalue	I_{SENSE} > Maximum I_{SENSE} Threshold [1] = I_{SENSE} Overvalue [0] = I_{SENSE} Not Overvalue	0
S1[4]	I_{SENSE} Undervalue	I_{SENSE} < Minimum I_{SENSE} Threshold [1] = I_{SENSE} Undervalue [0] = I_{SENSE} Not Undervalue	0
S1[3]	V_{IN} Overvalue	V_{IN} > Maximum V_{IN} Threshold [1] = V_{IN} Overvalue [0] = V_{IN} Not Overvalue	0
S1[2]	V_{IN} Undervalue	VIN < Minimum V_{IN} Threshold [1] = V_{IN} Undervalue [0] = V_{IN} Not Undervalue	0
S1[1]	ADIN Overvalue	ADIN > Maximum ADIN Threshold [1] = ADIN Overvalue [0] = ADIN Not Overvalue	0
S1[0]	ADIN Undervalue	ADIN < Minimum ADIN Threshold [1] = ADIN Undervalue [0] = ADIN Not Undervalue	0

APPLICATIONS INFORMATION

Table 7. FAULT1 Register (04h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
F1[7]	POWER Overvalue Fault	POWER > Maximum POWER Threshold [1] = POWER Overvalue Fault Occurred [0] = No POWER Overvalue Fault Occurred	0
F1[6]	POWER Undervalue Fault	POWER < Minimum POWER Threshold [1] = POWER Undervalue Fault Occurred [0] = No POWER Undervalue Fault Occurred	0
F1[5]	I_{SENSE} Overvalue Fault	I_{SENSE} > Maximum I_{SENSE} Threshold [1] = I_{SENSE} Overvalue Fault Occurred [0] = No I_{SENSE} Overvalue Fault Occurred	0
F1[4]	I_{SENSE} Undervalue Fault	I_{SENSE} < Minimum I_{SENSE} Threshold [1] = I_{SENSE} Undervalue Fault Occurred [0] = No I_{SENSE} Undervalue Fault Occurred	0
F1[3]	V_{IN} Overvalue Fault	VIN > Maximum V_{IN} Threshold [1] = V_{IN} Overvalue Fault Occurred [0] = No V_{IN} Overvalue Fault Occurred	0
F1[2]	V_{IN} Undervalue Fault	VIN < Minimum V_{IN} Threshold [1] = V_{IN} Undervalue Fault Occurred [0] = No V_{IN} Undervalue Fault Occurred	0
F1[1]	ADIN Overvalue Fault	ADIN > Maximum ADIN Threshold [1] = ADIN Overvalue Fault Occurred [0] = No ADIN Overvalue Fault Occurred	0
F1[0]	ADIN Undervalue Fault	ADIN < Minimum ADIN Threshold [1] = ADIN Undervalue Fault Occurred [0] = No ADIN Undervalue Fault Occurred	0

Table 8. ALERT2 Register (32h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
AL2[7]	ADC Conversion Done Alert	Alert When ADC Finishes a Conversion [1] = Enable [0] = Disable	0
AL2[6]	GPIO1 Input Alert	Alert if GPIO1 Is Low When GP[7:6] = [01] (GPIO1 Input Active Low), or GPIO1 Is High When GP[7:6] = [00] (GPIO1 Input Active High) [1] = Enable Alert [0] = Disable Alert	0
AL2[5]	GPIO2 Input Alert	Alert if GPIO2 Is Low When GP[5:4] = [01] (GPIO2 Input Active Low), or GPIO2 Is High When GP[5:4] = [00] (GPIO2 Input Active High) [1] = Enable Alert [0] = Disable Alert	0
AL2[4]	Reserved		0
AL2[3]	Stuck-Bus Timeout Wake-Up Alert	Alert if Part Exits Shutdown Mode After Stuck-Bus Timer Expires with CB[4] = 1 [1] = Enable Alert [0] = Disable Alert	0
AL2[2]	Energy Overflow Alert	Alert if Energy Register Overflow [1] = Enable Alert [0] = Disable Alert	0

APPLICATIONS INFORMATION

AL2[1]	Charge Overflow Alert	Alert if Charge Register Overflow [1] = Enable Alert [0] = Disable Alert	0
AL2[0]	Time Counter Overflow Alert	Alert if Time Counter Register Overflow [1] = Enable Alert [0] = Disable Alert	0

Table 9. GPIO_CFG Register (33h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
GP[7:6]	GPIO1 Configure	[11] = General Purpose Input, Active High [10] = General Purpose Input, Active Low [01] = General Purpose Output, Hi-Z [00] = General Purpose Output, Pulls Low	00
GP[5:4]	GPIO2 Configure	[11] = General Purpose Input, Active High [10] = General Purpose Input, Active Low [01] = General Purpose Output, GPIO = GP[1] [00] = Accumulate Input	00
GP[3:2]	GPIO3 Configure	[11] = General Purpose Input, Active High [10] = General Purpose Input, Active Low [01] = General Purpose Output, See Register 42h (Table 12) [00] = $\overline{\text{ALERT}}$ Output	00
GP[1]	GPIO2 Output	[1] = Pulls Low [0] = Hi-Z	0
GP[0]	Reserved		0

APPLICATIONS INFORMATION

Table 10. STATUS2 Register (40h): Read

<table>
<tr><th>BIT</th><th>NAME</th><th>OPERATION</th><th>DEFAULT</th></tr>
<tr><td>S2[7]</td><td>Reserved</td><td></td><td>0</td></tr>
<tr><td>S2[6]</td><td>GPIO1 State</td><td>
<table>
<tr><th>GP[7]</th><th>GP[6]</th><th>Function</th><th>GPIO State</th></tr>
<tr><td>1</td><td>0</td><td>GPIO1 Input = Active Low</td><td>[1] = GPIO1 Low
[0] = GPIO1 High</td></tr>
<tr><td>1</td><td>1</td><td>GPIO1 Input = Active High</td><td>[1] = GPIO1 High
[0] = GPIO1 Low</td></tr>
</table>
</td><td>0</td></tr>
<tr><td>S2[5]</td><td>GPIO2 State</td><td>
<table>
<tr><th>GP[5]</th><th>GP[4]</th><th>Function</th><th>GPIO State</th></tr>
<tr><td>0</td><td>0</td><td>GPIO2 Input = ACC</td><td>[1] = ACC High
[0] = ACC Low</td></tr>
<tr><td>1</td><td>0</td><td>GPIO2 Input = Active Low</td><td>[1] = GPIO2 Low
[0] = GPIO2 High</td></tr>
<tr><td>1</td><td>1</td><td>GPIO2 Input = Active High</td><td>[1] = GPIO2 High
[0] = GPIO2 Low</td></tr>
</table>
</td><td>0</td></tr>
<tr><td>S2[4]</td><td>GPIO3 State</td><td>
<table>
<tr><th>GP[3]</th><th>GP[2]</th><th>Function</th><th>GPIO State</th></tr>
<tr><td>1</td><td>0</td><td>GPIO3 Input = Active Low</td><td>[1] = GPIO3 Low
[0] = GPIO3 High</td></tr>
<tr><td>1</td><td>1</td><td>GPIO3 Input = Active High</td><td>[1] = GPIO3 High
[0] = GPIO3 Low</td></tr>
</table>
</td><td>0</td></tr>
<tr><td>S2[3]</td><td>ADC Busy in Snapshot Mode</td><td></td><td>0</td></tr>
<tr><td>S2[2]</td><td>Energy Register Overflow</td><td>Energy Register Overflow
[1] = Energy Register Overflow
[0] = Energy Register Not Overflow</td><td>0</td></tr>
<tr><td>S2[1]</td><td>Charge Register Overflow</td><td>Charge Register Overflow
[1] = Charge Register Overflow
[0] = Charge Register Not Overflow</td><td>0</td></tr>
<tr><td>S2[0]</td><td>Time Counter Register Overflow</td><td>Time Counter Register Overflow
[1] = Time Counter Register Overflow
[0] = Time Counter Register Not Overflow</td><td>0</td></tr>
</table>

APPLICATIONS INFORMATION

Table 11. FAULT2 Register (41h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
F2[7]	Reserved		1
F2[6]	GPIO1 Input Fault	Indicates GPIO1 Was at Active Level as a General Purpose Input [1] = GPIO1 Input Was Active [0] = GPIO1 Input Was Inactive	0
F2[5]	GPIO2 Input Fault	Indicates GPIO2 Was at Active Level as a General Purpose Input [1] = GPIO2 Input Was Active [0] = GPIO2 Input Was Inactive	0
F2[4]	GPIO3 Input Fault	Indicates GPIO3 Was at Active Level as a General Purpose Input [1] = GPIO3 Input Was Active [0] = GPIO3 Input Was Inactive	0
F2[3]	Stuck-Bus Timeout Wake-Up Fault	With CB[4] = 1 [1] = Part Exited Shutdown Mode After Stuck-Bus Timer Expired [0] = No Stuck Bus Timeout Wake-Up Fault Occurred	0
F2[2]	Energy Register Overflow Fault	Energy Register Overflow [1] = Energy Register Overflow Fault [0] = No Energy Overflow Fault	0
F2[1]	Charge Register Overflow Fault	Charge Register Overflow [1] = Charge Register Overflow Fault [0] = No Charge Overflow Fault	0
F2[0]	Time Counter Register Overflow Fault	Time Counter Register Overflow [1] = Time Counter Register Overflow Fault [0] = No Time Counter Overflow Fault	0

Table 12. GPIO3_CTRL Register (42h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
GC[7]	Alert Generated	If GPIO3 is configured as $\overline{\text{ALERT}}$ output, it pulls low when alert is generated. Otherwise, this bit does not have an effect on GPIO3. This bit is set when an alert is generated or a 1 is written. To clear this bit, write 0 via I^2C.	0
GC[6]	GPIO3 Pull-Down Control	Controls GPIO3 as a General Purpose Output [1] = GPIO3 Pulls Low [0] = GPIO3 Hi-Z This bit does not have effect on GPIO3 if it is configured otherwise.	0
GC[5:0]	Reserved	Read Only	00000b

Table 13. CLK_DIV Register (43h): Read/Write

BIT	REGISTER NAME	OPERATION	DEFAULT
CD[7:5]	Reserved	Read Only	000b
CD[4:0]	Clock Divider Integer	Input clock frequency at CLKIN is divided by 4× of this integer to produce the target 250kHz system clock.	00100b

APPLICATIONS INFORMATION

Table 14. Register Data Format: Read/Write

REGISTER	BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
ADC, Min/Max ADC, Min/Max ADC Threshold MSB	Data (11)	Data (10)	Data (9)	Data (8)	Data (7)	Data (6)	Data (5)	Data (4)
ADC, Min/Max ADC, Min/Max ADC Threshold LSB	Data (3)	Data (2)	Data (1)	Data (0)	Read as 0	Read as 0	Read as 0	Read as 0
Power, Min/Max Power, Min/ Max Power Threshold MSB2	Data (23)	Data (22)	Data (21)	Data (20)	Data (19)	Data (18)	Data (17)	Data (16)
Power, Min/Max Power, Min/ Max Power Threshold MSB1	Data (15)	Data (14)	Data (13)	Data (12)	Data (11)	Data (10)	Data (9)	Data (8)
Power, Min/Max Power, Min/ Max Power Threshold LSB	Data (7)	Data (6)	Data (5)	Data (4)	Data (3)	Data (2)	Data (1)	Data (0)
Time Counter, Charge, Energy MSB3	Data (31)	Data (30)	Data (29)	Data (28)	Data (27)	Data (26)	Data (25)	Data (24)
Time Counter, Charge, Energy MSB2	Data (23)	Data (22)	Data (21)	Data (20)	Data (19)	Data (18)	Data (17)	Data (16)
Time Counter, Charge, Energy MSB1	Data (15)	Data (14)	Data (13)	Data (12)	Data (11)	Data (10)	Data (9)	Data (8)
Time Counter, Charge, Energy LSB	Data (7)	Data (6)	Data (5)	Data (4)	Data (3)	Data (2)	Data (1)	Data (0)
MFR_SPECIAL_ID MSB	Data (15)	Data (14)	Data (13)	Data (12)	Data (11)	Data (10)	Data (9)	Data (8)
MFR_SPECIAL_ID LSB	Data (7)	Data (6)	Data (5)	Data (4)	Data (3)	Data (2)	Data (1)	Data (0)

Table 15. Time per LSB of Timer Register

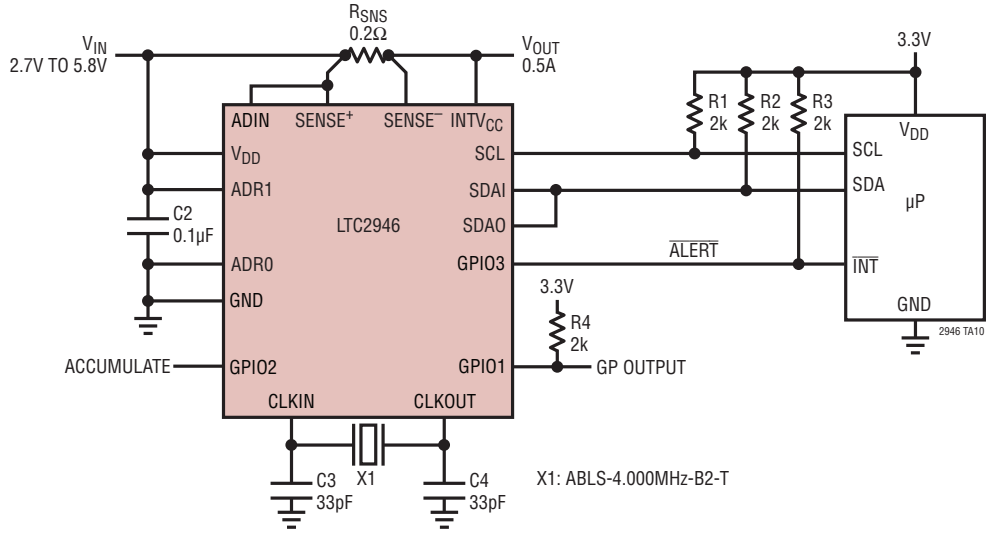
CA[6:5] SEE TABLE 3	CA[2:0] SEE TABLE 3	N
XX	110	4098.5
11	011	4099.75
	010, 101	4098.5098
	001, 100	4098.5806
	000	4099.3333
10	011	4099.7355
	010, 101	4098.5097
	001, 100	4098.5800
	000	4099.3549
01	011	4099.6429
	010, 101	4098.5092
	001, 100	4098.5758
	000	4099.2692
00	011	4099
	010, 101	4098.5049
	001, 100	4098.5397
	000	4098.8571

$$Time/LSB = N \bullet \frac{4 \bullet CLK\_DIV}{f_{CLKIN}}$$

or N • 4µs if internal clock used.

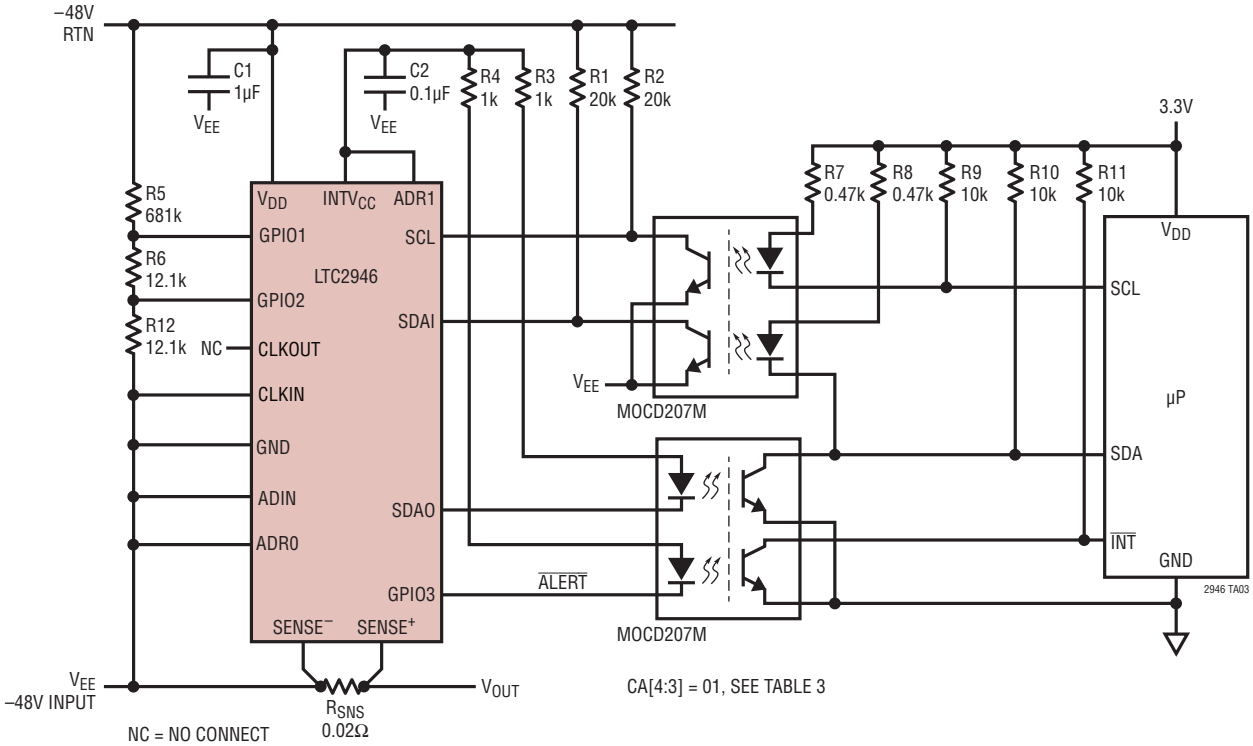
TYPICAL APPLICATIONS

Bidirectional Power Monitor with Energy and Charge Monitor in Forward Path



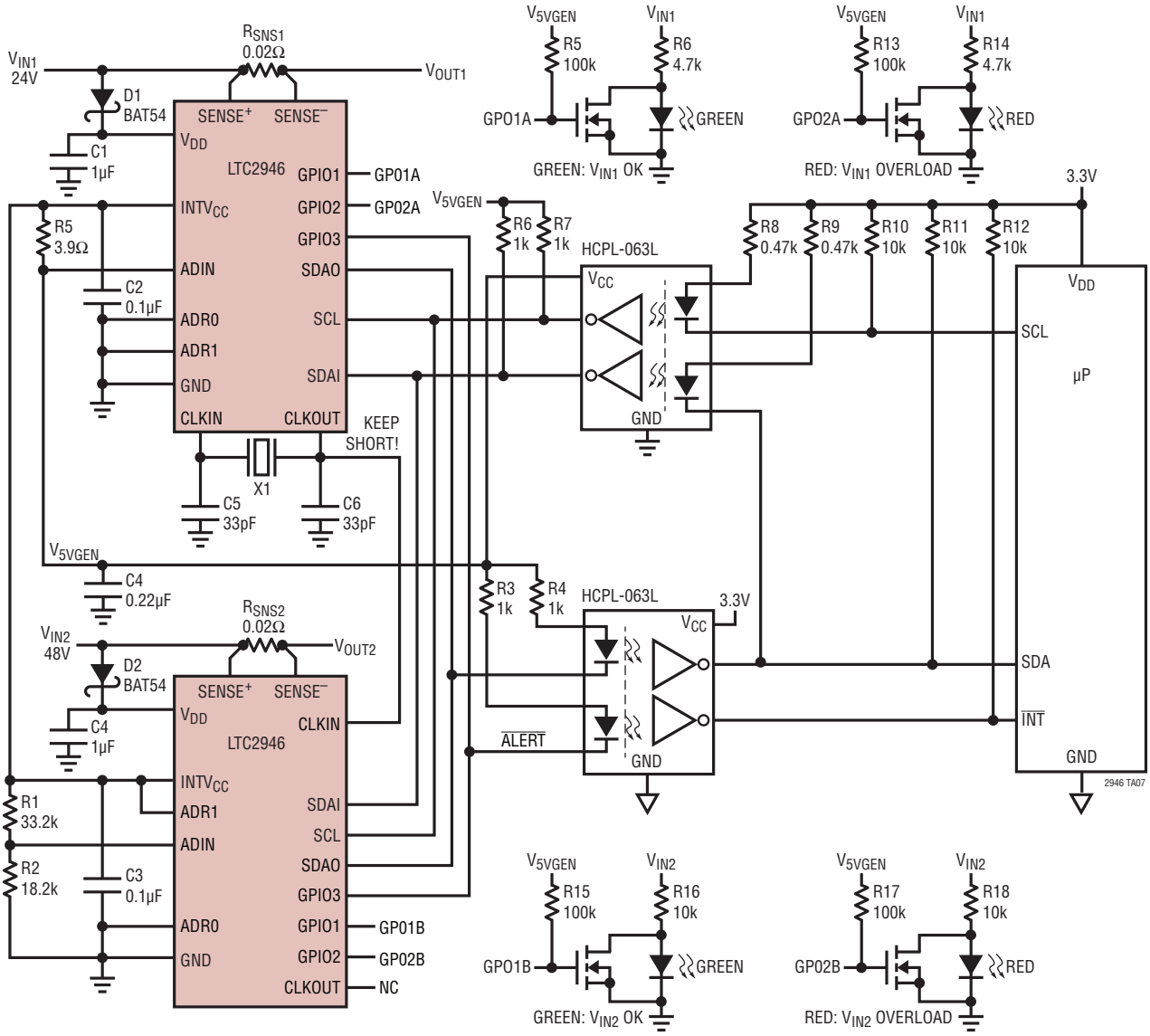
POWER FOR REVERSE PATH = $CODE_{ADIN} \times CODE_{VDD}$ TO BE PERFORMED BY µP
CA[7] = 1, SEE TABLE 3

Power, Charge and Energy Monitoring in –48V System Using Low Side Sensing (1.5kHz I²C Interface)



TYPICAL APPLICATIONS

Dual Power, Charge and Energy Monitor Using Single Opto-Coupler for Galvanic Isolation and Blocking Diodes for Data Retention When Either Supply Fails

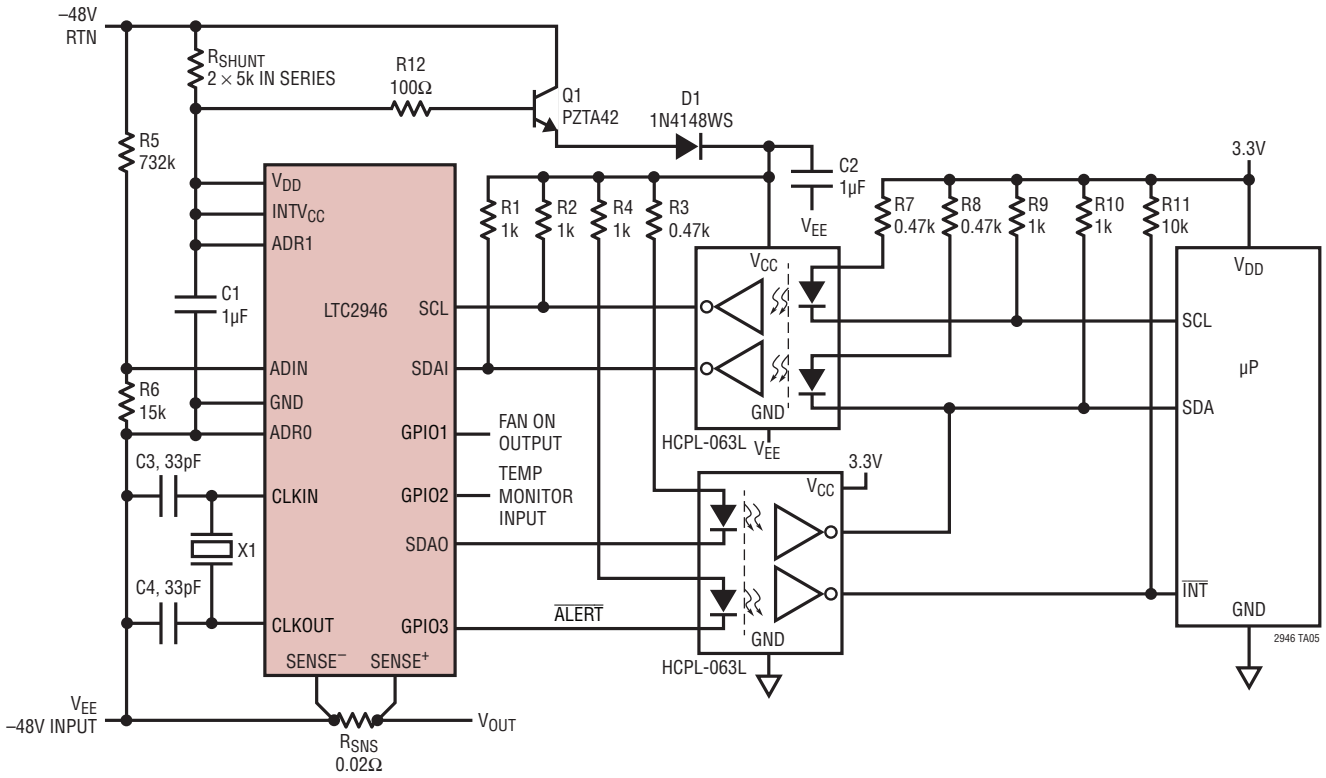


X1: ABLS-4.000MHz-B2-T

GPO1A, GPO2A, GPO1B AND GPO2B ARE CONTROLLED BY MICROPROCESSOR WRITING COMMANDS TO LTC2946s VIA I^2C

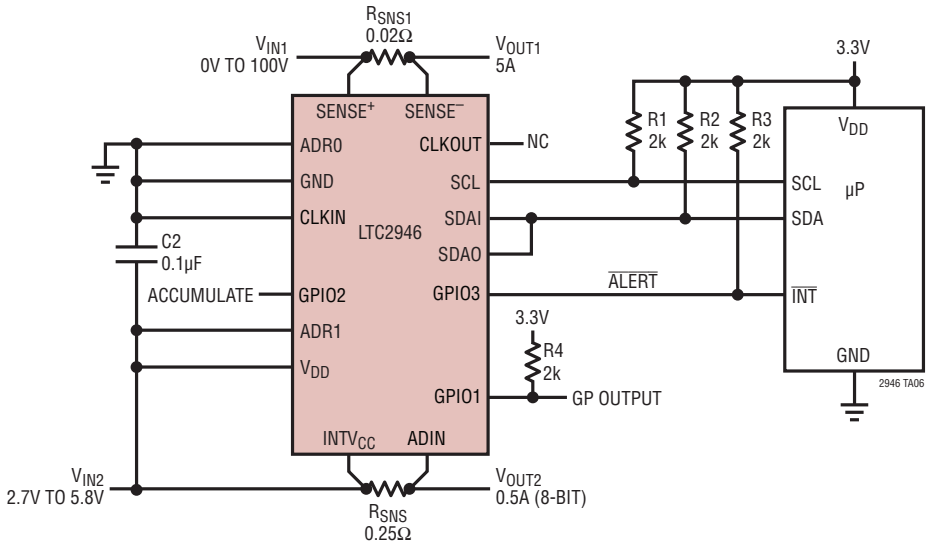
TYPICAL APPLICATIONS

Power, Charge and Energy Monitor in –48V Harsh Environment Using $INTV_{CC}$ Shunt Regulator to Tolerate 200V Transients



X1: ABLS-4.000MHz-B2-T
CA[4:3] = 10, SEE TABLE 3

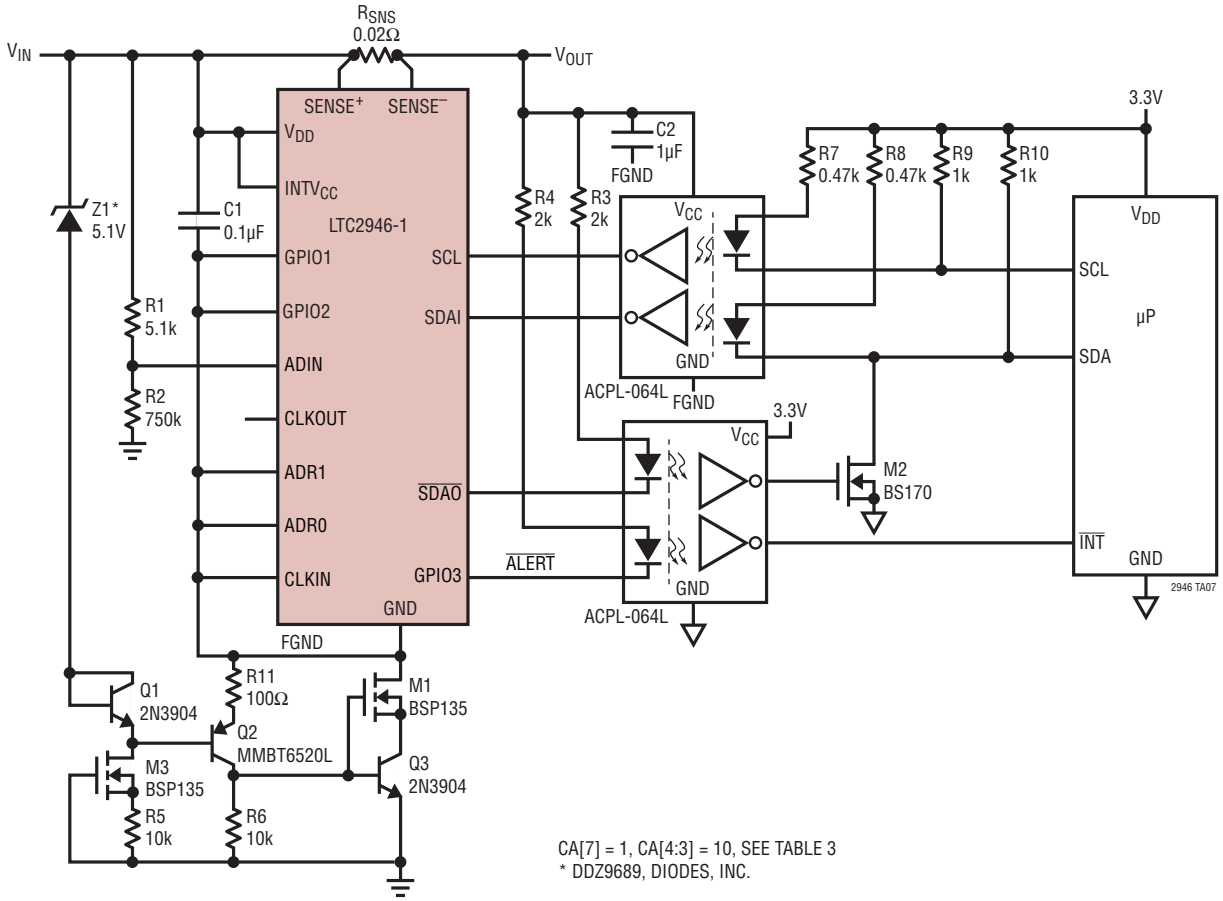
Power, Charge and Energy Monitor for Main Supply and Power Monitor for Secondary Supply with Single LTC2946



CA[7] = 1, SEE TABLE 3
POWER FOR SECONDARY SUPPLY = $CODE_{ADIN} \times CODE_{VDD}$. TO BE PERFORMED BY µP

TYPICAL APPLICATIONS

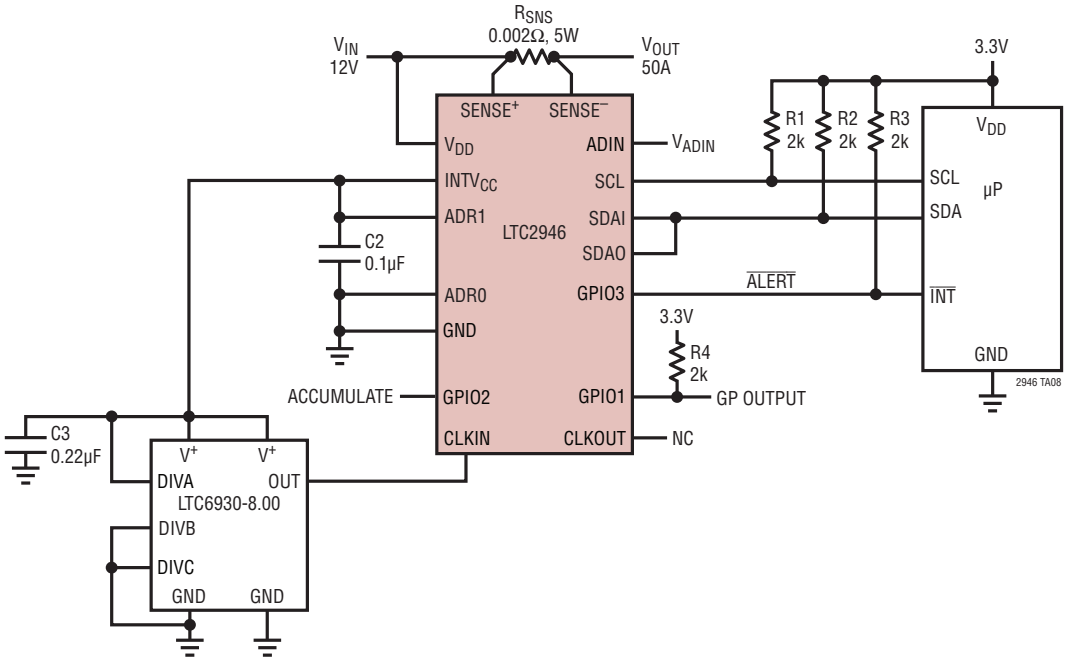
6V to 300V High Side Power, Charge and Energy Monitor



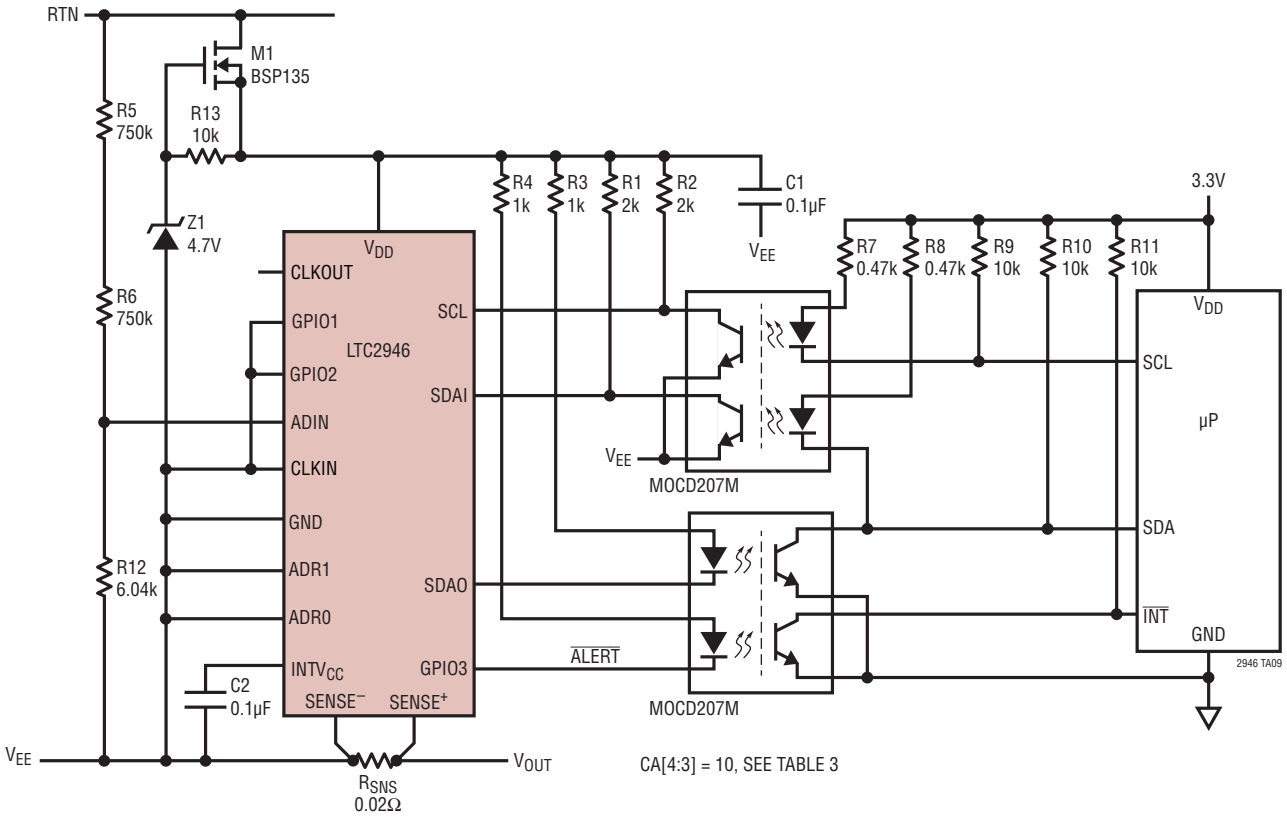
CA[7] = 1, CA[4:3] = 10, SEE TABLE 3
* DDZ9689, DIODES, INC.

TYPICAL APPLICATIONS

12V, 50A Power, Charge and Energy Monitor



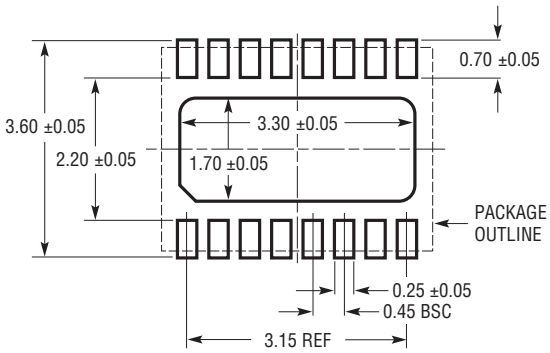
Wide Range –4V to –500V Negative Power, Charge and Energy Monitor (10kHz I²C Interface)



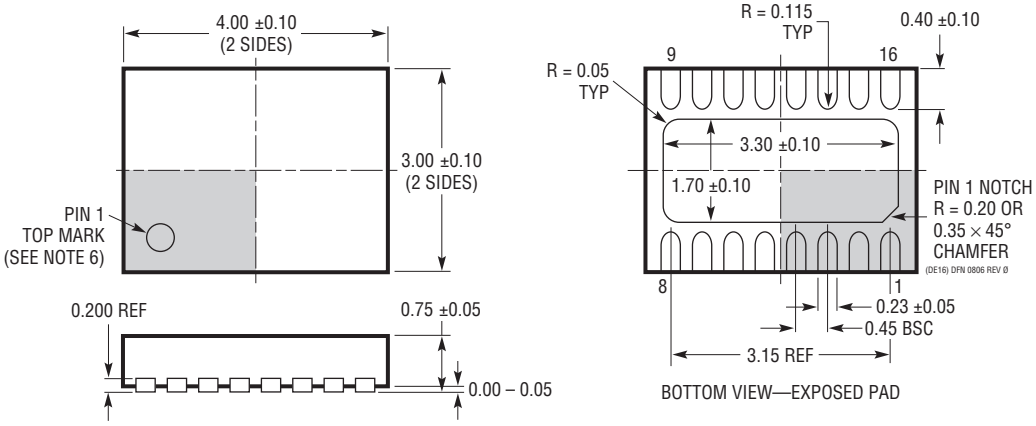
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



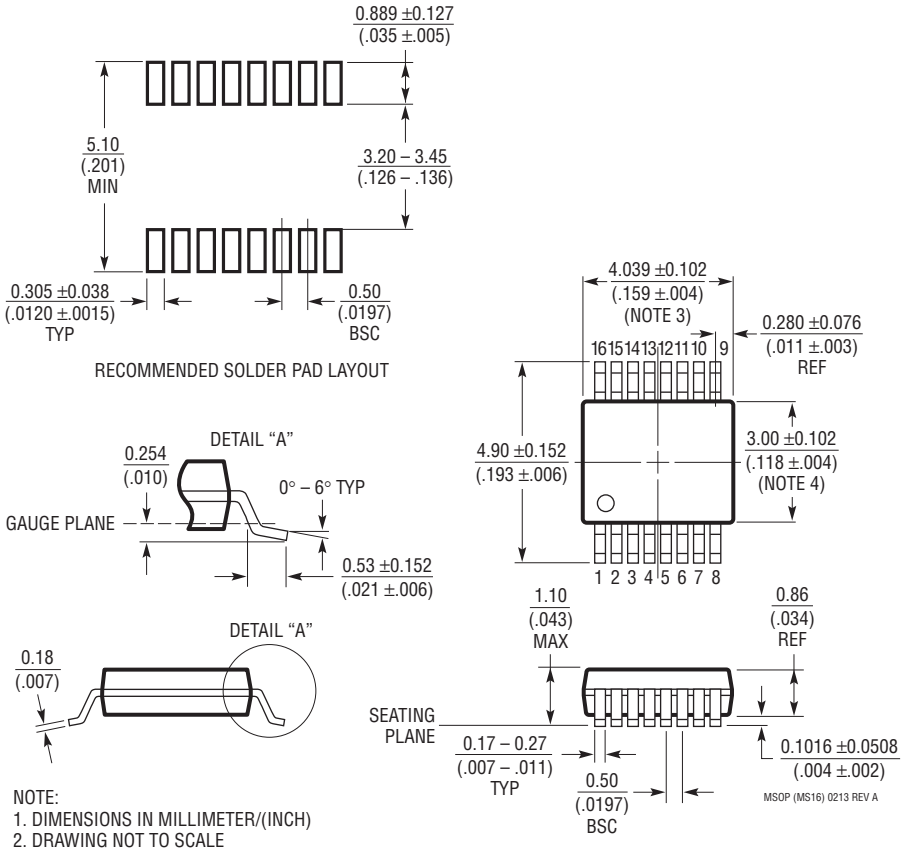
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

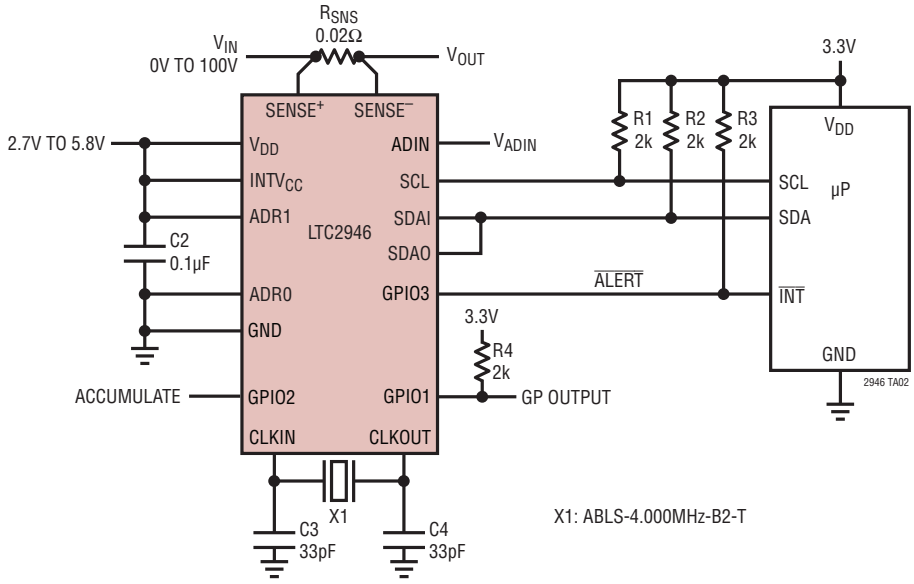
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/15	Changed Y-axis of Typical Applications graph.	1
		Corrected $I_{SENSE(LO)}^-$ Conditions.	4
		Corrected R_{SHUNT} equation.	16

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Rail-to-Rail Power, Charge and Energy Monitor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®2940	Power and Current Monitor	4-Quadrant Multiplication, ±5% Power Accuracy, 4V to 80V Operation
LTC2941	I²C Battery Gas Gauge	2.7V to 5.5V Operation, 1% Charge Accuracy
LTC2942	I²C Battery Gas Gauge	2.7V to 5.5V Operation, 1% Charge, Voltage and Temperature
LTC2943	High Voltage Battery Gas Gauge	3.6V to 20V Operation, 1% Charge, Voltage, Current and Temperature
LTC2945	Wide Range I²C Power Monitor	0V to 80V Operation, 12-Bit ADC with ±0.75% TUE
LTC2990	Quad I²C Temperature, Voltage and Current Monitor	3V to 5.5V Operation, 14-Bit ADC
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation, Voltage-to-Frequency Converter
LTC4151	High Voltage I²C Current and Voltage Monitor	7V to 80V Operation, 12-Bit Resolution with ±1.25% TUE
LTC4215	Single Channel, Hot Swap™ Controller with I²C Monitoring	8-Bit ADC, Adjustable Current Limit and Inrush, 2.9V to 15V Operation
LTC4222	Dual Channel, Hot Swap Controller with I²C Monitoring	10-Bit ADC, Adjustable Current Limit and Inrush, 2.9V to 29V Operation
LTC4260	Positive High Voltage Hot Swap Controller with I²C Monitoring	8-Bit ADC, Adjustable Current Limit and Inrush, 8.5V to 80V Operation
LTC4261	Negative High Voltage Hot Swap Controller with I²C Monitoring	10-Bit ADC, Floating Topology, Adjustable Inrush

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