THE DATASHEET OF

LTC2910CGN#TRPBF

LTC2910

Octal Positive/Negative Voltage Monitor

FEATURES

- **8 Low Voltage Adjustable Inputs (0.5V)**
- **Guaranteed Threshold Accuracy: ±1.5%**
- **Input Glitch Rejection**
- **Pin Selectable Input Polarity Allows Negative and 0V Monitoring**
- Buffered 1V Reference Output
- Adjustable Reset Timeout with Timeout Disable
- 50µA Quiescent Current
- Open Drain RST and $\overline{\text{RST}}$ Outputs
- Guaranteed RST and $\overline{\text{RST}}$ for $V_{CC} \geq 1V$
- Available in 16-Lead SSOP and 16-Lead (5mm × 3mm) DFN Packages

APPLICATIONS

- Desktop and Notebook Computers
- Network Servers
- Core, I/O Voltage Monitors

DESCRIPTION

The LTC®2910 is an octal input voltage monitor intended for monitoring multiple voltages in a variety of applications. Each input has a nominal 0.5V threshold, featuring 1.5% tight threshold accuracy over the entire operating temperature range. Glitch filtering ensures reliable reset operation without false or noisy triggering.

Polarity selection and a buffered reference allow monitoring up to two separate negative voltages. A three state input pin allows setting the polarity of two inputs without requiring any external components.

The LTC2910 provides a precise, versatile, space-conscious, micropower solution for voltage monitoring.

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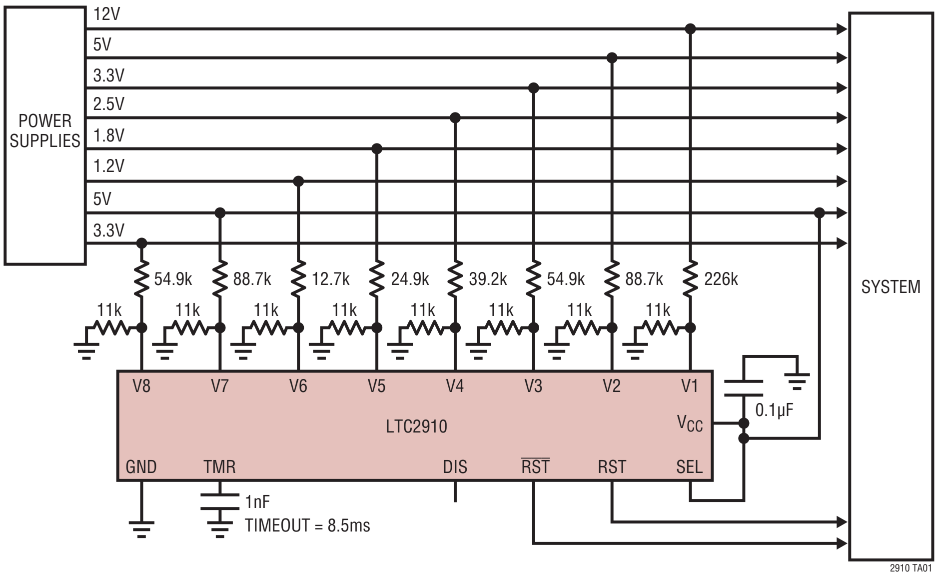
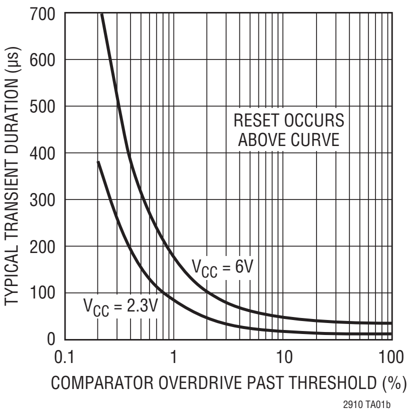
TYPICAL APPLICATION

Octal Supply Monitor, 10% Tolerance, 12V, 5V (x2), 3.3V (x2), 2.5V, 1.8V, 1.2V



Typical Transient Duration vs Comparator Overdrive



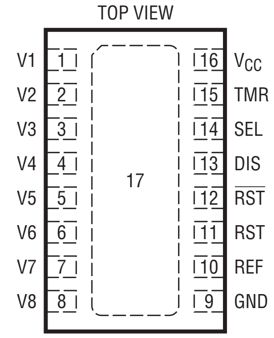
ABSOLUTE MAXIMUM RATINGS

(Note 1, 2)

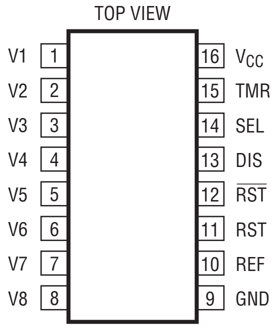
Terminal Voltages	
V_{CC} (Note 3)	–0.3V to 6V
RST, $\overline{\text{RST}}$	–0.3V to 16V
TMR	–0.3V to (V_{CC} + 0.3V)
Vn, DIS, SEL	–0.3V to 7.5V
Terminal Current	
I_{VCC}	10mA
Reference Load Current (I_{REF})	±1mA
$I_{RST/\overline{RST}}$	10mA

Operating Temperature Range	
LTC2910C	0°C to 70°C
LTC2910I	–40°C to 85°C
LTC2910H	–40°C to 125°C
Storage Temperature Range	
SSOP, DFN	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	
SSOP	300°C

PACKAGE/ORDER INFORMATION



DHC16 PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43.5°C/W
EXPOSED PAD (PIN 17) PCB GND CONNECTION OPTIONAL



GN16 PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER	DHC16 PART MARKING*	ORDER PART NUMBER	GN16 PART MARKING*
LTC2910CDHC LTC2910IDHC LTC2910HDHC	2910 2910 2910	LTC2910CGN LTC2910IGN LTC2910HGN	2910 2910I 2910H

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, Vn = 0.55V, SEL = V_{CC}, DIS = OPEN unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SHUNT}	V_{CC} Shunt Regulator Voltage	I_{CC} = 5mA	●	6.2	6.6	6.9	V
		–40°C < T_A <125°C	●	6.2	6.6	7.0	V
ΔV_{SHUNT}	V_{CC} Shunt Regulator Load Regulation	I_{CC} = 2mA to 10mA	●		200	300	mV
V_{CC}	Supply Voltage		●	2.3		V_{SHUNT}	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, Vn = 0.55V, SEL = V_{CC}, DIS = OPEN unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(MIN)}$	Minimum V_{CC} Output Valid	DIS = 0V	●			1	V
$V_{CC(UVLO)}$	Supply Undervoltage Lockout	V_{CC} Rising, DIS = 0V	●	1.9	2	2.1	V
$\Delta V_{CC(UVHYST)}$	Supply Undervoltage Lockout Hysteresis	DIS = 0V	●	5	25	50	mV
I_{CC}	Supply Current	V_{CC} = 2.3V to 6V	●		50	100	µA
V_{REF}	Reference Output Voltage	I_{VREF} = ±1mA	●	0.985	1	1.015	V
		–40°C < T_A < 125°C	●	0.985	1	1.020	V
V_{RT}	Vn Input Voltage Threshold		●	492	500	508	mV
t_{PROP}	Vn Input Threshold to Output Delay	$V_n = V_{RT}$ – 5mV	●	50	125	500	µs
I_{VN}	Vn Input Current		●			±15	nA
		–40°C < T_A < 125°C	●			±30	nA
t_{RST}	Reset Timeout Period	C_{TMR} = 1nF	●	6	8.5	12.5	ms
		–40°C < T_A < 125°C	●	6	8.5	14	ms
$V_{DIS(VIH)}$	DIS Input Threshold Voltage High		●	1.2			V
$V_{DIS(VIL)}$	DIS Input Threshold Voltage Low		●			0.8	V
I_{DIS}	DIS Input Current	V_{DIS} > 0.5V	●	1	2	3	µA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 0V	●	–1.3	–2.1	–2.8	µA
		–40°C < T_A < 125°C	●	–1.2	–2.1	–2.8	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1.6V	●	1.3	2.1	2.8	µA
		–40°C < T_A < 125°C	●	1.2	2.1	2.8	µA
$V_{TMR(DIS)}$	Timer Disable Voltage	Referenced to V_{CC}	●	–180	–270		mV
V_{OH}	Output Voltage High RST/$\overline{RST}$	V_{CC} = 2.3V, $I_{\overline{RST}/RST}$ = –1µA	●	1			V
V_{OL}	Output Voltage Low RST/$\overline{RST}$	V_{CC} = 2.3V, $I_{\overline{RST}/RST}$ = 2.5mA V_{CC} = 1V, $I_{\overline{RST}}$ = 100µA	●		0.1 0.01	0.3 0.15	V V
Three-State Input SEL							
V_{IL}	Low Level Input Voltage		●			0.4	V
V_{IH}	High Level Input Voltage		●	1.4			V
V_Z	Pin Voltage when Left in Hi-Z State	I_{SEL} = ±10µA	●	0.6	0.9	1.1	V
		–40°C < T_A < 125°C	●	0.6	0.9	1.2	V
I_{SEL}	SEL High, Low Input Current		●			±25	µA
$I_{SEL(MAX)}$	Maximum SEL Input Current	SEL tied to either V_{CC} or GND	●			±30	µA

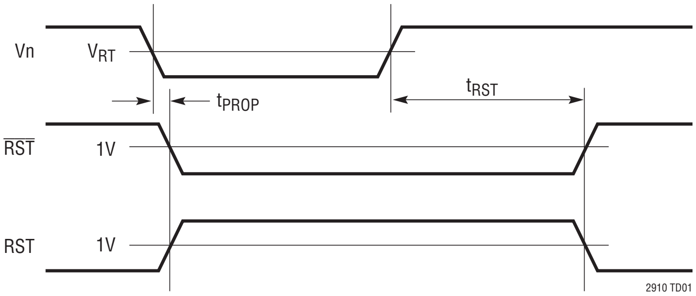
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

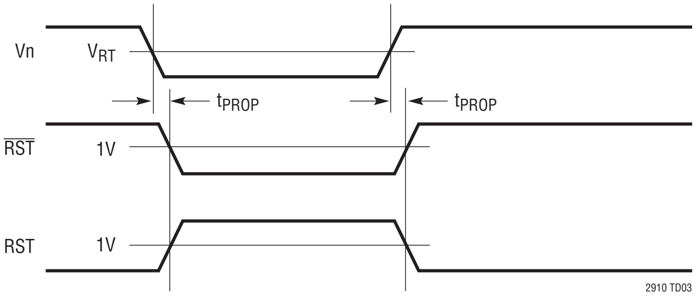
Note 3: V_{CC} maximum pin voltage is limited by input current. Since the V_{CC} pin has an internal 6.5V shunt regulator, a low impedance supply that exceeds 6V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

TIMING DIAGRAM

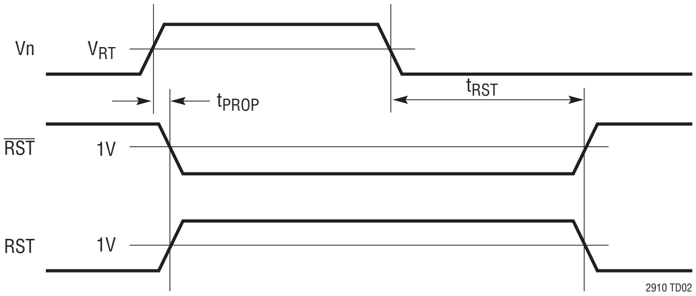
Vn Positive Monitor Timing



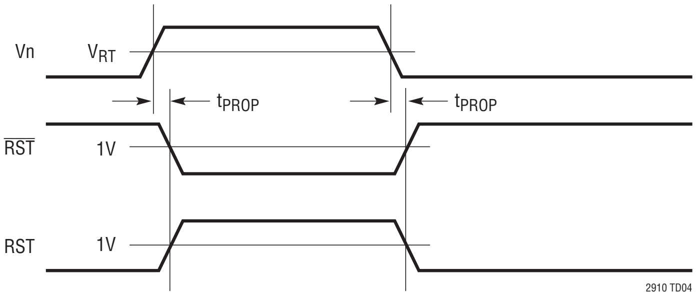
Vn Positive Monitor Timing (TMR strapped to V_{CC})



Vn Negative Monitor Timing



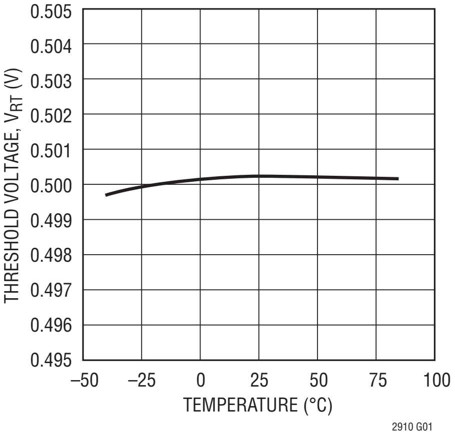
Vn Negative Monitor Timing (TMR strapped to V_{CC})



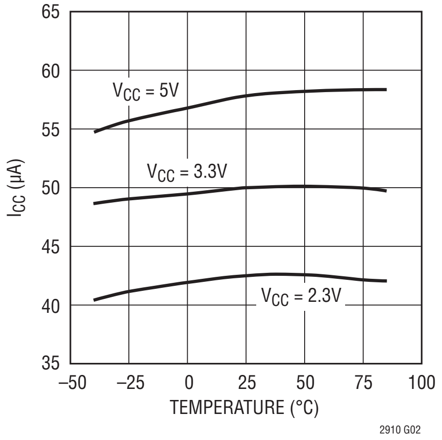
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at $T_A = 25°C$ and $V_{CC} = 3.3V$ unless otherwise noted. (Note 2)

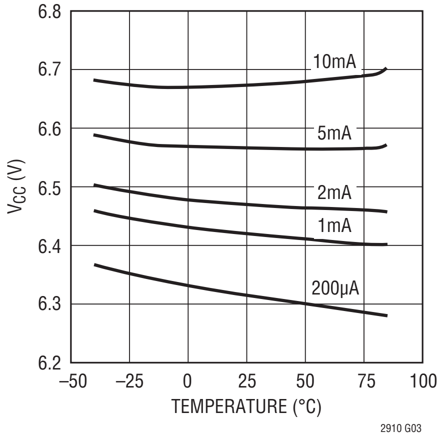
Input Threshold Voltage vs Temperature



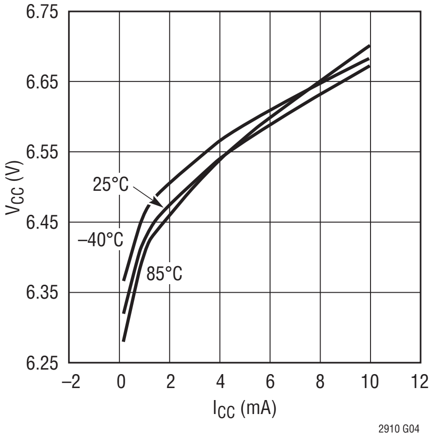
Supply Current vs Temperature



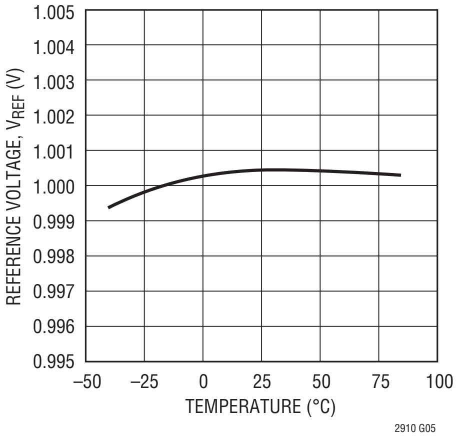
V_{CC} Shunt Voltage vs Temperature



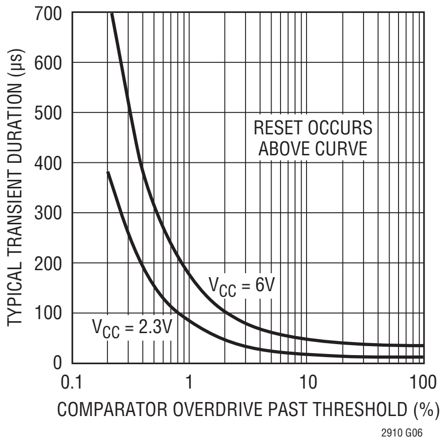
V_{CC} Shunt Voltage vs I_{CC}



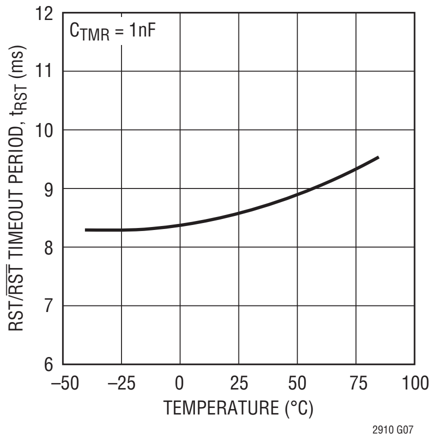
Buffered Reference Voltage vs Temperature



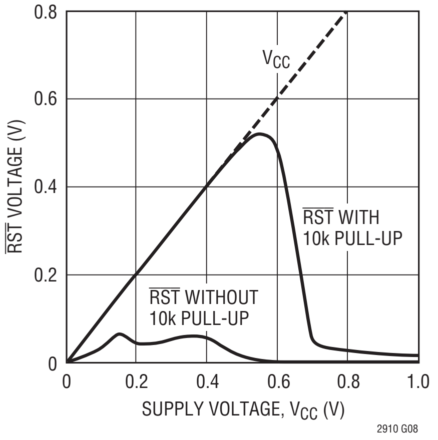
Transient Duration vs Comparator Overdrive



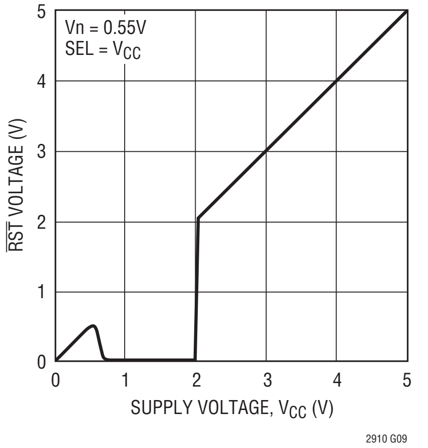
Reset Time-Out Period vs Temperature



$\overline{RST}$ Output Voltage vs V_{CC}



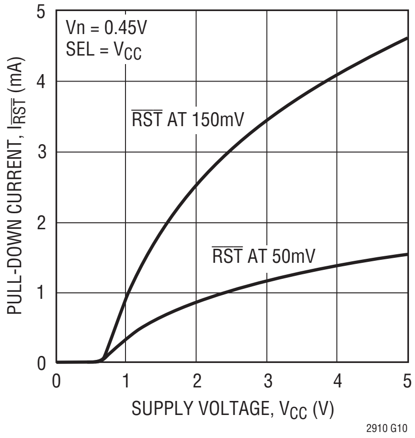
$\overline{RST}$ Output Voltage vs V_{CC}



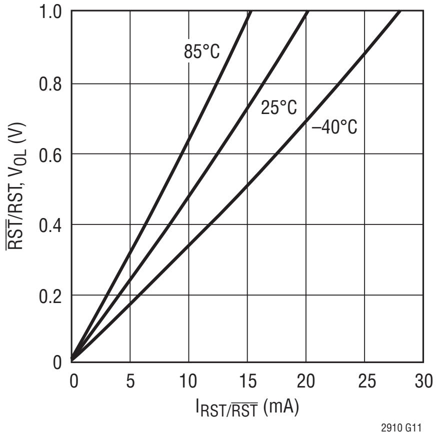
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at $T_A = 25°C$ and $V_{CC} = 3.3V$ unless otherwise noted. (Note 2)

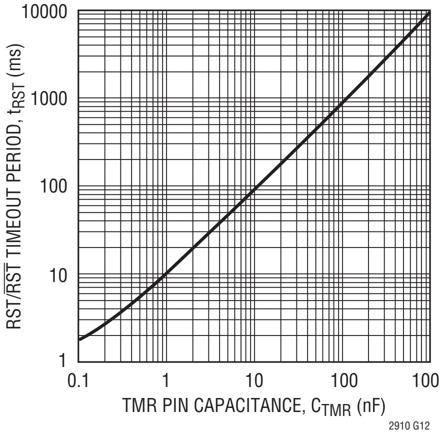
$\overline{\text{RST}}$, I_{SINK} vs V_{CC}



RST/$\overline{\text{RST}}$ Voltage Output Low vs Output Sink Current



Reset Timeout Period vs Capacitance



PIN FUNCTIONS

DIS (Pin 13): Output Disable Input. Disables the RST and $\overline{\text{RST}}$ output pins. When DIS is pulled high, the RST and $\overline{\text{RST}}$ pins are not asserted except during a UVLO condition. Pin has a weak (2µA) internal pull-down to GND. Leave pin open if unused.

Exposed Pad (Pin 17, DFN Package): Exposed pad may be left open or connected to device ground.

GND (Pin 9): Device Ground

REF (Pin 10): Buffered Reference Output. 1V reference used for the offset of negative-monitoring applications. The buffered reference sources and sinks up to 1mA. The reference drives capacitive loads up to 1nF. Larger capacitive loads may cause instability. Leave pin open if unused.

RST (Pin 11): Open-Drain Reset Logic Output. Asserts high when any positive polarity input voltage is below threshold or any negative polarity input voltage is above threshold. Held high for an adjustable delay time after all voltage inputs are valid. Pin has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave pin open if unused.

$\overline{\text{RST}}$ (Pin 12): Open-Drain Inverted Reset Logic Output. Asserts low when any positive polarity input voltage is below threshold or any negative polarity input voltage is above threshold. Held low for an adjustable delay time after all voltage inputs are valid. Pin has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. Leave pin open if unused.

SEL (Pin 14): Input Polarity Select Three-State Input. Connect to V_{CC}, GND or leave unconnected in open state to select one of three possible input polarity combinations (refer to Table 1).

TMR (Pin 15): Reset Delay Timer. Attach an external capacitor (C_{TMR}) of at least 10pF to GND to set a reset delay time of 9ms/nF. A 1nF capacitor will generate an 8.5ms reset delay time. Tie pin to V_{CC} to bypass timer.

V1-V6 (Pin 1, 2, 3, 4, 5 & 6): Voltage Inputs 1 through 6. When the voltage on this pin is below 0.5V, a reset condition is triggered. Tie pin to V_{CC} if unused.

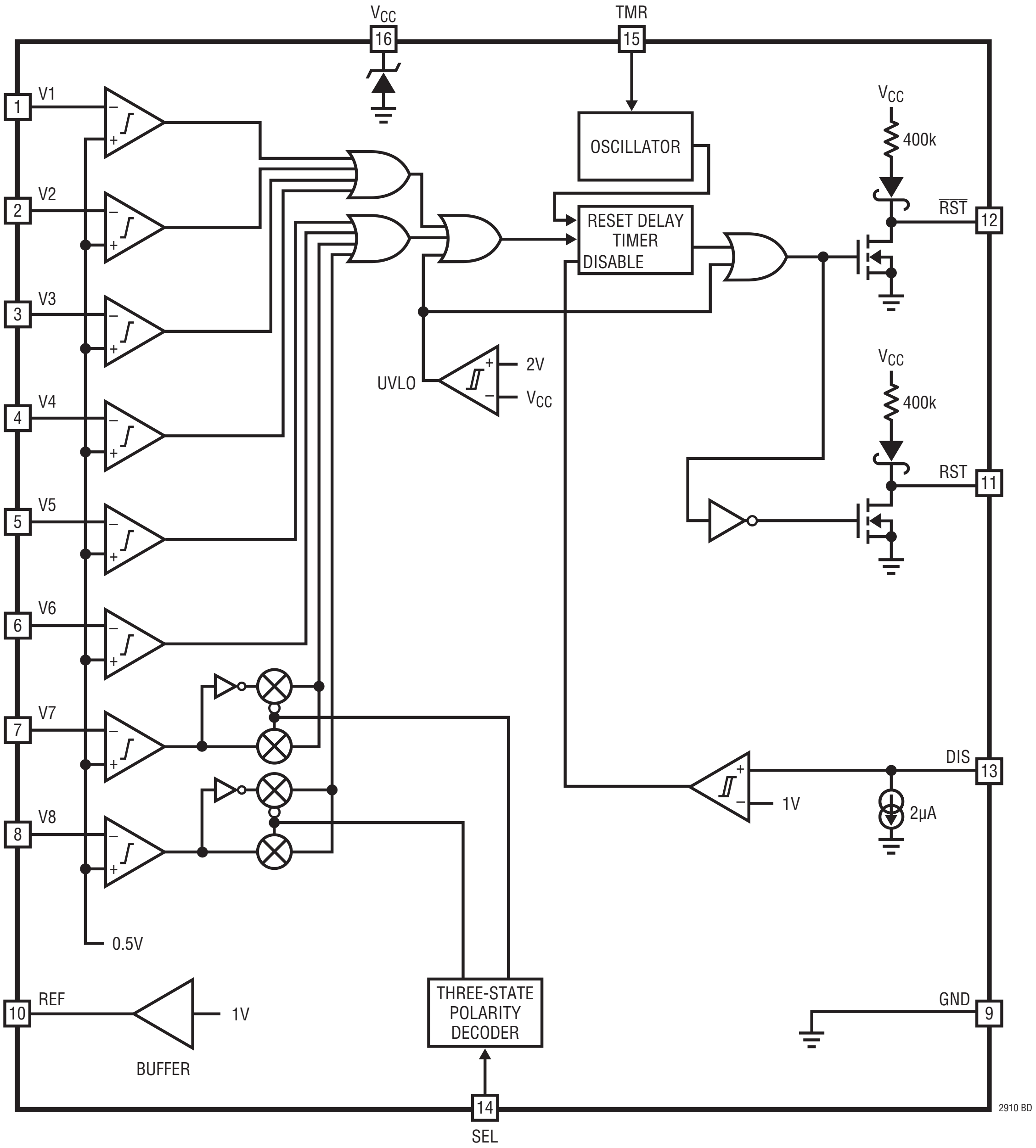
V7-V8 (Pin 7 & 8): Voltage Inputs 7 and 8. The polarity of the input is selected by the state of the SEL pin (refer

PIN FUNCTIONS

to Table 1). When the monitored input is configured as a positive voltage, a reset condition is triggered when the pin is below 0.5V. When the monitored input is configured as a negative voltage, a reset condition is triggered when the pin is above 0.5V. Tie pin to V_{CC} if unused and configured as a positive supply. Tie pin to GND if unused and configured as a negative supply.

V_{CC} (Pin 16): Supply Voltage. Bypass this pin to GND with a 0.1µF (or greater) capacitor. Operates as a direct supply input for voltages up to 6V. Operates as a shunt regulator for supply voltages greater than 6V and must have a resistance between the pin and the supply to limit input current to no greater than 10mA. When used without a current-limiting resistance, pin voltage must not exceed 6V.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Voltage Monitoring

The LTC2910 is a low power octal voltage monitoring circuit with eight individual undervoltage monitor inputs. A timeout period that holds a reset after all faults have cleared is adjustable using an external capacitor and is disabled, by tying TMR to V_{CC}.

Each voltage monitor is compared to a fixed 0.5V reference for detecting undervoltage conditions. When configured to monitor a positive voltage V_m, the application is connected as shown in Figure 1. For negative inputs V_m is connected as shown in Figure 2. R_A is now connected to the REF pin and R_B remains connected to the monitored voltage V_m.

Using the configurations in Figures 1 and 2, a UV condition will result when the magnitude of the voltage at V_m is less than its designed threshold.

Polarity Selection

The three-state polarity-select pin (SEL) selects one of three possible polarity combinations for the input thresholds, as described in Table 1. When an input is configured for negative supply monitoring, a reset condition occurs when the supply voltage is less negative than the configured threshold.

The three-state input pin SEL is connected to GND, V_{CC}, or left unconnected during normal operation. When the pin is left unconnected, the maximum leakage allowed from the pin is ±10μA to ensure it remains in the open state. Table 1 shows the three possible selections of polarity based on the SEL pin connection.

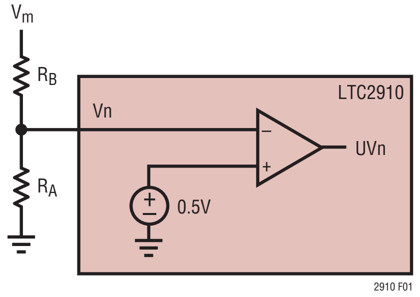


Figure 1. Positive UV Monitoring Configuration

Table 1. Voltage Polarity Programming (V_{RT} = 0.5V Typical)

SEL	V7 INPUT	V8 INPUT
V_{CC}	Positive $V7 < V_{RT} \rightarrow$ UV	Positive $V8 < V_{RT} \rightarrow$ UV
Open	Positive $V7 < V_{RT} \rightarrow$ UV	Negative $V8 > V_{RT} \rightarrow$ UV
GND	Negative $V7 > V_{RT} \rightarrow$ UV	Negative $V8 > V_{RT} \rightarrow$ UV

2-Step Design Procedure

The following 2-step design procedure allows selecting appropriate resistances to obtain the desired UV trip point for the positive voltage monitor circuit in Figure 1 and the negative voltage monitor circuit in Figure 2.

For positive supply monitoring, V_m is the desired nominal operating voltage, I_m is the desired nominal current through the resistive divider, and V_{UV} is the desired undervoltage trip point.

For negative supply monitoring, to compensate for the 1V reference, 1V must be subtracted from V_m and V_{UV} before using each in the following equations.

1. Choose R_A to obtain the desired UV trip point

R_A is chosen to set the desired trip point for the undervoltage monitor.

$$R_A = \left| \frac{0.5V}{I_m} \bullet \frac{V_m}{V_{UV}} \right| \quad (1)$$

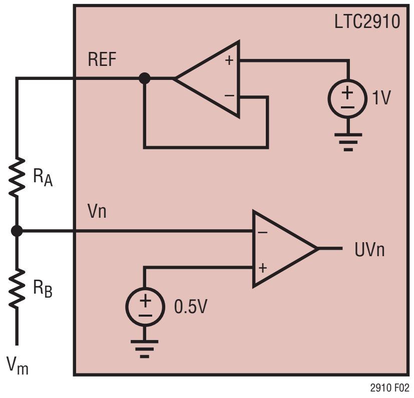


Figure 2. Negative UV Monitoring Configuration

APPLICATIONS INFORMATION

2. Choose R_B to complete the design

Once R_A is known, R_B is determined by:

$$R_B = \left|\frac{V_m}{I_m}\right| - R_A \qquad (2)$$

If any of the variables V_m, I_m, or V_{UV} change, then both steps must be recalculated.

Positive Voltage Monitor Example

A positive voltage monitor application is shown in Figure 3. The monitored voltage is a 5V ±10% supply. Nominal current in the resistive divider is 10μA.

1. *Find R_A to set the UV trip point of the monitor.*

$$R_A = \left|\frac{0.5V}{10\mu A} \bullet \frac{5V}{4.5V}\right| \approx 56.2k$$

2. *Determine R_B to complete the design.*

$$R_B = \left|\frac{5V}{10\mu A}\right| - 56.2k \approx 499k$$

Negative Voltage Monitor Example

A negative voltage monitor application is shown in Figure 4. The monitored voltage is a –5V ±10% supply. Nominal current in the resistive divider is 10μA. For the negative case, 1V is subtracted from V_m and V_{UV}.

1. *Find R_A to set the UV trip point of the monitor.*

$$R_A = \left|\frac{0.5V}{10\mu A} \bullet \frac{-5V - 1V}{-4.5V - 1V}\right| \approx 54.9k$$

2. *Determine R_B to complete the design.*

$$R_B = \left|\frac{-5V - 1V}{10\mu A}\right| - 57.6k \approx 549k$$

Power-Up/Down

As soon as V_{CC} reaches 1V during power up, the $\overline{RST}$ output asserts low and the RST output weakly pulls to V_{CC}.

The LTC2910 is guaranteed to assert $\overline{RST}$ low and RST high under conditions of low V_{CC}, down to V_{CC} = 1V. Above V_{CC} = 2V (2.1V maximum) the Vn inputs take control.

Once all inputs and V_{CC} become valid, an internal timer is started. After an adjustable delay time, RST pulls low and $\overline{RST}$ weakly pulls high.

Threshold Accuracy

Reset threshold accuracy is important in a supply sensitive system. Ideally, such a system would reset only if supply

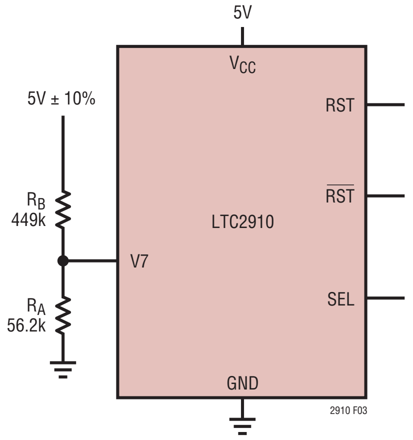


Figure 3. Positive Supply Monitor

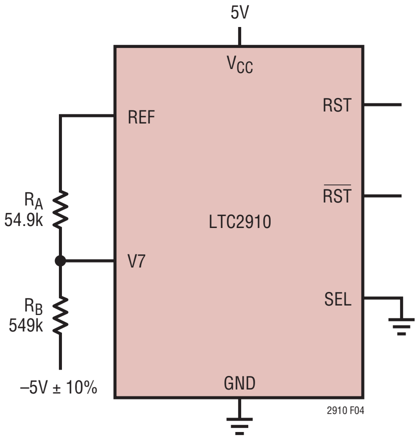


Figure 4. Negative Supply Monitor

APPLICATIONS INFORMATION

voltages fell below the exact threshold for a specified margin. All LTC2910 inputs have a relative threshold accuracy of ±1.5% over the full operating temperature range.

For example, when the LTC2910 is programmed to monitor a 5V input with a 10% tolerance, the desired UV trip point is 4.5V. Because of the ±1.5% relative accuracy of the LTC2910, the UV trip point is between 4.433V and 4.567V which is 4.5V ±1.5%.

The accuracy of the resistances chosen for R_A and R_B affect the UV trip point as well. Using the example just given, if the resistances used to set the UV trip point have 1% accuracy, the UV trip range is between 4.354V and 4.650V. This is illustrated in the following calculations.

The UV trip point is given as

$$V_{UV} = 0.5V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

The two extreme conditions, with a relative accuracy of 1.5% and resistance accuracy of 1%, result in

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1 + \frac{R_B \bullet 0.99}{R_A \bullet 1.01}\right)$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1 + \frac{R_B \bullet 1.01}{R_A \bullet 0.99}\right)$$

For a desired trip point of 4.5V, $\frac{R_B}{R_A} = 8$

Therefore,

$$V_{UV(MIN)} = 0.5V \bullet 0.985 \bullet \left(1 + 8 \bullet \frac{0.99}{1.01}\right) = 4.354V$$

and

$$V_{UV(MAX)} = 0.5V \bullet 1.015 \bullet \left(1 + 8 \bullet \frac{1.01}{0.99}\right) = 4.650V$$

Glitch Immunity

In any supervisory application, noise riding on the monitored DC voltage causes spurious resets. To solve this problem without adding hysteresis, which causes a new error term in the trip voltage, the LTC2910 lowpass filters the output of the first stage comparator at each input. This filter integrates the output of the comparator before asserting the reset output logic. A transient at the input of the comparator of sufficient magnitude and duration triggers the output logic. The Typical Performance Characteristics section shows a graph of the Transient Duration vs. Comparator Overdrive.

RST/$\overline{\text{RST}}$ Timing

The LTC2910 has an adjustable timeout period (t_{RST}) that holds RST and $\overline{\text{RST}}$ asserted after all faults have cleared. This assures a minimum reset pulse width allowing a settling time delay for the monitored voltage after it has entered the valid region of operation.

When any input drops below its designed threshold, the $\overline{\text{RST}}$ pin asserts low and the RST pin asserts high. When all inputs recover above their designed thresholds, the reset delay timer starts. If all inputs remain above their designed thresholds when the timer finishes, the $\overline{\text{RST}}$ pin weakly pulls high and the RST pin strongly pulls low. However, if any input falls below its designed threshold during this timeout period, the timer resets and restarts when all inputs are above the designed thresholds.

Selecting the Reset Timing Capacitor

The reset timeout period (t_{RST}) for the LTC2910 is adjustable to accommodate a variety of applications. Connecting a capacitor, C_{TMR}, between the TMR pin and ground sets the timeout period. The value of capacitor needed for a particular timeout period is:

$$C_{TMR} = t_{RST} \bullet 115 \bullet 10^{-9} \text{ (F/s)}$$

The Reset Timeout Period vs. Capacitance graph found in the Typical Performance Characteristics section shows

APPLICATIONS INFORMATION

the desired delay time as a function of the value of the timer capacitor. The TMR pin must have a minimum of 10pF or be tied to V_{CC}. For long timeout periods, the only limitation is the availability of a large value capacitor with low leakage. Capacitor leakage current must not exceed the minimum TMR charging current of 1.3µA. Tying the TMR pin to V_{CC} bypasses the timeout period.

Undervoltage Lockout

When V_{CC} falls below 2V, the LTC2910 asserts an undervoltage lockout (UVLO) condition. During UVLO, $\overline{\text{RST}}$ is asserted and pulled low and RST is pulled high. When V_{CC} rises above 2V, RST and $\overline{\text{RST}}$ follow the same timing procedure as an undervoltage condition on any input.

Shunt Regulator

The LTC2910 has an internal shunt regulator. The V_{CC} pin operates as a direct supply input for voltages up to 6V. In this range, the quiescent current of the device remains below a maximum of 100µA. For V_{CC} voltages higher than 6V, the pin functions as a shunt regulator and must have a resistance R_Z between the supply and the V_{CC} pin to limit the current to no greater than 10mA.

When selecting this resistance value, choose an appropriate location on the I-V curve shown in the Typical Performance Characteristics to accommodate any variations in V_{CC} due to changes in current through R_Z.

RST/$\overline{\text{RST}}$ Output Characteristics

The DC characteristics of the RST and $\overline{\text{RST}}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics. Each has a weak internal pull-up to V_{CC} and a strong pull-down to ground. This arrangement allows each pin to have open-drain behavior while possessing several other beneficial characteristics. The weak pull-up eliminates the need for an external pull-up resistor when the rise time on this pin is not critical. On the other hand, the open drain configuration allows for wired-OR connections and is useful when more than one signal needs to pull down on the RST or $\overline{\text{RST}}$ lines. V_{CC} of 1V guarantees a maximum V_{OL} = 0.15V.

At V_{CC} = 1V, the weak pull-up current on RST is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the RST pin if the state and pull-up strength of the RST pin is crucial at very low V_{CC}. Note however, by adding an external pull-up resistor, the pull-up strength on the RST pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device must accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The RST and $\overline{\text{RST}}$ outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor, typically 50Ω at V_{CC} > 1V, and at room temperature (25°C). C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is 16.5ns.

The rise time on the RST and $\overline{\text{RST}}$ pins is limited by a 400k internal pull-up resistance to V_{CC}. A similar formula estimates the output rise time (10% to 90%) at the RST and $\overline{\text{RST}}$ pins:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the pull-up resistance.

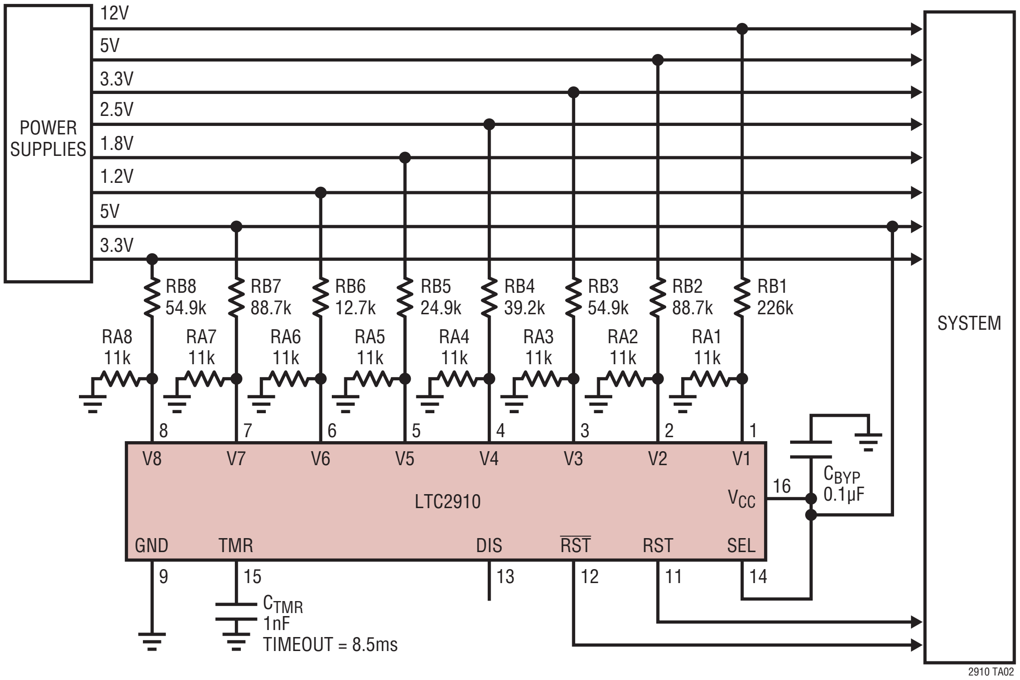
Disable

The LTC2910 allows disabling the RST and $\overline{\text{RST}}$ outputs via the DIS pin. Pulling DIS high forces both outputs to remain unasserted, regardless of any faults that occur on the inputs. However, if a UVLO condition occurs, $\overline{\text{RST}}$ asserts and pulls low, RST asserts and pulls high, but the timeout function is bypassed. $\overline{\text{RST}}$ pulls high and RST pulls low as soon as the UVLO condition is cleared.

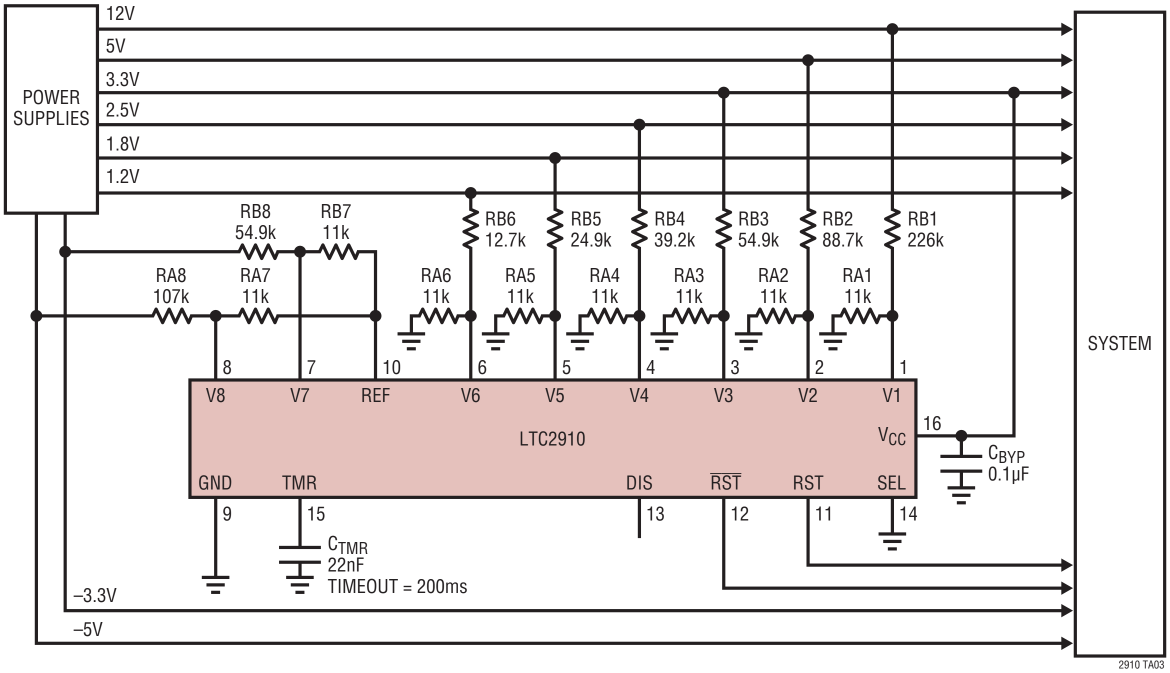
DIS has a weak 2µA (typical) internal pull-down current guaranteeing normal operation with the pin left open.

TYPICAL APPLICATIONS

Eight UV Supply Monitor, 10% Tolerance, 12V, 5V (x2), 3.3V (x2), 2.5V, 1.8V, 1.2V

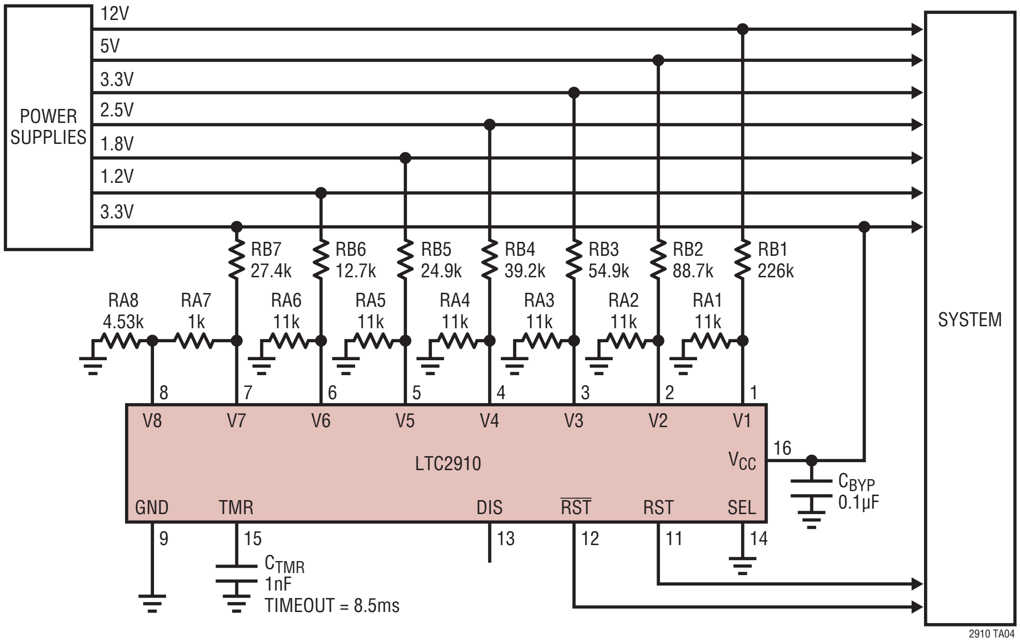


Six Positive and Two Negative UV Supply Monitor, 10% Tolerance, 12V, 5V, 3.3V, 2.5V, 1.8V, 1.2V, –5V, –3.3V

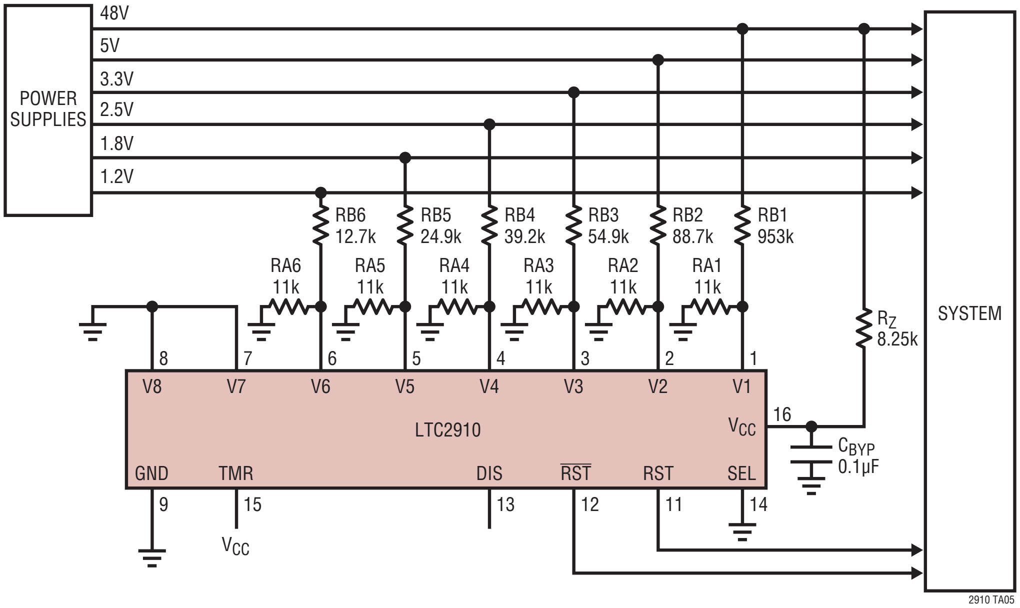


TYPICAL APPLICATIONS

Six UV and One OV/UV Supply Monitor, 10% Tolerance, 12V, 5V, 3.3V (x2), 2.5V, 1.8V, 1.2V

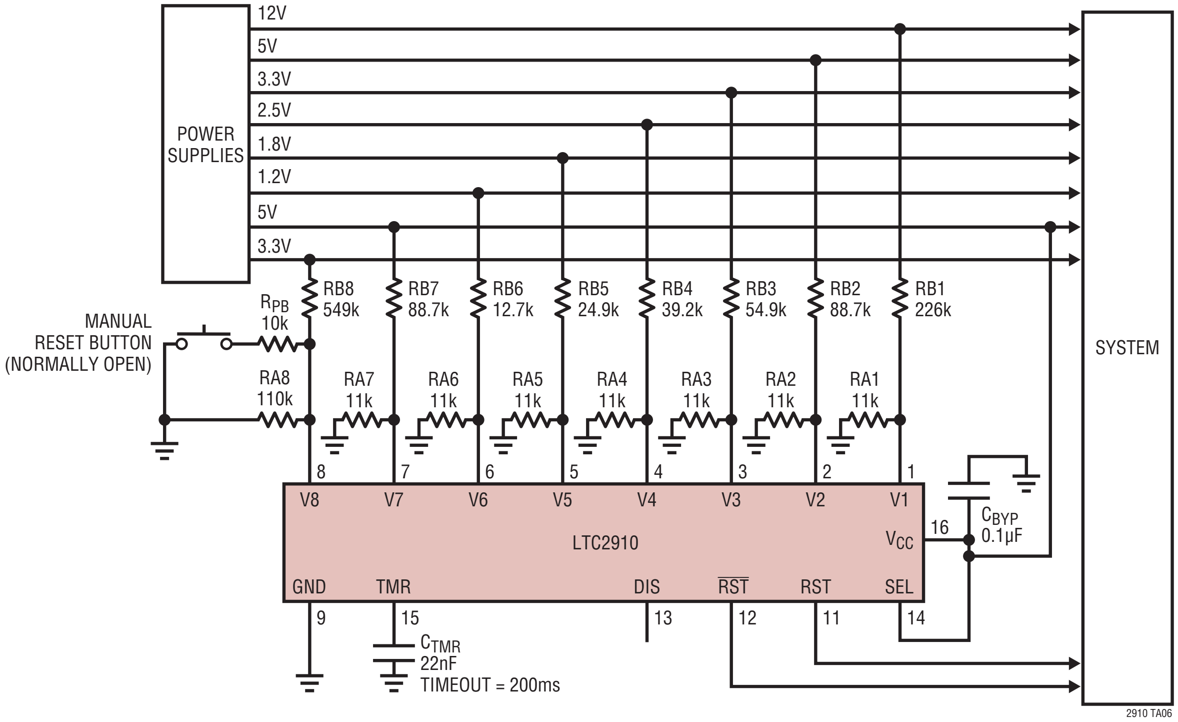


Six UV Supply Monitor Powered from 48V, 10% Tolerance, 48V, 5V, 3.3V, 2.5V, 1.8V, 1.2V



TYPICAL APPLICATIONS

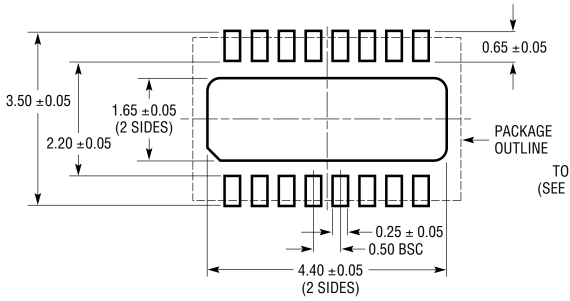
Eight UV Supply Monitor with Manual Reset Button, 10% Tolerance, 12V, 5V (x2), 3.3V (x2), 2.5V, 1.8V, 1.2V



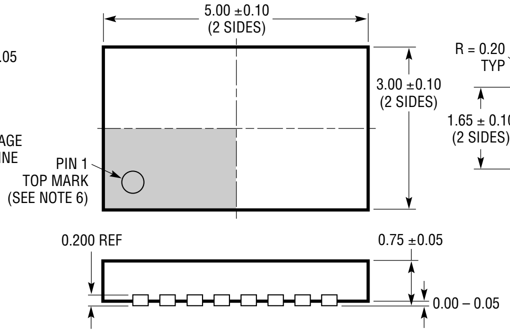
PACKAGE DESCRIPTION

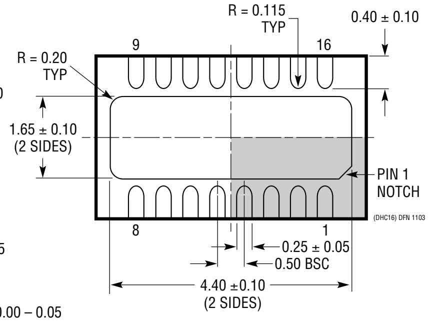
DHC Package
16-Lead Plastic DFN (5mm × 3mm)

(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



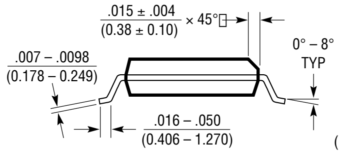


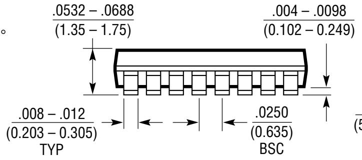
BOTTOM VIEW—EXPOSED PAD

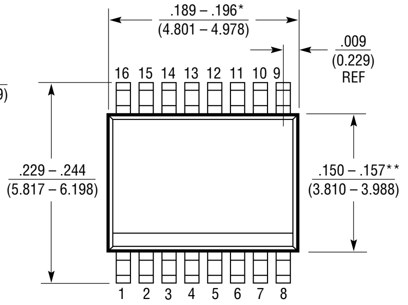
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

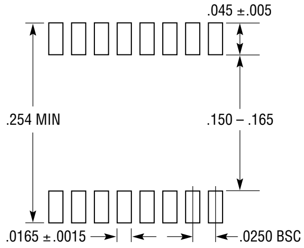
GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1641)









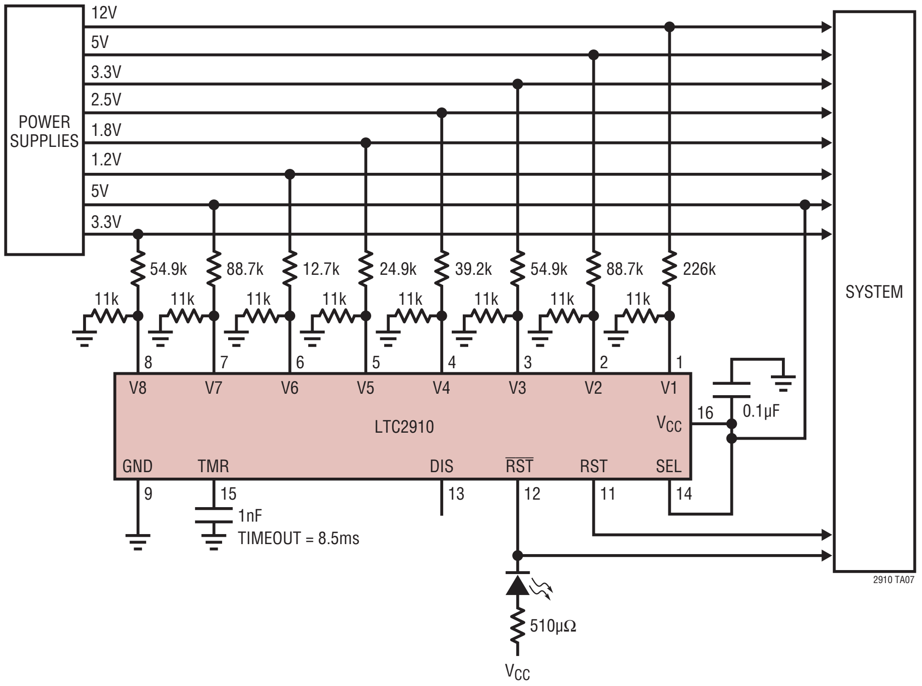
RECOMMENDED SOLDER PAD LAYOUT

GN16 (SSOP) 0204

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Eight UV Supply Monitor with LED Indicator, 10% Tolerance, 12V, 5V (x2), 3.3V (x2), 2.5V, 1.8V, 1.2V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC2900	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$, 10-Lead MSOP and 3mm × 3mm 10-Lead DFN Package
LTC2901	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Tolerance, 16-Lead SSOP Package, Margining Functions
LTC2903	Precision Qual Supply Monitor	6-Lead SOT-23 Package, Ultra Low Voltage Reset
LTC2904	3-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 Package
LTC2905	3-State Programmable Precision Dual Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Tolerance, 8-Lead SOT-23 Package
LTC2906	Precision Dual Supply Monitor One Selectable and One Adjustable	Separate V_{CC} Pin, RST/$\overline{\text{RST}}$ Outputs
LTC2907	Precision Dual Supply Monitor One Selectable and One Adjustable	Separate V_{CC}, Adjustable Reset Timer
LTC2908	Precision Six Supply Monitor (Four Fixed and Two Adjustable)	8-Lead SOT-23 and DDB Packages
LTC2909	Prevision Dual Input UV, OV and Negative Voltage Monitor	Separate V_{CC} Pin, Adjustable Reset Timer, 8-Lead SOT-23 and DDB Packages
LTC2914	Quad UV/OV Positive/Negative Voltage Monitor	Separate V_{CC} Pin, Four Inputs, Up to Two Negative Monitors, Adjustable Reset Timer, 16-Lead SSOP and DFN Packages

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