THE DATASHEET OF

LMR61428XMMEVM/NOPB

AN-2281 LMR61428 Evaluation Module

1 Introduction

The LMR61428 evaluation module is designed to provide the power supply design engineer with a fully functional regulator design. The evaluation module takes the input from a single Li-Ion battery and boosts the voltage up to 5V at a constant load capability of 500mA. The switching frequency of the boost regulator is set to about 1200 kHz which helps in reducing the solution size and keeping switching noise out of the AM radio band. The printed circuit board consists of 4 layers of copper on FR4 material. The first middle layer is a solid ground layer which helps in minimizing the AC current loop. This user's guide contains the evaluation module schematic, a quick setup procedure using a bench power supply, and a Bill-of-Materials (BOM). For complete circuit design information, see *LMR61428 SIMPLE SWITCHER 14Vout, 2.85A Step-Up Voltage Regulator in VSSOP* (SNVS815).

2 Features

- One cell Li-Ion battery for Input Voltage
- 5V Output Voltage at 500mA Output Current
- Switching Frequency of 1.2 MHz
- Small Solution Size: 2.287 × 1.058 inches (58.09 × 26.87 mm)

3 Evaluation Board Schematic

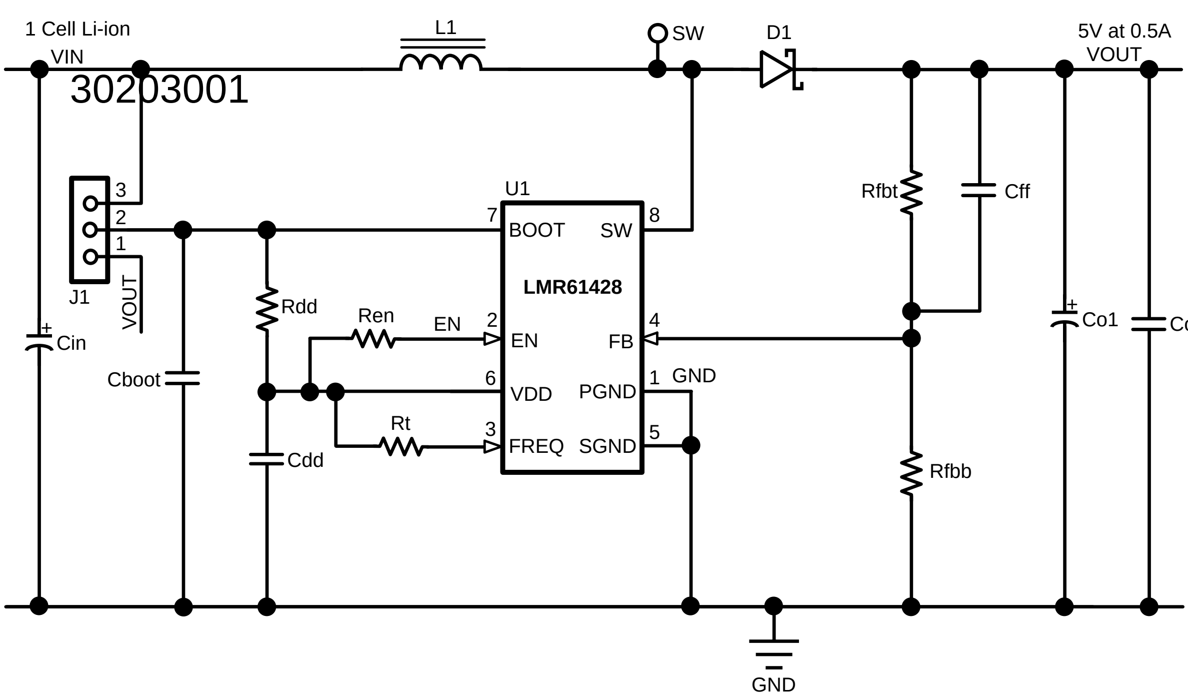


Figure 1. LMR61428 Evaluation Module Schematic

4 Powering and Loading Considerations

Read this entire section prior to attempting to power the evaluation board.

4.1 Quick Start Procedure

Step 1: Set the bench power supply current limit to 3A. Set the power supply voltage to 3.5V. Turn off the power supply output. Connect the power supply to the LMR61428 demo board. Positive connection to V_{IN} and negative connection to GND.

Step 2: Connect a load, as high as 0.5A, to the V_{OUT} terminal. Positive connection to V_{OUT} and negative connection to GND.

Step 3: Connect the shunt so as to short the pins 1 and 2 of the jumper J1. This sets the bootstrap to V_{OUT}

Step 4: The EN pin should be left open for normal operation.

Step 5: Turn on the bench power supply with no load applied to the LMR61428. If the shunt for the jumper J1 was in place, the V_{OUT} would be in regulation at a nominal 5V.

Step 6: Gradually increase the load and V_{OUT} should remain in regulation as the load is increased up to 0.5 Amps.

4.2 Shutdown Operation

The EVM includes a pull-up resistor Ren to enable the device. Use the EN post to disable the device by pulling this node to GND.

4.3 Bootstrap Operation

The EVM has a jumper installed to select the bootstrap option. The default condition is that the jumper be set such that the bootstrap voltage is obtained from the output. For more information, see *LMR61428 SIMPLE SWITCHER 14Vout, 2.85A Step-Up Voltage Regulator in VSSOP* (SNVS815).

4.4 Setting the Output Voltage

The output voltage of the step-up regulator can be set between 1.24V and 14V. But because of the gated oscillator scheme, the maximum possible input to output boost ratio is fixed. For a boost regulator,

$$V_{OUT} / V_{IN} = 1 / [1 - D] \tag{1}$$

The LMR61428 has a fixed duty cycle, D, of 70% typical. Therefore,

$$V_{OUT} / V_{IN} = 1 / 0.3 \tag{2}$$

This sets the maximum possible boost ratio of V_{IN} to V_{OUT} to about 3 times. The user can now estimate what the minimum design inputs should be in order to achieve a desired output, or what the output would be when a certain minimum input is applied. For example, if the desired V_{OUT} was 14V, then the least V_{IN} should be higher than V_{OUT} / 3. If the input voltage fell below this threshold, the output voltage would not be regulated because of the fixed duty cycle. If the minimum V_{IN} was guaranteed at 2V, the max possible V_{OUT} would be $V_{IN} \times 3$.

The V_{OUT} is set by connecting a feedback resistive divider made of R_{fbt} and R_{fbb}. The feedback resistor values are selected as follows:

$$R_{fbb} = R_{fbt} / [(V_{OUT} / 1.24) - 1] \tag{3}$$

A value of 150kΩ is suggested for R_{fbt}. Then, R_{fbb} can be selected using Equation 3. A 39pF capacitor (C_{ff}) connected across R_{fbt} helps in feeding back most of the AC ripple at V_{OUT} to the FB pin. This helps reduce the peak-to-peak output voltage ripple as well as improve the efficiency of the step-up regulator, because a set hysteresis of 30mV at the FB pin is used for the gated oscillator control scheme.

4.5 Typical Test Setup

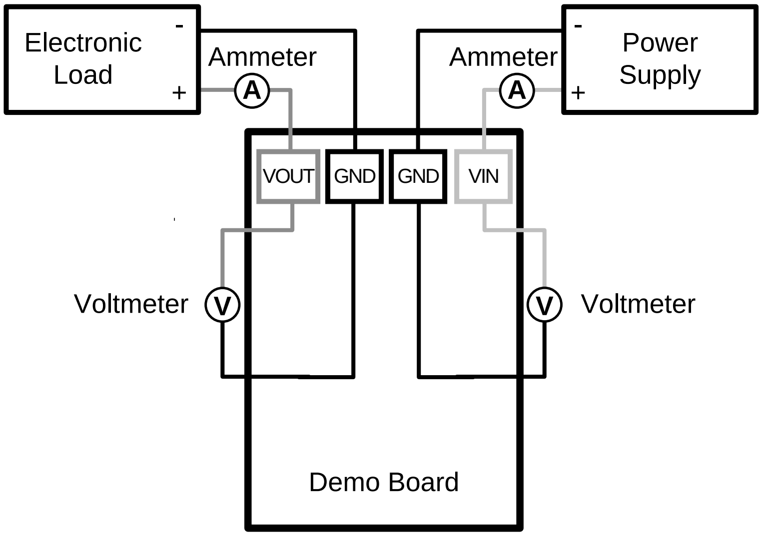


Figure 2. Efficiency Measurements

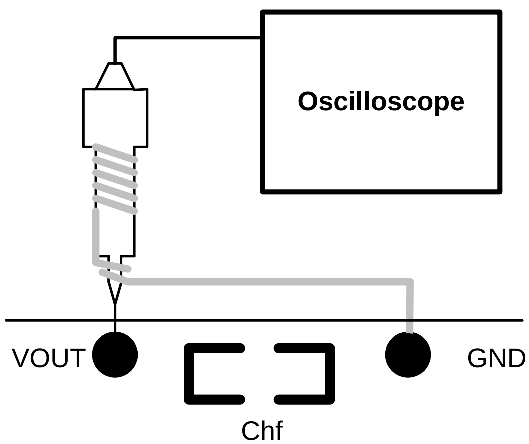


Figure 3. Voltage Ripple Measurements

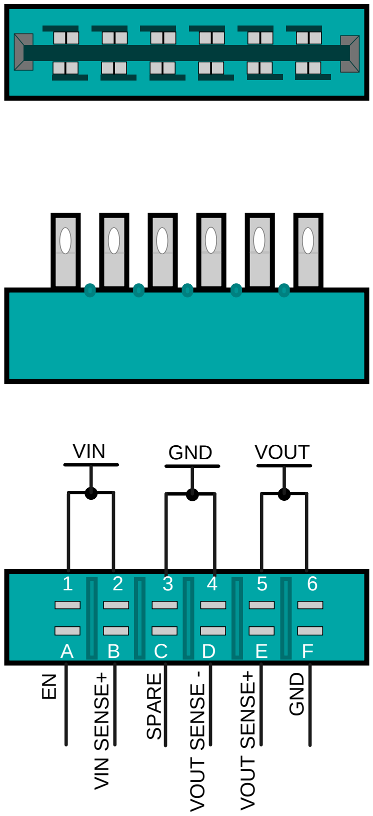


Figure 4. Edge Connector Schematic

4.6 Board Images

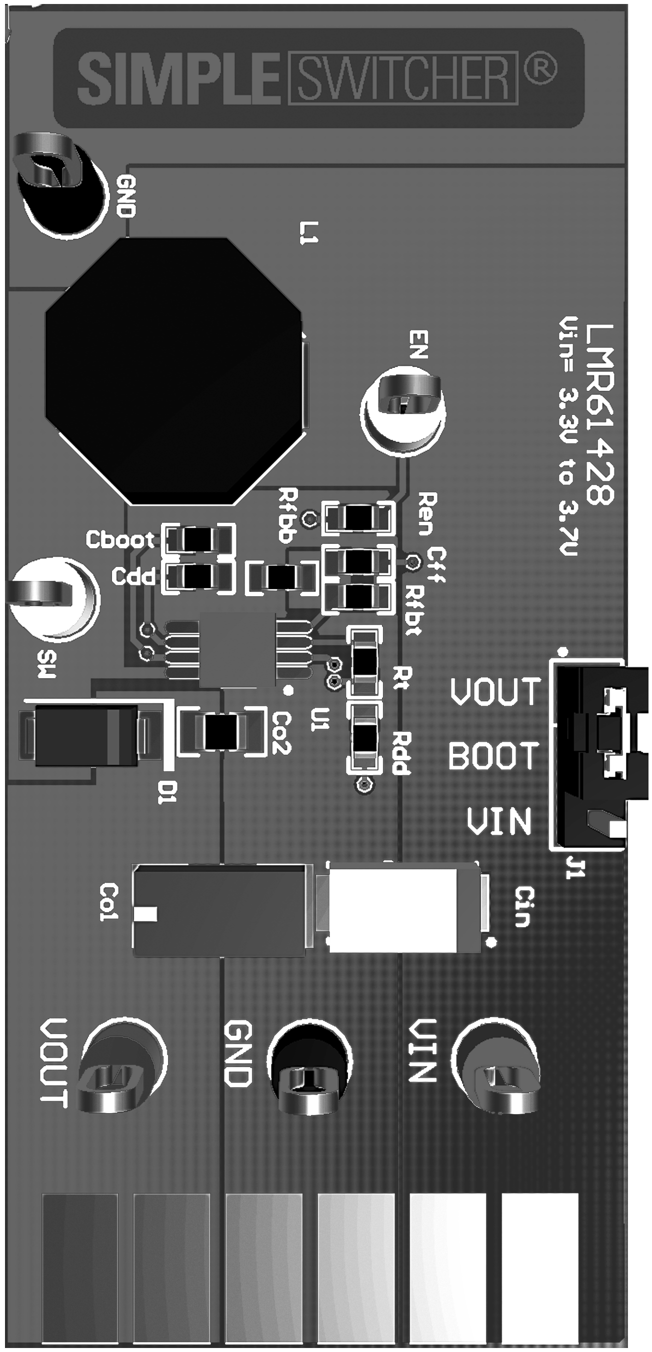


Figure 5. Top Side

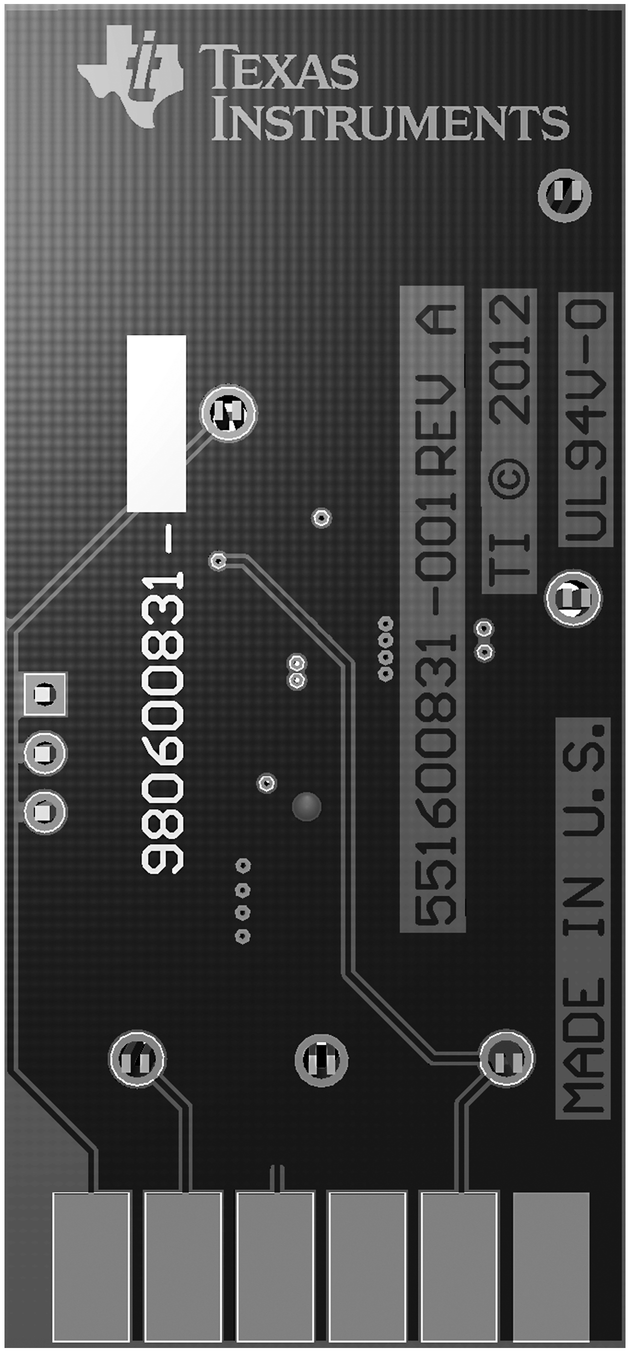
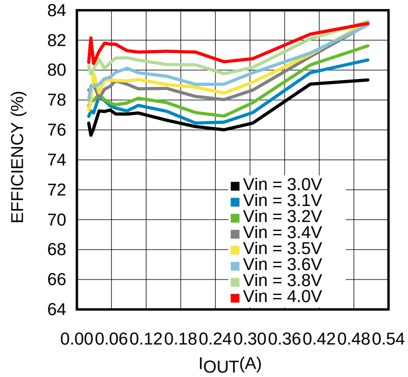


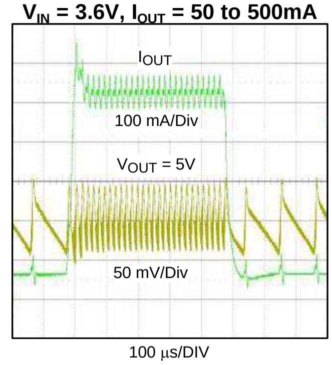
Figure 6. Bottom Side

5 Typical Performance Characteristics

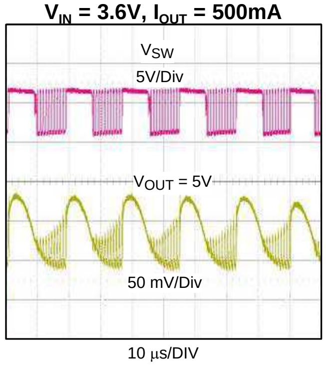
Efficiency vs. Load Current
V_{OUT} = 5V



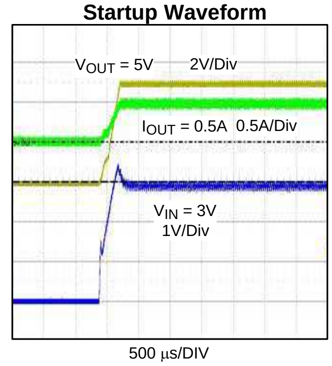
Load Transient Waveforms
V_{IN} = 3.6V, I_{OUT} = 50 to 500mA



Switching Node and Output Voltage Waveforms
V_{IN} = 3.6V, I_{OUT} = 500mA



Startup Waveform



6 Bill of Materials

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LMR61428	Boost Regulator	SOT-23		1	Texas Instruments
L1	SRU1048-8R2Y	Inductor	SMD	8.2uH, 4.6A, 0.015 ohm,	1	Bourns
D1	B220A-13-F	Diode	SMA	Schottky, 20V, 2A	1	Toshiba
Cin	293D226X9010C2TE3	Capacitor	SMD	Tantalum, 22uF, 10V	1	Vishay-Sprague
Co1	594D686X0010C2T	Capacitor	SMD	Tantalum, 68uF, 10V	1	Vishay-Sprague
Co2	08053D105KAT2A	Capacitor	0805	Ceramic, 1uF, 25V, X5R	1	AVX
Cdd	C0603C105K4PACTU	Capacitor	0603	Ceramic, 1uF, 16V, X5R	1	Kemet
Cff	GRM1885C2A390JA01D	Capacitor	0603	Ceramic, 39pF, 100V, C0G/NP0	1	MuRata
Rfbt	RG1608P-154-B-T5	Resistor	0603	150 kΩ	1	Susumu Co Ltd
Rfbb	RG1608P-4992-B-T5	Resistor	0603	49.9 kΩ	1	Susumu Co Ltd
Rt	CRCW0603118KFKEA	Resistor	0603	118 kΩ	1	Vishay-Dale
Rdd	CRCW060349R9FKEA	Resistor	0603	49.9 Ω	1	Vishay-Dale
Ren	CRCW060310K0FKEA	Resistor	0603	10.0 kΩ	1	Vishay-Dale
EN	5014	Test Point Loop		Yellow	1	Keystone
VIN	5010	Test Point Loop		Red	1	Keystone
VOUT	5013	Test Point Loop		Orange	1	Keystone
GND	5011	Test Point Loop		Black	2	Keystone
SW	5012	Test Point Loop		White	1	Keystone
J1	PBC03SAAN	Header		100mil, 1x3	1	Sullins Connector Solutions
SH-J1	969102-0000-DA	Shunt		100mil, Black	1	3M

7 PCB Layout

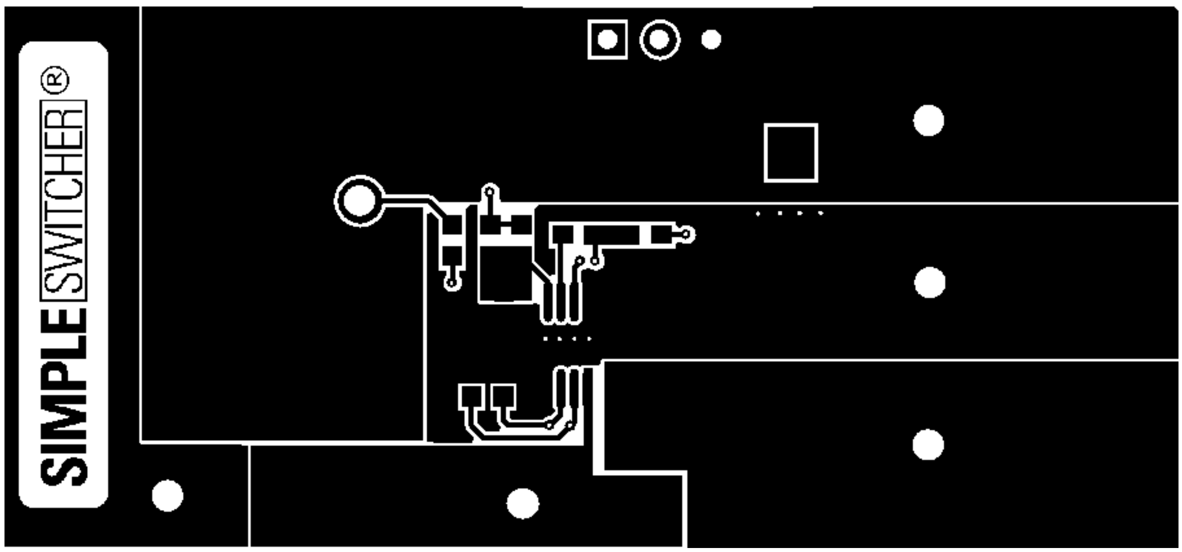


Figure 7. Top Copper

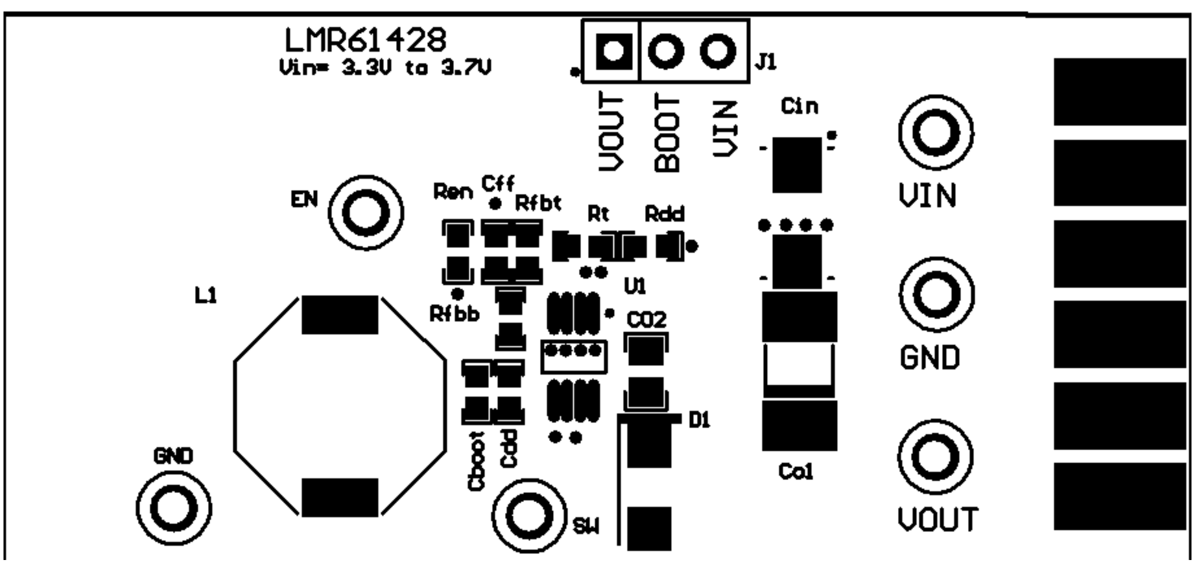


Figure 8. Top Overlay

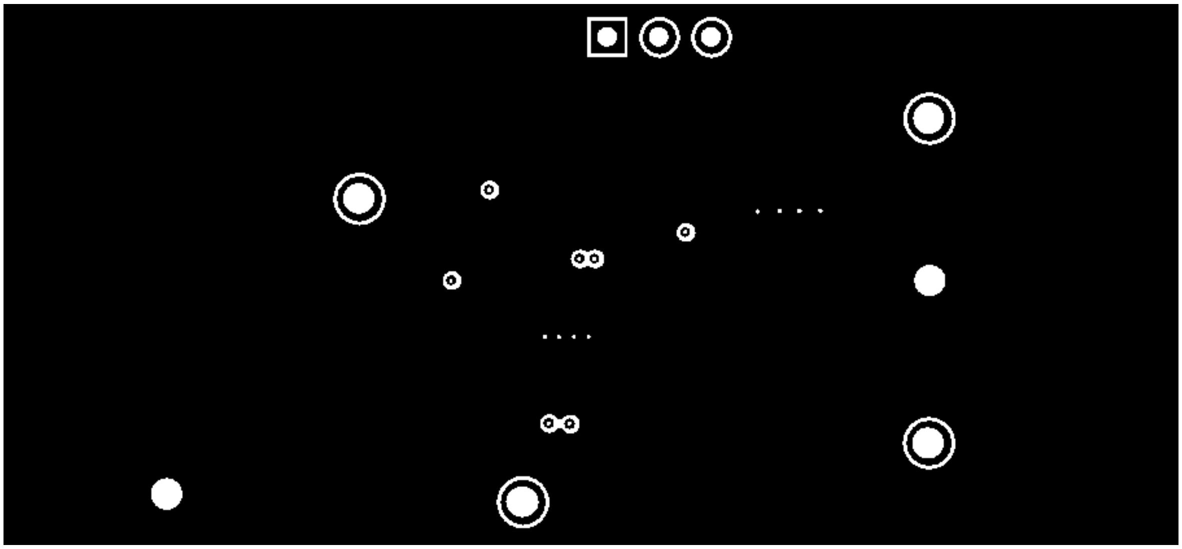


Figure 9. Internal Layer 1

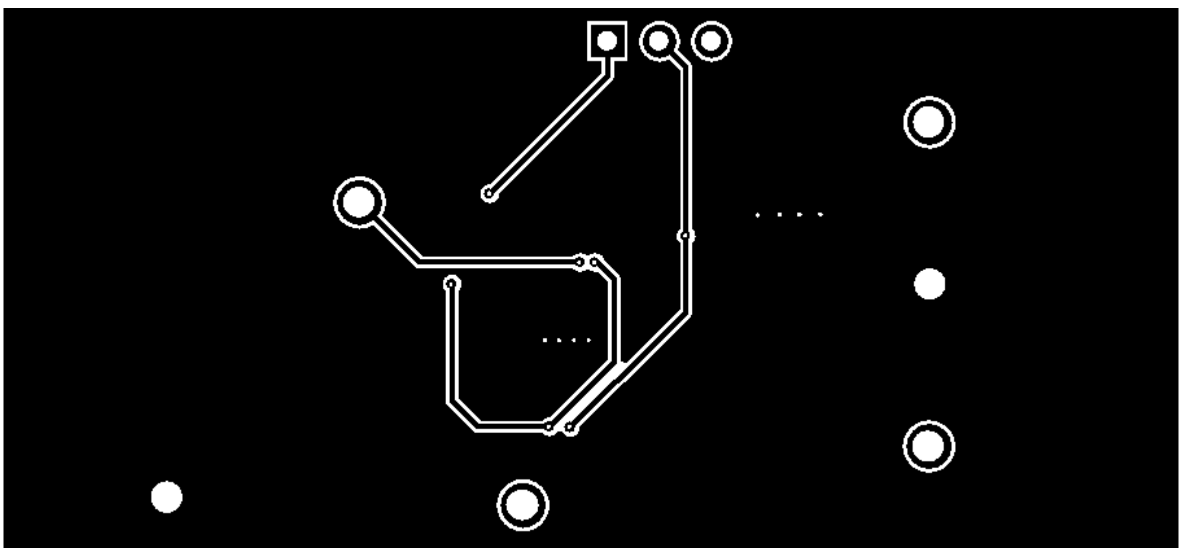


Figure 10. Internal Layer 2

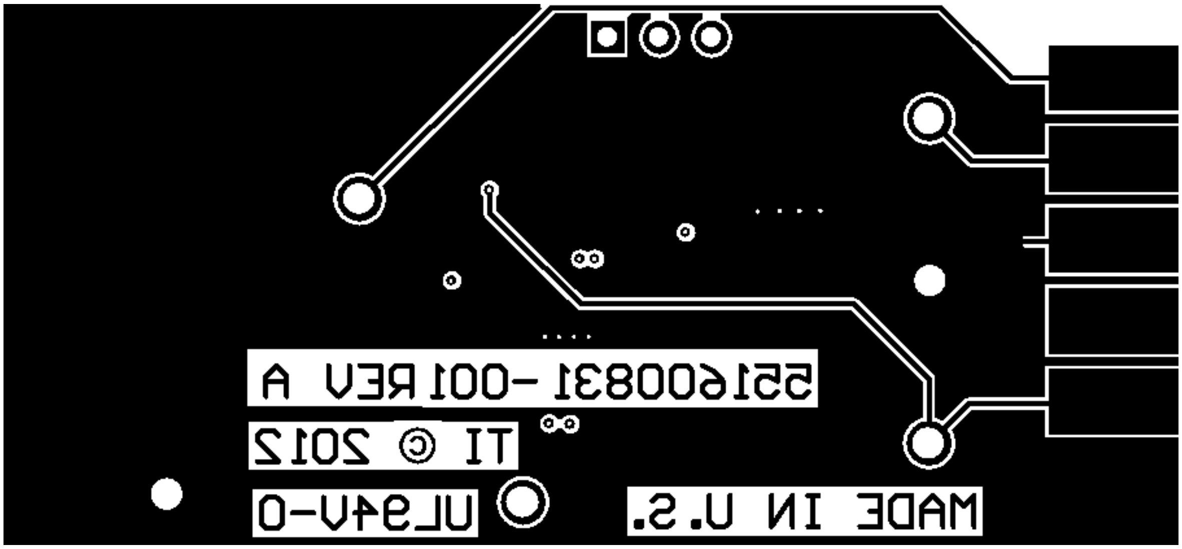


Figure 11. Bottom Copper

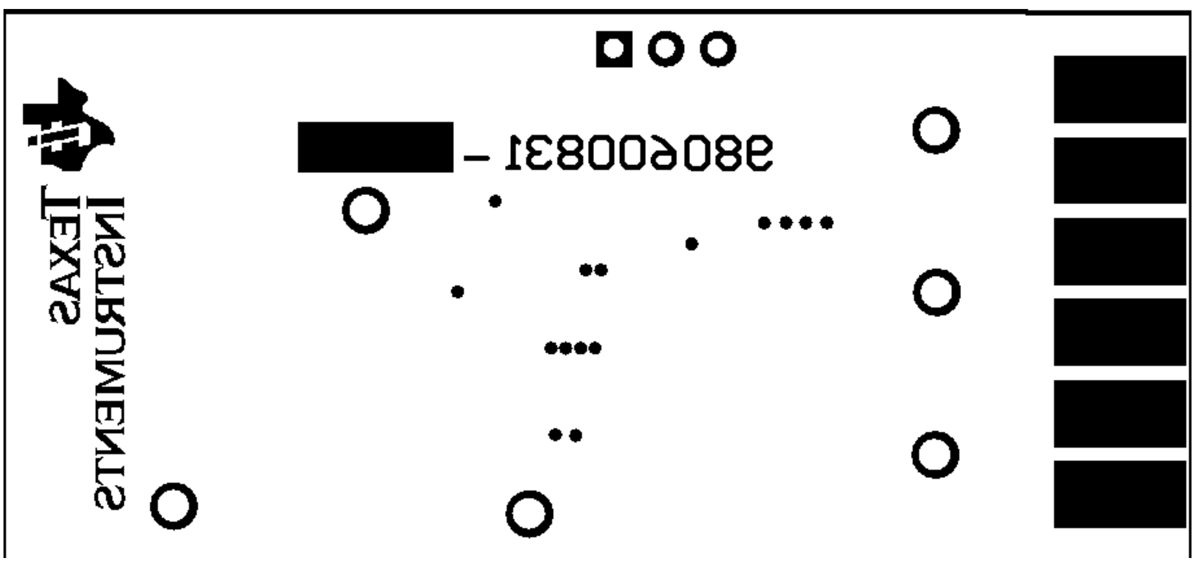


Figure 12. Bottom Overlay

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