



**THE DATASHEET OF
LMH730275/NOPB**



LMH730275 Triple High Speed SSOP Op Amp Evaluation Board

General Description

The LMH730275 evaluation board is designed to aid in the characterization of National Semiconductor's high speed triple SSOP operational amplifiers.

Use the evaluation board as a guide for high frequency layout and as a tool to aid in device testing and characterization.

The evaluation board schematic is shown below in *Figure 1*. Refer to the product data sheets for recommendations for component values.

Basic Operation

By changing R_{IN} and R_{OUT} different input and output impedances can be matched. The SMA connectors and board traces are optimized for 50 to 75 Ω operation. Other impedances can be matched but performance will be noticeably different, especially high frequency response. Even with optimal layout board parasitics play a large part in high frequency performance and different termination resistors will change the frequency of the dominant parasitic poles/zeros.

Inverting configuration

The evaluation board is set up for non inverting operation. For inverting operation make the following modifications (see *Figure 4* and *Figure 5*): On the bottom of the board cut the input trace just before the via to the R1 resistors and run jumpers to the vias that connect to the ground side of R_G (R_G is on the top side of the board). On the top side of the board cut the tab between the ground plane and the grounded pad of R_G . An additional resistor R_T can be used to lower the input impedance of the board it can be soldered between R_G and the ground plane where the tab was cut (the board is labeled for R_T).

Layout Considerations

Printed circuit board layout and supply bypassing play major roles in determining high frequency performance. When designing your own board use these evaluation boards as a guide and follow these steps to optimize high frequency performance:

1. Use a ground plane
2. Include large ($\sim 6.8 \mu\text{F}$) capacitors on both supplies: C5 & C6.
3. Near the device use .01 μF ceramic capacitors from both supplies to ground: C1-C4
4. For improved bypassing .1 μF ceramic capacitors can be stacked on top of C1-C4.
5. Remove the ground and power planes from under the input and output pins.
6. Minimize all trace lengths
7. Use terminated transmission lines for long traces.
8. 2nd Harmonic Distortion performance is impacted by board layout and power supply bypassing experiment with bypass capacitor values for best results.

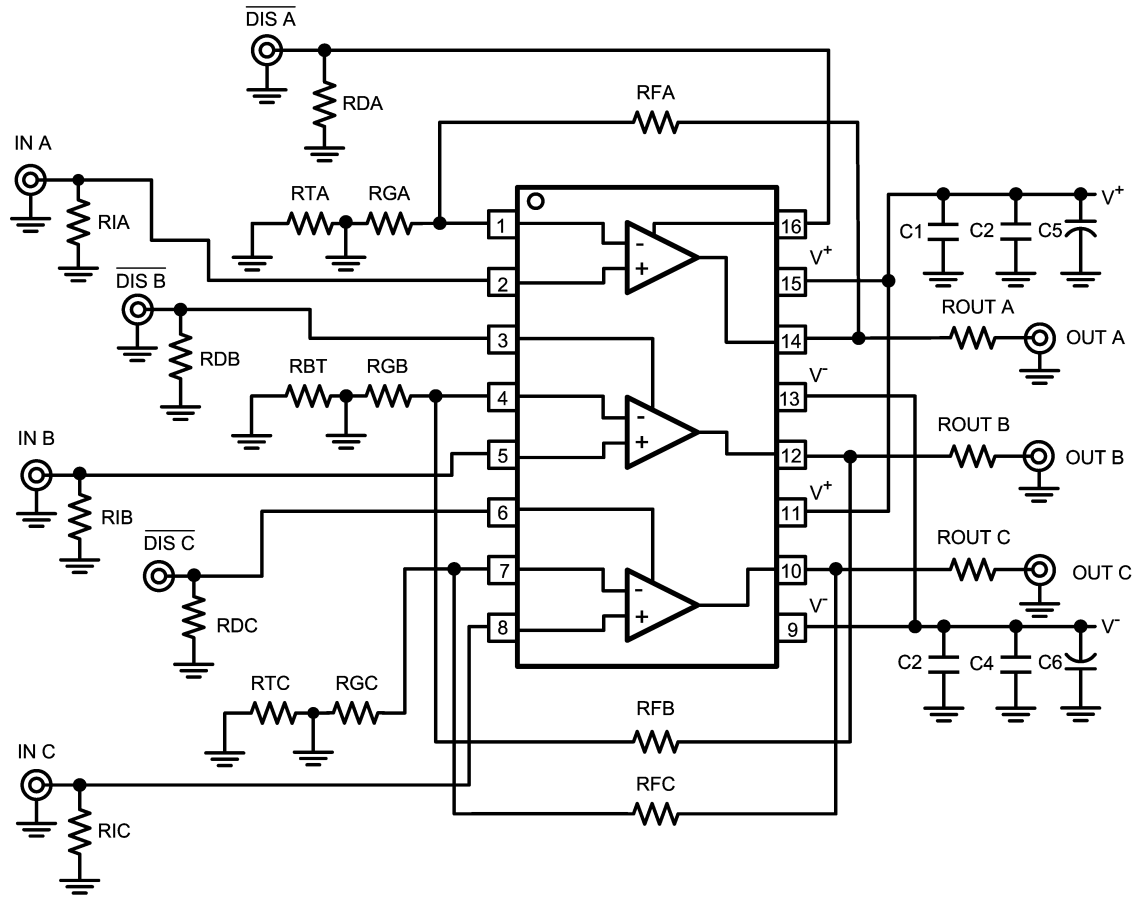
R1A, R1B and R1C are input matching resistors. R0UA, R0UB and R0UC are output matching resistors. RDA, RDB and RDC are input matching resistors for high speed signals applied to the disable inputs. If the disable inputs are not used leave RDA, RDB and RDC empty. Sample artwork for the LMH730275 Evaluation board is included on the next page in *Figure 2*.

Measurement Hints

The board is designed for 50 Ω input and output connections into coaxial cables. For other impedances the terminating resistors can be modified to help match different impedances.

Do not use normal oscilloscope probes to test these circuits. The capacitive loading will change circuit performance drastically. Instead use low impedance resistive divider probes of 100 to 500 Ω . See *Figure 3* for a sample resistive probe. The Low impedance resistor should be 50- 450 Ω . The ground connection should be as short as possible ($\sim 1/2"$). Even with careful use of these probes results should be considered preliminary until verified with controlled impedance measurements. Even the best probes will interfere with circuit operation to some degree. Also, tools, power cables, fingers etc. near the device will change measurement results often dramatically.

Measurement Hints (Continued)



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FIGURE 1. Board Schematic

Measurement Hints (Continued)

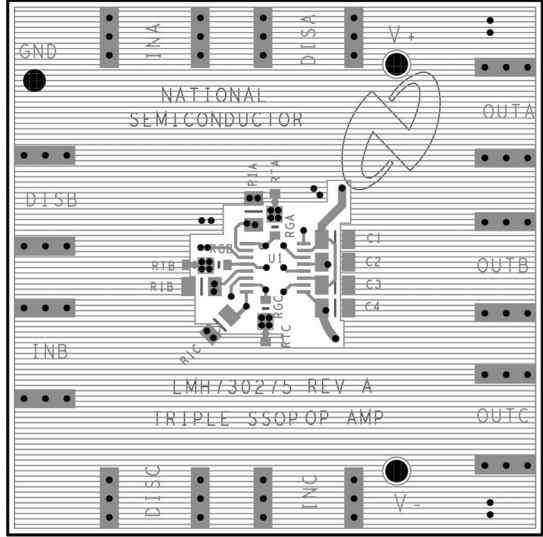
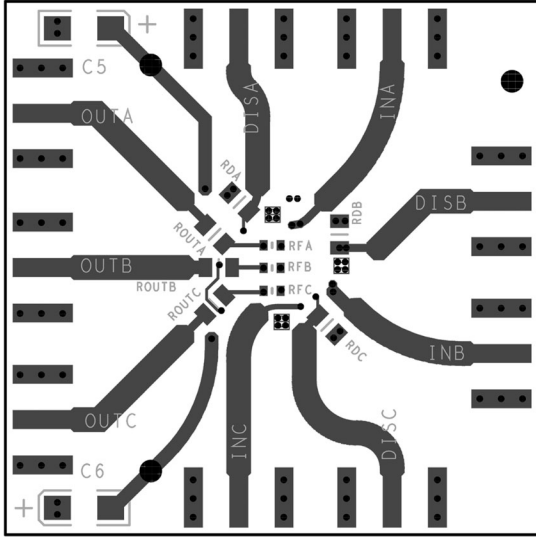
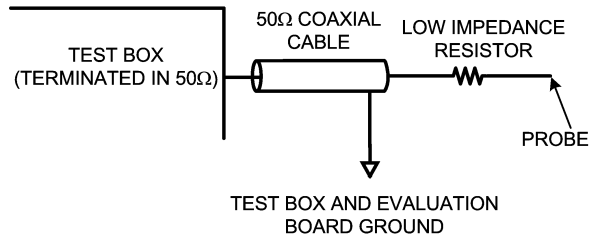


FIGURE 2. Board Layout (Actual size = 1.5" x 1.5")

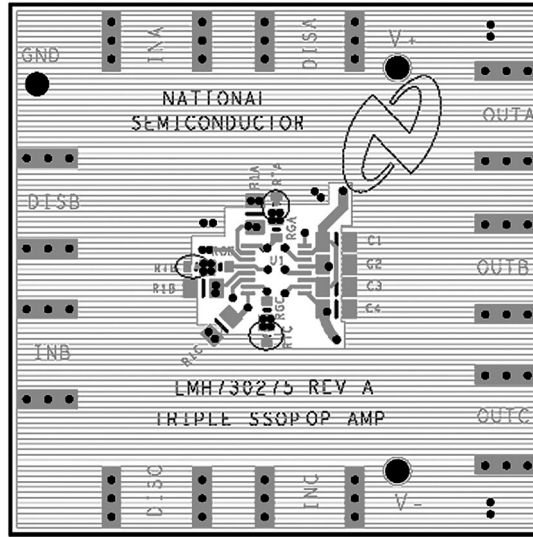


$$\text{PROBE ATTENUATION} = \frac{50}{R + 50}$$

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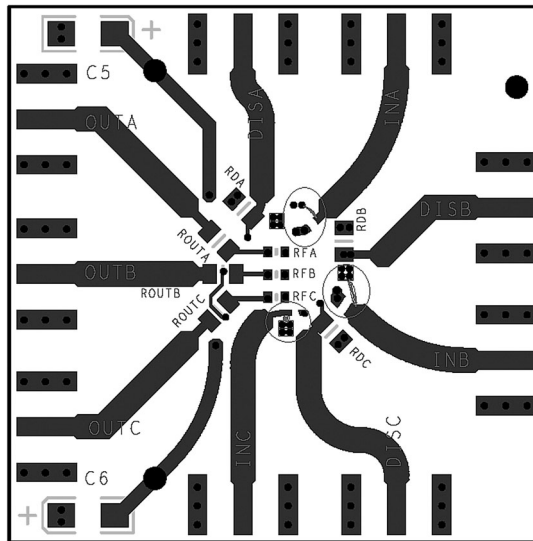
FIGURE 3. Probe Schematic

Measurement Hints (Continued)



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FIGURE 4. Top Layer Modification for Inverting Operation



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FIGURE 5. Bottom Layer Modifications of Board for Inverting Operation

Notes

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