THE DATASHEET OF

ISL97691IRTZ

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ISL97691

2.4V LED Driver with Independent Analog and PWM Dimming Controls of 2 Backlights for 3D Application

FN7840
Rev.2.00
Sep 8, 2017

The ISL97691 is Intersil's highly integrated 4 channel LED driver for single cell Li-Ion battery operated mobile displays requiring analog dimming, and for 3D mobile display applications. It drives four 40mA channels of LEDs up to 26V from an input supply 2.4V to 5.5V. The ISL97691 will also drive 60mA channels up to 21V at 30% duty for high peak current 3D modes.

The ISL97691 provides 4 channels of current with 2 independent analog dimming controls and 2 independent PWM dimming controls. Channels 1 and 2 form one channel group and channels 3 and 4 form the other channel group. Each channel group's analog dimming is controlled through 1-Wire communication with 6-bit resolution and each channel group's PWM dimming is controlled by a separate PWM input. This unique setup allows 2D or 3D application where independent and dynamic channel control of LED peak current and PWM dimming duty cycle are possible. The ISL97691 employs adaptive boost architecture that allows ultra low dimming duty cycle as low as 0.005% at 100Hz dimming frequency.

The driver features dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for the minimum output regulation.

The ISL97691 incorporates extensive protection functions including string open and short circuit detections, OVP, and OTP. The switching frequency can be adjusted from 400kHz to 1.5MHz. The device is offered in a 16 Ld TQFN 3x3mm package and can operate in ambient temperature from -40°C to +85°C.

Features

- 2.4V minimum input voltage, no need for higher voltage supplies
- 4 x 60mA (Note 1) and 4 x 40mA (Note 2) LED current
- 2 groups of independent analog and pwm current controls
  - 1-wire interfaces for 6-bit analog dimming
  - PWM inputs for PWM dimming
  - 0.005% minimum PWM dimming duty cycle at 100Hz
- Low 0.8mA quiescent current
- ±2.5% current matching
- Adjustable switching frequency from 400kHz to 1.5MHz
- Fault protection
  - OVP, OTP, channel open/short circuit protections

NOTES:

1. Not exceeding 30% of the frame rate ($1/t_{FRAME}$), with V_{IN} > 2.7V and T_A < +55°C.
2. V_{IN} > 2.7V

Applications

- Tablet, notebook PC, and smart phone displays LED backlighting
- Mobile displays for 2D or 3D LED backlighting

Related Literature

- For a full list of related documents, visit our website
  - ISL97691 product page

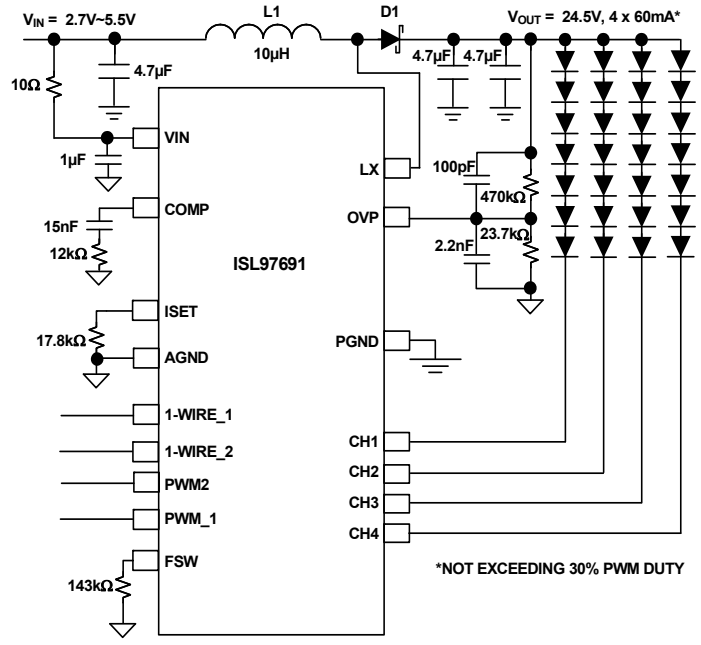


FIGURE 1. TYPICAL APPLICATION CIRCUIT

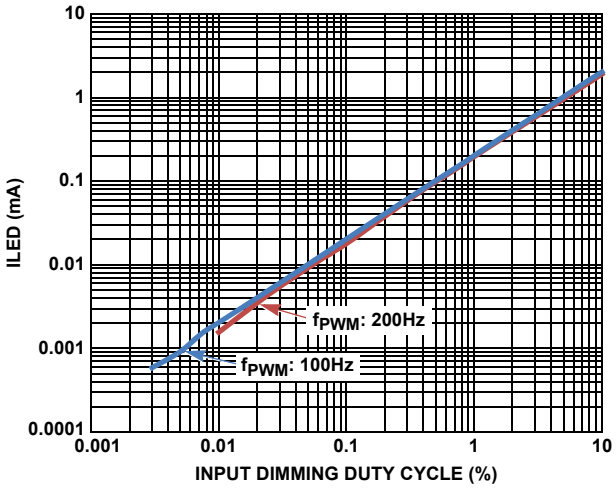
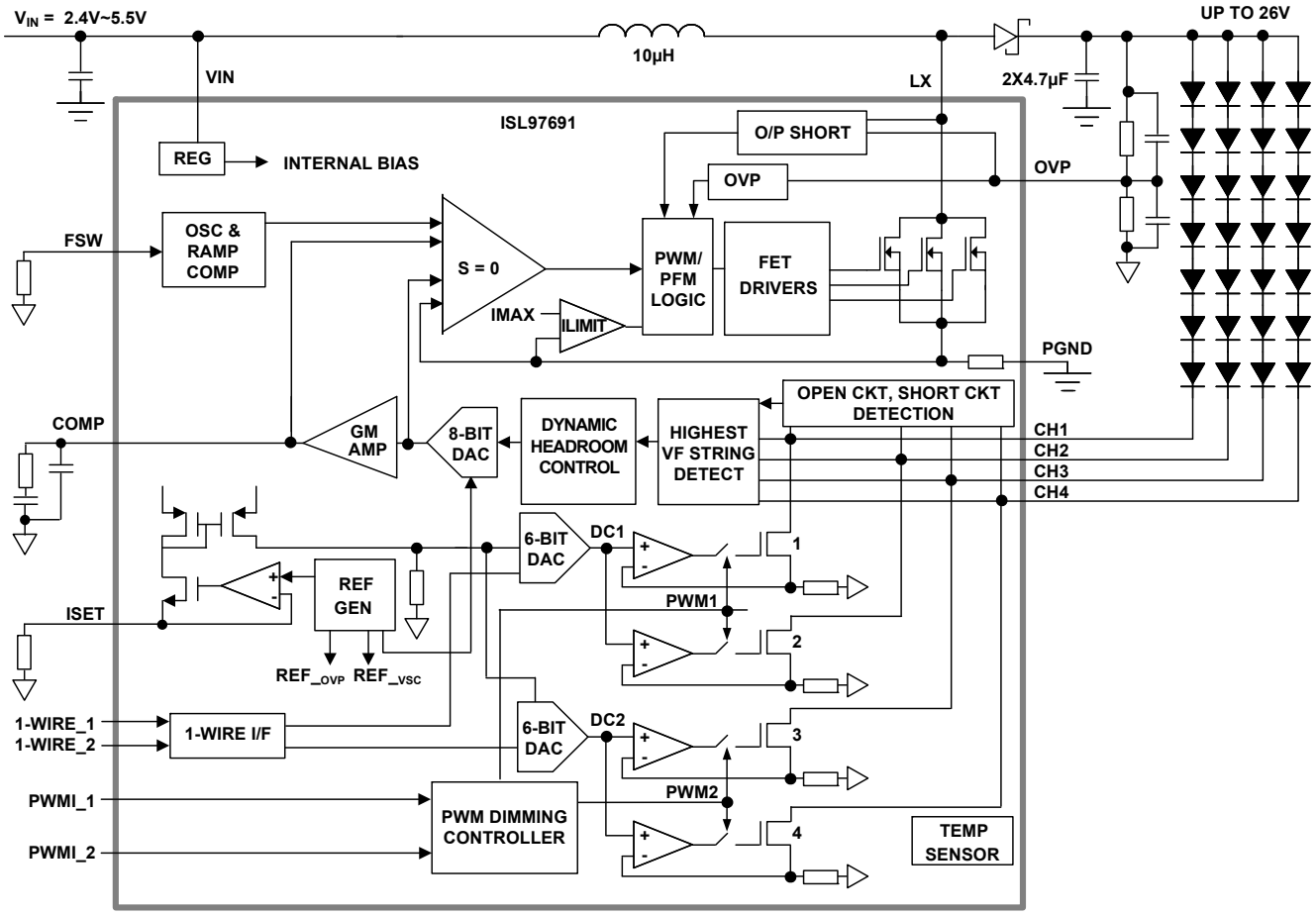


FIGURE 2. ULTRA LOW PWM DIMMING LINEARITY

Block Diagram



Ordering Information

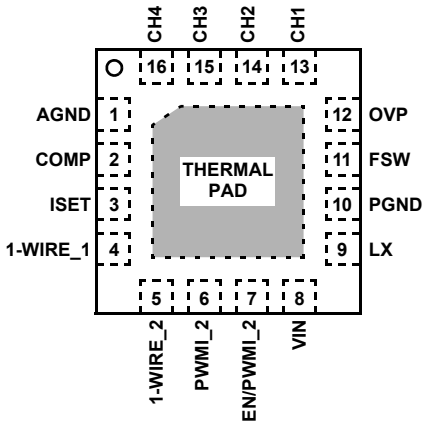
PART NUMBER (Notes 3, 4, 5)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL97691IRTZ	7691	-40 to +85	16 Ld TQFN	L16.3x3D
ISL97691IRTZ-EVALZ	Evaluation Board			

NOTES:

3. Add “-T” suffix for 6k unit or “-TK” suffix for 1k unit tape and reel. Refer to TB347 for details on reel specifications.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), see the product information page for ISL97691. For more information on MSL see TB363.

Pin Configuration

ISL97691
(16 LD 3mmx3mm TQFN)
TOP VIEW



Pin Description

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	AGND	S	Analog Ground for precision circuits.
2	COMP	I	External compensation. Fit a series RC comprising 12kΩ and 15nF from COMP to GND.
3	ISET	I	Channel current setting. The LED channel current is adjusted from 15mA to 60mA with resistor R_{SET} from ISET pin to GND.
4	1-WIRE_1	I	1-Wire interface 1 for controlling channels 1 and 2 with 6-bit analog dimming.
5	1-WIRE_2	I	1-Wire interface 2 for controlling channels 3 and 4 with 6-bit analog dimming.
6	PWMI_1	I	PWM Input 1 for controlling channels 1 and 2 PWM dimming. During the PWM Off period, the 1-WIRE_1 data will remain at the previous programmed level.
7	PWMI_2	I	PWM Input 2 for controlling channels 3 and 4 PWM dimming. During the PWM Off period, the 1-WIRE_2 data will remain at the previous programmed level.
8	VIN	I	Input supply voltage.
9	LX	O	Input to boost switch.
10	PGND	S	Power ground (LX, C_{IN}, and C_{OUT} power return).
11	FSW	I	Switching Frequency Adjustment. The boost switching frequency is adjusted from 400kHz to 1.5MHz with resistor R_{FSW} from FSW pin to GND.
12	OVP	I	Overvoltage protection input.
13	CH1	I	Channel 1 current sink and channel monitoring. Tie pin to GND if channel unused.
14	CH2	I	Channel 2 current sink and channel monitoring. Tie pin to GND if channel unused.
15	CH3	I	Channel 3 current sink and channel monitoring. Tie pin to GND if channel unused.
16	CH4	I	Channel 4 current sink and channel monitoring. Tie pin to GND if channel unused.
	EPAD	X	No electrical connection but should be used to connect PGND and AGND. For example, uses top plane as PGND and bottom plane as AGND with vias on EPAD to allow heat dissipation and minimum noise coupling from PGND to AGND operation.

Table of Contents

Absolute Maximum Ratings

VIN, FSW, ISET, COMP, OVP . . . . . -0.3V to 5.5V
PWMI_1, PWMI_2 . . . . . -0.3V to 5.5V
1-WIRE_1, 1-WIRE_2 . . . . . -0.3V to 5.5V
CH1 to CH4, LX . . . . . -0.3V to 28V
PGND, AGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin

ESD Ratings
Human Body Model (Tested per JESD22-A114F) 2.5kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (JESD22-C101E) 2kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 LD TQFN (Notes 6, 7)	51	4.6
Thermal Characterization (Typical)		**PSI_{JT} (°C/W)**
16 Ld TQFN (Note 8)		0.11

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
8. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 3.3V, PWMI_1 = 3.3V, R_{ISET} = 26.7kΩ, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
GENERAL						
V_{IN}	Backlight Supply Voltage	T_A = +25°C	**2.4**		**5.5**	V
I_{VIN}	V_{IN} Active Current, All Strings 100% Duty, I_{LED} = 40mA	All channels 100% duty		2.5		mA
		All channels 0% duty		0.8		mA
$I_{AUTOSHUTDOWN}$	V_{IN} Shutdown Current, both 1-Wire Interface Inputs Inactive	PWMI_1 and PWMI_2 low longer than $t_{PWMTIMEOUT}$		1		µA
V_{OUT}	Output Voltage	$V_{IN} \geq$ 2.7V, I_{LED} = 40mA			**26**	V
t_{WAKE}	Wakeup Time from Sleep	Boost and channels operating		1.5	**2.2**	ms
V_{UVLO}	Undervoltage Lockout Threshold		**2**	2.15	**2.35**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			150		mV
BOOST SWITCHING REGULATOR						
SS	Soft-start	100% LED Duty Cycle		7		ms
SWILimit	Boost FET Current Limit		**2.5**	2.8	**3.2**	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance	T_A = +25°C		212		mΩ
Eff_peak	Peak Efficiency	V_{IN} = 5.5V, V_{OUT} = 21V, T_A = +25°C, R_{FSW} = 144kΩ, $I_{CH1-CH4}$ = 20mA, L = 10µH with DCR ≤ 150mΩ		90		%
		V_{IN} = 2.4V, V_{OUT} = 21V, T_A = +25°C, R_{FSW} = 144kΩ, $I_{CH1-CH4}$ = 20mA, L = 10µH with DCR ≤ 150mΩ		74		%
D_{MAX}	Boost Maximum Duty Cycle	FSW = 400kHz	**93.5**			%
		FSW = 1.5MHz	**93**			%

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PARAMETER	DESCRIPTION	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
D_{MIN}	Boost Minimum Duty Cycle	FSW = 400kHz			**11**	%
		FSW = 1.5MHz			**15**	%
f_{SW}	Boost Switching Frequency	R_{FSW} = 216kΩ	**360**	400	**440**	kHz
		R_{FSW} = 72.1kΩ		1.2		MHz
		R_{FSW} = 57.7kΩ	**1.35**	1.5	**1.65**	MHz
ILX_leakage	LX Leakage Current	LX = 26V			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel DC Current Matching	I_{LED} = 20mA	**-2.5**		**+2.5**	%
I_{ACC}	Current Accuracy	I_{LED} = 20mA	**-3**		**+3**	%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**6.75**	8	**9.25**	V
V_{temp}	Over-Temperature Threshold			150		°C
V_{OVPlo}	Overvoltage Limit on OVP Pin		**1.18**	1.22	**1.245**	V
OVP_{fault}	OVP Short Detection Fault Level			70		mV
CHANNEL CURRENT SINKS						
$V_{HEADROOM}$	Dominant Channel Current Sink Headroom at CH Pin	I_{LED} = 20mA, T_A = +25°C		300 (Note 11)		mV
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 20mA, T_A = +25°C		65		mV
$I_{LED(max)}$	Maximum LED Current per Channel	2.7V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 21V, 30% of T_{FRAME}, T_A ≤ +70°C	**60**			mA
	Maximum Total LED Current For All Strings Limited to 120mA	2.7V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 21V, 30% of T_{FRAME}, T_A ≤ +70°C	**60**			mA
	Maximum Total LED Current For All Strings Limited to 110mA	2.7V ≤ V_{IN} ≤ 5.5V, V_{OUT} = 24.5V, 31.25% of T_{FRAME}, T_A ≤ +70°C	**60**			mA
1-WIRE INTERFACE						
t_{LOGIC1}	Timing Range for Logic 1	Device in normal operation	15		45	µs
t_{LOGIC1_WAKE}	Timing Range for Logic 1 for First Bit Transmission During Shutdown	Device in autoshutdown	25		45	µs
t_{LOGIC0}	Timing Range for Logic 0	Device in normal operation	90		120	µs
t_{LOGIC0_WAKE}	Timing Range for Logic 0 for First Bit Transmission During Shutdown	Device in autoshutdown	100		120	µs
t_{LOAD}	Timing Range for Load	Device in normal operation	218			µs
t_{HI}	Valid 1-Wire_1 or 1-Wire_2 High Time	Device in normal operation	3			µs
PWM GENERATOR						
V_{IL}	PWM Input Low Voltage				**0.5**	V
V_{IH}	PWM Input High Voltage		**1.5**			V

Electrical Specifications All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 3.3V, PWMI_1 = 3.3V, R_{ISET} = 26.7kΩ, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
F_{PWMI}	PWMI Input Frequency Range ($1/t_{PWM}$)		**100**		**30,000**	Hz
$t_{PWMTIMEOUT}$	Low duration on both PWMI_1 and PWMI_2 for driver to enter auto low-power shutdown			120		ms
PWM_{ACC}	PWM Dimming Output Resolution			80		ns
$t_{PWM\_ON\_MIN}$	PWM Dimming Minimum On-Time			350		ns
t_L	Channels 1 and 2 ON time in 1 frame	t_{FRAME} = 4.17ms, I_{LED} = 60mA		30%*t_{FRAME}	35%*t_{FRAME}	ms
		t_{FRAME} = 16.67ms, I_{LED} = 60mA		30%*t_{FRAME}	35%*t_{FRAME}	ms
t_R	Channels 3 and 4 on time in 1 frame	t_{FRAME} = 4.17ms, I_{LED} = 60mA		30%*t_{FRAME}	35%*t_{FRAME}	ms
		t_{FRAME} = 16.67ms, I_{LED} = 60mA		30%*t_{FRAME}	35%*t_{FRAME}	ms

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. At maximum V_{IN} of 5.5V, minimum V_{OUT} is 6V. Minimum V_{OUT} can be lower at lower V_{IN}.
11. Varies within the range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

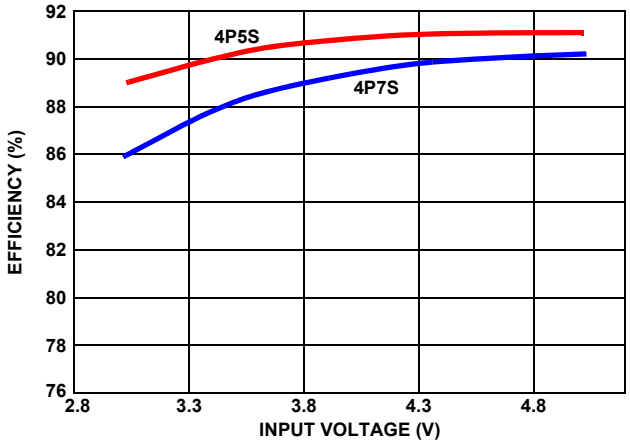

FIGURE 3. EFFICIENCY vs V_{IN} (I_{CH} = 20mA, f_{DIM} = 200Hz, V_{OUT} = 21V, LEDs = 4P7S)

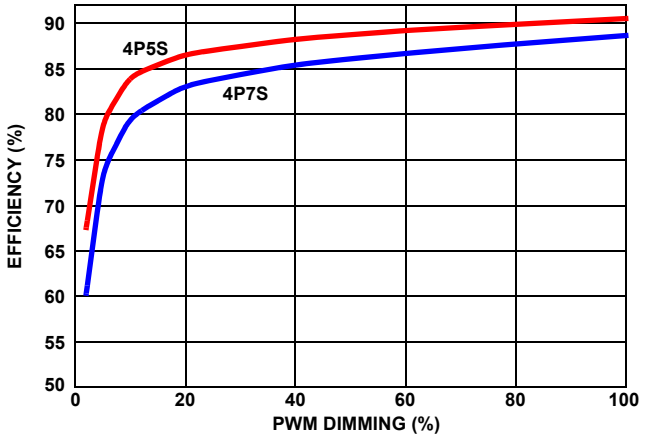

FIGURE 4. EFFICIENCY vs PWM DIMMING (V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, V_{OUT} = 21V, LEDs = 4P7S)

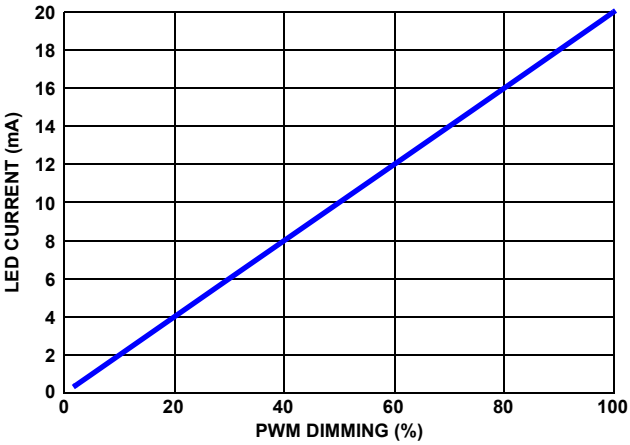

FIGURE 5. PWM DIMMING LINEARITY (V_{IN} = 3.7V, f_{DIM} = 200Hz, V_{OUT} = 21V, LEDs = 4P7S)

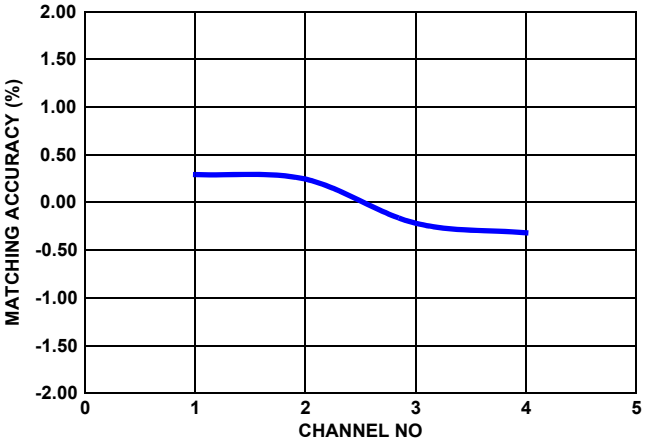

FIGURE 6. CHANNEL MATCHING ACCURACY (V_{IN} = 3.7V, I_{CH} = 20mA, V_{OUT} = 21V, LEDs = 4P7S)

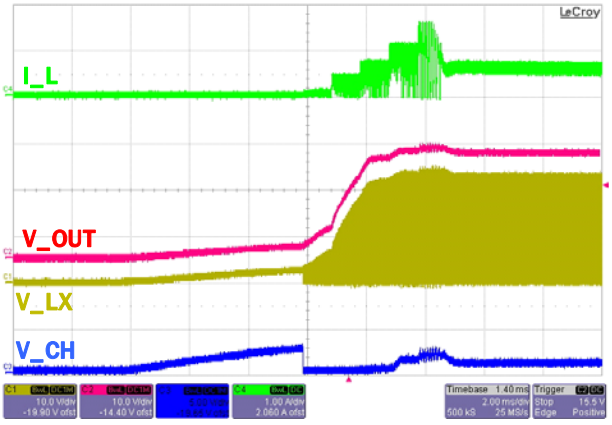

FIGURE 7. START-UP (100% DIRECT PWM DIMMING, V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, LEDs = 4P7S)

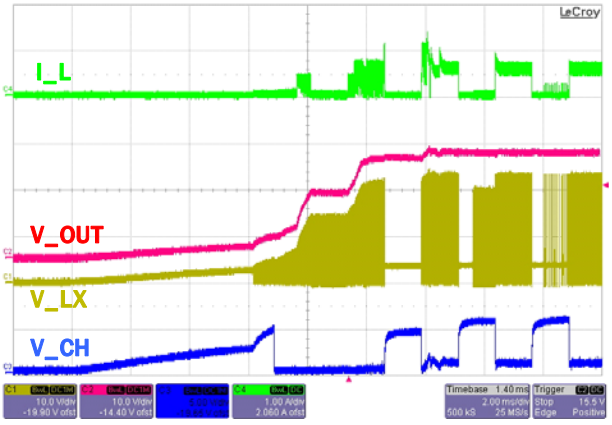

FIGURE 8. START-UP (50% DIRECT PWM DIMMING, V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, LEDs = 4P7S)

Typical Performance Curves (Continued)

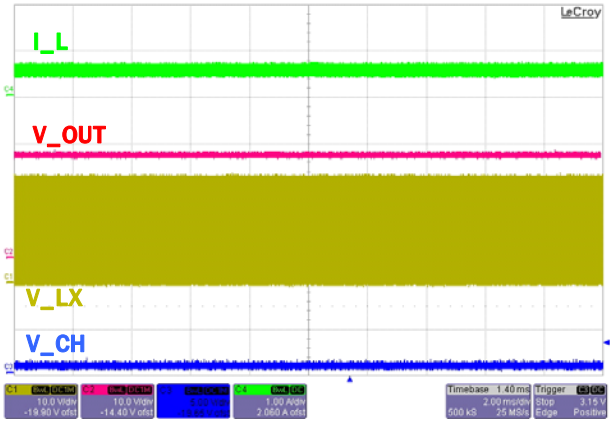

FIGURE 9. 100% DIRECT PWM DIMMING (V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, LEDs = 4P7S)

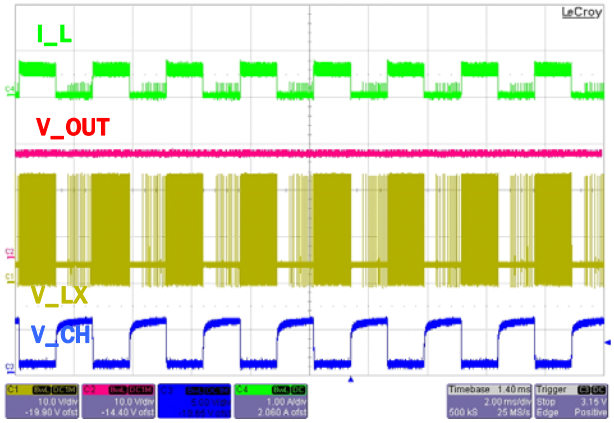

FIGURE 10. 50% DIRECT PWM DIMMING (V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, LEDs = 4P7S)

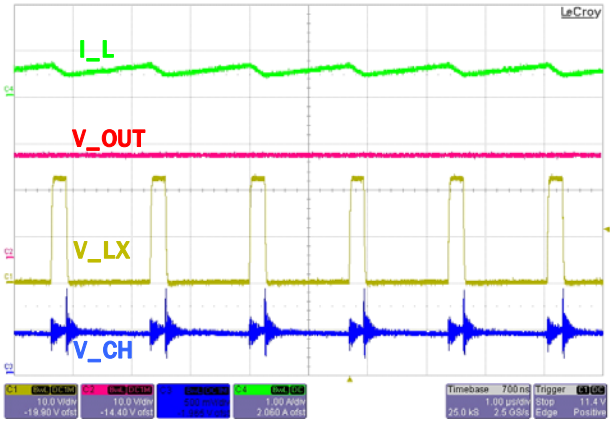

FIGURE 11. BOOST SWITCHING AND CHANNEL VOLTAGE RIPPLE (V_{IN} = 3.7V, I_{CH} = 20mA, f_{DIM} = 200Hz, LEDs = 4P7S, 22µH, f_{SW} = 600kHz)

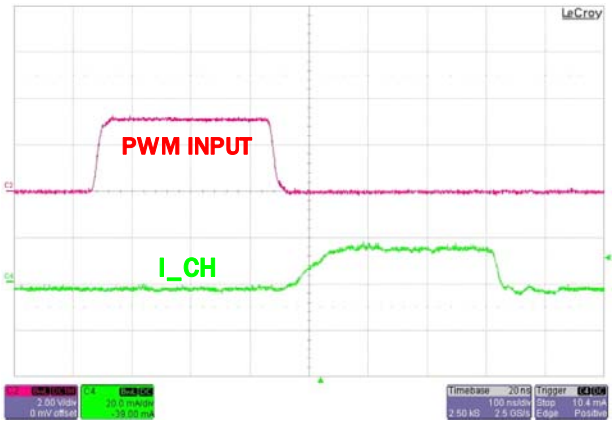

FIGURE 12. MINIMUM DIMMING DUTY CYCLE (PWM DIMMING INPUT 0.003%, f_{DIM} = 100Hz)

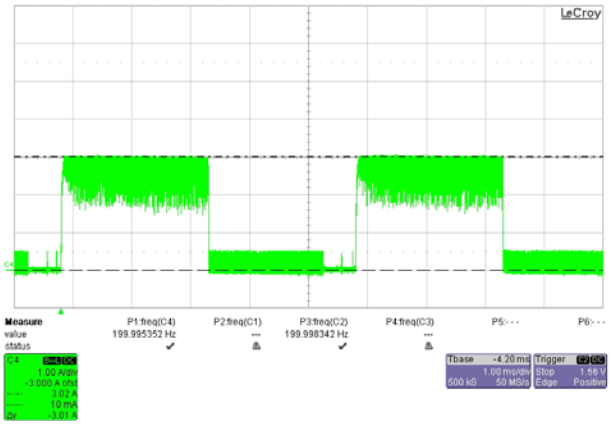

FIGURE 13. BOOST FET CURRENT LIMIT

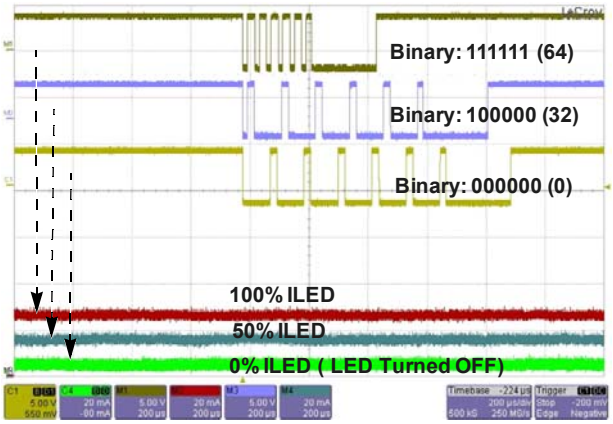

FIGURE 14. LED DC CURRENT CONTROL WITH 1-WIRE INTERFACE

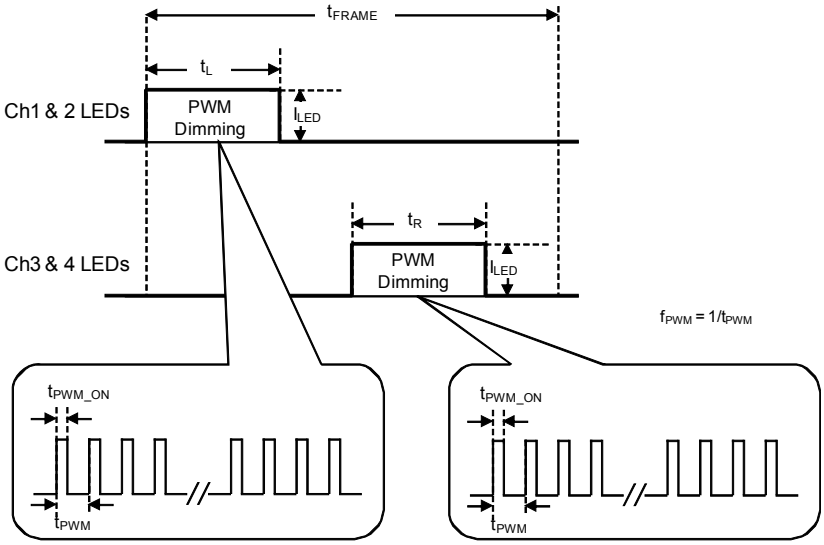

FIGURE 15. 3D APPLICATION TIMING DIAGRAM

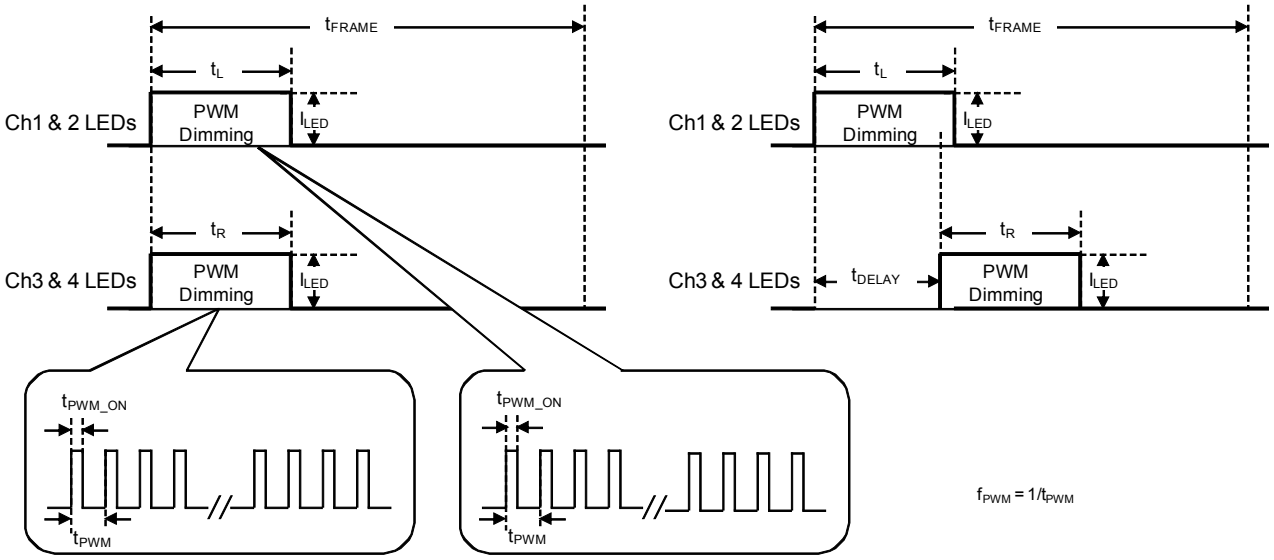

FIGURE 16. 2D APPLICATION TIMING DIAGRAM

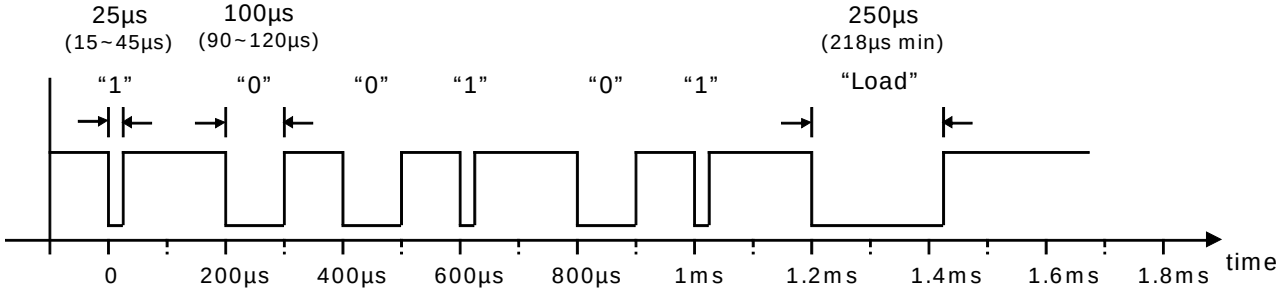

FIGURE 17. 1-WIRE INTERFACE

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97691 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. This architecture achieves the fast transient response which is essential for portable product backlight applications where the backlight must not flicker when the power source is changed from a drained battery to an AC/DC adapter.

The number of LEDs that can be driven by the ISL97691 depends on the type of LED chosen in the application. The maximum output is 26V at 40mA from 2.7V input, or 21V at 60mA from 2.7V input with 30% dimming duty.

AutoShutdown

The ISL97691 simplifies the implementation of low power shutdown by detecting that both PWM inputs 1-WIRE_1 and 1-WIRE_2 have been low for 120ms (typical). When this timeout is detected on both 1-WIRE_1 and 1-WIRE_2, the boost converter and LED string drivers are turned off while retaining the value of the two internal 6-bit 1-Wire registers which store the analog dimming values.

The 1-Wire interfaces may be written during shutdown mode subject to the following constraints:

- Any interface (1-WIRE_1 or 1-WIRE_2) to be written during shutdown should idle high between transmissions
- The first bit of every 6-bit 1-Wire transmission must be sent with a tighter timing tolerance than normal (25µs minimum for logic 1, 100µs minimum for logic 0). The extra 10µs allows the ISL97691 to wakeup and measure the transmission.

It is recommended that applications requiring 1-Wire transmissions during shutdown simply apply the constraints described above to all transmissions.

Dimming Controls

The ISL97691 provides two groups, channels 1 and 2 as one group and channels 3 and 4 as the other group, with independent analog and PWM dimming.

The maximum LED current is set globally for all channels by R_{SET} in the range 15mA to 60mA per Equation 1:

$$I_{LEDmax} = \frac{1066}{R_{SET}} \quad \text{(EQ. 1)}$$

Where:

R_{SET} is resistor from ISET pin to GND (Ω)

I_{LEDmax} is the peak current set by resistor R_{SET} (A)

For example, if the maximum required LED current (I_{LEDmax}) is 60mA, then the R_{SET} value needed is:

$$R_{SET} = 1066/0.06 = 17.8k\Omega \quad \text{(EQ. 2)}$$

Choose nearest standard resistor: 17.8kΩ, 0.1%

ANALOG DIMMING

The channel peak current for the two groups may be reduced from the maximum LED current set by R_{SET} by analog dimming through two 6-bit DACs. The DACs are updated with simple negative pulse duration and pulse counting 1-Wire interfaces.

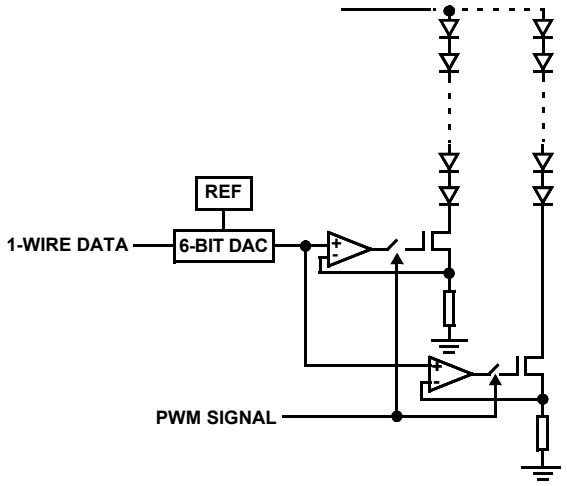

FIGURE 18.

Channels 1 and 2 are set through the 1-WIRE_1 pin, and channels 3 and 4 are set through the 1-WIRE_2 pin. The two 1-Wire interfaces are independent of the two PWM inputs PWMI_1 and PWMI_2, and any combination of these 4 inputs may be active at the same time.

The 1-Wire interface provides 6-bit (64-level) analog dimming resolution. The interface uses a normally high connection for use with open-drain driving schemes and Intersil's 1-Wire interface. When held low for between 15µs and 45µs, the interface reads a logic 1. When held low for between 90µs and 120µs the interface reads a logic 0. When held low for greater that 215µs, the interface loads the last 6 bits into the brightness control register and updates the peak current. The required minimum high time is 3µs.

The 1-Wire programming is summarized as follows:

- Logic 0 = Negative pulse >90µs and <120µs
- Logic 1 = Negative pulse >15µs and <45µs
- Load = Negative pulse >215µs

Figure 18 shows an example of transmitting and loading the value b'100101'.

The serial interface defaults to b'111111' (63) on power-up. The maximum LED current I_{LEDmax} set by resistor R_{SET} for each of the two channel groups 1 and 2 is digitally adjusted by each channel's brightness control register per Equation 3:

$$I_{LED} = I_{LEDmax} \times \frac{N}{63} \quad \text{(EQ. 3)}$$

Where:

N is the integer value 1 to 63 in the channel groups' brightness control register

I_{LEDmax} is the peak current set by resistor R_{SET} (A)

PWM DIMMING

The ISL97691 employs direct PWM dimming such that the output PWM dimming follows directly with the input PWM signal without modifying the input frequency. PWM dimming for channels 1 and 2 are set by the PWMI_1 pin, and channels 3 and 4 are set by the

PWMI_2 pin. These two PWM inputs are independent of the two 1-Wire interfaces 1-WIRE_1 and 1-WIRE_2, and any combination of these 4 inputs may be active at the same time. The average LED current of each channel can be calculated as Equation 4:

$$I_{LED(ave)} = I_{LED} \times PWM \quad \text{(EQ. 4)}$$

Where:
I_{LED} is the current set by 1-WIRE_n interface (A)
PWM is the duty of the signal at the PWMI_n pin

During the PWM off-time, the two 1-WIRE data will remain at the previous programmed levels.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by a current sink circuit.

The LED peak current is set by the external R_{SET} resistor according to Equation 1. The current sink MOSFETs in each LED driver channel output are designed to operate within a range of about 300mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from internal amplifier offsets, internal layout and reference accuracy. These parameters are optimized for current matching and absolute current accuracy. Absolute accuracy is also determined by the external resistor R_{SET}, so a 0.1% tolerance resistor is recommended.

Dynamic Headroom Control

The ISL97691 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage on any of the channel pins. When this lowest channel voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used to help set the output voltage of the boost regulator. The boost regulates the output to the correct level such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current sink circuit on each channel will ensure that each channel has the same current.

Soft-Start

Once the ISL97691 is powered up, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97691 includes a soft-start feature where this current limit starts at a low value (350mA). This is stepped up to the final 2.8A current limit in 7 further steps of 350mA. These steps will happen over typically 7ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

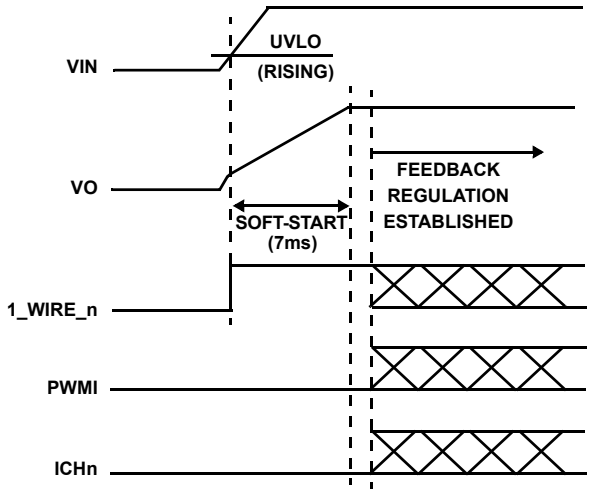

FIGURE 19.

Note that there will be also an initial in-rush current to C_{OUT} when V_{IN} is applied. This is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L.

Power-Off Sequence

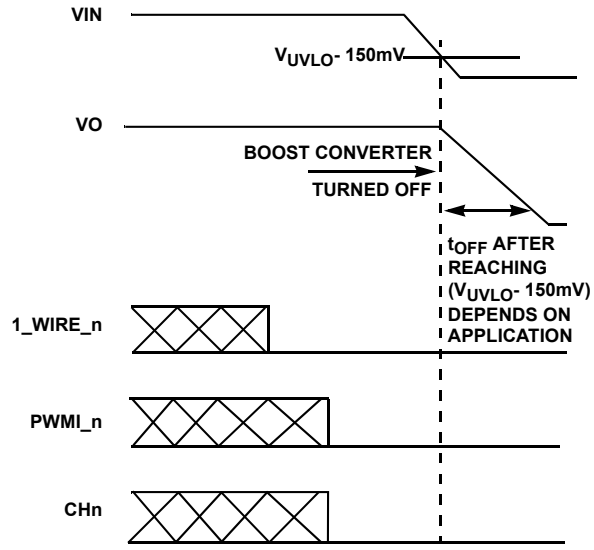

FIGURE 20.

Operation with Input Voltage Greater than 5.5V

The ISL97691 boost regulator can operate from an input voltage higher than 5.5V, and up to 23V, as long as an additional supply voltage between 2.4V and 5.5V is available for the VIN pin. Please refer to Figure 21 for a typical application schematic adopting this solution.

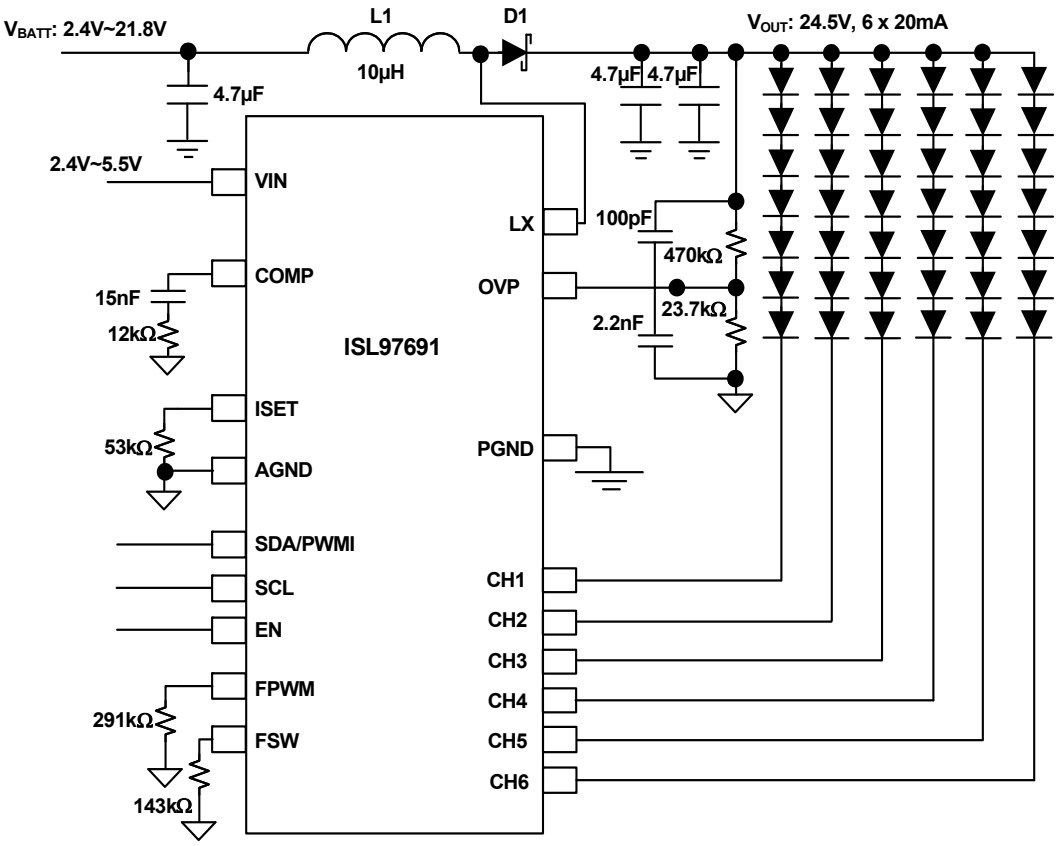

FIGURE 21. LED DRIVER OPERATION WITH INPUT VOLTAGE UP TO 26V

Component Selection

The design of the boost converter is simplified by an internal compensation scheme allowing easy design without complicated calculations. Please select your component values using the recommendations below.

Input Capacitor

It is recommended that a 4.7µF to 10µF X5R/X7R or equivalent ceramic input capacitor is used.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the boost output voltage, V_{OUT}, and keeps the voltage at a safe level. The OVP threshold is set as shown in Equation 5:

$$V_{OVP}(typ) = 1.22V \times \frac{R1 + R2}{R2} \quad \text{(EQ. 5)}$$

Where:
V_{OVP} is the maximum boost output voltage, V_{OUT} (V)
R_1 is the resistor from OVP pin to the boost output (Ω)
R_2 is the resistor from OVP pin to GND (Ω)

The total R_1 plus R_2 series resistance should be high to minimize power loss through the resistor network. For example, choosing R_1 = 470kΩ and R_2 = 23.7kΩ per the "Typical Application Circuit" on page 1, sets V_{OVP} (typ) to 25.41V (Equation 6).

$$V_{OVP}(typ) = 1.22V \times \frac{470 + 23.7}{23.7} = 25.41V \quad \text{(EQ. 6)}$$

The OVP threshold, R_1, and R_2 tolerances should also be taken into account (Equations 7 and 8).

$$V_{OVP}(min) = 1.18V \times \frac{R1min + R2max}{R2max} \quad \text{(EQ. 7)}$$

$$V_{OVP}(max) = 1.24V \times \frac{R1max + R2min}{R2min} \quad \text{(EQ. 8)}$$

Calculating V_{OVP} using the OVP threshold range (1.18V to 1.24V) and 0.1% resistor tolerances gives an actual V_{OVP} range of 24.53V to 25.88V for the 25.4V example above (Equations 9 and 10).

$$V_{OVP}(min) = 1.18V \times \frac{(470 \times 0.999) + (23.7 \times 1.001)}{(23.7 \times 1.001)} = 24.53V \quad \text{(EQ. 9)}$$

$$V_{OVP}(max) = 1.24V \times \frac{(470 \times 1.001) + (23.7 \times 0.999)}{(23.7 \times 0.999)} = 25.88V \quad \text{(EQ. 10)}$$

It is recommended that parallel capacitors are placed across the OVP resistors such that $R_1/R_2 = C_2/C_1$. Using a C_1 value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which reduces noise susceptibility when using high value resistors.

Boost Output Voltage Range

The working range of the boost output voltage, V_{OUT} is from 40% to 100% of the maximum output voltage, V_{OVP}, set by resistors R_1 and R_2 as described in the previous section.

The target applications should be considered carefully to ensure that V_{OVP} is not set unnecessarily high. For example, using R_1 = 470kΩ and R_2 = 23.7kΩ per the Typical Application Circuit on page 2 sets V_{OVP} to between 24.53V to 25.88V when tolerancing is considered.

The minimum voltage, V_{OVP} (min) = 24.53V, sets the maximum number of LEDs per channel because this the worst case minimum voltage that the boost converter is guaranteed to supply.

The maximum voltage, V_{OVP}(max) = 25.88V, sets the minimum number of LEDs per channel because it sets the lowest voltage that the boost converter is guaranteed to reach: 40% x 25.88V = 10.35V.

Using LEDs with a V_F tolerance of 3V to 4V, this V_{OVP} example is suitable for strings of 4 to 6 LEDs. If fewer than 4 LEDs per channel are specified, V_{OVP} must be reduced.

Switching Frequency

The boost switching frequency is adjusted by resistor R_{FSW} (Equation 11):

$$f_{SW} = \frac{(8.65 \times 10^{10})}{R_{FSW}} \quad \text{(EQ. 11)}$$

Where:
f_{SW} is the desirable boost switching frequency (Hz)
R_{FSW} is resistor from FSW pin to GND (Ω)

Inductor

Choose the inductance according to Table 1:

TABLE 1. INDUCTOR SELECTION

BOOST FREQUENCY	INDUCTANCE
400kHz to 700kHz	10µH to 15µH
700kHz to 1MHz	6.8µH to 10µH
1MHz to 1.5MHz	4.7µH to 8.2µH
1.5MHz	3.3µH to 4.7µH

The inductor saturation current rating should be at least the figure provided by Equation 12:

$$I_L = \frac{1.35 \times V_{OUT} \times I_{LED}}{V_{IN}} \quad \text{(EQ. 12)}$$

Where:
I_L is the minimum inductor saturation current rating (A)
V_{OUT} is the maximum output voltage set by OVP (V)
I_{LED} is the sum of the channel currents (A)
VIN is the minimum input voltage (V)

If the calculation produces a current rating higher than the 3.15A maximum boost switch current limit, then a 3A inductor current rating is adequate.

For example, for a system using 4 LED channels with 30mA per channel and a maximum output voltage (OVP) of 24.53V with an input supply of 2.7V minimum:

$$I_L = \frac{1.35 \times 24.53 \times (4 \times 0.03)}{2.7} = 1.47A \quad \text{(EQ. 13)}$$

Output Capacitor

It is recommended that a 2.2µF to 3.3µF X5R/X7R or equivalent ceramic output capacitor is used.

Schottky Diode

The Schottky diode should be rated for at least the same forward current as the inductor, and for reverse voltage to at least the maximum output voltage, OVP.

Compensation

The ISL97691's boost regulator uses a current mode control architecture with a standardised external compensation network connected to the COMP pin. The component values shown in the Typical Application Circuit, Figure 1, on page 1 should be used. The network comprises a series RC of 12kΩ and 15nF also from COMP to GND.

Applications

Unused LED Channels

Connect unused LED channels to GND.

High Current Applications

Each channel of the ISL97691 supports 40mA continuous sink current. For applications that need higher current, multiple channels can be paralleled (Table 2).

TABLE 2. PARALLELING CHANNELS FOR HIGHER CURRENT

TOTAL CHANNELS	CHANNEL CURRENT	CHANNEL CONNECTIONS
4	40mA per channel	CH1, CH2, CH3, CH4
2	80mA per channel	{CH1 & CH2}, {CH3 & CH4}
1	160mA	{CH1 & CH2 & CH3 & CH4}

NOTE: PWMI_1 and PWMI_2 must driven together for total channels 1.

The example below shows CH1 and CH2 paralleled.

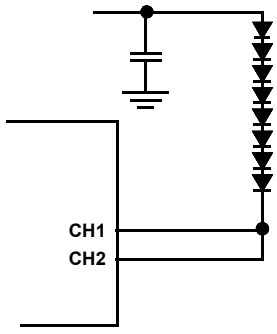

FIGURE 22.

PCB Layout Considerations

PCB Layout with TQFN Package

Great care is needed in designing a PC board for stable ISL97691 operation. As shown in the "Typical Application Circuit" on page 1, the separation of PGND and AGND is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors form high current flow in resistive PC board traces. PGND and AGND should be on the top and bottom layers respectively in the two layer PCB. A star ground connection should be formed by connecting the LED ground return and AGND pins to the thermal pad with vias (Figure 23). The ground connection should be into this ground net, on the top plane. The bottom plane then forms a quiet analog ground area that both shields components on the top plane, as well as providing easy access to all sensitive components. For example, the ground side of the ISET resistor can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be sized sufficiently large to dissipate the required power. For multi-layer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

Figure 24 shows the example of the PCB layout of ISL97691. This type of layout is particularly important for this type of product, resulting in high current flow in the main loop's traces. Careful attention should be focused in the following layout details:

1. Boost input capacitors (CIN), output capacitors (COUT), inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input, and output connected with low impedance and wide metal is very important to keep these nodes closely coupled.
2. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close to the VIN pin.
3. For optimum load regulation and true VOUT sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation.
4. The COMP network and the rest of the analog components (on ISET, FSW, etc.) should be referenced to AGND.
5. The heat of the chip is mainly dissipated through the exposed thermal pad so maximizing the copper area around is a good idea. A solid ground is always helpful for the thermal and EMI performance.
6. The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.

General Power PAD Design Considerations

Figure 23 shows an example of how to use vias to remove heat from the IC. We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad foot print with vias spaced such that the centre to centre spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

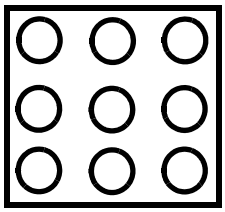

FIGURE 23. VIA PATTERN OF ISL97691 TQFN

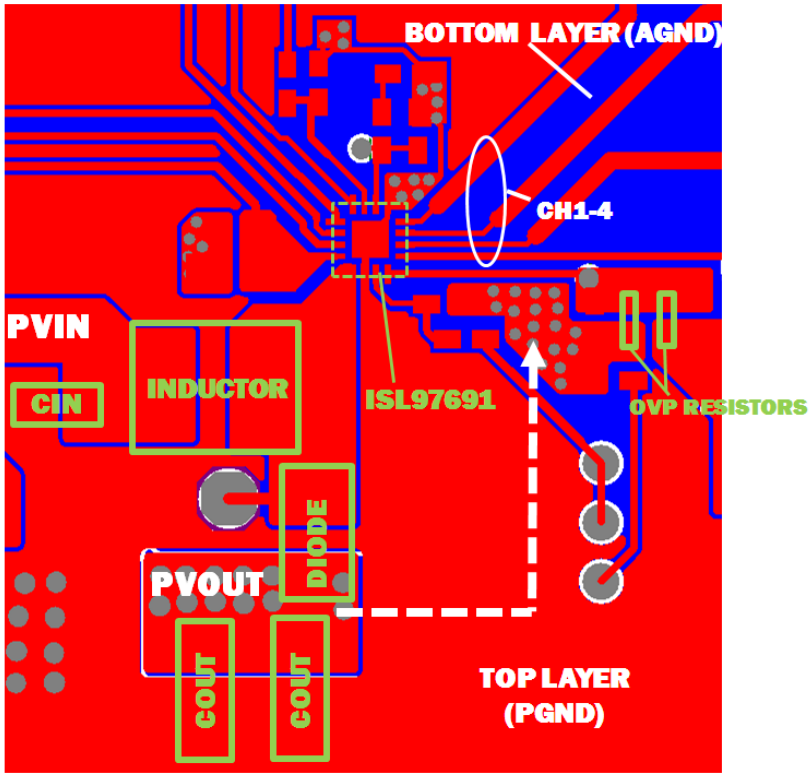

FIGURE 24. EXAMPLE OF PCB LAYOUT

Fault Protection and Monitoring

The ISL97691 features extensive protection functions to handle failure conditions automatically. Refer to Figure 15 and Table 3 for details of the fault protections.

The LED failure mode is either open or short circuit. An open circuit failure of an LED only results in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97691 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 3 for more details.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are above the short circuit protection threshold, nominally 8V (the action taken is described in Table 3).

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97691 monitors the current in each channel such that any string which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97691 reach the V_{OVP} limit, all channels which are not “good” will immediately be considered as “open circuit”.

Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel.

Undervoltage Lockout

If the input voltage falls below the V_{UVLO} level of ~2.15V, the ISL97691 will stop switching and be reset. Operation will restart only if the V_{IN} is back in the normal operating range.

Over-Temperature Protection (OTP)

The ISL97691 has an over-temperature protection threshold set to +150°C. If this threshold is reached, the boost stops switching and the channel output current sinks are switched off. The ISL97691 can be restarted by toggling V_{IN} to below the V_{UVLO} level of ~2.15V, then back up to the normal input voltage level.

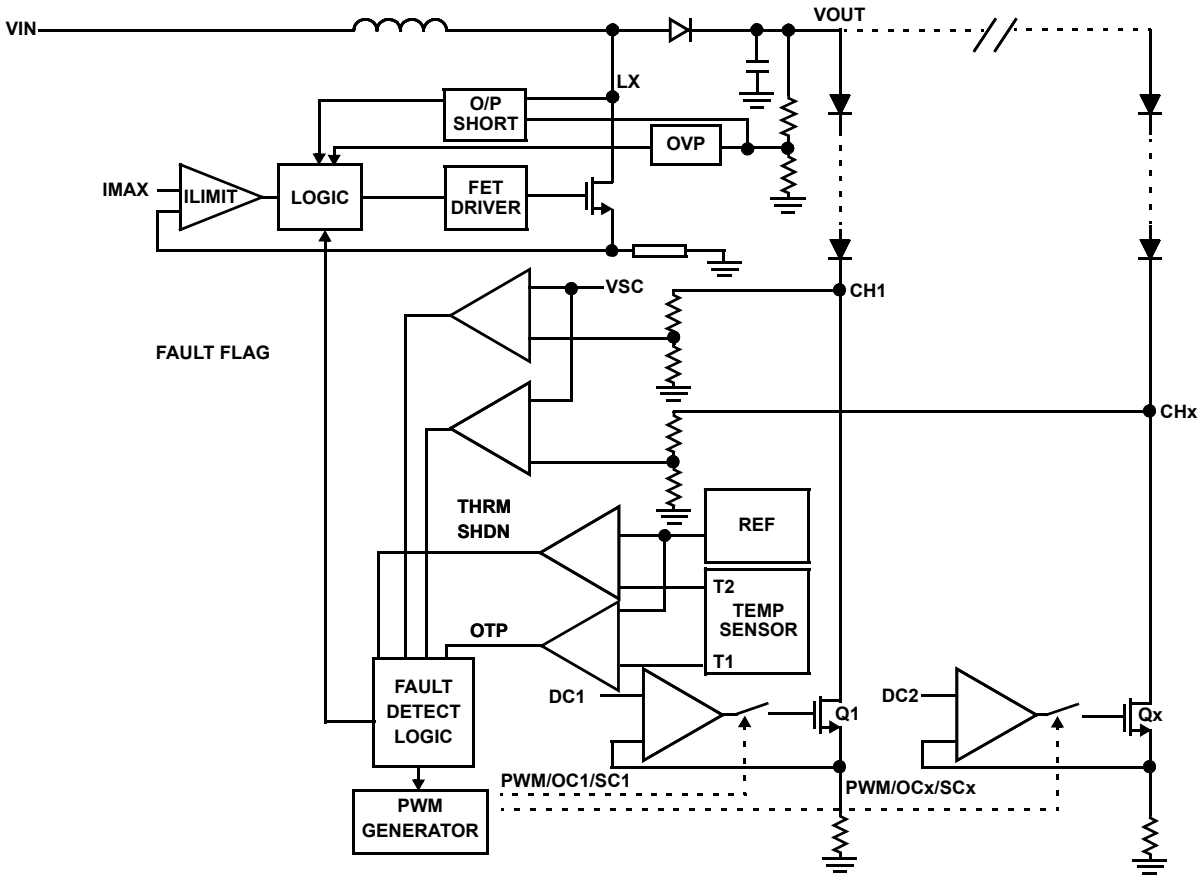

FIGURE 25. SIMPLIFIED FAULT PROTECTIONS

TABLE 3. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short Circuit	Over-Temperature Protection (OTP) not triggered, CH1 < 8V	CH1 ON and burns power	CH2 through CH4 Normal	Highest LED string V_F of CH2 - CH4
2	CH1 Short Circuit	OTP triggered	Boost converter and channels are shut down until V_{IN} is cycled		-
3	CH1 Short Circuit	OTP not triggered, CH1 > 8V	CH1 disabled after 190ms time-out	CH2 through CH4 Normal	Highest LED string V_F of CH2 - CH4
4	CH1 Open Circuit with infinite resistance	OTP not triggered, CH1 < 8V	V_{OUT} will ramp to OVP. CH1 will time-out after 190ms and switch off. V_{OUT} will then reduce to normal level	CH2 through CH4 Normal	Highest LED string V_F of CH2 - CH4
5	Output LED stack voltage too high	$V_{OUT} = V_{OVP}$	Any channel that is below the target current will time-out after 190ms while V_{OUT} is regulated at V_{OVP}, and V_{OUT} will then return to the normal regulation voltage required for other channels		Highest LED string V_F of CH1 - CH4

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 8, 2017	FN7840.2	Applied new header/footer. Added Related Literature on page 1. Updated Ordering Information notes. Added $V_{HEADROOM\_RANGE}$ spec to Electrical Specifications table. Added corresponding Note 11. In the Current Matching and Current Accuracy section - updated 2nd sentence in paragraph 2 for clarification. Updated About Intersil section.
November 26, 2012	FN7840.1	Updated Features on page 1. Removed EN from PWM_2 pin in Typical Application Circuit on page 1 and from the PWMI_2 in Block Diagram on page 2. Added “Operation with Input Voltage Greater than 5.5V” on page 12. Added Figure “LED DRIVER OPERATION WITH INPUT VOLTAGE UP TO 26V” on page 13.
		In “Absolute Maximum Ratings” on page 5, changed HBM from 2kV to 2.5kV. Changed CDM from 1kV to 2kV.
June 13, 2012	FN7840.0	Initial release.

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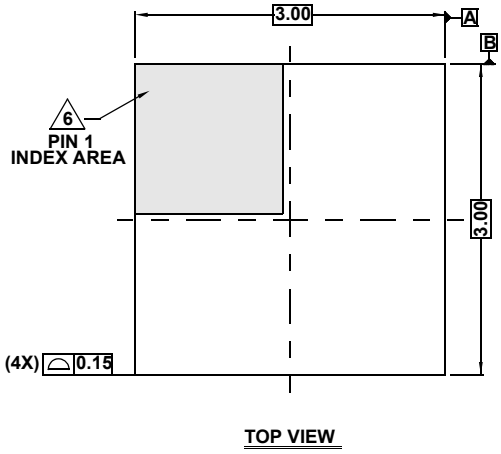
Package Outline Drawing

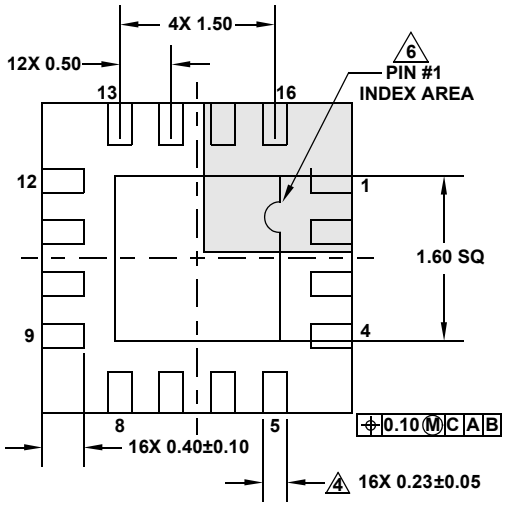
For the most recent package outline drawing, see L16.3x3D.

L16.3x3D

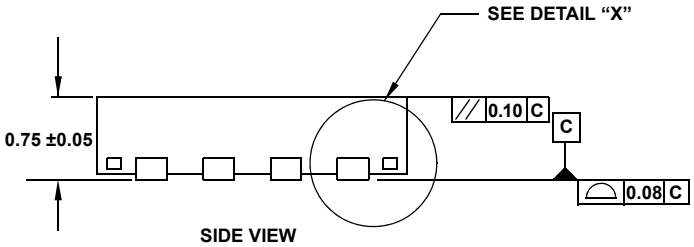
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



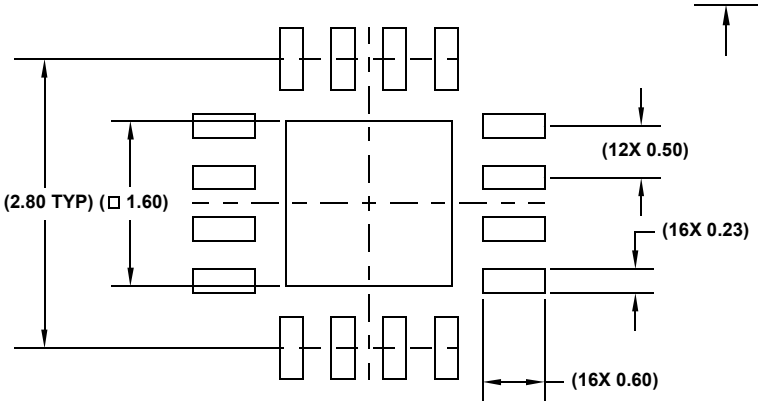
TOP VIEW



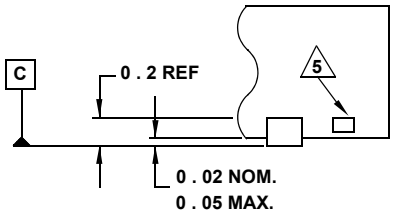
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

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