THE DATASHEET OF

ISL1221IUZ

ISL1221

Low Power RTC with Battery Backed SRAM and Event Detection

FN6316
Rev 1.00
July 15, 2010

The ISL1221 device is a low power real time clock with Event Detect and Time Stamp function, timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching with separate F_{OUT} output and 2 Bytes of battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

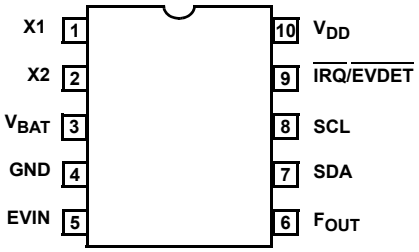
Ordering Information

PART NUMBER (Note)	PART MARKING	V_{DD} RANGE	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL1221IUZ	1221Z	2.7V to 5.5V	-40 to +85	10 Ld MSOP
ISL1221IUZ-T*	1221Z	2.7V to 5.5V	-40 to +85	10 Ld MSOP Tape and Reel

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL1221
(10 LD MSOP)
TOP VIEW



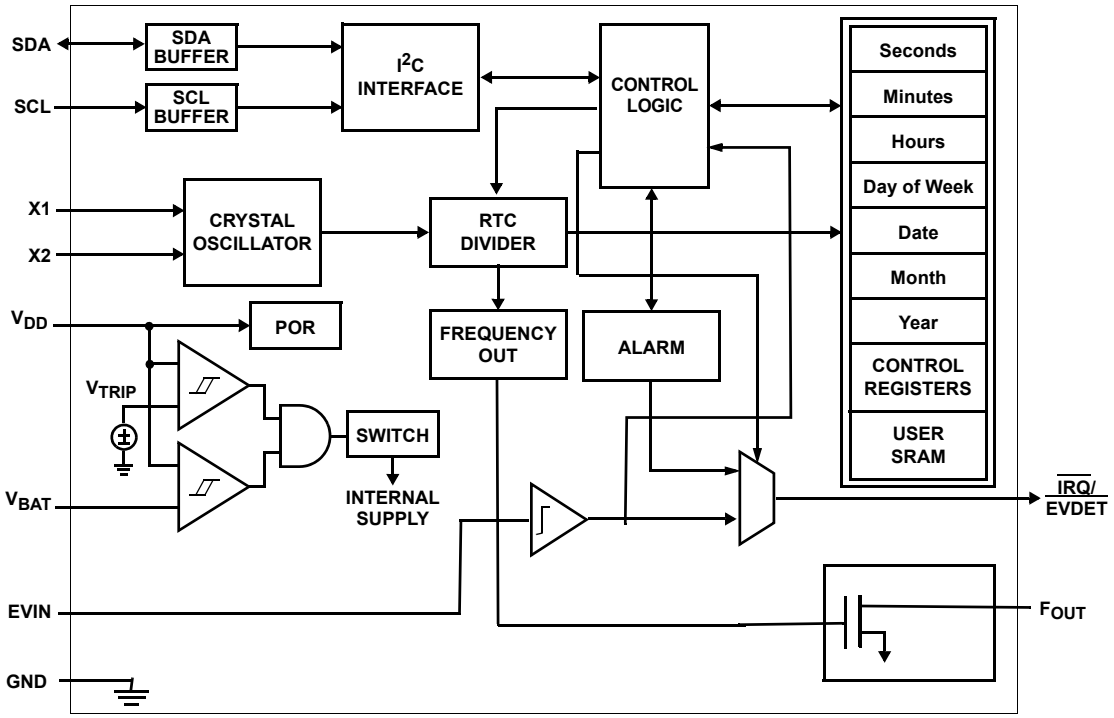
Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Day, Month, and Year
- Security and Event Functions
  - Tamper detection with Time Stamp in Normal and Battery Backed modes
  - Event Detection During Battery Backed or Normal Modes
  - Selectable Event Input Sampling Rates Allows Low Power Operation
  - Selectable Glitch Filter on Event Input Monitor
- Separate F_{OUT} pin with 15 Selectable Frequencies
- Single Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Super Cap
- Power Failure Detection
- On-Chip Oscillator Compensation
- 2 Bytes Battery-Backed User SRAM
- I^2C Interface
  - 400kHz Data Transfer Rate
- 400nA Battery Supply Current
- Small Package
  - 10 Ld MSOP
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- Set Top Box/Modem
- POS Equipment
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Test Meters/Fixtures
- Vending Machine Management
- Security and Anti Tampering Applications
  - Panel/Enclosure Status
  - Warranty Reporting
  - Time Stamping Applications
  - Patrol/Security Check (Fire or Light Equipment)
  - Automotive Applications

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	**X1.** The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	X2	**X2.** The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X2 should be left open when X1 is driven from external source.
3	V_{BAT}	**V_{BAT}.** This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
4	GND	**Ground**.
5	EVIN	**Event Input** (**EVIN**). The EVIN is an input pin that is used to detect an externally monitored event. When a high signal is present at the EVIN pin an “event” is detected.
6	F_{OUT}	**Frequency Output F_{OUT}**, Frequency output pin, 15 selectable frequencies. Open drain output.
7	SDA	**Serial Data** (**SDA**). SDA is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR’ed with other open drain or open collector outputs.
8	SCL	**Serial Clock** (**SCL**). The SCL input is used to clock all serial data into and out of the device.Open drain output.
9	$\overline{IRQ}$/$\overline{EVDET}$	**Interrupt ($\overline{IRQ}$)/Event Detect ($\overline{EVDET}$) Output.** Multi-functional pin that can be used as interrupt for Alarm and Event Detect. Open Drain Output.
10	V_{DD}	**V_{DD}.** Power supply.

Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{IRQ/EVDET}$ Pins (respect to ground) . . . . . -0.5V to 7.0V
Voltage on X1 and X2 Pins (respect to ground) . . . . . -0.5V to V_{DD} + 0.5 (V_{DD} Mode) -0.5V to V_{BAT} + 0.5 (V_{BAT} Mode)
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
ESD Rating (Human Body Model) . . . . . >2kV
ESD Rating (Machine Model . . . . . >175V
Output Current Sink (F_{OUT}, $\overline{IRQ}$ 3mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
10Ld MSOP Package	120

Moisture Sensitivity (see Technical Brief TB363) . . . . . Level 2

Recommended Operating Conditions

Ambient Temperature . . . . . -40°C to +85°C
V_{DD} Voltage . . . . . 2.7V to 5.5V
V_{BAT} Voltage . . . . . 1.8V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics – RTC

Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 5)	MAX (Note 9)	UNITS	NOTES
V_{DD}	Main Power Supply		2.7		5.5	V	
V_{BAT}	Battery Supply Voltage		1.8		5.5	V	
I_{DD1}	Supply Current	V_{DD} = 5V		2	6	µA	2, 3
		V_{DD} = 3V		1.2	4	µA	
I_{DD2}	Supply Current With I^2C Active	V_{DD} = 5V		40	120	µA	2, 3
I_{DD3}	Supply Current (Low Power Mode)	V_{DD} = 5V, LPMODE = 1		1.4	5	µA	2, 8
I_{BAT}	Battery Supply Current	V_{BAT} = 3V		400	950	nA	2
I_{BATLKG}	Battery Input Leakage	V_{DD} = 5.5V, V_{BAT} = 1.8V			100	nA	
I_{LI}	Input Leakage Current on SCL			100		nA	
I_{LO}	I/O Leakage Current on SDA			100		nA	
V_{TRIP}	V_{BAT} Mode Threshold		1.6	2.2	2.64	V	
$V_{TRIPHYS}$	V_{TRIP} Hysteresis		10	35	60	mV	
V_{BATHYS}	V_{BAT} Hysteresis		10	50	100	mV	
EVIN							
V_{IL}			-0.3		0.3 x V_{DD}	V	
V_{IH}			0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis			0.05 x V_{DD}			V	
I_{EVPU}	EVIN Pullup Current	V_{SUP} = 3V		1.5		µA	6
$\overline{IRQ/EVDET}$ and F_{OUT}							
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 3mA			0.4	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			0.4	V	
I_{LO}	Output Leakage Current	V_{DD} = 5.5V V_{OUT} = 5.5V		100	400	nA	

Power-Down Timing

Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 5)	MAX (Note 9)	UNITS	NOTES
$V_{DD\ SR-}$	V_{DD} Negative Slew rate				10	V/ms	4

I^2C Interface Specifications Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP (Note 5)	MAX (Note 9)	UNITS	NOTES
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05 x V_{DD}			V	
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} = 5V, I_{OL} = 3mA			0.4	V	
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL falLing Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}.	20 + 0.1 x Cb		300	ns	7
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}.	20 + 0.1 x Cb		300	ns	7
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	7

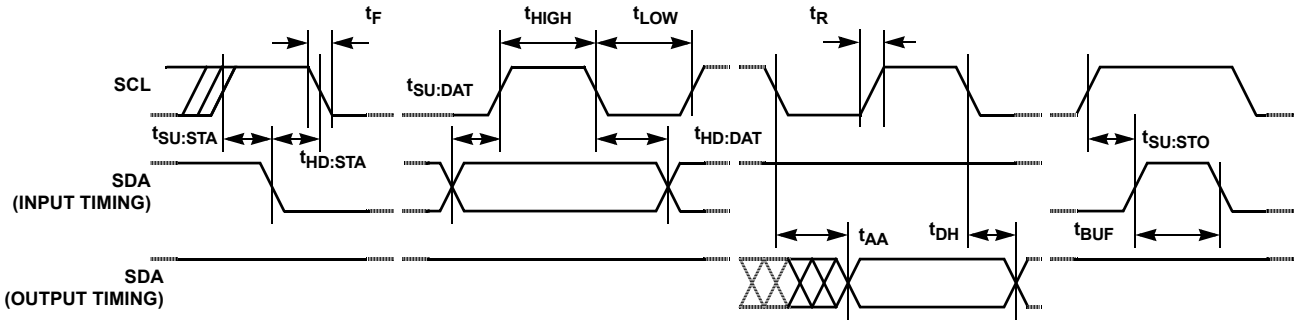
I^2C Interface Specifications Test Conditions: V_{DD} = +2.7 to +5.5V, Temperature = -40°C to +85°C, unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP (Note 5)	MAX (Note 9)	UNITS	NOTES
Rpu	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ	7

NOTES:

2. $\overline{IRQ}$ and F_{OUT} and $\overline{EVDET}$ Inactive.
3. LPMODE = 0 (default).
4. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
5. Typical values are for T = 25°C and 3.3V supply voltage.
6. $V_{SUP} = V_{DD}$ if in V_{DD} Mode, $V_{SUP} = V_{BAT}$ if in V_{BAT} Mode.
7. These are I^2C specific parameters and are not directly tested, however they are used during device testing to validate device specification.
8. A write to register 08h should only be done if $V_{DD} > V_{BAT}$, otherwise the device will be unable to communicate using I^2C.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs. SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Typical Performance Curves Temperature is +25°C unless otherwise specified

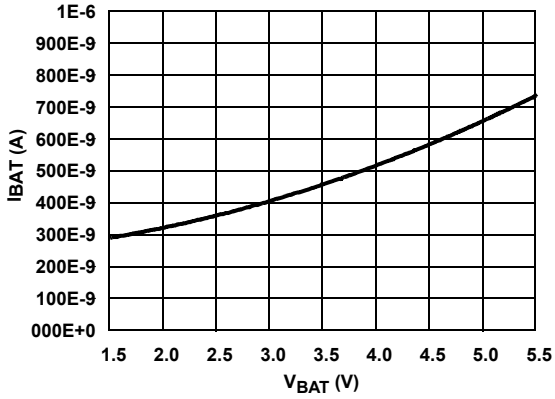


FIGURE 1. I_{BAT} vs V_{BAT}

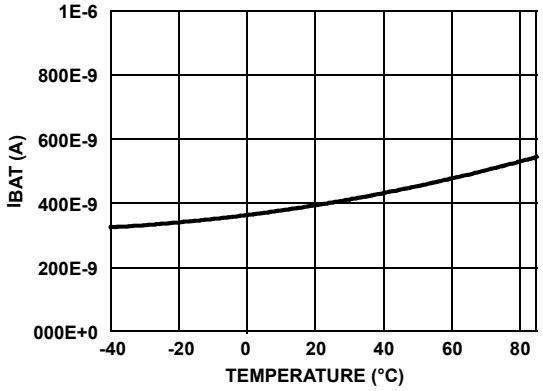


FIGURE 2. I_{BAT} vs TEMPERATURE AT V_{BAT} = 3V

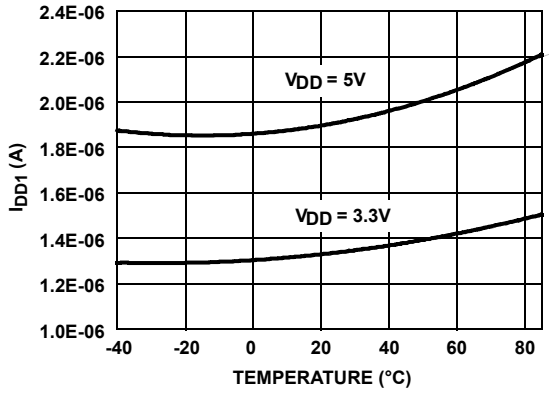


FIGURE 3. I_{DD1} vs TEMPERATURE

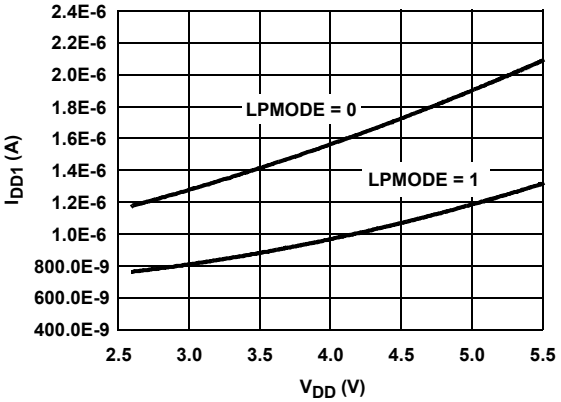


FIGURE 4. I_{DD1} vs V_{DD} WITH LPMODE ON AND OFF

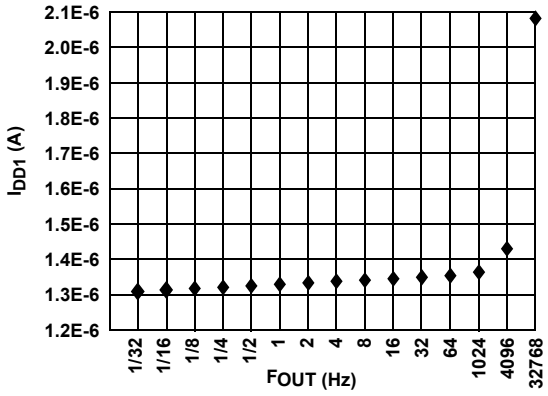


FIGURE 5. I_{DD1} vs F_{OUT} AT V_{DD} = 3.3V

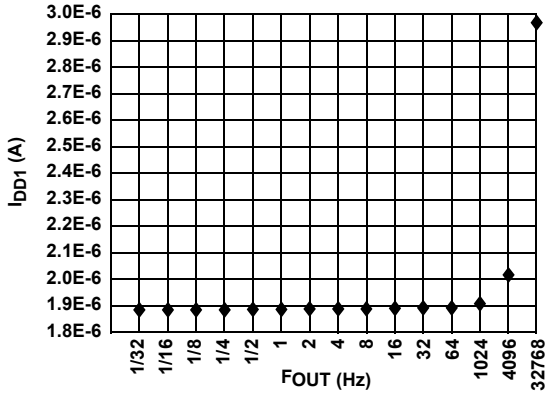


FIGURE 6. I_{DD1} vs F_{OUT} AT V_{DD} = 5V

Typical Performance Curves Temperature is +25°C unless otherwise specified **(Continued)**

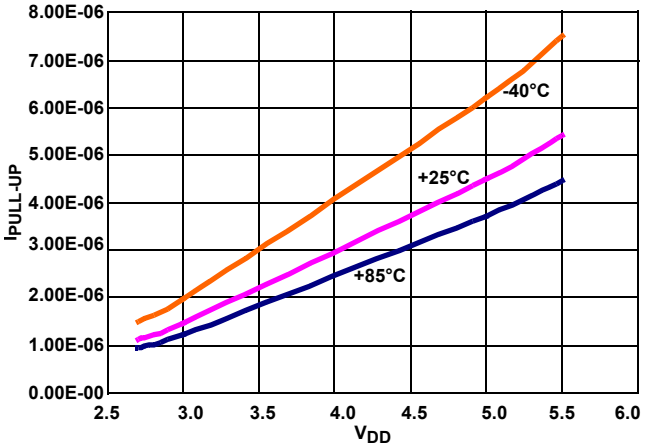


FIGURE 7. EVIN I_{PULLUP} vs V_{DD}

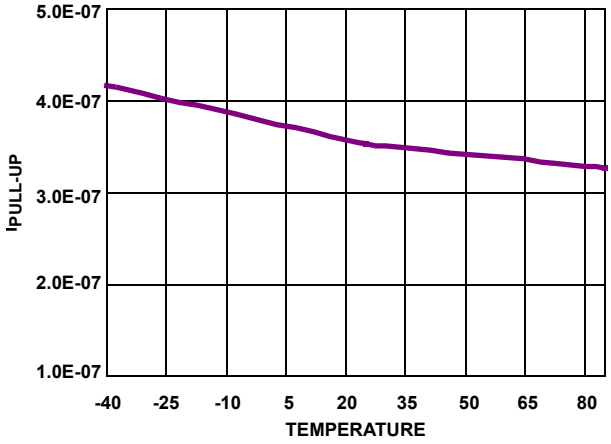


FIGURE 8. I_{PULLUP} vs TEMPERATURE AT V_{BAT} = 1.8V

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

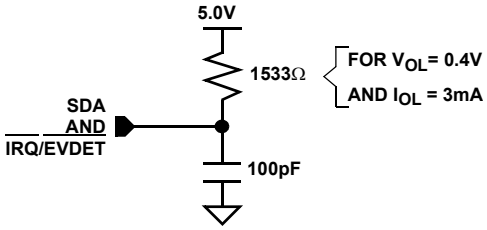


FIGURE 9. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL1221 device is a low power Real Time Clock with Security and Event function, Time Stamp in both normal and battery modes, timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching, and battery-backed user SRAM.

The Event Detection function can be used for tamper detection, security or other chassis or generic system monitoring. Upon a valid event detection, the ISL1221 sets the Event Detection bit (EVT bit) in the status register, stores time stamp information on board memory, and, can optionally: 1) Issue an Event Output signal (EVDET pin), 2) At the time the event occurred, stop the RTC registers from advancing. The event monitor and time stamp functions in both main V_{DD} and battery back up modes. The event monitor can also be configured for various input detection rates to optimize power consumption for the application. In addition, the Event Monitor pin (EVIN) has a selectable glitch filter to avoid switch de-bouncing.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL1221's alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the IRQ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or SuperCap with automatic switchover from V_{DD} to V_{BAT}. The entire ISL1221 device is fully operational from V_{DD} = 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational in battery backup mode down to 1.8V (Standby Mode).

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL1221 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over temperature either during manufacturing or with an external temperature sensor and microcontroller for active compensation. The device can also be driven directly from a 32.768kHz source at pin X1.

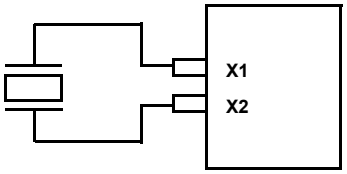


FIGURE 10. RECOMMENDED CRYSTAL CONNECTION

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin can be connected to a battery, a Super Cap or tied to ground if not used.

EVIN (Event Input)

The EVIN pin is an input that is used to detect an externally monitored event. When a high signal is present at the EVIN pin, an “event” is detected. This input may be used for various monitoring functions, such as the opening of a detection switch on a chassis or door. The event detection circuit can be user enabled or disabled (see EVEN bit) and provides the option to be operational in battery backup modes (see EVBATB bit). When the event detection is disabled the EVIN pin is gated OFF. See“Functional Description” on page 8 for more details.

F_{OUT} (Frequency Output)

The F_{OUT} pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus. It is an open drain active low output. When not used, the output is high.

$\overline{IRQ}/\overline{EVDET}$ (Alarm/Event Detect Output)

This dual function pin can be used as an interrupt alarm or event detect output pin. Checking the status register will show the type of interrupt, Alarm or Event Detect.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.
- The output will go low when an event is detected at the EVIN pin. If the event detection function is enabled, the $\overline{IRQ}/\overline{EVDET}$ output will go low and stay low until the EVT bit is cleared (see the EVIN pin description in the “Pin Description” on page 7).

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V_{BAT} pin is activated to minimize power consumption.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds. It is disabled when the backup power supply on the V_{BAT} pin is activated.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from V_{DD}=2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL1221 for up to 10 years. Another option is to use a Super Cap for applications where V_{DD} is interrupted for up to a month. See the “Application Section” on page 20 for more information.

Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

Condition 1:

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL1221 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

Condition 1:

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

Condition 2:

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 11 and 12.

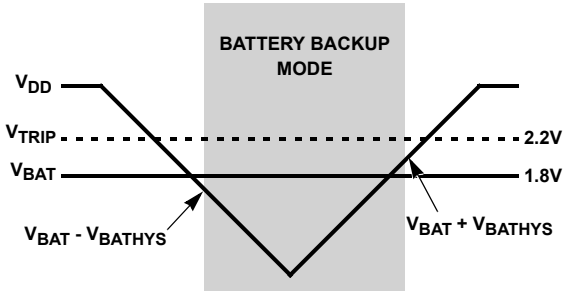


FIGURE 11. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

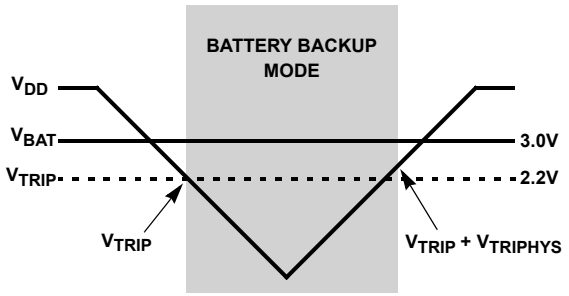


FIGURE 12. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

The I^2C bus is deactivated in battery backup mode to provide lower power. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL1221 are active during battery backup mode unless disabled via the control register. The User SRAM is operational in battery backup mode down to 1.8V.

Power Failure Detection

The ISL1221 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both V_{DD} and V_{BAT}).

Low Power Mode

The normal power switching of the ISL1221 is designed to switch into battery backup mode only if the V_{DD} power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs. V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated via the LPMODE bit in the control and status registers.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq$ 3.0V, and when there is a finite I-R voltage drop in the V_{DD} line.

InterSeal™ Battery Saver

The ISL1221 has the InterSeal™ Battery Saver which prevents initial battery current drain before it is first used. For example, battery-backed RTCs are commonly packaged on a board with a battery connected. In order to preserve battery life, the ISL1221 will not draw any power from the battery source until after the device is first powered up from the V_{DD} source. Thereafter, the device will switchover to battery backup mode whenever V_{DD} power is lost.

Event/Tamper Monitor and Detection

The ISL1221 provides an event detection, time stamp and alarm function to be used in a wide variety of applications ranging from security, warranty monitoring, data collection and recording.

The tamper detect input pin, EVIN, can be used as a event or tamper detection input of an external switch (mechanical or electronic). When the EVIN pin is a valid HIGH, the ISL1221 sets the EVT bit in the status register and, can optionally:

1. Issue an Event output signal ($\overline{\text{EVDET}}$ pin) and store time stamp information in on board SRAM (second, minute, hour, date, month and year)
2. At the time event occurred, stop the RTC registers from advancing.

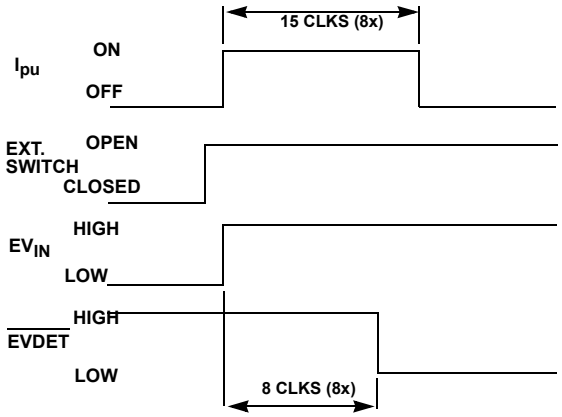
To allow for flexibility of external switches used at the EVIN pin, the internal pull-up (~1µA in full on mode) can be disabled/enabled. This will allow more flexibility depending on the capacitive and resistive loading at the EVIN pin.

A noise filter option is also provided for the event monitor circuit. The EVIN pin has a time based filter where the EVIN signal must be stable for a period of time to trigger a valid detection. The time hysteresis filter can vary from 0, 3.9ms, 15.2ms or 31.25ms.

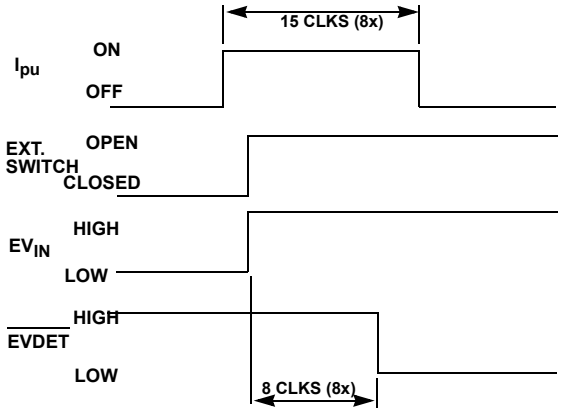
For low power applications the event monitor can be sampled at a user selectable rate. The EVIN pin can be always ON or periodically sampled with a frequency of 1/4, 1 or 2Hz.

Event Detect Timing Diagram with Sampling Mode Enabled

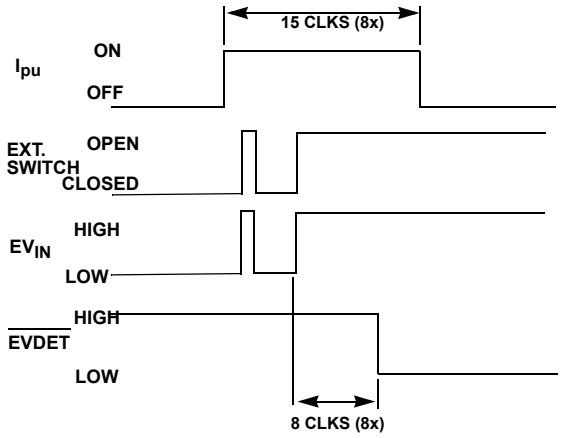
Case 1, Switch Opened Before I_{pu}



Case 2, Switch Opened After I_{pu}



Case 3, Switch Bounced



The ISL1221 can operate independently or in conjunction with a microcontroller for low power operation modes or in battery backup modes.

The event detection and time stamp circuits operate in either main V_{DD} power or battery backup mode.

Users have the option to connect EVIN (see EVINEB bit) to an internal pull-up current source that operates at 1µA (always on mode), which can drop to 400nA in battery backup mode. User selectable event sampling modes are also available which will effectively reduce power consumption with 1/4-Hz, 1-Hz and 2-Hz sample detection rates. The EVIN input is pulsed ON/OFF when in sampling mode for power savings advantages (see Table 1, 2, 3, and 4).

The EVIN also has a user selectable time based hysteresis filter (see EHYS bits) to implement switch de-bouncing during an event detection. The EVIN signal must be high for the duration of the selected time period. The time periods available are 0 times delay (no time based hysteresis) to 3.9ms, 15.625ms or 31.25ms (see Table 1, 2, 3, and 4).

TABLE 1. ΔI_{DD} (V_{DD} = 3V, t_{HYS} = 3.9ms)

f_{SMP}	DELTA I_{DD}
1/4Hz	20.5nA
1Hz	82nA
2Hz	164nA

TABLE 2. ΔI_{DD} (V_{DD} = 5.0V, t_{HYS} = 3.9ms)

f_{SMP}	DELTA I_{DD}
1/4Hz	65.8nA
1Hz	263.3nA
2Hz	526.5nA

TABLE 3. ΔI_{DD} (V_{DD} = 3.0V, t_{HYS} = 15.625ms)

f_{SMP}	DELTA I_{DD}
1/4Hz	82nA
1Hz	328nA
2Hz	656.3nA

TABLE 4. ΔI_{DD} (V_{DD} = 5.0V, t_{HYS} = 15.625ms)

f_{SMP}	DELTA I_{DD}
1/4Hz	264nA
1Hz	1.05µA
2Hz	2.1µA

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL1221 powers up after the loss of both V_{DD} and V_{BAT}, the clock will not begin incrementing until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer. The ISL1221 provides on-chip crystal compensation networks to adjust load capacitance to tune oscillator frequency from -94ppm to +140ppm. For more detailed information see the "Application Section" on page 20.

Single Event and Interrupt

The alarm mode is enabled via the ALME bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, an $\overline{IRQ}/\overline{EVDET}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}/\overline{EVDET}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to "1".

The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see "Auto Reset Enable Bit (ARST)" on page 14).

The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, please see the "Alarm Registers" on page 16.

Frequency Output Mode

The ISL1221 has the option to provide a frequency output signal using the F_{OUT} pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 0 to 32kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit.

General Purpose User SRAM

The ISL1221 provides 2 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the I^2C bus is disabled in battery backup mode.

I^2C Serial Interface

The ISL1221 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bidirectional data signal (SDA) and a clock signal (SCL).

Oscillator Compensation

The ISL1221 provides the option of timing correction due to temperature variation of the crystal oscillator for either manufacturing calibration or active calibration. The total possible compensation is typically -94ppm to +140ppm. Two compensation mechanisms that are available are as follows:

1. An analog trimming (ATR) register that can be used to adjust individual on-chip digital capacitors for oscillator capacitance trimming. The individual digital capacitor is selectable from a range of 9pF to 40.5pF (based upon 32.758kHz). This translates to a calculated compensation of approximately -34ppm to +80ppm. (see "Analog Trimming Register" on page 15).
2. A digital trimming register (DTR) that can be used to adjust the timing counter by ±60ppm. (see "Digital Trimming Register (DTR <2:0>)" on page 16).

Also provided is the ability to adjust the crystal capacitance when the ISL1221 switches from V_{DD} to battery backup mode. (see "Battery Mode ATR Selection (BMATR <1:0>)" on page 15 for more details).

Register Descriptions

The battery-backed registers are accessible following a slave byte of "1101111x" and reads or writes to addresses [00h:19h]. The defined addresses and default values are described in the Table 1. Address 09h is not used. Reads or writes to 09h will not affect operation of the device but should be avoided.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 5 sections. These are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (5 bytes): Address 07h to 0Bh.
3. Alarm (6 bytes): Address 0Ch to 11h.
4. User SRAM (2 bytes): Address 12h to 13h.
5. Time Stamp (6 bytes): Address 14h to 19h

There are no addresses above 19h.

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 4 of address 07h) is set to "1". **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register

location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

TABLE 5. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0-59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0-59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0-23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1-31	00h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1-12	00h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0-99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0-6	00h
07h	Control and Status	SR	ARST	XTOSCB	Reserved	WRTC	EVT	ALM	BAT	RTCF	N/A	01h
08h		INT	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0	N/A	00h
09h		EV	EVIENB	EVBATB	RTCHLT	EVEN	EHYS1	EHYS0	ESMP1	ESMP0	N/A	00h
0Ah		ATR	BMATR1	BMATR0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0	N/A	00h
0Bh		DTR	Reserved					DTR2	DTR1	DTR0	N/A	00h
0Ch	Alarm	SCA	ESCA	ASC22	ASC21	ASC20	ASC13	ASC12	ASC11	ASC10	00-59	00h
0Dh		MNA	EMNA	AMN22	AMN21	AMN20	AMN13	AMN12	AMN11	AMN10	00-59	00h
0Eh		HRA	EHRA	0	AHR21	AHR20	AHR13	AHR12	AHR11	AHR10	0-23	00h
0Fh		DTA	EDTA	0	ADT21	ADT20	ADT13	ADT12	ADT11	ADT10	1-31	00h
10h		MOA	EMOA	0	0	AMO20	AMO13	AMO12	AMO11	AMO10	1-12	00h
11h		DWA	EDWA	0	0	0	0	ADW12	ADW11	ADW10	0-6	00h
12h	User	USR1	USR17	USR16	USR15	USR14	USR13	USR12	USR11	USR10	N/A	00h
13h		USR2	USR27	USR26	USR25	USR24	USR23	USR22	USR21	USR20	N/A	00h
14h	Time Stamp	SCT	0	SCT22	SCT21	SCT20	SCT13	SCT12	SCT11	SCT10	00-59	00h
15h		MNT	0	MNT22	MNT21	MNT20	MNT13	MNT12	MNT11	MNT10	00-59	00h
16h		HRT	MILT	0	HRT21	HRT20	HRT13	HRT12	HRT11	HRT10	0-23	00h
17h		DTT	0	0	DTT21	DTT20	DTT13	DTT12	DTT11	DTT10	1-31	00h
18h		MOT	0	0	0	MOT20	MOT13	MOT12	MOT11	MOT10	1-12	00h
19h		YRT	YRT23	YRT22	YRT21	YRT20	YRT13	YRT12	YRT11	YRT10	0-99	00h

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL1221 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure, battery mode, alarm trigger, event detection, write protection of clock counter, crystal oscillator enable and auto reset of status bits.

TABLE 6. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	ARST	XTOSCB	reserved	WRTC	EVT	ALM	BAT	RTCF
Default	0	0	0	0	0	0	0	0

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL1221 internally) when the device powers up after having lost all power to the device. The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

BATTERY BIT (BAT)

This bit is set to a “1” when the device enters battery backup mode. This bit can be reset either manually by the user or automatically reset by enabling the auto-reset bit (see “Auto Reset Enable Bit (ARST)” on page 14). A write to this bit in the SR can only set it to “0”, not “1”.

ALARM BIT (ALM)

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”.

NOTE: An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

EVENT DETECT BIT (EVT)

The event detect bit indicates status of the event input pin (EVIN). When the Event Detect function is enabled and the EVIN pin is triggered, the EVT bit is set to “1” to indicate a detection of an event, and the Time Stamp Register records the current RTC time. A write to this bit in the SR can only set it to “0” not “1”.

When a HIGH signal is present at the EVIN pin (or a LOW to HIGH transition), an “event” is detected. On detection the EVT bit is set HIGH, the open drain $\overline{\text{EVDET}}$ pin is asserted (pulled LOW), and the RTC time is recorded in the Time Stamp registers. The EVT bit will be reset to LOW:

- When the EVT bit is set to 0 with a Status Register write
- When there is a read from the Status Register, with the ARST bit set to “1” (auto-reset enabled).

If the EVT bit has not been cleared, only the initial (first occurrence) Timestamp is retained in the Timestamp register, subsequent triggers of the EVIN pin will not record new timestamps. If the EVT bit is cleared to “0”, the Timestamp register will record the time of the next event went the EVIN pin is triggered.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

CRYSTAL OSCILLATOR ENABLE BIT (XTOSCB)

This bit enables/disables the internal crystal oscillator. When the XTOSCB is set to “1”, the oscillator is disabled, and the X1 pin allows for an external 32kHz signal to drive the RTC. The XTOSCB bit is set to “0” on power up.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the BAT and ALM, EVT status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the Status Register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the BAT, ALM, and EVT bits.

INTERRUPT CONTROL REGISTER (INT)

TABLE 7. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	IM	ALME	LPMODE	FOBATB	FO3	FO2	FO1	FO0
Default	0	0	0	0	0	0	0	0

FREQUENCY OUT CONTROL BITS (FO <3:0>)

These bits enable/disable the frequency output function and select the output frequency at the F_{OUT} pin. See Table 8 for frequency selection.

TABLE 8. FREQUENCY SELECTION OF F_{OUT} PIN

FREQUENCY, F_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the F_{OUT} pin during battery backup mode (i.e. V_{BAT} power source active). When the FOBATB is set to “1” the F_{OUT} pin is disabled during battery backup mode. When the FOBATB is cleared to “0”, the F_{OUT} pin is enabled during battery backup mode. The F_{OUT} pin is open drain configuration, and when used in battery backup mode requires a pull up resistor to VBAT.

LOW POWER MODE BIT (LPMODE)

This bit enables/disables low power mode. With LPMODE = “0”, the device will be in normal mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$ and $V_{DD} < V_{TRIP}$. With LPMODE = “1”, the device will be in low power mode and the V_{BAT} supply will be used when $V_{DD} < V_{BAT} - V_{BATHYS}$. There is a supply current saving of about 600nA when using LPMODE = “1” with V_{DD} = 5V. (See Typical Performance Curves: I_{DD} vs V_{DD} with LPMODE ON & OFF.)

It should be noted that any writes to the LPMODE bit that may put the device into Low Power Mode should be avoided if $V_{DD}<V_{BAT}$, as the device will no longer communicate over the I^2C interface (until V_{DD} rises above V_{BAT}).

ALARM ENABLE BIT (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to “1”, the alarm function is enabled. When the ALME is cleared to “0”, the alarm function is disabled. The alarm function can operate in either a single event alarm or a periodic interrupt alarm (see “Interrupt/Alarm Mode Bit (IM)” on page 14).

NOTE: When the frequency output mode is enabled, the alarm function is disabled.

INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}/\overline{EVDET}$ pin when the RTC is triggered by the alarm as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ}/\overline{EVDET}$ pin will be tied low until the ALM status bit is cleared to “0”.

TABLE 9.

IM BIT	INTERRUPT/ALARM FREQUENCY
0	Single Time Event Set By Alarm
1	Repetitive/Recurring Time Event Set By Alarm

EVENT DETECTION REGISTER (EV)

The ISL1221 provides an easy to use event and tamper detection circuit. The Event Detection Register configures the functionality of the event detection circuits.

EVENT INPUT SAMPLING SELECTION BITS (ESMP<1:0>)

These two bits select the rate of sampling of the EVIN pin to trigger an event detection. For example, a 2Hz sampling rate would configure the ISL1221 to check the status of the EV pin twice a second. Slower sampling significantly reduces the supply current drain.

TABLE 10.

ESMP1	ESMP0	EVENT SAMPLING RATE
0	0	Always ON

TABLE 10.

ESMP1	ESMP0	EVENT SAMPLING RATE
0	1	2Hz
1	0	1Hz
1	1	1/4Hz

NOTE: In order to use the sampling mode time-based hysteresis must be activated. See Table 11.

EVENT INPUT TIME BASE HYSTERESIS SELECTION BITS (EHYS<1:0>)

These two bits select the time base hysteresis of the EVIN pin to filter bouncing or noise of external event detection circuits. The time filter can be set between 0 to 31.25ms.

TABLE 11.

EHYS1	EHYS0	TIME BASE HYSTERESIS
0	0	0 (pull-up always on)
0	1	3.9ms
1	0	15.625ms
1	1	31.25ms

EVENT DETECT ENABLE BIT (EVEN)

This bit enables/disables the Event Detect function of the ISL1221. When this bit is set to “1”, the Event Detect and Time Stamp are active. When this bit is cleared to “0”, the Event Detect and Time Stamp are disabled. Only the first Event is Time Stamped in a series of Events between Event resets (see EVT bit in the Status Register).

RTC HALT ON EVENT DETECT BIT (RTCHLT)

This bit sets the RTC registers to continue or halt counting upon an Event Detect triggered by the EV pin. The time keeping function will cease when RTCHLT is set to “1”, the RTC will discontinue incrementing if an event is detected. Counting will resume when there is a valid write to the RTC registers (i.e. time set). The RTCHLT is cleared to “0” after the write to the RTC registers.

Note: This function requires that the event detection is enabled (see EVEN bit).

EVENT OUTPUT IN BATTERY MODE ENABLE BIT (EVBATB)

This bit enables/disables the $\overline{\text{EVDET}}$ pin during battery backup mode (i.e. V_{BAT} pin supply ON). When the EVBATB is set to “1”, the Event Detect Output is disabled in battery backup mode. When the EVBATB is cleared to “0”, the Event Detect output is enabled in battery backup mode.This feature can be used to save power during battery mode.

EVENT CURRENT SOURCE ENABLE BIT (EVIENB)

This bit enables/disables the internal pullup current source used for the EVIN pin. When the EVIENB bit is set to “1”, the pullup current source is always disabled. When the EVIENB bit is cleared to “0”, the pullup current source is enabled (current source is approximately 1µA).

Analog Trimming Register

ANALOG TRIMMING REGISTER (ATR<5:0>)

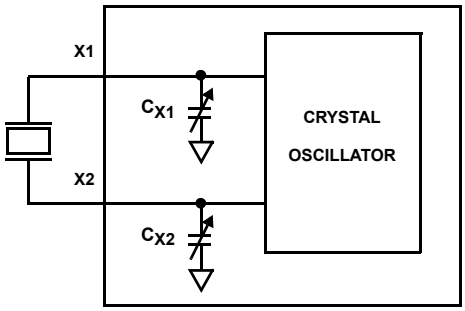


FIGURE 13. DIAGRAM OF ATR

Six analog trimming bits, **ATR0** to **ATR5**, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34 to +80ppm to the nominal frequency compensation. The combination of analog and digital trimming can give up to -94 to +140ppm of total adjustment.

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 13). The value of C_{X1} and C_{X2} is given by the following formula in Equation 1.

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)\text{pF} \quad \text{(EQ. 1)}$$

The effective series load capacitance is the combination of C_{X1} and C_{X2}:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)\text{pF}$$

For example, C_{LOAD}(ATR=00000) = 12.5pF, C_{LOAD}(ATR=100000) = 4.5pF, and C_{LOAD}(ATR=011111) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

BATTERY MODE ATR SELECTION (BMATR <1:0>)

Since the accuracy of the crystal oscillator is dependent on the V_{DD}/V_{BAT} operation, the ISL1221 provides the capability to

adjust the capacitance between V_{DD} and V_{BAT} when the device switches between power sources.

TABLE 12.

BMATR1	BMATR0	DELTA CAPACITANCE (C_{BAT} TO C_{VDD})
0	0	0pF
0	1	-0.5pF (≈ +2ppm)
1	0	+0.5pF (≈ -2ppm)
1	1	+1pF (≈ -4ppm)

DIGITAL TRIMMING REGISTER (DTR <2:0>)

The digital trimming bits DTR0, DTR1, and DTR2 adjust the average number of counts per second and average the ppm error to achieve better accuracy.

- DTR2 is a sign bit. DTR2 = “0” means frequency compensation is >0. DTR2 = “1” means frequency compensation is <0.
- DTR1 and DTR0 are both scale bits. DTR1 gives 40ppm adjustment and DTR0 gives 20ppm adjustment.

A range from -60ppm to +60ppm can be represented by using these three bits (Table 13).

TABLE 13. DIGITAL TRIMMING REGISTERS

DTR REGISTER			ESTIMATED FREQUENCY PPM
DTR2	DTR1	DTR0	
0	0	0	0 (default)
0	0	1	+20
0	1	0	+40
0	1	1	+60
1	0	0	0
1	0	1	-20
1	1	0	-40
1	1	1	-60

Alarm Registers

Addresses [0Ch to 11h]

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the ALME bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
- **Interrupt Mode** is enabled by setting the ALME bit to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear an alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to 1 (address 07h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1 – Alarm set with single interrupt (IM = “0”)

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm registers as follows:

ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also the ALME bit must be set as follows:

CONTROL REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
INT	0	1	x	x	0	0	0	0	x0h	Enable Alarm

Note: xx indicate other control bits

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to “1” and also bringing the $\overline{IRQ}$ output low.

Example 2 – Pulsed interrupt once per minute (IM = “1”)

Interrupts at one minute intervals when the seconds register is at 30 seconds.

A. Set Alarm registers as follows:

ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA	0	0	0	0	0	0	0	0	00h	Date disabled
MOA	0	0	0	0	0	0	0	0	00h	Month disabled
DWA	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	1	1	x	x	0	0	0	0	x0h	Enable Alarm and Int Mode

Note: xx indicate other control bits

Once the registers are set, the following waveform will be seen at $\overline{IRQ}$-:

Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared.

User Registers

Addresses [12h to 13h]

These registers are 2 bytes of battery-backed user memory storage.

Time Stamp Registers

Addresses [14h to 19h]

These registers contain the time stamp information in a similar format to the RTC registers. When a valid Event is triggered at the EVIN pin (low to high transition), these registers record the values from the RTC registers. At the same time the EVT bit is set and the $\overline{EVDET}$- pin changes state (if it is enabled). The six registers include second, minute, hour, date, month and year of the event. Day of week is not recorded as it is not normally required and is arbitrarily set.

Only the first Event in a series of events is time stamped, all subsequent events are ignored. The current time stamp is retained until the EVT bit is cleared and the next Event occurs (EVIN pin is triggered). The contents of these registers are cleared only after full power cycling.

I^2C Serial Interface

The ISL1221 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL1221 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 14). On power up of the ISL1221, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL1221 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 14). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 14). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 15).

The ISL1221 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL1221 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

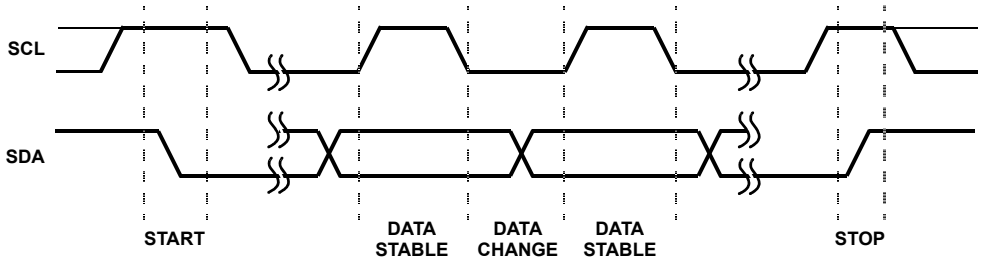


FIGURE 14. VALID DATA CHANGES, START AND STOP CONDITIONS

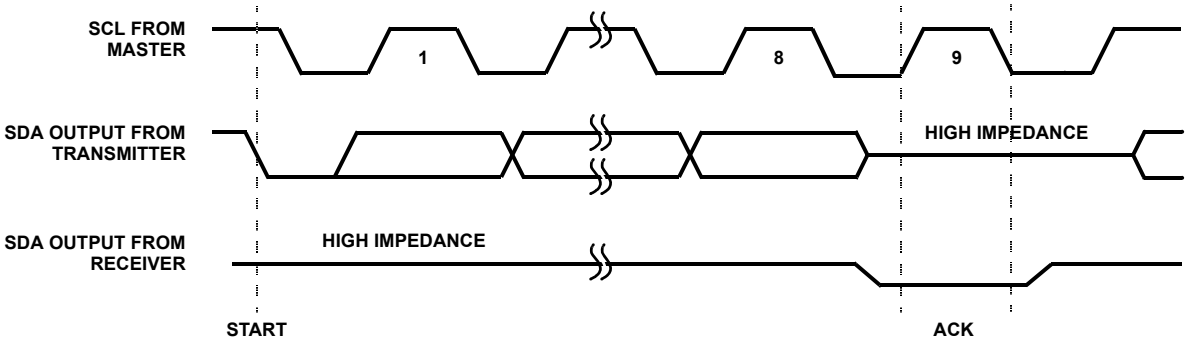


FIGURE 15. ACKNOWLEDGE RESPONSE FROM RECEIVER

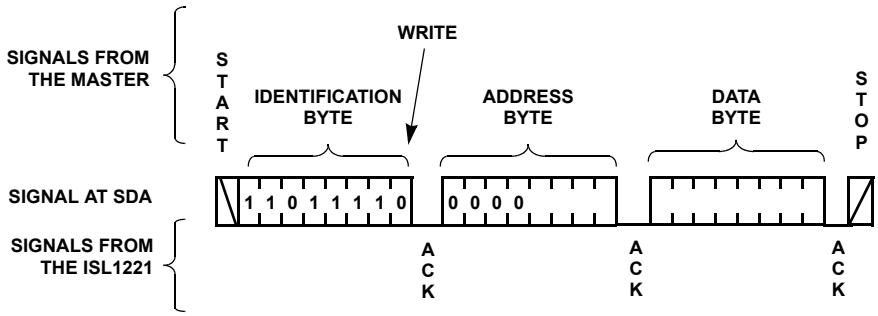


FIGURE 16. BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111”. Slave bits “1101” access the register. Slave bits “111” specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (Refer to Figure 17).

After loading the entire Slave Address Byte from the SDA bus, the ISL1221 compares the device identifier and device select bits with “1101111”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 0h, so a current address read of the CCR array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 18.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Clock/Control Registers, the slave byte must be “1101111x” in both places.

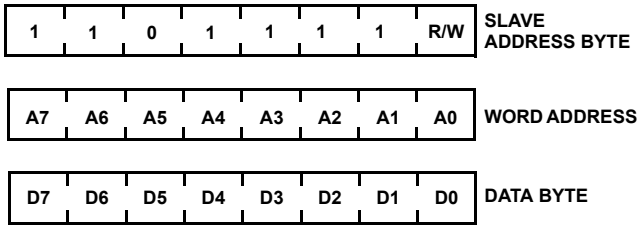


FIGURE 17. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL1221 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL1221 responds with an ACK. Then the ISL1221 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 18).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 19h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

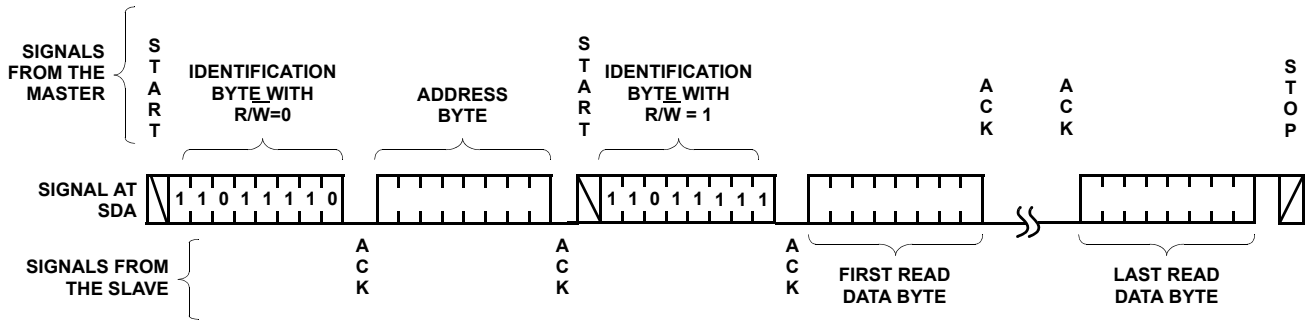


FIGURE 18. READ SEQUENCE

Application Section

Event Detection

The event detection feature of the ISL1221 is intended to be used for recording the time of single events that involve the opening of an enclosure, door, etc. The normal method of detection is with normally closed switch function that opens to initiate the event. This mechanism is ideal for applications such as set top boxes, utility meters, security alarm and camera systems or vending machines.

A typical application diagram is shown in Figure 19. A microcontroller communicates with the ISL1221 through the I^2C serial bus, to set up and read time of the day, alarms, or set up the outputs frequency control.

The ISL1221 is capable of recording individual event time/dates using the on-chip registers (Event Registers, addresses 14h to 19h). Single event times are recorded and can be read using a multiple address read, similar to reading the RTC registers. The Event Registers record the initial event time of a series of events, until the EVT bit is reset. After EVT is reset, the Timestamp Registers retain the previous event time until the next Event happens, at which time the current RTC register contents will be placed in the Event Registers. The Timestamp Registers cannot be cleared, only a full power down cycle (V_{CC} and V_{BAT} = 0V) will erase their contents.

For example, the event function is enabled and the EVT bit in the Status Register is cleared. Then the EVEN pin is triggered 3 times before the timestamp register is read. Only the first Event time will be recorded in the Timestamp Registers, and will be read. Then the EVT bit is cleared in the Status Register, and two more events happen. The previous Timestamp contents are replaced by the time of the next event after the EVT bit reset.

An additional event action available in the ISL1221 is to stop the real time clock from advancing. If the event register is set to enable this function (Register 09h, RTCHLT bit 5 set to 1), then when the EVIN pin is triggered, the clock counters will stop and hold the time of the event. This is useful for one time occurrences such as opening a warranted consumer product enclosure or exceeding a maximum temperature inside a device. Once the clock is stopped, the clock registers must be written with an updated time, then they will begin advancing immediately. If the RTCHLT bit is still set, then the next event will again stop the clock.

Event Detect Input Details

The EVIN input is a Schmitt trigger logic input. An event is detected when it is asserted high. The ISL1221 device has internal configuration settings which add detection flexibility. There are four configuration bits in register 09h which are for EVIN sampling. The ESMP1 and ESMP0 bits control sampling of the event input status. Reducing the sampling rate will lower the supply current drain, with the tradeoff of adding a delay in detecting an event. An event that is long in duration (i.e. opening a door) would obviously be served well with the lowest frequency sampling rate and lowest supply current drain.

The EHYS1 and EHYS0 bits control timer circuits to filter out switch bouncing, noise or intermittent contacts, by effectively adding time-based hysteresis to the EVIN input. They are used only in conjunction with the sampling rate, they cannot be used alone. The most appropriate use for the hysteresis function is for glitch or noise filtering on the EVIN input signal.

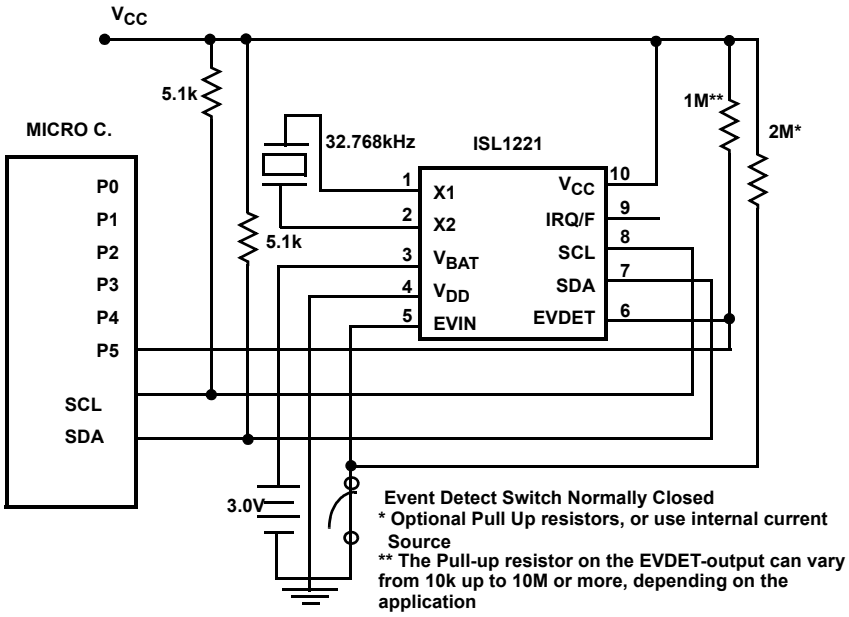


FIGURE 19.

Battery Backup Details

The event detection function has been designed to minimize power drain for extended life in battery backed applications. Many applications will need detection while in battery backup. Another bit, the EVBATB bit, is used to control if the event input is active in battery backup mode. Note that to DISABLE event sampling in battery backup, this bit is set to 1. The occurrence of an event is recorded and can be read by the microprocessor the next time the circuit is powered up. The input current sources and sampling are also usable in battery backup mode. If the EVIENB bit is set to disable the input current source, a large value pullup resistor must be tied to the V_{BAT} input to allow event detection in battery backup.

Note that any input signal conditioning circuitry that is added in regular operation or battery backup should have minimum supply current drain, or have the capability to be put in a low power standby mode. Op amps such as the EL8176 have low normal supply current (50µA) and standby power drain (3µA), so can be used in battery backup applications.

Oscillator Crystal Requirements

The ISL1221 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 14 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL1221 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 14. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
Epson	MC-405, MC-406
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Crystal Oscillator Frequency Adjustment

The ISL1221 device contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are six bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern pulling show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. These values typically vary from 6-10 ppm/bit at the low end to <1ppm/bit at the highest capacitance settings. The range afforded by the ATR adjustment with a typical surface mount crystal is typically -34 to +80ppm around the ATR=0 default setting because of this property. The user should note this when using the ATR for calibration. The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the ISL1221. There are 3 bits known as the Digital Trimming Register (DTR). The range provided is ±60ppm in increments of 20ppm. DTR operates by adding or skipping pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over temperature or extending the adjustment range available with the ATR register.

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the F_{OUT} pin with a calibrated frequency counter. The frequency used is unimportant, although 1Hz is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The ATR should be set to the center position, or 100000Bh, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note that increasing the ATR register for increased capacitance will lower the frequency, and vice-versa. If the initial measurement shows the frequency is far off, it will be necessary to use the DTR register to do a coarse adjustment. Note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 20. There is a turnover temperature (T_0) where the drift is very near 0. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature.

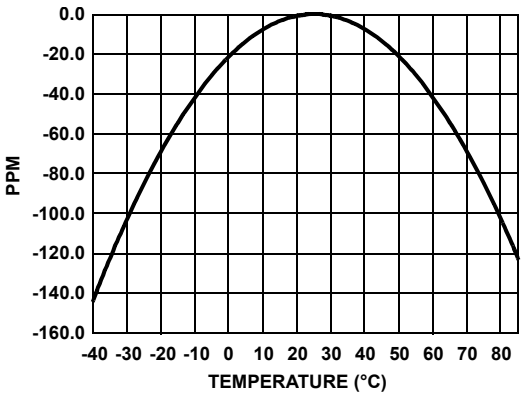


FIGURE 20. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an ISL1221 circuit, then both the DTR and ATR registers will need to be utilized (total correction range = -94 to +140ppm).

A system to implement temperature compensation would consist of the ISL1221, a temperature sensor, and a microcontroller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal manufacturer's specifications for the turnover temperature T_0 and the drift coefficient (β). The formula for calculating the oscillator adjustment necessary is:

$$\text{Adjustment (ppm)} = (T - T_0)^2 * \beta$$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than +20°C from T_0.

A sample curve of the ATR setting vs. Frequency Adjustment for the ISL1221 and a typical RTC crystal is given in Figure 21. This curve may vary with different crystals, so it is good practice to evaluate a given crystal in an ISL1221 circuit before establishing the adjustment values.

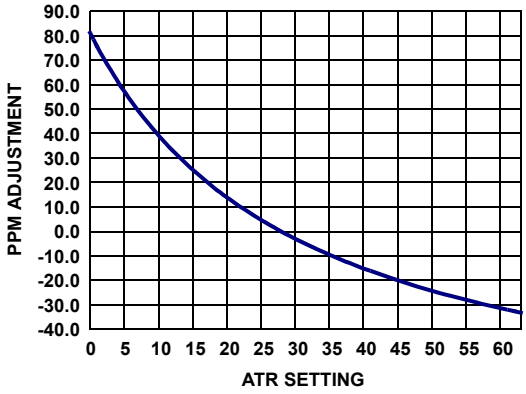


FIGURE 21. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

This curve is then used to figure what ATR and DTR settings are used for compensation. The results would be placed in a lookup table for the microcontroller to access.

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 22 shows a suggested layout for the ISL1221 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

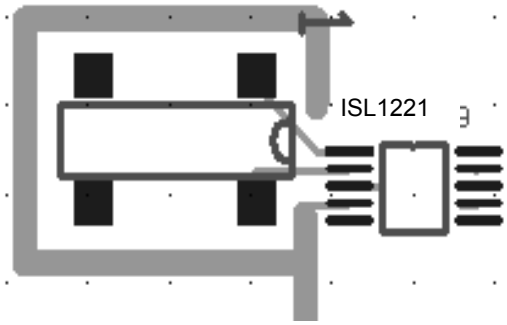


FIGURE 22. SUGGESTED LAYOUT FOR ISL1221 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the F_{OUT} pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and VDD pins can be treated as a ground, and should be routed around the crystal.

Super Capacitor Backup

The ISL1221 device provides a V_{BAT} pin which is used for a battery backup input. A Super Capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL1221 is extremely low, it is possible to get months of backup operation using a Super Capacitor. Typical capacitor values are a few µF to 1 Farad or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity Super Capacitor is the

best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a Super Capacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Following are some examples with equations to assist with calculating backup times and required capacitance for the ISL1221 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

Example 1. Calculating Backup Time Given Voltages and Capacitor Value

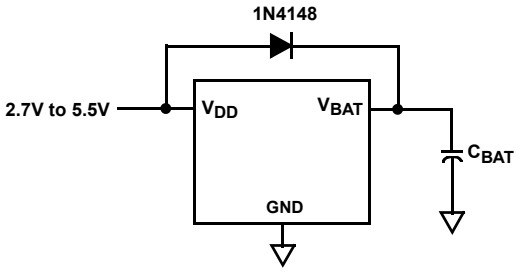


FIGURE 23. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 23, use C_{BAT} = 0.47F and V_{DD} = 5.0V. With V_{DD} = 5.0V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL1221 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge equation is used to estimate the total backup time (see Equation 2 and 3).

$$I = C_{BAT} * dV/dT \quad \text{(EQ. 2)}$$

Rearranging gives

$$dT = C_{BAT} * dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 3)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL1221 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over 50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (see Typical Performance Curves). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs. V_{BAT} is shown in Equation 4.

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 4)}$$

Using this equation to solve for the average current given 2 voltage points gives (see Equation 5).

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7 \text{ Amps} \quad \text{(EQ. 5)}$$

Combining with Equation 3 gives the equation for backup time (see Equation 6).

$$T_{BACKUP} = C_{BAT} * (V_{BAT2} - V_{BAT1}) / (I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 6)}$$

where :

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving Equation 5 for this example, I_{BATAVG} = 4.387E-7 A

T_{BACKUP} = 0.47 * (2.9) / 4.38E-7 = 3.107E6 sec

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be:

C_{BAT} = 0.70 * 35.96 = 25.2 days

Example 2. Calculating a capacitor value for a given backup time

Referring to Figure 23 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{DD} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 3 to solve for capacitance (see Equation 7).

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 7)}$$

Using the terms described above, this equation becomes (see Equation 8):

$$C_{BAT} = T_{BACKUP} * (I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 8)}$$

where:

T_{BACKUP} = 60 days * 86,400 sec/day = 5.18 E6 sec

I_{BATAVG} = 4.387 E-7 A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

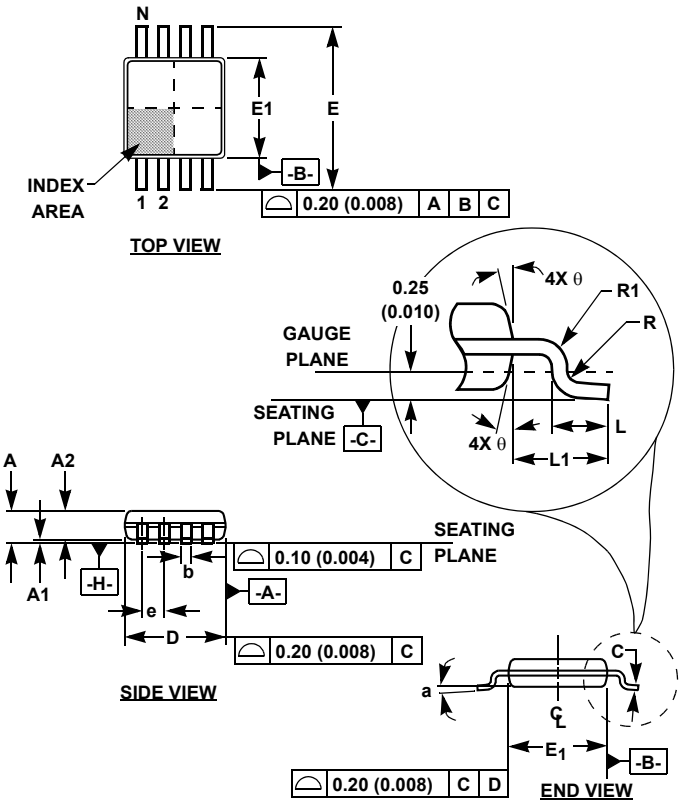
Solving gives:

C_{BAT} = 5.18 E6 * (4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case cap value would be:

C_{BAT} = 1.3 *.784 = 1.02F

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

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