



**THE DATASHEET OF
7052L35PQF**



Features

- ◆ **High-speed access**
 - Commercial: 20/25/35ns (max.)
 - Industrial: 25ns (max.)
 - Military: 35ns (max.)
- ◆ **Low-power operation**
 - IDT7052S
Active: 750mW (typ.)
Standby: 7.5mW (typ.)
 - IDT7052L
Active: 750mW (typ.)
Standby: 1.5mW (typ.)
- ◆ **True FourPort memory cells which allow simultaneous access of the same memory locations**
- ◆ **Fully asynchronous operation from each of the four ports: P1, P2, P3, P4**
- ◆ **Versatile control for write-inhibit: separate $\overline{\text{BUSY}}$ input to control write-inhibit for each of the four ports**

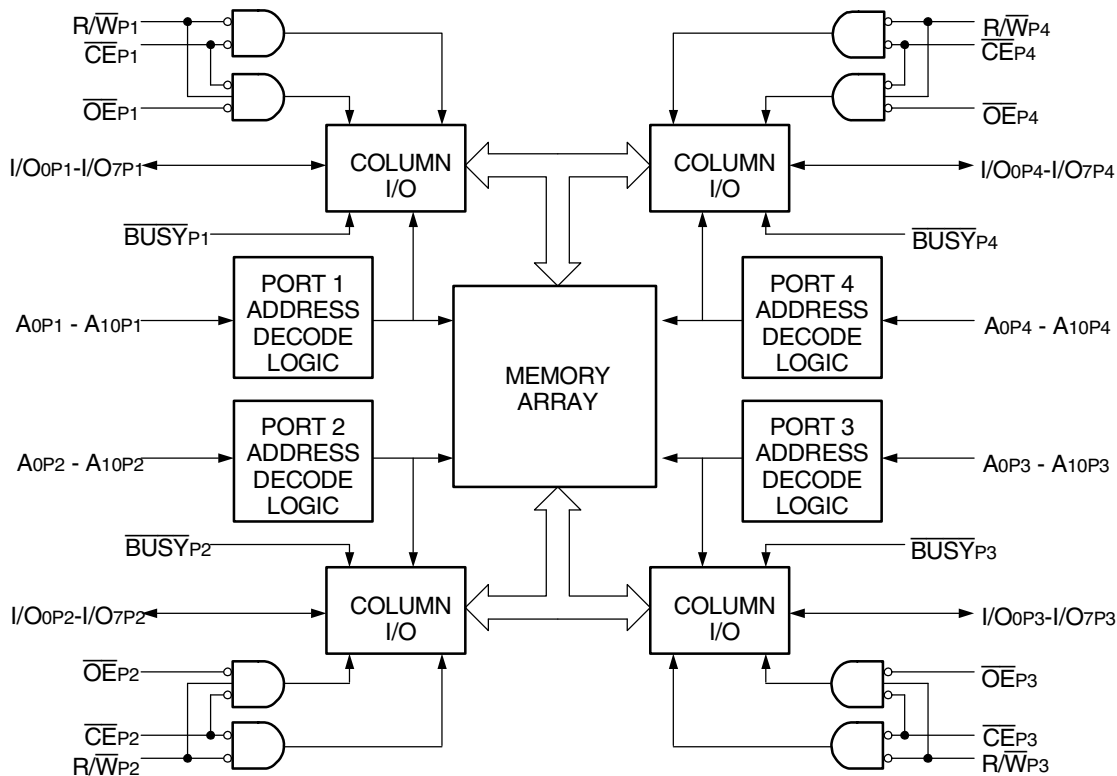
- ◆ **Battery backup operation—2V data retention**
- ◆ **TTL-compatible; single 5V ($\pm 10\%$) power supply**
- ◆ **Available in 120 pin Thin Quad Flatpacks and 108 pin PGA**
- ◆ **Military product compliant to MIL-PRF-38535 QML**
- ◆ **Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds**
- ◆ **Green parts available, see ordering information**

Description

The IDT7052 is a high-speed 2K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those

Functional Block Diagram



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systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin Pin Grid Array (PGA) and 120-pin Thin Quad Flatpack (TQFP). Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations^(1,2,3)

81	R/W P2	80	NC	77	A7 P2	74	A5 P2	72	A3 P2	69	A0 P2	68	A0 P3	65	A3 P3	63	A5 P3	60	A7 P3	57	NC	54	R/W P3	12											
84	BUSY P2	83	\overline{OE} P2	78	A8 P2	76	A10 P2	73	A4 P2	70	A1 P2	67	A1 P3	64	A4 P3	61	A10 P3	59	A8 P3	56	\overline{OE} P3	53	BUSY P3	11											
87	A2 P1	86	A1 P1	82	\overline{CE}	79	A9 P2	75	A6 P2	71	A2 P2	66	A2 P3	62	A6 P3	58	A9 P3	55	\overline{CE} P3	51	A1 P4	50	A2 P4	10											
90	A5 P1	88	A3 P1	85	A0 P1	IDT7052G GU108 ⁽⁴⁾ 108-Pin PGA Top View ⁽⁵⁾											52	A0 P4	49	A3 P4	47	A5 P4	09												
92	A10 P1	91	A6 P1	89	A4 P1												48	A4 P4	46	A6 P4	45	A10 P4	08												
95	A8 P1	94	A7 P1	93	VCC												44	GND	43	A7 P4	42	A8 P4	07												
96	A9 P1	97	NC	98	\overline{CE} P1												39	\overline{CE} P4	40	NC	41	A9 P4	06												
99	R/W P1	100	\overline{OE} P1	102	I/O0 P1												35	GND	37	\overline{OE} P4	38	R/W P4	05												
101	BUSY P1	103	I/O1 P1	106	GND												31	GND	34	I/O7 P4	36	BUSY P4	04												
104	I/O2 P1	105	I/O3 P1	1	I/O6 P1												4	VCC	8	GND	12	VCC	17	VCC	21	GND	25	VCC	28	I/O2 P4	32	I/O5 P4	33	I/O6 P4	03
107	I/O4 P1	2	I/O7 P1	5	I/O0 P2												7	I/O2 P2	10	I/O4 P2	13	I/O6 P2	16	I/O1 P3	19	I/O3 P3	22	I/O5 P3	24	I/O7 P3	29	I/O3 P4	30	I/O4 P4	02
108	I/O5 P1	3	NC	6	I/O1 P2	9	I/O3 P2	11	I/O5 P2	14	I/O7 P2	15	I/O0 P3	18	I/O2 P3	20	I/O4 P3	23	I/O6 P3	26	I/O0 P4	27	I/O1 P4	01											
		A	B	C	D	E	F	G	H	J	K	L	M																						

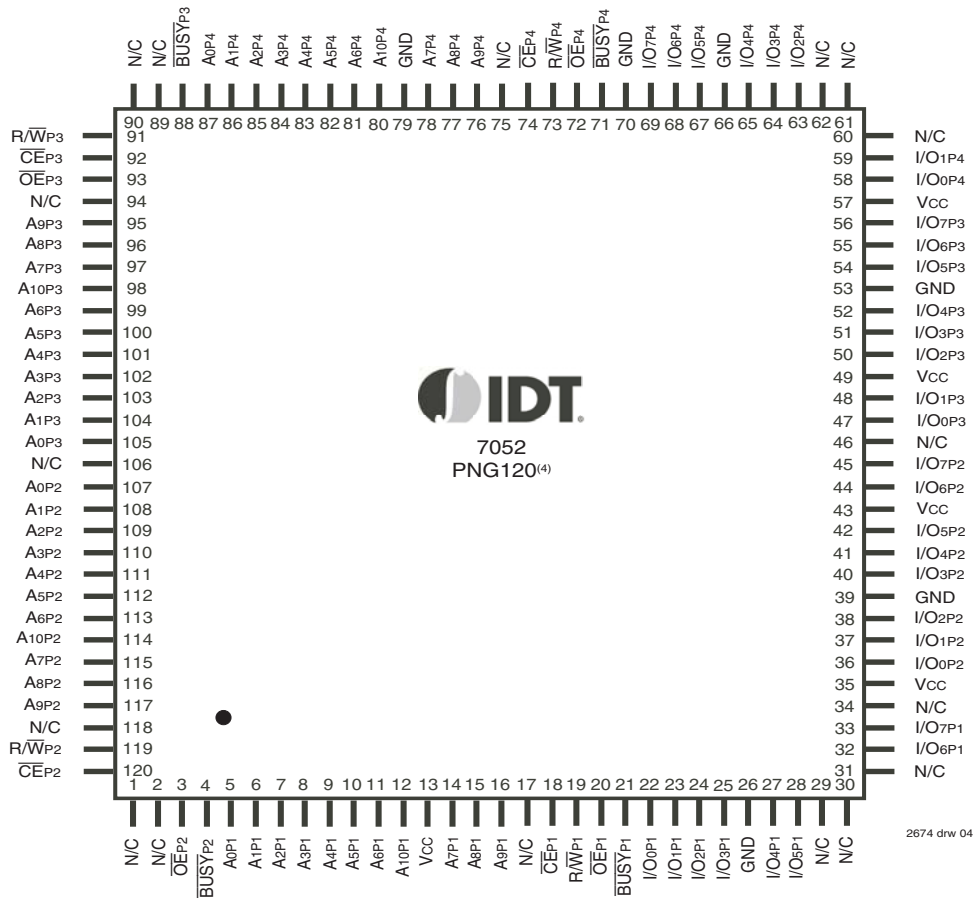
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NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 1.21 in x 1.21 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2,3) (con't.)



NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. PNG120 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Pin Configurations^(1,2)

Symbol	Pin Name
A0 P1 - A10 P1	Address Lines - Port 1
A0 P2 - A10 P2	Address Lines - Port 2
A0 P3 - A10 P3	Address Lines - Port 3
A0 P4 - A10 P4	Address Lines - Port 4
I/O0 P1 - I/O7 P1	Data I/O - Port 1
I/O0 P2 - I/O7 P2	Data I/O - Port 2
I/O0 P3 - I/O7 P3	Data I/O - Port 3
I/O0 P4 - I/O7 P4	Data I/O - Port 4
R/W P1	Read/Write - Port 1
R/W P2	Read/Write - Port 2
R/W P3	Read/Write - Port 3
R/W P4	Read/Write - Port 4
GND	Ground
CE P1	Chip Enable - Port 1
CE P2	Chip Enable - Port 2
CE P3	Chip Enable - Port 3
CE P4	Chip Enable - Port 4
OE P1	Output Enable - Port 1
OE P2	Output Enable - Port 2
OE P3	Output Enable - Port 3
OE P4	Output Enable - Port 4
BUSY P1	Write Disable - Port 1
BUSY P2	Write Disable - Port 2
BUSY P3	Write Disable - Port 3
BUSY P4	Write Disable - Port 4
Vcc	Power

NOTES:

- All Vcc pins must be connected to the power supply.
- All GND pins must be connected to the ground supply

2674 tbl 01

Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz) TQFP only

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
COU	Output Capacitance	VOUT = 0V	10	pF

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

2674 tbl 03

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2674 tbl 02

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2674 tbl 04

NOTE:

- This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2674 tbl 05

NOTES:

- VIL ≥ -1.5V for pulse width less than 10ns.
- VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,5) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Condition	Version	7052X20 Com'1 Only		7052X25 Com'1, Ind & Military		7052X35 Com'1 & Military		Unit
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
I _{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = 0^{(3)}$	COM'L. S	150	300	150	300	150	300	mA
			L	150	250	150	250	150	250	
			MIL. & IND. S	—	—	150	360	150	360	
			L	—	—	150	300	150	300	
I _{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(4)}$	COM'L. S	240	370	225	350	210	335	mA
			L	210	325	195	305	180	290	
			MIL. & IND. S	—	—	225	400	210	395	
			L	—	—	195	340	180	330	
I _{SB}	Standby Current (All Ports - TTL Level Inputs)	$\overline{CE} = V_{IH}$ $f = f_{MAX}^{(4)}$	COM'L. S	70	95	45	85	40	75	mA
			L	60	80	40	70	35	60	
			MIL. & IND. S	—	—	45	115	40	110	
			L	—	—	40	85	35	80	
I _{SB1}	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(3)}$	COM'L. S	1.5	15	1.5	15	1.5	15	mA
			L	0.3	1.5	0.3	1.5	0.3	1.5	
			MIL. & IND. S	—	—	1.5	30	1.5	30	
			L	—	—	0.3	4.5	0.3	4.5	

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NOTES:

- 'X' in part number indicates power rating (S or L).
- V_{CC} = 5V, T_A = +25°C and are not production tested.
- f = 0 means no address or control lines change.
- At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current above by four.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7052S		7052L		Unit
			Min.	Max.	Min.	Max.	
I _L	Input Leakage Current ⁽¹⁾	V _{CC} = 5.5V, V _{IN} = 0V to V _{CC}	—	10	—	5	μA
I _O	Output Leakage Current	$\overline{CE} = V_{IH}$, V _{OUT} = 0V to V _{CC}	—	10	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 4mA	—	0.4	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2674 tbl 07

NOTE:

- At V_{CC} ≤ 2.0V input leakages are undefined.

Data Retention Characteristics Over All Temperature Ranges⁽⁴⁾

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

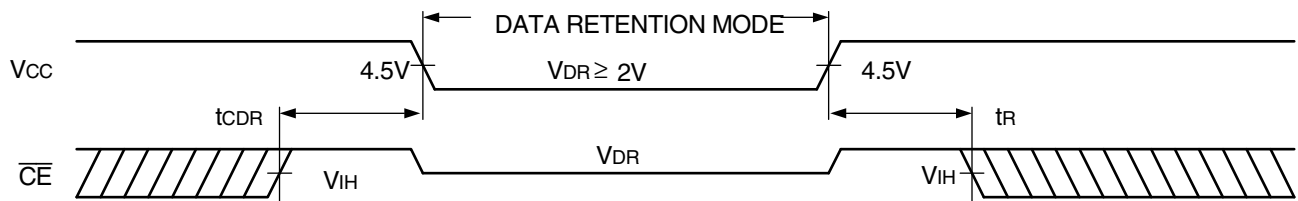
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{CC} for Data Retention	V _{CC} = 2V	2.0	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	Com'l.	25	600	μA
			Mil. & Ind.	25	1800	
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns

2674 tbl 08a

NOTES:

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.
4. Industrial temperature: For other speeds, packages and powers contact your sales office.

Low V_{CC} Data Retention Waveform



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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2674 tbl 08b

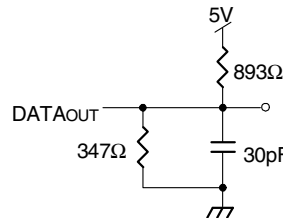


Figure 1. AC Output Test Load

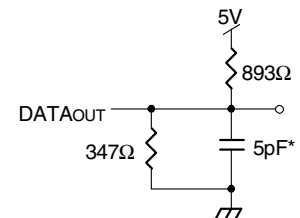


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{wz}, t_{ow})
*Including scope and jig

2674 drw 06

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽³⁾

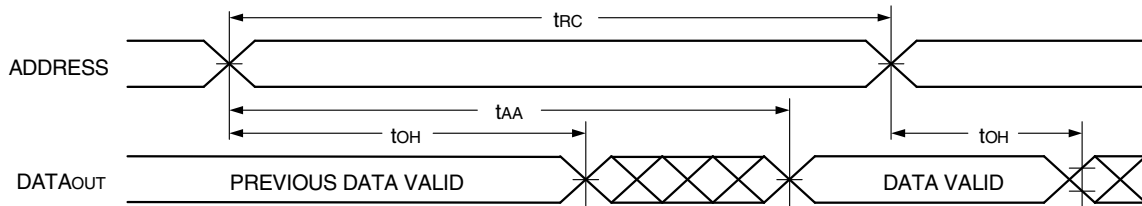
Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l, Ind & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	35	ns
t _{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t _{AOE}	Output Enable Access Time	—	10	—	15	—	25	ns
t _{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	5	—	5	—	5	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	12	—	15	—	15	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	20	—	25	—	35	ns

2674 tbl 09

NOTES:

1. Transition is measured 0mV from Low or High-Impedance voltage with the Output Test Load (Figure 2)
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L)

Timing Waveform of Read Cycle No. 1, Any Port⁽¹⁾

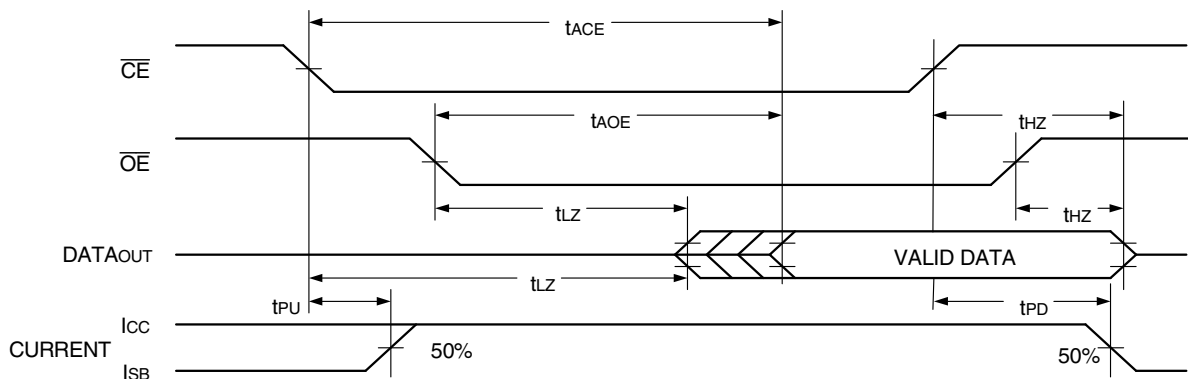


2674 drw 07

NOTE:

1. $R/\bar{W} = V_{IH}$, $\bar{OE} = V_{IL}$ and $\bar{CE} = V_{IL}$.

Timing Waveform of Read Cycle No. 2, Any Port^(1,2)



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NOTES:

1. $R/\bar{W} = V_{IH}$ for Read Cycles.
2. Addresses valid prior to or coincident with \bar{CE} transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁷⁾

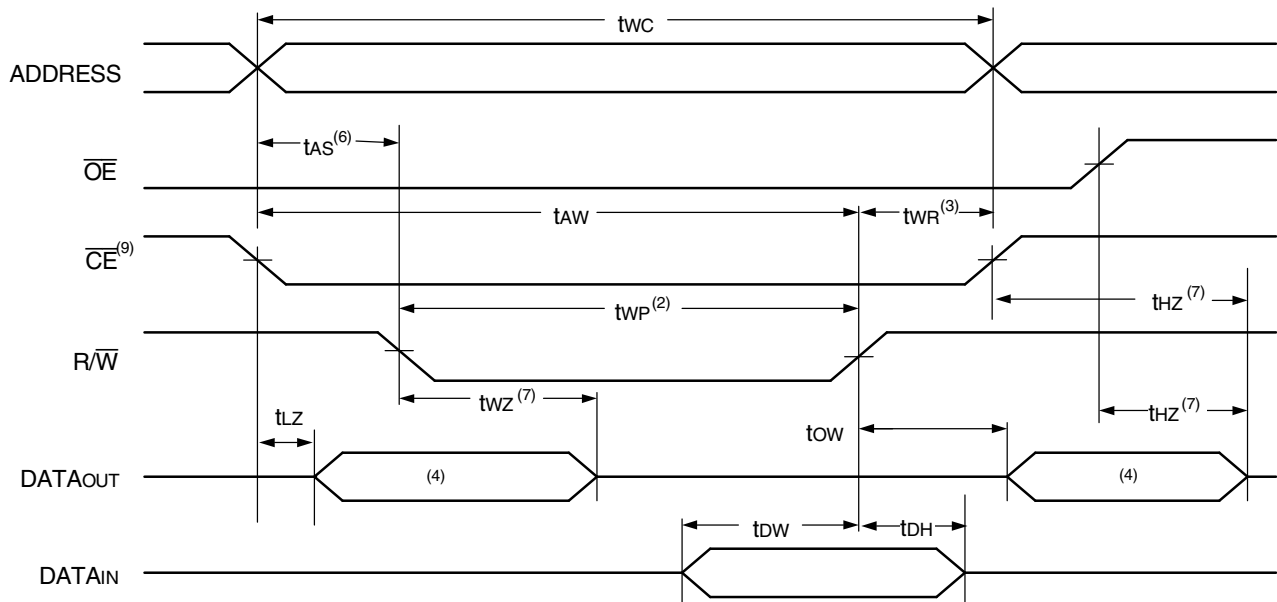
Symbol	Parameter	7052X20 Com'l Only		7052X25 Com'l & Military		7052X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t _{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t _{EW}	Chip Enable to End-of-Write ⁽³⁾	15	—	20	—	30	—	ns
t _{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width ⁽³⁾	15	—	20	—	30	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t _{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	15	—	15	—	15	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	12	—	15	—	15	ns
t _{OW}	Output Active from End-of-Write ^(1,2)	0	—	0	—	0	—	ns
t _{WDD}	Write Pulse to Data Delay ⁽⁴⁾	—	35	—	45	—	55	ns
t _{WDD}	Write Data Valid to Read Data Delay ⁽⁴⁾	—	30	—	35	—	45	ns
BUSY INPUT TIMING								
t _{WB}	Write to $\overline{\text{BUSY}}^{\text{(6)}}$	0	—	0	—	0	—	ns
t _{WH}	Write Hold After $\overline{\text{BUSY}}^{\text{(6)}}$	15	—	15	—	20	—	ns

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NOTES:

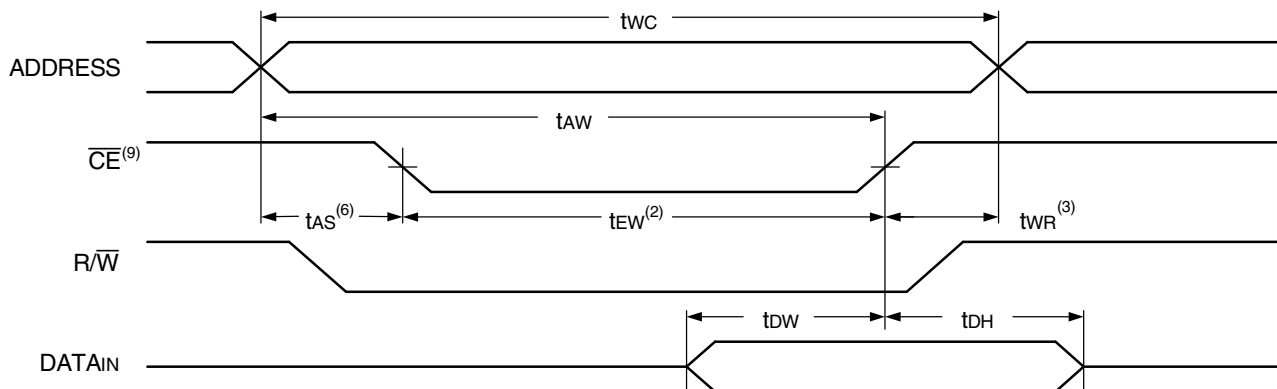
- Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- This parameter is guaranteed by device characterization but is not production tested.
- If $\overline{\text{OE}} = V_{\text{IL}}$ during a R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{OW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW}. If $\overline{\text{OE}} = V_{\text{IH}}$ during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}. Specified for $\overline{\text{OE}} = V_{\text{IH}}$ (refer to "Timing Waveform of Write Cycle", Note 8).
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
- To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
- To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
- 'X' in part number indicates power rating.

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing^(5,8)



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Timing Waveform of Write Cycle No. 2, CE Controlled Timing^(1, 5)

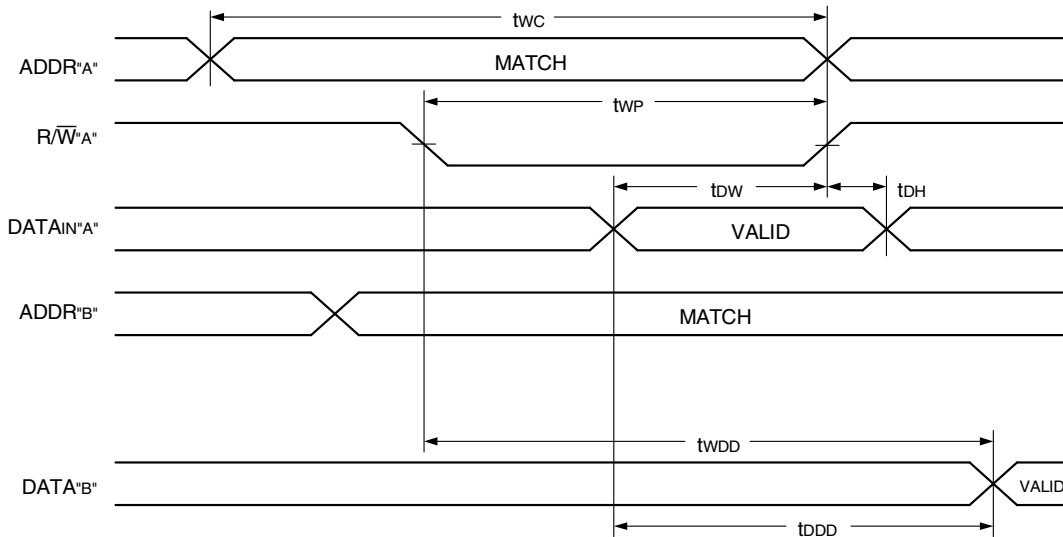


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NOTES:

1. R/\bar{W} or $\bar{CE} = V_{IH}$ during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\bar{CE} = V_{IL}$ and a $R/\bar{W} = V_{IL}$.
3. t_{WR} is measured from the earlier of \bar{CE} or $R/\bar{W} = V_{IH}$ to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\bar{CE} = V_{IL}$ transition occurs simultaneously with or after the $R/\bar{W} = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \bar{CE} or R/\bar{W} .
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If $\bar{OE} = V_{IL}$ during a R/\bar{W} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{OW})$ to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW} . If $\bar{OE} = V_{IH}$ during an R/\bar{W} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Timing Waveform of Write with Port-to-Port Read^(1,2,3)

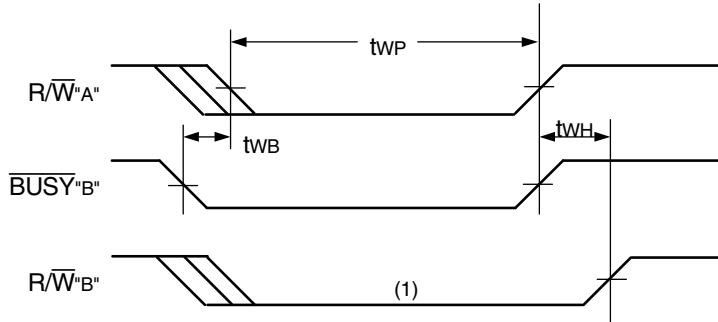


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NOTES:

1. Assume $\overline{\text{BUSY}}$ input = V_{IH} and $\overline{\text{CE}} = V_{IL}$ for the writing port.
2. $\overline{\text{OE}} = V_{IL}$ for the reading ports.
3. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

Timing Waveform of Write with **BUSY** Input



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NOTE:

1. $\overline{\text{BUSY}}$ is asserted on Port "B" blocking $\overline{\text{R/W}}^{\text{B}}$ until $\overline{\text{BUSY}}^{\text{B}}$ goes HIGH.

Functional Description

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{\text{CE}} = V_{IH}$). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{\text{OE}}$). In the read mode, the port's $\overline{\text{OE}}$ turns on the output drivers when set LOW. READ/ WRITE conditions are illustrated in the table below.

Truth Table I – Read/Write Control⁽³⁾

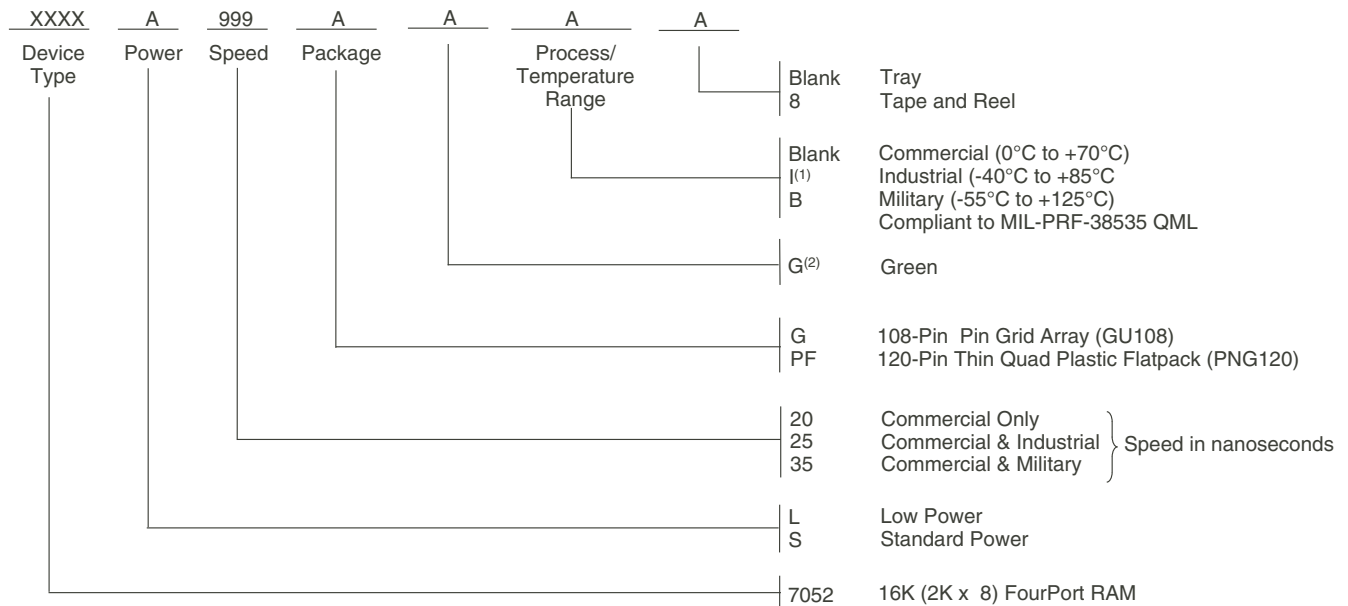
Any Port ⁽¹⁾				Function
R/W	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0-7	
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{\text{CE}}_{P1} = \overline{\text{CE}}_{P2} = \overline{\text{CE}}_{P3} = \overline{\text{CE}}_{P4} = V_{IH}$ Power Down Mode LSB or ISB1
L	L	X	DATAIN	Data on port written into memory ⁽²⁾
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	Outputs Disabled

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NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care, "Z" = High Impedance
2. If $\overline{\text{BUSY}} = V_{IL}$, write is blocked.
3. For valid write operation, no more than one port can write to the same address location at the same time.

Ordering Information



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NOTES:

1. Industrial temperature range is available. For specific speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	7052L20G	GU108	PGA	C
	7052L20PFG	PNG120	TQFP	C
	7052L20PFG8	PNG120	TQFP	C
25	7052L25G	GU108	PGA	C
	7052L25PFGI	PNG120	TQFP	I
	7052L25PFG8	PNG120	TQFP	I
35	7052L35G	GU108	PGA	C
	7052L35GB	GU108	PGA	M

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	7052S20G	GU108	PGA	C
25	7052S25G	GU108	PGA	C
35	7052S35G	GU108	PGA	C
	7052S35GB	GU108	PGA	M

Datasheet Document History

- 01/18/99: Initiated datasheet document history
 Converted to new format
 Cosmetic typographical corrections
 Added additional notes to pin configurations
- 06/04/99: Changed drawing format
 Page1 Corrected DSC number
- 11/10/99: Replaced IDT logo
- 11/18/99: Page 10 Fixed typo in caption for $\overline{\text{BUSY}}$ Input waveform
- 05/23/00: Page 4 Increased storage temperature parameter
 Clarified TA parameter
 Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
 Changed $\pm 200\text{mV}$ to 0mV in notes
- 10/22/01: Pages 2 & 3 Added date revision for pin configurations
 Page 5, 7 & 8 Added Industrial temp to column heading for 25ns speed to DC & AC Electrical Characteristics
 Page 11 Added Industrial temp offering to 25ns ordering information
 Page 4, 5, 7 & 8 Removed Industrial temp footnote from all tables
 Page 1 & 11 Replace TM logo with ® logo
- 07/24/06: Page 1 Added green availability to features
 Page 11 Added green indicator to ordering information
- 01/19/09: Page 11 Removed "IDT" from orderable part number
- 02/05/15: Page 2 Removed IDT in reference to fabrication
 Page 2,3 & 11 The package codes G108-1 & PN120-1 changed to G108 & PN120 respectively to match standard package codes
 Page 11 Added Tape and Reel to Ordering Information
 Page 1&3 Removed 132-pin PQF offering from the Features & the pin configuration
 Page 11 Removed the 132-pin PQF package from the Ordering Information
- 07/08/16: Page 3 Changed diagram for the PN120 pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1
 Added the IDT logo to the PN120 pin configurations and changed the text to be in alignment with new diagram marking specs and removed the date revision indicator from all pin configurations
 Updated footnote references for PN120 pin configuration by removing footnote 4 & 5
- 06/07/18: Product Discontinuation Notice - PDN# SP-17-02
 Last time buy expires June 15, 2018
- 07/11/19: Page 2 & 3 Updated package codes G108 to GU108 and PN180 to PNG180
 Page 11 Added Orderable Part Information tables

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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