



**THE DATASHEET OF
ISPLSI 2032VE-135LT48**



Asymmetrical Discrete Series - DO-214



Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

Not Applicable

Schematic Symbol



Description

The Asymmetrical Discrete Series are SIDACtor® components designed to protect LCAS (Line Circuit Access Switch) devices from damaging overvoltage transients.

The series provides a specialized asymmetrical overvoltage protection solution that enables equipment to comply with various global regulatory standards.

Features and Benefits

- Low voltage overshoot ratings
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- LCAS specific tip and ring thresholds
- RoHS Compliant, Lead-Free, and Halogen-Free
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Additional Information



Datasheet



Resources



Samples

Electrical Characteristics

Part Number	Marking	V_{DRM} @ $I_{DRM}=5\mu A$	V_S @ 100V/ μs	I_H	I_S	I_T	V_T @ $I_T=2.2 A$	Capacitance @ 1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P1200SALRP	P12A	100	130	120	800	2.2	4	15	40
P2000SALRP	P20A	180	220	120	800	2.2	4	15	35
P2500SALRP	P25A	230	290	120	800	2.2	4	15	35
P1200SBLRP	P12B	100	130	120	800	2.2	4	20	50
P2000SBLRP	P20B	180	220	120	800	2.2	4	20	50
P2500SBLRP	P25B	230	290	120	800	2.2	4	20	50
P1200SCLRP	P12C	100	130	120	800	2.2	4	20	35
P2000SCLRP	P20C	180	220	120	800	2.2	4	25	35
P2500SCLRP	P25C	230	290	120	800	2.2	4	30	70

Notes:
- Absolute maximum ratings measured at $T_A = 25^\circ C$ (unless otherwise noted).
- Components are bi-directional.

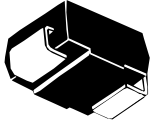
Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 ¹	2/10 ¹	8/20 ¹	10/160 ¹	10/560 ¹	5/320 ¹	10/360 ¹	10/1000 ¹	5/310 ¹		
	0.5/700 ²	2/10 ²	1.2/50 ²	10/160 ²	10/560 ²	9/720 ²	10/360 ²	10/1000 ²	10/700 ²		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	Amps/μs max
A	20	150	150	90	50	75	75	45	75	25	500
B	25	250	250	150	100	100	125	80	100	30	500
C	50	500	400	200	150	200	175	100	200	35	500

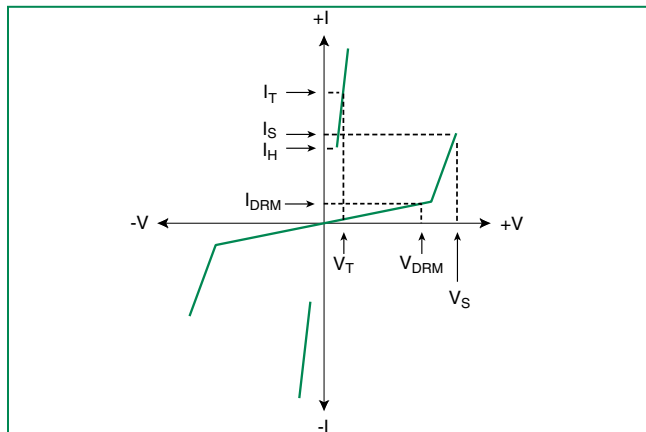
Notes:

- 1 Current waveform in μs
- 2 Voltage waveform in μs
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

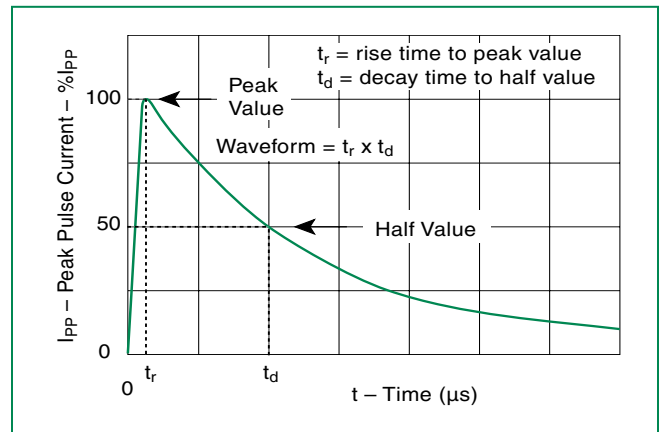
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

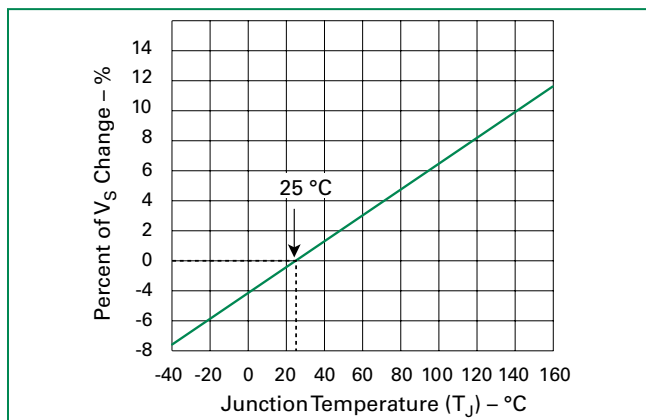
V-I Characteristics



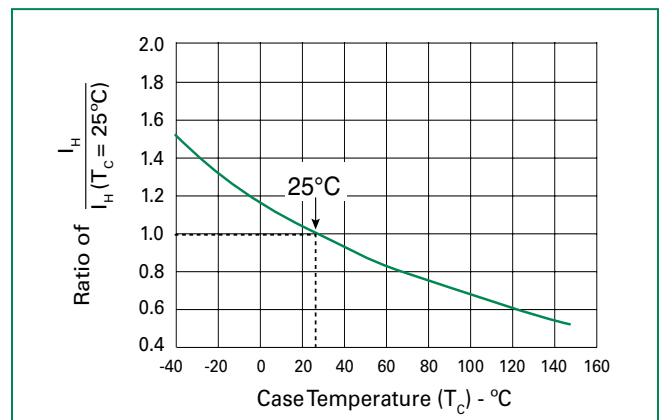
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature

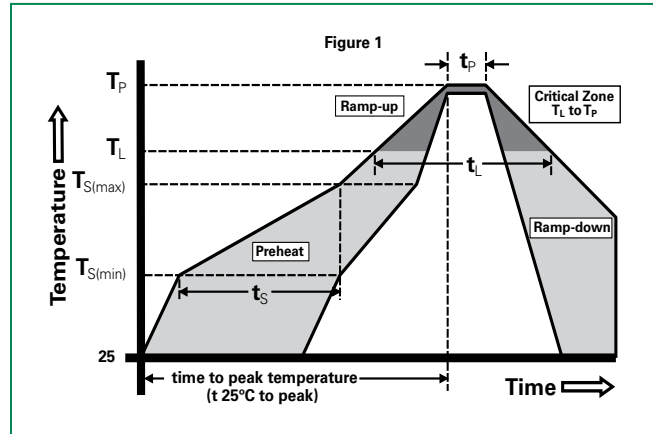


Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_p)		8 min. Max.
Do not exceed		+260°C



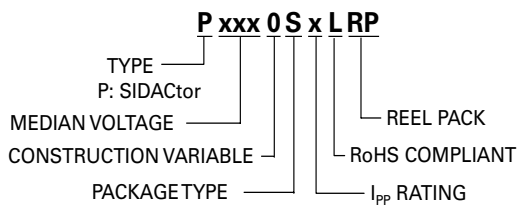
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

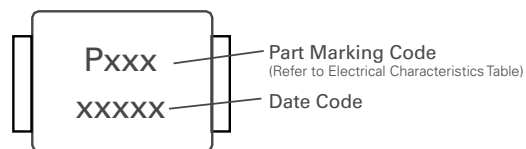
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

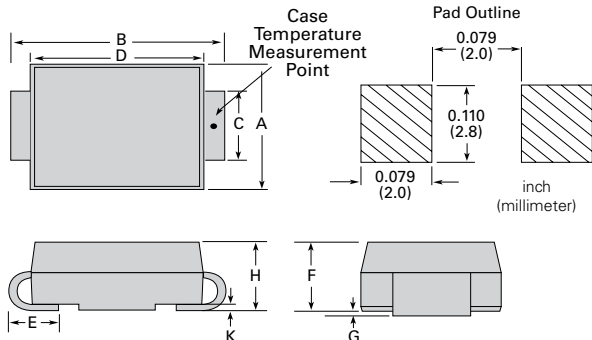
Part Numbering



Part Marking



Dimensions — DO-214AA

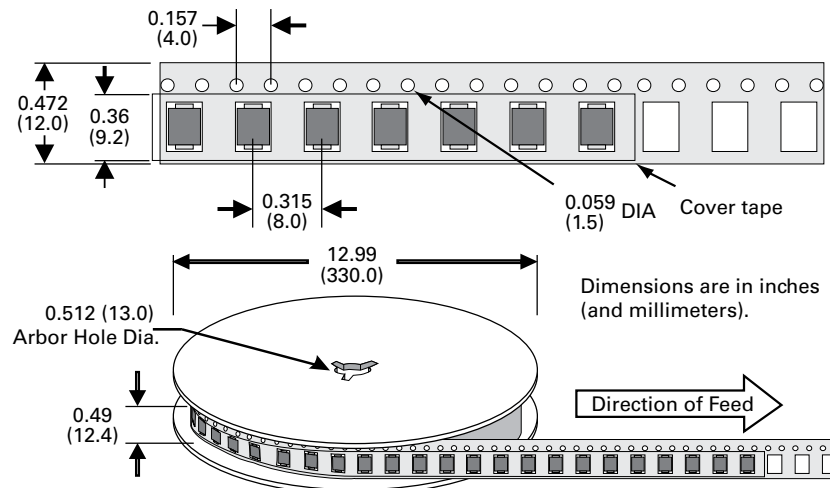


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Packing Options



Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — DO-214AA



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View ISPLSI 2032VE-135LT48 on WIN SOURCE](#)
-  [Lattice Semiconductor Corporation Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management