



**THE DATASHEET OF
FH12-34S-0.5SH(55)**



MSP430FR25x2 Capacitive Touch Sensing Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- **CapTIvate™ technology** – capacitive touch
 - Performance
 - Fast electrode scanning with two simultaneous scans
 - Proximity sensing
 - Reliability
 - Increased immunity to power line, RF, and other environmental noise
 - Built-in spread spectrum, automatic tuning, noise filtering, and debouncing algorithms
 - Enables **reliable touch solutions** with 10-V RMS common-mode noise, 4-kV electrical fast transients, and 15-kV electrostatic discharge, allowing for IEC-61000-4-6, IEC-61000-4-4, and IEC-61000-4-2 compliance
 - Reduced RF emissions to simplify electrical designs
 - Support for metal touch and water rejection designs
 - Flexibility
 - Up to 8 self-capacitance and 16 mutual-capacitance electrodes
 - Mix and match **self- and mutual-capacitive electrodes in the same design**
 - Supports multi-touch functionality
 - Wide range of capacitance detection, wide electrode range of 0 to 300 pF
 - Low power
 - <4 μ A wake-on-touch with two sensors
 - Wake-on-touch state machine allows electrode scanning while CPU is asleep
 - Hardware acceleration for environmental compensation, filtering, and threshold detection
 - Ease of use
 - **CapTIvate Design Center**, PC GUI lets engineers design and tune capacitive buttons in real time without having to write code
 - CapTIvate software library in ROM provides ample FRAM for customer application
- Embedded microcontroller
 - 16-bit RISC architecture
 - Clock supports frequencies up to 16 MHz
 - Wide supply voltage range from 3.6 V down to 1.8 V (minimum supply voltage is restricted by SVS levels, see the **SVS Specifications**)
- Optimized ultra-low-power modes
 - Active mode: 120 μ A/MHz (typical)
 - Standby: <4 μ A wake-on-touch with two sensors
 - Shutdown (LPM4.5): 36 nA without SVS
- Low-power ferroelectric RAM (FRAM)
 - Up to 7.5 KB of nonvolatile memory
 - Built-in error correction code (ECC)
 - Configurable write protection
 - Unified memory of program, constants, and storage
 - 10^{15} write cycle endurance
 - Radiation resistant and nonmagnetic
 - High FRAM-to-SRAM ratio, up to 4:1
- High-performance analog
 - Up to 8-channel 10-bit analog-to-digital converter (ADC)
 - Internal 1.5-V reference
 - Sample-and-hold 200 ksp/s
- Intelligent digital peripherals
 - Two 16-bit timers with three capture/compare registers each (Timer_A3)
 - One 16-bit timer associated with CapTIvate™ technology
 - One 16-bit counter-only RTC
 - 16-bit cyclic redundancy check (CRC)
- Enhanced serial communications with support for pin remap feature (see **Device Comparison**)
 - One eUSCI_A supports UART, IrDA, and SPI
 - One eUSCI_B supports SPI and I²C
- Clock system (CS)
 - on-chip 32-kHz RC oscillator (REFO)
 - on-chip 16-MHz digitally controlled oscillator (DCO) with frequency-locked loop (FLL)
 - $\pm 1\%$ accuracy with on-chip reference at room temperature
 - On-chip very low-frequency 10-kHz oscillator (VLO)
 - On-chip high-frequency modulation oscillator (MODOSC)
 - External 32-kHz crystal oscillator (LFXT)
 - Programmable MCLK prescaler of 1 to 128
 - SMCLK derived from MCLK with programmable prescaler of 1, 2, 4, or 8



- General input/output and pin functionality
 - Total of 15 I/Os on VQFN-20 package
 - 15 interrupt pins (P1 and P2) can wake MCU from low-power modes
- Development tools and software
 - Development tools
 - MSP CapTlvate™ MCU development kit evaluation: use with [CAPTIVATE-PGMR](#) programmer and capacitive touch MSP430FR2522 MCU board [BOOSTXL-CAPKEYPAD](#)
 - Target development board [MSP-TS430RHL20](#)
 - Ease-of-use ecosystem
 - [CapTlvate Design Center](#) – code generation, customizable GUI, real-time tuning
- 12KB ROM library includes CapTlvate touch libraries and driver libraries
- Family Members (Also See [Device Characteristics](#))
 - MSP430FR2522: 7.25KB of program FRAM, 256B of information FRAM, 2KB of RAM up to 8 self-capacitive and 16 mutual-capacitive sensors
 - MSP430FR2512: 7.25KB of program FRAM, 256B of information FRAM, 2KB of RAM up to 4 self-capacitive or mutual-capacitive sensors
- Package options
 - 20-pin: VQFN (RHL)
 - 16-pin: TSSOP (PW)

1.2 Applications

- Electronic smart locks, door keypads, and readers
- Garage door systems
- Intrusion HMI keypads and control panels
- Elevator call buttons
- Personal electronics
- Wireless speakers and headsets
- A/V receivers
- Appliances
- Power tools
- Light switches
- Video doorbells

1.3 Description

The MSP430FR25x2 is a family of ultra-low-power MSP430™ microcontrollers (MCUs) for capacitive touch sensing that feature [CapTlvate™ touch technology](#) for cost-sensitive applications featuring 1 to 16 capacitive buttons or proximity sensing. The MSP430FR25x2 MCUs offer value and performance for industrial applications exposed to electromagnetic disturbances, oil, water, and grease. The devices offer IEC-certified solutions with 5x lower power consumption than competition and support proximity sensing as well as touch through glass, plastic, and metal overlays.

TI capacitive touch sensing MSP430 MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get your design started quickly. The [BOOSTXL-CAPKEYPAD](#) BoosterPack™ plug-in module can be used with the [CAPTIVATE-PGMR](#) programmer board (standalone or as part of the [MSP-CAPT-FR2633](#) CapTlvate development kit) or with the LaunchPad development kit ecosystem. TI also provides free software including the [CapTlvate Design Center](#), where engineers can quickly develop applications with an easy-to-use GUI and [MSP430Ware™ software](#), and comprehensive documentation with the [CapTlvate technology guide](#).

MSP430 MCUs with CapTlvate technology provide the most integrated and autonomous capacitive-touch solutions in the market with high reliability and noise immunity at the lowest power. For more information visit ti.com/captivate.

For complete module descriptions, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|-------------------|------------|--------------------------|
| MSP430FR2522IPW16 | TSSOP (16) | 5 mm × 4.4 mm |
| MSP430FR2522IRHL | VQFN (20) | 4.5 mm × 3.5 mm |
| MSP430FR2512IPW16 | TSSOP (16) | 5 mm × 4.4 mm |
| MSP430FR2512IRHL | VQFN (20) | 4.5 mm × 3.5 mm |

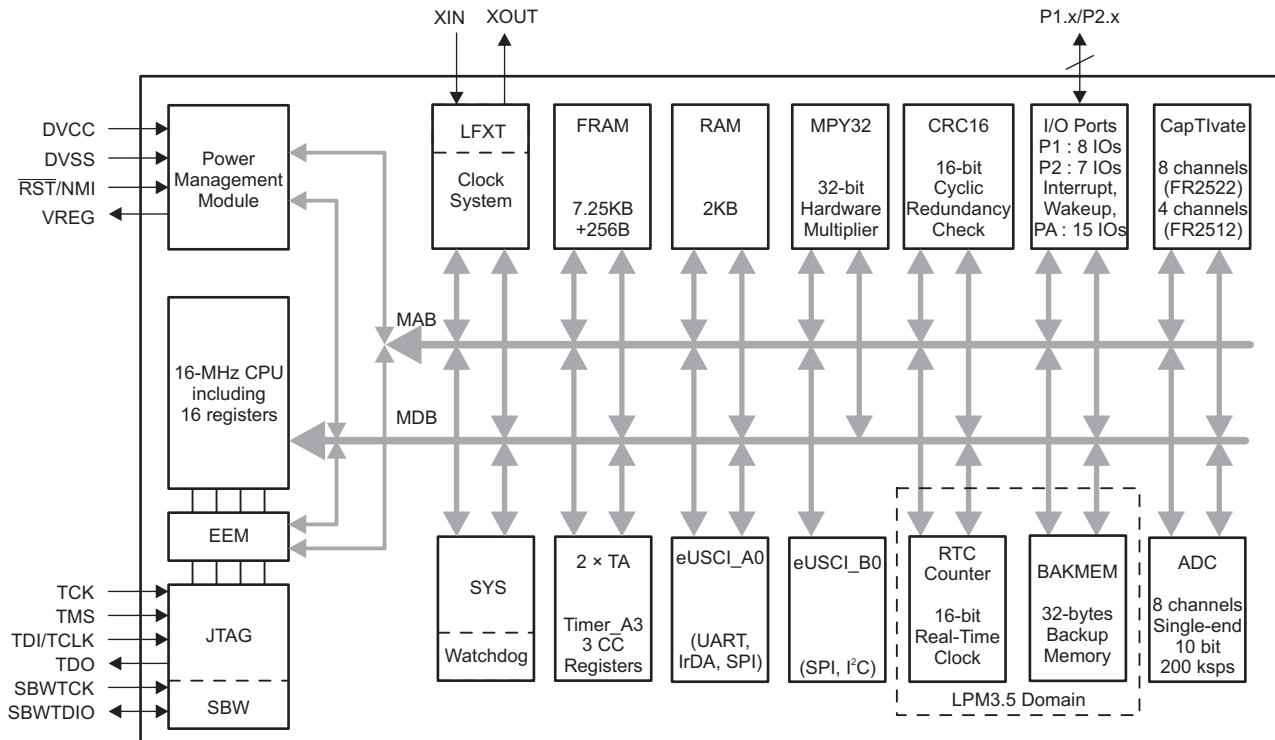
- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 9](#), or see the TI website at www.ti.com.
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See [MSP430 System-Level ESD Considerations](#) for more information.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



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Figure 1-1. Functional Block Diagram

- The MCU has one main power pair of DVCC and DVSS that supplies digital and analog modules. Recommended bypass and decoupling capacitors are 4.7 μF to 10 μF and 0.1 μF , respectively, with $\pm 5\%$ accuracy.
- VREG is the decoupling capacitor of the CapTIvate regulator. The recommended value for the required decoupling capacitor is 1 μF , with a maximum ESR of $\leq 200 \text{ m}\Omega$.
- P1 and P2 feature the pin interrupt function and can wake the MCU from all LPMs, including LPM3.5 and LPM4.
- Each Timer_A3 has three capture/compare registers. Only CCR1 and CCR2 are externally connected. CCR0 registers can be used only for internal period timing and interrupt generation.
- In LPM3 or LPM4 mode, the CapTIvate module can be functional while the rest of the peripherals are off.

Table of Contents

| | | | | | |
|----------|---|---------------------------|--|---|---------------------------|
| 1 | Device Overview | 1 | | | |
| | 1.1 Features | 1 | | 6.1 Overview | 43 |
| | 1.2 Applications | 2 | | 6.2 CPU | 43 |
| | 1.3 Description | 2 | | 6.3 Operating Modes | 43 |
| | 1.4 Functional Block Diagram | 4 | | 6.4 Interrupt Vector Addresses | 44 |
| 2 | Revision History | 6 | | 6.5 Bootloader (BSL) | 46 |
| 3 | Device Comparison | 7 | | 6.6 JTAG Standard Interface | 46 |
| | 3.1 Related Products | 7 | | 6.7 Spy-Bi-Wire Interface (SBW) | 47 |
| 4 | Terminal Configuration and Functions | 8 | | 6.8 FRAM | 47 |
| | 4.1 Pin Diagrams | 8 | | 6.9 Memory Protection | 47 |
| | 4.2 Pin Attributes | 10 | | 6.10 Peripherals | 47 |
| | 4.3 Signal Descriptions | 12 | | 6.11 Input/Output Diagrams | 56 |
| | 4.4 Pin Multiplexing | 15 | | 6.12 Device Descriptors | 60 |
| | 4.5 Buffer Types | 15 | | 6.13 Memory | 61 |
| | 4.6 Connection of Unused Pins | 15 | | 6.14 Identification | 69 |
| 5 | Specifications | 16 | | 7 Applications, Implementation, and Layout | 70 |
| | 5.1 Absolute Maximum Ratings | 16 | | 7.1 Device Connection and Layout Fundamentals | 70 |
| | 5.2 ESD Ratings | 16 | | 7.2 Peripheral- and Interface-Specific Design Information | 73 |
| | 5.3 Recommended Operating Conditions | 16 | | 7.3 CapTIvate Technology Evaluation | 76 |
| | 5.4 Active Mode Supply Current Into V _{CC} Excluding External Current | 17 | | 8 Device and Documentation Support | 77 |
| | 5.5 Active Mode Supply Current Per MHz | 17 | | 8.1 Getting Started and Next Steps | 77 |
| | 5.6 Low-Power Mode (LPM0) Supply Currents Into V _{CC} Excluding External Current | 17 | | 8.2 Device Nomenclature | 77 |
| | 5.7 Low-Power Mode (LPM3, LPM4) Supply Currents (Into V _{CC}) Excluding External Current | 18 | | 8.3 Tools and Software | 79 |
| | 5.8 Low-Power Mode (LPMx.5) Supply Currents (Into V _{CC}) Excluding External Current | 20 | | 8.4 Documentation Support | 81 |
| | 5.9 Typical Characteristics - Low-Power Mode Supply Currents | 21 | | 8.5 Related Links | 82 |
| | 5.10 Thermal Resistance Characteristics | 22 | | 8.6 Community Resources | 82 |
| | 5.11 Timing and Switching Characteristics | 22 | | 8.7 Trademarks | 82 |
| 6 | Detailed Description | 43 | | 8.8 Electrostatic Discharge Caution | 83 |
| | | | | 8.9 Export Control Notice | 83 |
| | | | | 8.10 Glossary | 83 |
| | | | | 9 Mechanical, Packaging, and Orderable Information | 84 |

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision B to revision C

Changes from August 20, 2019 to December 10, 2019

Page

| | |
|---|--------------------|
| • Changed the note that begins "Supply voltage changes faster than 0.2 V/μs can trigger a BOR reset..." in Section 5.3, Recommended Operating Conditions | 16 |
| • Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, Recommended Operating Conditions | 16 |
| • Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, Recommended Operating Conditions | 16 |
| • Added the note "See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing" to Table 5-4, XT1 Crystal Oscillator (Low Frequency) | 24 |
| • Changed the note that begins "Requires external capacitors at both terminals..." in Table 5-4, XT1 Crystal Oscillator (Low Frequency) | 24 |
| • Added the $t_{TA, cap}$ parameter in Table 5-13, Timer_A | 30 |
| • Corrected the test conditions for the R_I parameter in Table 5-20, ADC, Power Supply and Input Range Conditions | 37 |
| • Added the note that begins " $t_{sample} = \ln(2^{n+1}) \times \tau$..." in Table 5-21, ADC, 10-Bit Timing Parameters | 37 |
| • Changed the CRC covered end address to 0x1AF5 in note (1) in Table 6-18, Device Descriptors | 60 |
| • Added "1.5-V reference factor" in Table 6-18, Device Descriptors | 61 |

Changes from revision A to revision B

Changes from November 8, 2018 to August 19, 2019

Page

| | |
|--|--------------------|
| • Updated Section 1.1, Features | 1 |
| • Changed CapTIvate BSWP demonstration board to CapTIvate phone demonstration board in note (11) on Section 5.7, Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current | 18 |
| • Changed CapTIvate BSWP demonstration board to CapTIvate phone demonstration board in note (19) on Section 5.7, Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current | 19 |
| • Added the $t_{TA, cap}$ parameter in Table 5-13, Timer_A | 30 |
| • Moved C_{REG} and $C_{ELECTRODE}$ from Section 5.3, Recommended Operating Conditions to Table 5-23, CapTIvate Electrical Characteristics | 39 |
| • Added test condition for $C_{ELECTRODE}$ in Table 5-23, CapTIvate Electrical Characteristics | 39 |
| • Changed the symbol and description of the DC_{CAPCLK} parameter in Table 5-23, CapTIvate Electrical Characteristics | 39 |
| • Moved the SNR parameter to Table 5-24, CapTIvate Signal-to-Noise Ratio Characteristics | 39 |
| • Updated Section 7.2.2, CapTIvate Peripheral | 74 |
| • Updated Section 8.2, Device Nomenclature | 77 |

Changes from initial release to revision A

Changes from January 12, 2018 to November 7, 2018

Page

| | |
|--|--------------------|
| • Removed "15-cm" from the "Proximity Sensing" item in Section 1.1, Features | 1 |
| • Changed list item "Wide supply voltage range from 3.6 V down to 1.8 V..." in Section 1.1, Features | 1 |
| • Updated Section 3.1, Related Products | 7 |
| • Changed HBM limit to ±1000 V and CDM limit to ±250 V in Section 5.2, ESD Ratings | 16 |
| • Changed the MIN value of the V_{CC} parameter from 2 V to 1.8 V in Section 5.3, Recommended Operating Conditions | 16 |
| • Changed the crystal in the footnote that begins "Characterized with a Seiko Crystal SC-32S crystal..." in Section 5.7, Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current | 18 |
| • Changed the crystal in the footnote that begins "Characterized with a Seiko Crystal SC-32S crystal..." in Section 5.8, Low-Power Mode (LPMx.5) Supply Currents (Into V_{CC}) Excluding External Current | 20 |
| • Added note on V_{SVSH-} and V_{SVSH+} parameters to Table 5-2, PMM, SVS and BOR | 22 |

- Changed the minimum V_{CC} from 2.0 V to 1.8 V in the test conditions for the f_{REFO} , df_{REFO}/dV_{CC} , and f_{DC} parameters and in note (2) in [Table 5-7, REFO](#)..... [26](#)
- Changed the minimum V_{CC} from 2.0 V to 1.8 V in the test conditions for the df_{VLO}/dV_{CC} parameter and in note (2) in [Table 5-8, Internal Very-Low-Power Low-Frequency Oscillator \(VLO\)](#)..... [27](#)
- Changed the minimum V_{CC} from 2.0 V to 1.8 V in the test conditions for the f_{MODOSC}/dV_{CC} parameter in [Table 5-9, Module Oscillator \(MODOSC\)](#) [27](#)
- Added the $t_{TA, cap}$ parameter in [Table 5-13, Timer_A](#)..... [30](#)
- Added the SNR parameter in [Table 5-23, CapTivate Electrical Characteristics](#) [39](#)
- Corrected bitfield from RTCCLK to RTCKSEL in table note that starts "Controlled by ..." in [Table 6-8, Clock Distribution](#) [48](#)
- Corrected bitfield from IRDSEL to IRDSSEL in [Section 6.10.8, Timers \(Timer0_A3, Timer1_A3\)](#), in the description that starts "The interconnection of Timer0_A3 and ..." [53](#)
- Corrected ADCINCHx column heading in [Table 6-13, ADC Channel Connections](#) [54](#)
- Corrected ADCINCHx column heading in [Table 6-13, ADC Channel Connections](#) [55](#)
- Added P1SELC information in [Table 6-28, Port P1, P2 Registers \(Base Address: 0200h\)](#)..... [64](#)
- Added P2SELC information in [Table 6-28, Port P1, P2 Registers \(Base Address: 0200h\)](#) [64](#)

3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

| DEVICE | PROGRAM FRAM + INFORMATION FRAM (bytes) | SRAM (bytes) | TA0,TA1 | eUSCI_A | eUSCI_B | 10-BIT ADC CHANNELS | CapTIvate TECHNOLOGY CHANNELS | GPIOs | PACKAGE |
|-------------------|---|--------------|---------------------------|---------|---------|---------------------|-------------------------------|-------|---------------|
| MSP430FR2522IRHL | 7424 + 256 | 2048 | 2, 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 8 | 15 | 20 RHL (VQFN) |
| MSP430FR2522IPW16 | 7424 + 256 | 2048 | 2, 3 × CCR ⁽³⁾ | 1 | 1 | 5 | 8 | 11 | 16 PW (TSSOP) |
| MSP430FR2512IRHL | 7424 + 256 | 2048 | 2, 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 | 15 | 20 RHL (VQFN) |
| MSP430FR2512IPW16 | 7424 + 256 | 2048 | 2, 3 × CCR ⁽³⁾ | 1 | 1 | 5 | 4 | 11 | 16 PW (TSSOP) |

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 9, or see the TI website at www.ti.com

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging

(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

[TI 16-bit and 32-bit microcontrollers](#)

High-performance, low-power solutions to enable the autonomous future

[Products for MSP430 ultra-low-power sensing and measurement microcontrollers](#)

One platform. One ecosystem. Endless possibilities.

[Companion Products for MSP430FR2522](#)

Review products that are frequently purchased or used in conjunction with this product.

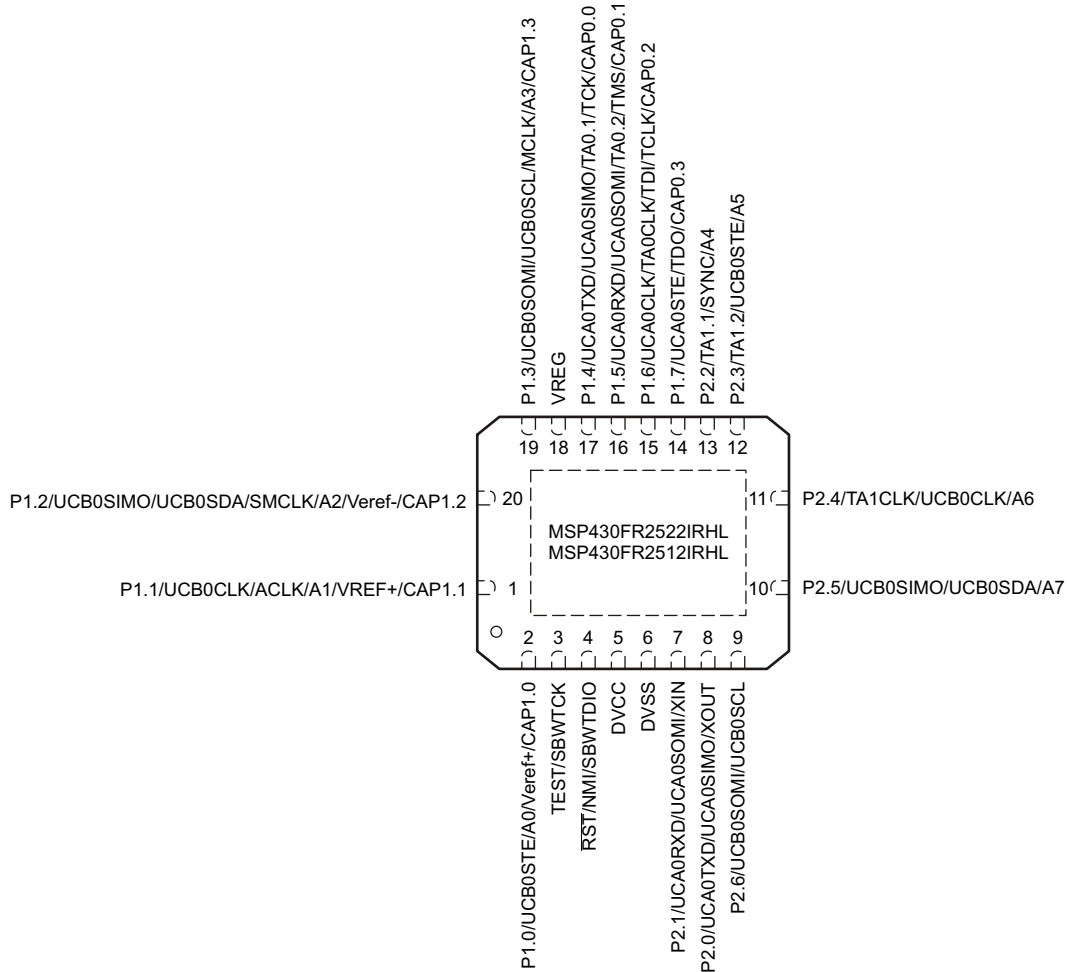
[Reference Designs](#)

Find reference designs leveraging the best in TI technology to solve your system-level challenges

4 Terminal Configuration and Functions

4.1 Pin Diagrams

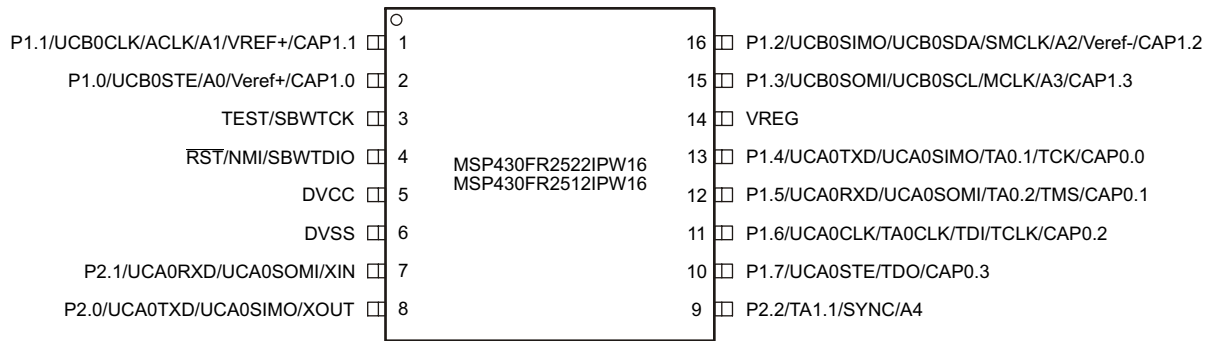
Figure 4-1 shows the pinout for the 20-pin RHL package.



NOTE: CAP1.x are available only on MSP430FR2522 device and NOT available on MSP430FR2512 device.

Figure 4-1. 20-Pin RHL Package (Top View)

Figure 4-2 shows the pinout for the 16-pin PW package.



NOTE: CAP1.x are available only on MSP430FR2522 device and NOT available on MSP430FR2512 device.

Figure 4-2. 16-Pin PW Package (Top View)

4.2 Pin Attributes

Table 4-1 lists the attributes of all pins.

Table 4-1. Pin Attributes

| PIN NUMBER | | SIGNAL NAME ^{(1) (2)} | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ |
|------------|------|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| RHL | PW16 | | | | | |
| 1 | 1 | P1.1 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0CLK | I/O | LVC MOS | DVCC | – |
| | | ACLK | I/O | LVC MOS | DVCC | – |
| | | CAP1.1 ⁽⁷⁾ | I/O | Analog | V _{REG} | – |
| | | A1 | I | Analog | DVCC | – |
| | | VREF+ | I | Analog | Power | – |
| 2 | 2 | P1.0 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0STE | I/O | LVC MOS | DVCC | – |
| | | CAP1.0 ⁽⁷⁾ | I/O | Analog | V _{REG} | – |
| | | A0 | I | Analog | DVCC | – |
| | | Veref+ | I | Analog | Power | – |
| 3 | 3 | TEST (RD) | I | LVC MOS | DVCC | OFF |
| | | SBWTCK | I | LVC MOS | DVCC | – |
| 4 | 4 | $\overline{\text{RST}}$ (RD) | I | LVC MOS | DVCC | OFF |
| | | NMI | I | LVC MOS | DVCC | – |
| | | SBWTDIO | I/O | LVC MOS | DVCC | – |
| 5 | 5 | DVCC | P | Power | DVCC | N/A |
| 6 | 6 | DVSS | P | Power | DVCC | N/A |
| 7 | 7 | P2.1 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0RXD | I | LVC MOS | DVCC | – |
| | | UCA0SOMI | I/O | LVC MOS | DVCC | – |
| | | XIN | I | LVC MOS | DVCC | – |
| 8 | 8 | P2.0 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0TXD | O | LVC MOS | DVCC | – |
| | | UCA0SIMO | I/O | LVC MOS | DVCC | – |
| | | XOUT | O | LVC MOS | DVCC | – |
| 9 | – | P2.6 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0SOMI | I/O | LVC MOS | DVCC | – |
| | | UCB0SCL | I/O | LVC MOS | DVCC | – |
| 10 | – | P2.5 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0SIMO | I/O | LVC MOS | DVCC | – |
| | | UCB0SDA | I/O | LVC MOS | DVCC | – |
| | | A7 | I | Analog | DVCC | – |
| 11 | – | P2.4 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | TA1CLK | I | LVC MOS | DVCC | – |
| | | UCB0CLK | I/O | LVC MOS | DVCC | – |
| | | A6 | I | Analog | DVCC | – |

(1) Signals names with (RD) denote the reset default pin name.

(2) To determine the pin mux encodings for each pin, see [Section 6.11](#).

(3) Signal Types: I = Input, O = Output, I/O = Input or Output

(4) Buffer Types: LVC MOS, Analog, or Power (see [Table 4-3](#))

(5) The power source shown in this table is the I/O power source, which may differ from the module power source.

(6) Reset States:

OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled

N/A = Not applicable

(7) MSP430FR2522 only

Table 4-1. Pin Attributes (continued)

| PIN NUMBER | | SIGNAL NAME ^{(1) (2)} | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE ⁽⁵⁾ | RESET STATE AFTER BOR ⁽⁶⁾ |
|------------|------|--------------------------------|----------------------------|----------------------------|-----------------------------|--------------------------------------|
| RHL | PW16 | | | | | |
| 12 | – | P2.3 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | TA1.2 | I/O | LVC MOS | DVCC | – |
| | | UCB0STE | I/O | LVC MOS | DVCC | – |
| | | A5 | I | Analog | DVCC | – |
| 13 | 9 | P2.2 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | TA1.1 | I/O | LVC MOS | DVCC | – |
| | | SYNC | I | LVC MOS | DVCC | – |
| | | A4 | I | Analog | DVCC | – |
| 14 | 10 | P1.7 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0STE | I/O | LVC MOS | DVCC | – |
| | | TDO | O | LVC MOS | DVCC | – |
| | | CAP0.3 | I/O | Analog | V _{REG} | – |
| 15 | 11 | P1.6 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0CLK | I/O | LVC MOS | DVCC | – |
| | | TA0CLK | I | LVC MOS | DVCC | – |
| | | TDI | I | LVC MOS | DVCC | – |
| | | TCLK | I | LVC MOS | DVCC | – |
| | | CAP0.2 | I/O | Analog | V _{REG} | – |
| 16 | 12 | P1.5 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0RXD | I | LVC MOS | DVCC | – |
| | | UCA0SOMI | I/O | LVC MOS | DVCC | – |
| | | TA0.2 | I/O | LVC MOS | DVCC | – |
| | | TMS | I | LVC MOS | DVCC | – |
| | | CAP0.1 | I/O | Analog | V _{REG} | – |
| 17 | 13 | P1.4 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCA0TXD | O | LVC MOS | DVCC | – |
| | | UCA0SIMO | I/O | LVC MOS | DVCC | – |
| | | TA0.1 | I/O | LVC MOS | DVCC | – |
| | | TCK | I | LVC MOS | DVCC | – |
| | | CAP0.0 | I/O | Analog | V _{REG} | – |
| 18 | 14 | VREG | P | Power | V _{REG} | N/A |
| 19 | 15 | P1.3 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0SOMI | I/O | LVC MOS | DVCC | – |
| | | UCB0SCL | I/O | LVC MOS | DVCC | – |
| | | MCLK | O | LVC MOS | DVCC | – |
| | | CAP1.3 ⁽⁷⁾ | I/O | Analog | V _{REG} | – |
| | | A3 | I | Analog | DVCC | – |
| 20 | 16 | P1.2 (RD) | I/O | LVC MOS | DVCC | OFF |
| | | UCB0SIMO | I/O | LVC MOS | DVCC | – |
| | | UCB0SDA | I/O | LVC MOS | DVCC | – |
| | | SMCLK | O | LVC MOS | DVCC | – |
| | | CAP1.2 ⁽⁷⁾ | I/O | Analog | V _{REG} | – |
| | | A2 | I | Analog | DVCC | – |
| | | Veref- | I | Analog | Power | – |

4.3 Signal Descriptions

Table 4-2 describes the signals for all device variants and package options.

Table 4-2. Signal Descriptions

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|-----------|-----------------------|------------|----|---|---|
| | | RHL | PW | | |
| ADC | A0 | 2 | 2 | I | Analog input A0 |
| | A1 | 1 | 1 | I | Analog input A1 |
| | A2 | 20 | 16 | I | Analog input A2 |
| | A3 | 19 | 15 | I | Analog input A3 |
| | A4 | 13 | 9 | I | Analog input A4 |
| | A5 | 12 | – | I | Analog input A5 |
| | A6 | 11 | – | I | Analog input A6 |
| | A7 | 10 | – | I | Analog input A7 |
| | Veref+ | 2 | 2 | I | ADC positive reference |
| | Veref- | 20 | 16 | I | ADC negative reference |
| CapTlvate | CAP0.0 | 17 | 13 | I/O | CapTlvate channel |
| | CAP0.1 | 16 | 12 | I/O | CapTlvate channel |
| | CAP0.2 | 15 | 11 | I/O | CapTlvate channel |
| | CAP0.3 | 14 | 10 | I/O | CapTlvate channel |
| | CAP1.0 ⁽²⁾ | 2 | 2 | I/O | CapTlvate channel |
| | CAP1.1 ⁽²⁾ | 1 | 1 | I/O | CapTlvate channel |
| | CAP1.2 ⁽²⁾ | 20 | 16 | I/O | CapTlvate channel |
| | CAP1.3 ⁽²⁾ | 19 | 15 | I/O | CapTlvate channel |
| SYNC | 13 | 9 | I | CapTlvate synchronous trigger input for processing and conversion | |
| Clock | ACLK | 1 | 1 | I/O | ACLK output |
| | MCLK | 19 | 15 | O | MCLK output |
| | SMCLK | 20 | 16 | O | SMCLK output |
| | XIN | 7 | 7 | I | Input terminal for crystal oscillator |
| | XOUT | 8 | 8 | O | Output terminal for crystal oscillator |
| Debug | SBWTCK | 3 | 3 | I | Spy-Bi-Wire input clock |
| | SBWTDIO | 4 | 4 | I/O | Spy-Bi-Wire data input/output |
| | TCK | 17 | 13 | I | Test clock |
| | TCLK | 15 | 11 | I | Test clock input |
| | TDI | 15 | 11 | I | Test data input |
| | TDO | 14 | 10 | O | Test data output |
| | TEST | 3 | 3 | I | Test mode pin – selected digital I/O on JTAG pins |
| | TMS | 16 | 12 | I | Test mode select |

(1) Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

(2) MSP430FR2522 only

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|-------------------------|----------------------------|------------|-----|----------------------------------|---|
| | | RHL | PW | | |
| GPIO | P1.0 | 2 | 2 | I/O | General-purpose I/O |
| | P1.1 | 1 | 1 | I/O | General-purpose I/O |
| | P1.2 | 20 | 16 | I/O | General-purpose I/O |
| | P1.3 | 19 | 15 | I/O | General-purpose I/O |
| | P1.4 | 17 | 13 | I/O | General-purpose I/O ⁽³⁾ |
| | P1.5 | 16 | 12 | I/O | General-purpose I/O ⁽³⁾ |
| | P1.6 | 15 | 11 | I/O | General-purpose I/O ⁽³⁾ |
| | P1.7 | 14 | 10 | I/O | General-purpose I/O ⁽³⁾ |
| | P2.0 | 8 | 8 | I/O | General-purpose I/O |
| | P2.1 | 7 | 7 | I/O | General-purpose I/O |
| | P2.2 | 13 | 9 | I/O | General-purpose I/O |
| | P2.3 | 12 | – | I/O | General-purpose I/O |
| | P2.4 | 11 | – | I/O | General-purpose I/O |
| | P2.5 | 10 | – | I/O | General-purpose I/O |
| P2.6 | 9 | – | I/O | General-purpose I/O | |
| I ² C | UCB0SCL ⁽⁴⁾ | 19 | 15 | I/O | eUSCI_B0 I ² C clock |
| | UCB0SDA ⁽⁴⁾ | 20 | 16 | I/O | eUSCI_B0 I ² C data |
| | UCB0SCL ⁽⁴⁾ | 9 | – | I/O | eUSCI_B0 I ² C clock |
| | UCB0SDA ⁽⁴⁾ | 10 | – | I/O | eUSCI_B0 I ² C data |
| Power | DVCC | 5 | 5 | P | Power supply |
| | DVSS | 6 | 6 | P | Power ground |
| | VREF+ | 1 | 1 | P | Output of positive reference voltage with ground as reference |
| | VREG | 18 | 14 | O | CapTIvate regulator external decoupling capacitor |
| SPI | UCA0STE | 14 | 10 | I/O | eUSCI_A0 SPI slave transmit enable |
| | UCA0CLK | 15 | 11 | I/O | eUSCI_A0 SPI clock input/output |
| | UCA0SOMI ⁽⁴⁾⁽⁵⁾ | 16 | 12 | I/O | eUSCI_A0 SPI slave out/master in |
| | UCA0SIMO ⁽⁴⁾⁽⁵⁾ | 17 | 13 | I/O | eUSCI_A0 SPI slave in/master out |
| | UCA0SOMI ⁽⁴⁾⁽⁵⁾ | 7 | 7 | I/O | eUSCI_A0 SPI slave out/master in |
| | UCA0SIMO ⁽⁴⁾⁽⁵⁾ | 8 | 8 | I/O | eUSCI_A0 SPI slave in/master out |
| | UCB0STE ⁽⁴⁾ | 2 | 2 | I/O | eUSCI_B0 slave transmit enable |
| | UCB0CLK ⁽⁴⁾ | 1 | 1 | I/O | eUSCI_B0 clock input/output |
| | UCB0SOMI ⁽⁴⁾ | 19 | 15 | I/O | eUSCI_B0 SPI slave out/master in |
| | UCB0SIMO ⁽⁴⁾ | 20 | 16 | I/O | eUSCI_B0 SPI slave in/master out |
| | UCB0STE ⁽⁴⁾ | 12 | – | I/O | eUSCI_B0 slave transmit enable |
| | UCB0CLK ⁽⁴⁾ | 11 | – | I/O | eUSCI_B0 clock input/output |
| UCB0SOMI ⁽⁴⁾ | 9 | – | I/O | eUSCI_B0 SPI slave out/master in | |
| UCB0SIMO ⁽⁴⁾ | 10 | – | I/O | eUSCI_B0 SPI slave in/master out | |
| System | NMI | 4 | 4 | I | Nonmaskable interrupt input |
| | RST | 4 | 4 | I | Active-low reset input |

(3) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.

(4) These signal assignments are controlled by the USCIARMP bit of the SYSCFG3 register or the USCIBRMP bit of the SYSCFG2 register. Only one group can be selected at one time.

(5) Signal assignments on these pins are controlled by the remap functionality and are selected by the USCIARMP bit in the SYSCFG3 register. Only one group can be selected at one time. The CLK and STE assignments are fixed and shared by both SPI function groups.

Table 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER | | PIN TYPE ⁽¹⁾ | DESCRIPTION |
|----------|------------------------|------------|----|-------------------------|--|
| | | RHL | PW | | |
| Timer_A | TA0.1 | 17 | 13 | I/O | Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs |
| | TA0.2 | 16 | 12 | I/O | Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs |
| | TA0CLK | 15 | 11 | I | Timer clock input TACLK for TA0 |
| | TA1.1 | 13 | 9 | I/O | Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs |
| | TA1.2 | 12 | – | I/O | Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs |
| | TA1CLK | 11 | – | I | Timer clock input TACLK for TA1 |
| UART | UCA0RXD ⁽⁴⁾ | 16 | 12 | I | eUSCI_A0 UART receive data |
| | UCA0TXD ⁽⁴⁾ | 17 | 13 | O | eUSCI_A0 UART transmit data |
| | UCA0RXD ⁽⁴⁾ | 7 | 7 | I | eUSCI_A0 UART receive data |
| | UCA0TXD ⁽⁴⁾ | 8 | 8 | O | eUSCI_A0 UART transmit data |
| QFN Pad | QFN thermal pad | Pad | – | – | QFN package exposed thermal pad. TI recommends connecting to V _{SS} . |

4.4 Pin Multiplexing

Pin multiplexing for this MCU is controlled by both register settings and operating modes (for example, if the MCU is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see [Section 6.11](#).

4.5 Buffer Types

[Table 4-3](#) defines the pin buffer types that are listed in [Table 4-1](#)

Table 4-3. Buffer Types

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (μ A) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|------------------------|-----------------|------------------|--------------|--------------------------------------|------------------------------------|--|
| LVC MOS | 3.0 V | Y ⁽¹⁾ | Programmable | See Section 5.11.4 | See Section 5.11.4 | |
| Analog | 3.0 V | N | N/A | N/A | N/A | See analog modules in Section 5 for details. |
| Power (DVCC) | 3.0 V | N | N/A | N/A | N/A | SVS enables hysteresis on DVCC. |
| Power (AVCC) | 3.0 V | N | N/A | N/A | N/A | |

(1) Only for input pins.

4.6 Connection of Unused Pins

[Table 4-4](#) lists the correct termination of unused pins.

Table 4-4. Connection of Unused Pins⁽¹⁾

| PIN | POTENTIAL | COMMENT |
|------------------------------------|------------------|---|
| Px.0 to Px.7 | Open | Switched to port function, output direction (PxDIR.n = 1) |
| $\overline{\text{RST}}/\text{NMI}$ | DV _{CC} | 47-k Ω pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown ⁽²⁾ |
| TEST | Open | This pin always has an internal pull-down enabled. |

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 1.1 nF when using MCUs with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|--------------------------------------|------|
| Voltage applied at DVCC pin to V _{SS} | -0.3 | 4.1 | V |
| Voltage applied to any pin in CapTlivate mode ⁽²⁾ | -0.3 | V _{REG} | V |
| Voltage applied to any other pin ⁽³⁾ | -0.3 | V _{CC} + 0.3 (4.1 V Max) | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, T _J | | 85 | °C |
| Storage temperature, T _{stg} ⁽⁴⁾ | -40 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This applies I/Os worked in CapTlivate mode.
- (3) All voltages referenced to V_{SS}.
- (4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|--|---|-----|-------------------|------|
| V _{CC} | Supply voltage applied at DVCC pin ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ | 1.8 | | 3.6 | V |
| V _{SS} | Supply voltage applied at DVSS pin | | 0 | | V |
| T _A | Operating free-air temperature | -40 | | 85 | °C |
| T _J | Operating junction temperature | -40 | | 85 | °C |
| C _{DVCC} | Recommended capacitor at DVCC ⁽⁵⁾ | 4.7 | 10 | | µF |
| f _{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽⁴⁾⁽⁶⁾ | No FRAM wait states (NWAITSx = 0) | | 8 | MHz |
| | | With FRAM wait states (NWAITSx = 1) ⁽⁷⁾ | 0 | 16 ⁽⁸⁾ | |
| f _{ACLK} | Maximum ACLK frequency | | | 40 | kHz |
| f _{SMCLK} | Maximum SMCLK frequency | | | 16 ⁽⁸⁾ | MHz |

- (1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
- (2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
- (4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in [Table 5-2](#).
- (5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
- (6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
- (8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

 See ⁽¹⁾

| PARAMETER | EXECUTION MEMORY | TEST CONDITION | FREQUENCY ($f_{MCLK} = f_{SMCLK}$) | | | | | | UNIT |
|-----------------------|------------------------------|----------------|---|-----|---|-----|---|-----|---------|
| | | | 1 MHz 0 WAIT STATES (NWAITS _x = 0) | | 8 MHz 0 WAIT STATES (NWAITS _x = 0) | | 16 MHz 1 WAIT STATE (NWAITS _x = 1) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, FRAM(0\%)}$ | FRAM 0% cache hit ratio | 3 V, 25°C | 454 | | 2620 | | 2935 | | μA |
| | | 3 V, 85°C | 471 | | 2700 | | 2980 3250 | | |
| $I_{AM, FRAM(100\%)}$ | FRAM 100% cache hit ratio | 3 V, 25°C | 191 | | 573 | | 950 | | μA |
| | | 3 V, 85°C | 199 | | 592 | | 974 1200 | | |
| $I_{AM, RAM}^{(2)}$ | RAM | 3 V, 25°C | 216 | | 772 | | 1300 | | μA |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. Characterized with program executing typical data processing.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency

Program and data entirely reside in FRAM. All execution is from FRAM.

(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

 $V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-------------------|--|--|--------------------|
| $dI_{AM,FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states | I_{AM} (75% cache hit rate) at 8 MHz – I_{AM} (75% cache hit rate) at 1 MHz / 7 MHz | 120 $\mu A/MHz$ |

5.6 Low-Power Mode (LPM0) Supply Currents Into V_{CC} Excluding External Current

 $V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | V_{CC} | FREQUENCY (f_{SMCLK}) | | | | | | UNIT |
|------------|----------|---------------------------|-----|-------|-----|--------|-----|---------|
| | | 1 MHz | | 8 MHz | | 16 MHz | | |
| | | TYP | MAX | TYP | MAX | TYP | MAX | |
| I_{LPM0} | 2 V | 145 | | 292 | | 395 | | μA |
| | 3 V | 155 | | 300 | | 394 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, f_{SMCLK} at specified frequency.

5.7 Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | | V_{CC} | -40°C | | 25°C | | 85°C | | UNIT |
|-------------------------|--|----------|-------|-----|------|-----|------|-----|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3,XT1}$ | Low-power mode 3, 12.5-pF crystal, includes SVS ⁽²⁾⁽³⁾⁽⁴⁾ | 3 V | 0.96 | | 1.11 | | 2.75 | 6.2 | μA |
| | | 2 V | 0.93 | | 1.08 | | 2.78 | | |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO, excludes SVS ⁽⁵⁾ | 3 V | 0.77 | | 0.92 | | 2.66 | 6.0 | μA |
| | | 2 V | 0.75 | | 0.90 | | 2.60 | | |
| $I_{LPM3,RTC}$ | Low-power mode 3, RTC, excludes SVS ⁽⁶⁾ | 3 V | 0.90 | | 1.05 | | 2.77 | | μA |
| $I_{LPM3,CapTivate,1}$ | Low-power mode 3, CapTivate, excludes SVS ⁽⁷⁾ | 3 V | | | 4.7 | | | | μA |
| $I_{LPM3,CapTivate,1}$ | Low-power mode 3, CapTivate, excludes SVS ⁽⁸⁾ | 3 V | | | 3.0 | | | | μA |
| $I_{LPM3,CapTivate,2}$ | Low-power mode 3, CapTivate, excludes SVS ⁽⁹⁾ | 3 V | | | 3.2 | | | | μA |
| $I_{LPM3,CapTivate,8}$ | Low-power mode 3, CapTivate, excludes SVS ⁽¹⁰⁾ | 3 V | | | 17 | | | | μA |
| $I_{LPM3,CapTivate,16}$ | Low-power mode 3, CapTivate, excludes SVS ⁽¹¹⁾ | 3 V | | | 38 | | | | μA |
| $I_{LPM4,SVS}$ | Low-power mode 4, includes SVS ⁽¹²⁾ | 3 V | 0.51 | | 0.64 | | 2.30 | | μA |
| | | 2 V | 0.49 | | 0.61 | | 2.25 | | |
| I_{LPM4} | Low-power mode 4, excludes SVS ⁽¹²⁾ | 3 V | 0.35 | | 0.48 | | 2.13 | | μA |
| | | 2 V | 0.34 | | 0.46 | | 2.10 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Not applicable for MCUs with HF crystal oscillator only.

(3) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.

(4) Low-power mode 3, 12.5-pF crystal, includes SVS test conditions:

Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),

$f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(5) Low-power mode 3, VLO, excludes SVS test conditions:

Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).

CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3)

$f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(6) RTC periodically wakes up every second with external 32768-Hz input as source.

(7) CapTivate technology works in LPM3 with one proximity sensor for wake on touch. [CapTivate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 800

(8) CapTivate technology works in LPM3 with one button, wake on touch. [CapTivate BSWP demonstration board](#) with 1.5-mm overlay, Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250

(9) CapTivate technology works in LPM3 with two self-capacitance buttons, wake on touch. [CapTivate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250

(10) CapTivate technology works in LPM3 with 8 self-capacitance buttons. The CPU enters active mode in between time cycles to configure the conversions and read the results. [CapTivate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250

(11) CapTivate technology works in LPM3 with 16 mutual-capacitance buttons. The CPU enters active mode in between time cycles to configure the conversions and read the results. [CapTivate phone demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0).

$f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250

(12) Low-power mode 4, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4), CPU and all clocks are disabled, WDT and RTC disabled

Low-Power Mode (LPM3, LPM4) Supply Currents (Into V_{CC}) Excluding External Current (continued)

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | | V_{CC} | -40°C | | 25°C | | 85°C | | UNIT |
|---|---|----------|-------|-----|------|-----|------|-----|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM4,VLO}$ | Low-power mode 4, RTC is sourced from VLO, excludes SVS ⁽¹³⁾ | 3 V | 0.43 | | 0.56 | | 2.21 | | μA |
| | | 2 V | 0.42 | | 0.55 | | 2.19 | | |
| $I_{LPM4,XT1}$ | Low-power mode 4, RTC is sourced from XT1, excludes SVS ⁽¹⁴⁾ | 3 V | 0.80 | | 0.96 | | 2.68 | | μA |
| | | 2 V | 0.79 | | 0.94 | | 2.64 | | |
| $I_{LPM4, CapTlvate, 1 proximity, wake on touch}$ | Low-power mode 4, CapTlvate, excludes SVS ⁽¹⁵⁾ | 3 V | | | 4.5 | | | | μA |
| $I_{LPM4, CapTlvate, 1 button, wake on touch}$ | Low-power mode 4, CapTlvate, excludes SVS ⁽¹⁶⁾ | 3 V | | | 2.7 | | | | μA |
| $I_{LPM4, CapTlvate, 2 buttons, wake on touch}$ | Low-power mode 4, CapTlvate, excludes SVS ⁽¹⁷⁾ | 3 V | | | 2.9 | | | | μA |
| $I_{LPM4, CapTlvate, 8 buttons}$ | Low-power mode 4, CapTlvate, excludes SVS ⁽¹⁸⁾ | 3 V | | | 18 | | | | μA |
| $I_{LPM4, CapTlvate, 16 buttons}$ | Low-power mode 4, CapTlvate, excludes SVS ⁽¹⁹⁾ | 3 V | | | 39 | | | | μA |

- (13) Low-power mode 4, VLO, excludes SVS test conditions:
Current for RTC clocked by VLO included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)
 $f_{XT1} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (14) Low-power mode 4, XT1, excludes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4)
 $f_{XT1} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (15) CapTlvate technology works in LPM4 with one proximity sensor for wake on touch. [CapTlvate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0). The VLO (10 kHz) sources the CapTlvate timer, no external crystal.
 $f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 800
- (16) CapTlvate technology works in LPM4 with one button, wake on touch. [CapTlvate BSWP demonstration board](#) with 1.5-mm overlay, Current for brownout included. SVS disabled (SVSHE = 0). The VLO (10 kHz) sources the CapTlvate timer, no external crystal.
 $f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250
- (17) CapTlvate technology works in LPM4 with two self-capacitance buttons, wake on touch. [CapTlvate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0). VLO (10 kHz) sources the CapTlvate timer, no external crystal.
 $f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250
- (18) CapTlvate technology works in LPM4 with 8 self-capacitance buttons. The CPU enters active mode in between time cycles to configure the conversions and read the results. [CapTlvate BSWP demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0). The VLO (10 kHz) sources the CapTlvate timer, no external crystal.
 $f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250
- (19) CapTlvate technology works in LPM4 with 16 mutual-capacitance buttons. The CPU enters active mode in between time cycles to configure the conversions and read the results. [CapTlvate phone demonstration board](#) with 1.5-mm overlay. Current for brownout included. SVS disabled (SVSHE = 0). The VLO (10 kHz) sources the CapTlvate timer, no external crystal.
 $f_{SCAN} = 8$ Hz, $f_{CONVER} = 2$ MHz, COUNTS = 250

5.8 Low-Power Mode (LPMx.5) Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V_{CC} | -40°C | | 25°C | | 85°C | | UNIT |
|-------------------|---|----------|-------|-----|-------|-----|-------|------|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5, XT1}$ | Low-power mode 3.5, 12.5-pF crystal, includes SVS ^{(1)(2) (3)} (also see Figure 5-3) | 3 V | 0.57 | | 0.63 | | 0.81 | 1.54 | μA |
| | | 2 V | 0.54 | | 0.60 | | 0.79 | | |
| $I_{LPM4.5, SVS}$ | Low-power mode 4.5, includes SVS ⁽⁴⁾ | 3 V | 0.23 | | 0.25 | | 0.31 | 0.45 | μA |
| | | 2 V | 0.21 | | 0.23 | | 0.29 | | |
| $I_{LPM4.5}$ | Low-power mode 4.5, excludes SVS ⁽⁵⁾ | 3 V | 0.027 | | 0.036 | | 0.080 | 0.15 | μA |
| | | 2 V | 0.022 | | 0.031 | | 0.073 | | |

- (1) Not applicable for MCUs with HF crystal oscillator only.
- (2) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
- (3) Low-power mode 3.5, 12.5-pF crystal, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = 0$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)
 $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz
- (5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5)
 $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

5.9 Typical Characteristics - Low-Power Mode Supply Currents

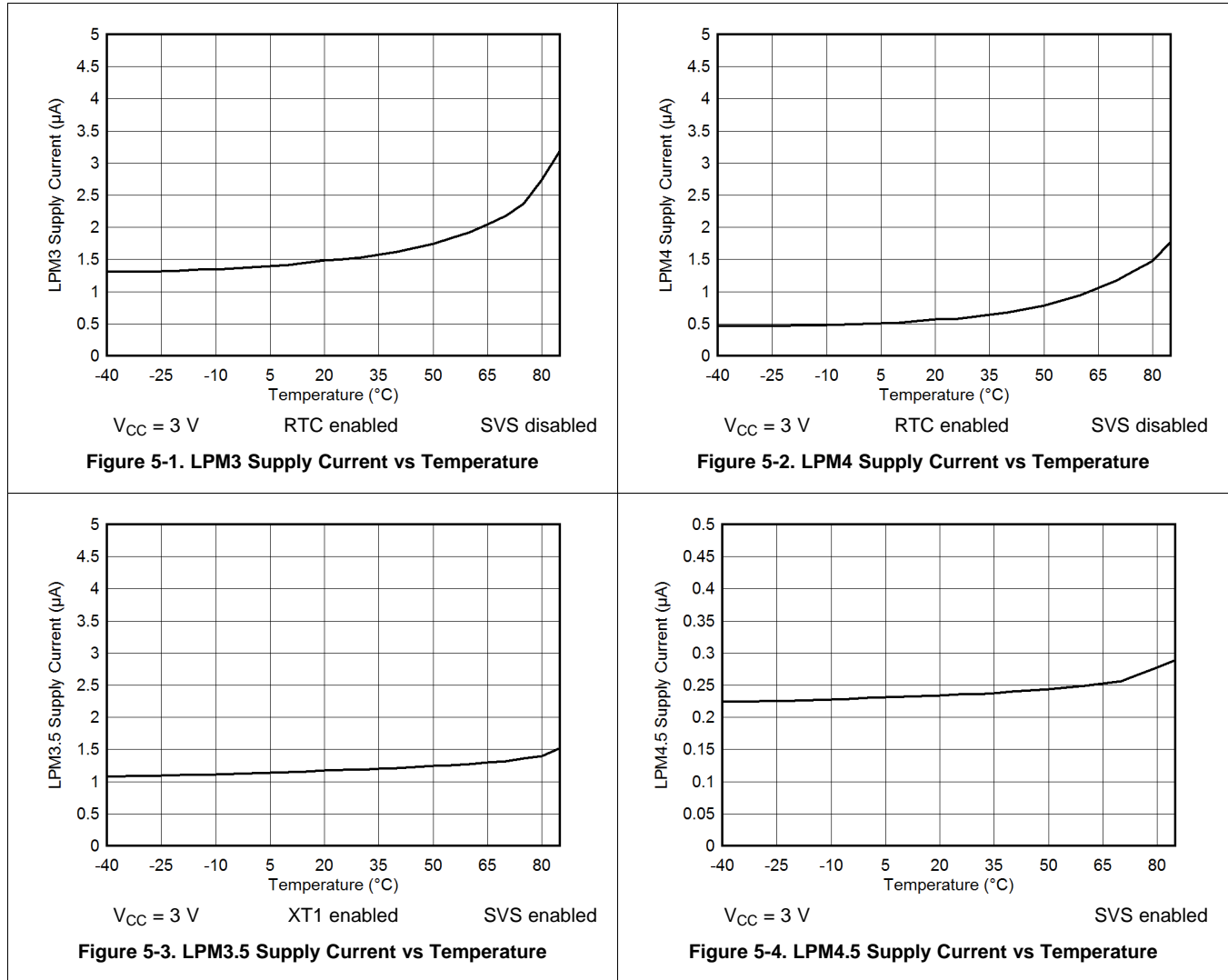


Table 5-1. Typical Characteristics – Current Consumption Per Module

| MODULE | TEST CONDITIONS | REFERENCE CLOCK | MIN | TYP | MAX | UNIT |
|---------|----------------------------------|--------------------|-----|-----|-----|--------|
| Timer_A | | Module input clock | | 5 | | μA/MHz |
| eUSCI_A | UART mode | Module input clock | | 7 | | μA/MHz |
| eUSCI_A | SPI mode | Module input clock | | 5 | | μA/MHz |
| eUSCI_B | SPI mode | Module input clock | | 5 | | μA/MHz |
| eUSCI_B | I ² C mode, 100 kbaud | Module input clock | | 5 | | μA/MHz |
| RTC | | 32 kHz | | 85 | | nA |
| CRC | From start to end of operation | MCLK | | 8.5 | | μA/MHz |

5.10 Thermal Resistance Characteristics

| THERMAL METRIC ⁽¹⁾ | | | VALUE ⁽²⁾ | UNIT |
|-------------------------------|---|---------------------|----------------------|------|
| R θ _{JA} | Junction-to-ambient thermal resistance, still air | VQFN 20 pin (RHL) | 37.8 | °C/W |
| | | TSSOP 16 pin (PW16) | 101.7 | |
| R θ _{JC} | Junction-to-case (top) thermal resistance | VQFN 20 pin (RHL) | 34.1 | °C/W |
| | | TSSOP 16 pin (PW16) | 33.7 | |
| R θ _{JB} | Junction-to-board thermal resistance | VQFN 20 pin (RHL) | 15.3 | °C/W |
| | | TSSOP 16 pin (PW16) | 47.5 | |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC (R θ _{JC}) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

5.11 Timing and Switching Characteristics

5.11.1 Power Supply Sequencing

Table 5-2 lists the characteristics of the SVS and BOR.

Table 5-2. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|-------------------------|------|------|------|------|
| V _{BOR, safe} | Safe BOR power-down level ⁽¹⁾ | | 0.1 | | | V |
| t _{BOR, safe} | Safe BOR reset delay ⁽²⁾ | | 10 | | | ms |
| I _{SVSH, AM} | SVS _H current consumption, active mode | V _{CC} = 3.6 V | | | 1.5 | μA |
| I _{SVSH, LPM} | SVS _H current consumption, low-power modes | V _{CC} = 3.6 V | | 240 | | nA |
| V _{SVSH-} | SVS _H power-down level ⁽³⁾ | | 1.71 | 1.80 | 1.87 | V |
| V _{SVSH+} | SVS _H power-up level ⁽³⁾ | | 1.76 | 1.88 | 1.99 | V |
| V _{SVSH_hys} | SVS _H hysteresis | | | 80 | | mV |
| t _{PD, SVSH, AM} | SVS _H propagation delay, active mode | | | | 10 | μs |
| t _{PD, SVSH, LPM} | SVS _H propagation delay, low-power modes | | | | 100 | μs |

- (1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
- (2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
- (3) For additional information, see the [Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design](#).

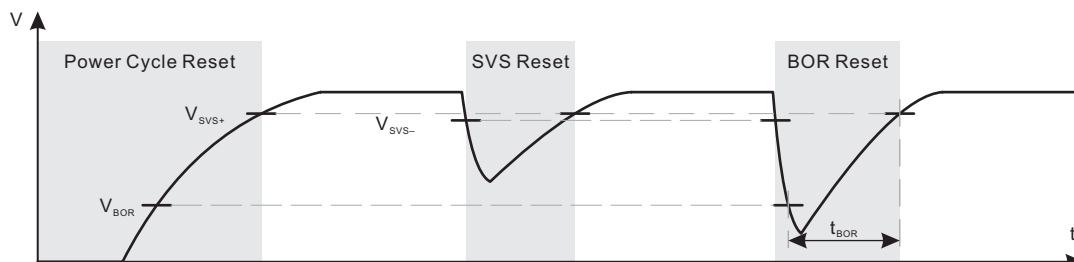


Figure 5-5. Power Cycle, SVS, and BOR Reset Conditions

5.11.2 Reset Timing

Table 5-3 lists the timing characteristics of wakeup from LPMs and reset.

Table 5-3. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----------------|-----------------|-----|-----|----------------------------------|------|
| t _{WAKE-UP FRAM} | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wakeup ⁽¹⁾ | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM0} | Wake-up time from LPM0 to active mode ⁽¹⁾ | | 3 V | | | 200 + 2.5 / f _{DCCO} | ns |
| t _{WAKE-UP LPM3} | Wake-up time from LPM3 to active mode ⁽²⁾ | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM4} | Wake-up time from LPM4 to active mode | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM3.5} | Wake-up time from LPM3.5 to active mode ⁽²⁾ | | 3 V | | 350 | | μs |
| t _{WAKE-UP LPM4.5} | Wake-up time from LPM4.5 to active mode ⁽²⁾ | SVSHE = 1 | 3 V | | 350 | | μs |
| | | SVSHE = 0 | | | 1 | | ms |
| t _{WAKE-UP-RESET} | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽²⁾ | | 3 V | | 1 | | ms |
| t _{RESET} | Pulse duration required at $\overline{\text{RST}}$ /NMI pin to accept a reset | | 3 V | | 2 | | μs |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

5.1.1.3 Clock Specifications

Table 5-4 lists the characteristics of the LF XT1.

Table 5-4. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|--|---|-----------------|-----|--------|------|------|
| f _{XT1, LF} | XT1 oscillator crystal, low frequency | LFXTBYPASS = 0 | | | 32768 | | Hz |
| DC _{XT1, LF} | XT1 oscillator LF duty cycle | Measured at MCLK, f _{LFXT} = 32768 Hz | | 30% | | 70% | |
| f _{XT1, SW} | XT1 oscillator logic-level square-wave input frequency | LFXTBYPASS = 1 ⁽³⁾⁽⁴⁾ | | | 32.768 | | kHz |
| DC _{XT1, SW} | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | | 40% | | 60% | |
| OA _{LFXT} | Oscillation allowance for LF crystals ⁽⁵⁾ | LFXTBYPASS = 0, LFXTDRIVE = {3}, f _{LFXT} = 32768 Hz, C _{L,eff} = 12.5 pF | | | 200 | | kΩ |
| C _{L,eff} | Integrated effective load capacitance ⁽⁶⁾ | See ⁽⁷⁾ | | | 1 | | pF |
| t _{START, LFXT} | Start-up time ⁽⁸⁾ | f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF | | | 1000 | | ms |
| f _{Fault, LFXT} | Oscillator fault frequency ⁽⁹⁾ | XTS = 0 ⁽¹⁰⁾ | | 0 | | 3500 | Hz |

- (1) To improve EMI on the LFXT oscillator, observe the following guidelines:
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) See [MSP430 32-kHz Crystal Oscillators](#) for details on crystal section, layout, and testing.
- (3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DC_{LFXT, SW}.
- (4) Maximum frequency of operation of the entire device cannot be exceeded.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For LFXTDRIVE = {0}, C_{L,eff} = 3.7 pF
 - For LFXTDRIVE = {1}, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - For LFXTDRIVE = {2}, 6 pF ≤ C_{L,eff} ≤ 10 pF
 - For LFXTDRIVE = {3}, 6 pF ≤ C_{L,eff} ≤ 12 pF
- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
- (7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
- (8) Includes start-up counter of 1024 clock cycles.
- (9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.
- (10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the frequency characteristics of the FLL.

Table 5-5. DCO FLL, Frequency

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-------|-----|------|------|
| f _{DCO, FLL} | FLL lock frequency, 16 MHz, 25°C | Measured at MCLK, Internal trimmed REFO as reference | 3 V | -1.0% | | 1.0% | |
| | FLL lock frequency, 16 MHz, -40°C to 85°C | | 3 V | -2.0% | | 2.0% | |
| | FLL lock frequency, 16 MHz, -40°C to 85°C | Measured at MCLK, XT1 crystal as reference | 3 V | -0.5% | | 0.5% | |

Table 5-5. DCO FLL, Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|-------------------------------|--|-----------------|-----|--------|-----|------|
| f _{DUTY} | Duty cycle | Measured at MCLK, XT1 crystal as reference | 3 V | 40% | 50% | 60% | |
| Jitter _{cc} | Cycle-to-cycle jitter, 16 MHz | | 3 V | | 0.25% | | |
| Jitter _{long} | Long term jitter, 16 MHz | | 3 V | | 0.022% | | |
| t _{FLL, lock} | FLL lock time, 16MHz | | 3 V | | 280 | | ms |

Table 5-6 lists the characteristics of the DCO.

Table 5-6. DCO Frequency

over recommended operating free-air temperature (unless otherwise noted) (see Figure 5-6)

| PARAMETER | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--|-----------------|------|------|
| f _{DCO, 16MHz} DCO frequency, 16 MHz | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 7.1 | MHz |
| | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 11.8 | |
| | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 17 | |
| | DCORSEL = 101b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 27.7 | |
| f _{DCO, 12MHz} DCO frequency, 12 MHz | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 5.5 | MHz |
| | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 9.1 | |
| | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 13.1 | |
| | DCORSEL = 100b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 21.5 | |
| f _{DCO, 8MHz} DCO frequency, 8 MHz | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 3.7 | MHz |
| | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 6.3 | |
| | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 9.0 | |
| | DCORSEL = 011b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 14.9 | |
| f _{DCO, 4MHz} DCO frequency, 4 MHz | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 1.9 | MHz |
| | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 3.2 | |
| | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 4.6 | |
| | DCORSEL = 010b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 7.8 | |
| f _{DCO, 2MHz} DCO frequency, 2 MHz | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 0.96 | MHz |
| | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 1.6 | |
| | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 2.3 | |
| | DCORSEL = 001b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 4.0 | |

Table 5-6. DCO Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted) (see [Figure 5-6](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--|-----------------|------|------|
| f _{DCO, 1MHz} DCO frequency, 1 MHz | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 0 | 3 V | 0.5 | MHz |
| | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 000b, DCO = 511 | | 0.85 | |
| | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 0 | | 1.2 | |
| | DCORSEL = 000b, DISMOD = 1b, DCOFTRIMEN = 1b, DCOFTRIM = 111b, DCO = 511 | | 2.0 | |

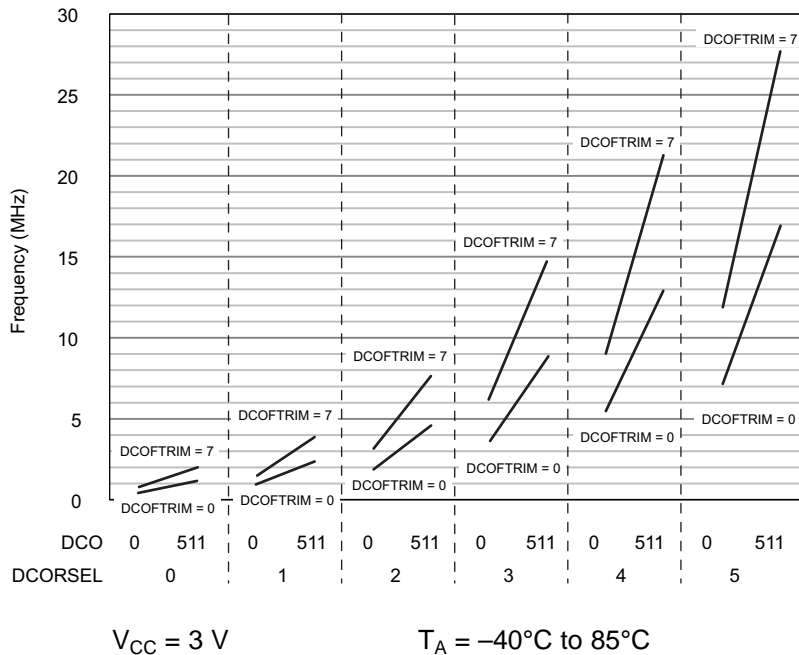


Figure 5-6. Typical DCO Frequency

[Table 5-7](#) lists the characteristics of the REFO.

Table 5-7. REFO

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---|----------------|-------|-------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | | 15 | | μA |
| f _{REFO} | REFO calibrated frequency | Measured at MCLK | | 32768 | | Hz |
| | REFO absolute calibrated tolerance | -40°C to 85°C | 1.8 V to 3.6 V | -3.5% | +3.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at MCLK ⁽¹⁾ | 3 V | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at MCLK at 25°C ⁽²⁾ | 1.8 V to 3.6 V | 1 | | %/V |
| f _{DC} | REFO duty cycle | Measured at MCLK | 1.8 V to 3.6 V | 40% | 50% | 60% |
| t _{START} | REFO start-up time | 40% to 60% duty cycle | | 50 | | μs |

(1) Calculated using the box method: (MAX(-40°C to 85°C) – MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the VLO.

Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|------|
| f _{VLO} | VLO frequency | Measured at MCLK | 3 V | 10 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at MCLK ⁽¹⁾ | 3 V | 0.5 | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at MCLK ⁽²⁾ | 1.8 V to 3.6 V | 4 | %/V |
| f _{VLO,DC} | Duty cycle | Measured at MCLK | 3 V | 50% | |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

NOTE

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see Table 5-8).

Table 5-9 lists the characteristics of the MODOSC.

Table 5-9. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------------|---------------------------------------|-----------------|-----------------|-----|-------|-----|------|
| f _{MODOSC} | MODOSC frequency | | 3 V | 3.8 | 4.8 | 5.8 | MHz |
| f _{MODOSC} /dT | MODOSC frequency temperature drift | | 3 V | | 0.102 | | %/°C |
| f _{MODOSC} /dV _{CC} | MODOSC frequency supply voltage drift | | 1.8 V to 3.6 V | | 1.02 | | %/V |
| f _{MODOSC,DC} | Duty cycle | | 3 V | 40% | 50% | 60% | |

5.11.4 Digital I/Os

Table 5-10 lists the characteristics of the digital inputs.

Table 5-10. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 2 V | 0.90 | | 1.50 | V |
| | | | 3 V | 1.35 | | 2.25 | |
| V _{IT-} | Negative-going input threshold voltage | | 2 V | 0.50 | | 1.10 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 2 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.2 | |
| R _{Pull} | Pullup or pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _{I,dig} | Input capacitance, digital only port pins | V _{IN} = V _{SS} or V _{CC} | | | 3 | | pF |
| C _{I,ana} | Input capacitance, port pins with shared analog functions | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |
| I _{lkg(Px.y)} | High-impedance leakage current of GPIO pins | See ⁽¹⁾ ⁽²⁾ | 2 V, 3 V | -20 | | 20 | nA |
| I _{lkg(Px.y)} | High-impedance leakage current of GPIO pins shared with CapTlvate functionality | See ⁽¹⁾ ⁽²⁾ ⁽³⁾ | 2 V, 3 V | -30 | | 30 | nA |
| t _(int) | External interrupt timing (external trigger pulse duration to set interrupt flag) ⁽⁴⁾ | Ports with interrupt capability (see block diagram and terminal function descriptions) | 2 V, 3 V | 50 | | | ns |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

(3) Applies only to GPIOs that are shared with CapTlvate I/Os

(4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Table 5-11 lists the characteristics of the digital outputs.

Table 5-11. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----------------|-----|-----|------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -3 mA ⁽¹⁾ | 2 V | 1.4 | | 2.0 | V |
| | | I _(OHmax) = -5 mA ⁽¹⁾ | 3 V | 2.4 | | 3.0 | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 3 mA ⁽¹⁾ | 2 V | 0.0 | | 0.60 | V |
| | | I _(OHmax) = 5 mA ⁽¹⁾ | 3 V | 0.0 | | 0.60 | |
| f _{Port_CLK} | Clock output frequency | C _L = 20 pF ⁽²⁾ | 2 V | 16 | | | MHz |
| | | | 3 V | 16 | | | |
| t _{rise,dig} | Port output rise time, digital only port pins | C _L = 20 pF | 2 V | | 10 | | ns |
| | | | 3 V | | 7 | | |
| t _{fall,dig} | Port output fall time, digital only port pins | C _L = 20 pF | 2 V | | 10 | | ns |
| | | | 3 V | | 5 | | |

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.11.4.1 Typical Characteristics – Outputs at 3 V and 2 V



Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

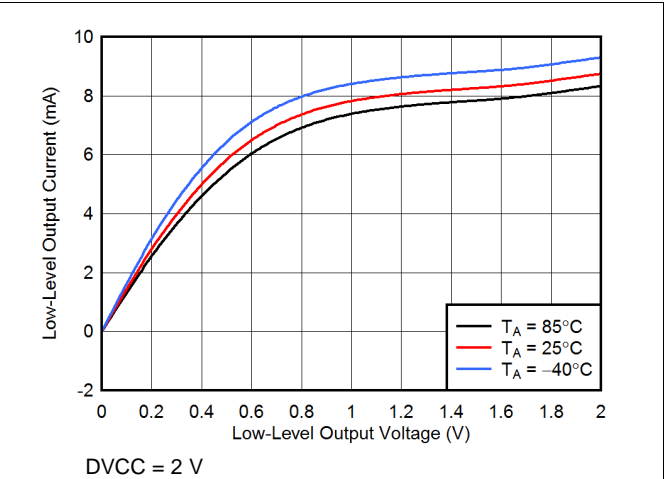


Figure 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

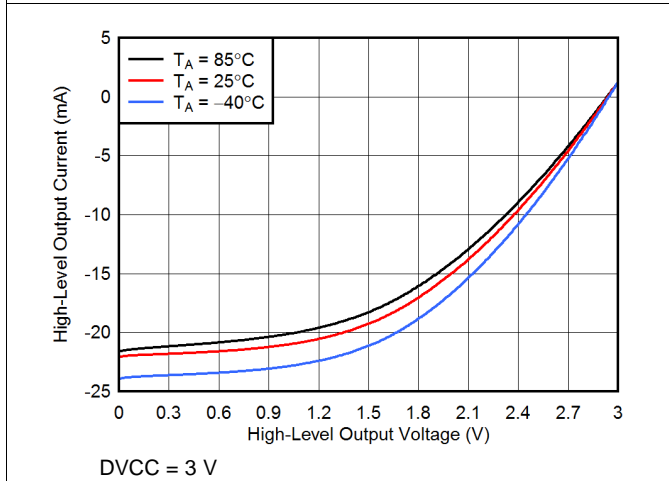


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

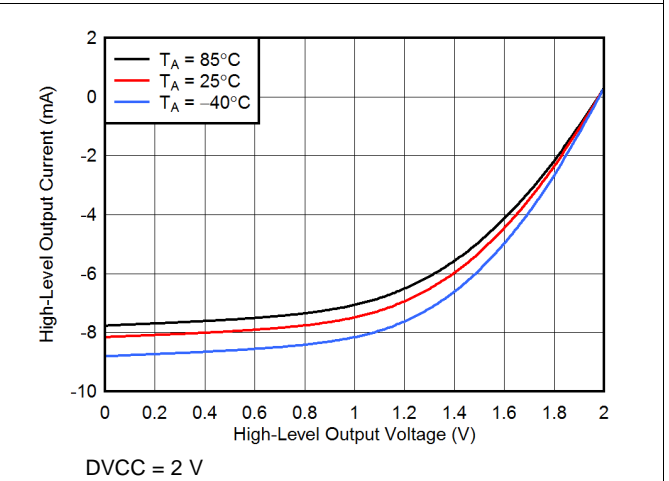


Figure 5-10. Typical High-Level Output Current vs High-Level Output Voltage

5.11.5 VREF+ Built-in Reference

Table 5-12 lists the characteristics of the VREF+.

Table 5-12. VREF+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|--------------------|---|-------------------------------------|----------|------|------|-------|---|
| V _{REF+} | Positive built-in reference voltage | EXTREFEN = 1 with 1-mA load current | 2 V, 3 V | 1.15 | 1.19 | 1.23 | V |
| TC _{REF+} | Temperature coefficient of built-in reference voltage | | | 30 | | μV/°C | |

5.11.6 Timer_A

Table 5-13 lists the characteristics of Timer_A.

Table 5-13. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|---|----------|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10% | 2 V, 3 V | | 16 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 2 V, 3 V | 20 | | ns |

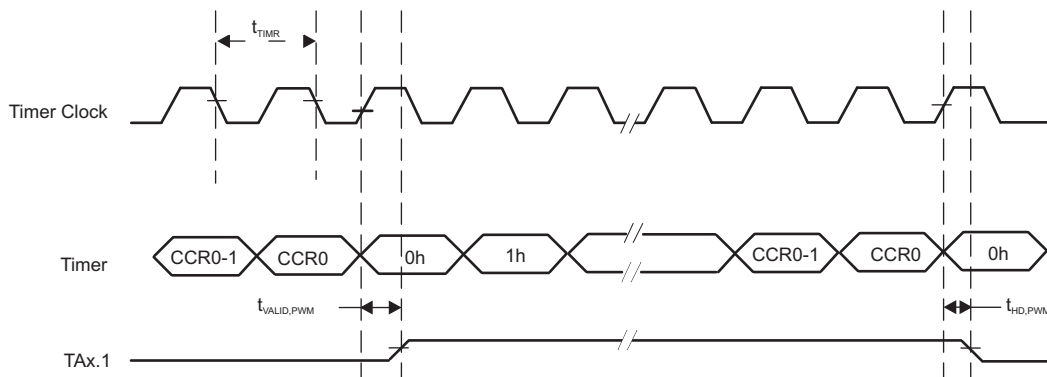


Figure 5-11. Timer PWM Mode

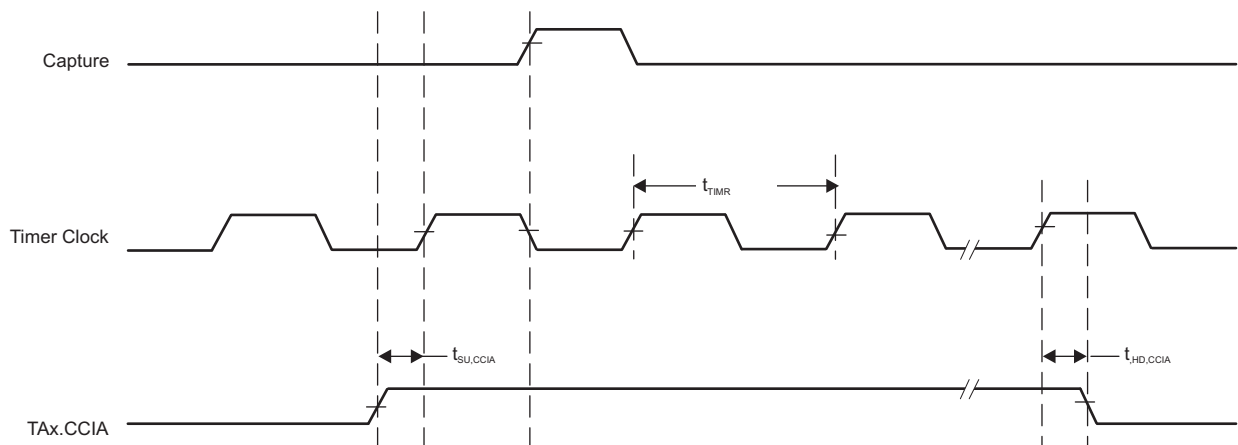


Figure 5-12. Timer Capture Mode

5.11.7 eUSCI

Table 5-14 lists the supported frequencies of the eUSCI in UART mode.

Table 5-14. eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|---|--|-----------------|-----|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10% | 2 V, 3 V | | 16 | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in Mbaud) | | 2 V, 3 V | | 5 | MHz |

Table 5-15 lists the characteristics of the eUSCI in UART mode.

Table 5-15. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|----------------|---|-----------------|-----------------|-----|------|
| t _t | UART receive deglitch time ⁽¹⁾ | UCGLITx = 0 | 2 V, 3 V | 12 | ns |
| | | UCGLITx = 1 | | 40 | |
| | | UCGLITx = 2 | | 68 | |
| | | UCGLITx = 3 | | 110 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-16 lists the supported frequencies of the eUSCI in SPI master mode.

Table 5-16. eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|-----------------------------|--|-----|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, MODCLK Duty cycle = 50% ±10% | | 8 | MHz |

Table 5-17 lists the characteristics of the eUSCI in SPI master mode.

Table 5-17. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|--|-----------------|-----|-----|---------------|
| t _{STE,LEAD} STE lead time, STE active to clock | UCSTEM = 0, UCMODEx = 01 or 10 | | 1 | | UCxCLK cycles |
| | UCSTEM = 1, UCMODEx = 01 or 10 | | | | |
| t _{STE,LAG} STE lag time, last clock to STE inactive | UCSTEM = 0, UCMODEx = 01 or 10 | | 1 | | UCxCLK cycles |
| | UCSTEM = 1, UCMODEx = 01 or 10 | | | | |
| t _{SU,MI} SOMI input data setup time | | 2 V | 48 | | ns |
| | | 3 V | 37 | | |
| t _{HD,MI} SOMI input data hold time | | 2 V | 0 | | ns |
| | | 3 V | 0 | | |
| t _{VALID,MO} SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 2 V | | 20 | ns |
| | | 3 V | | 20 | |
| t _{HD,MO} SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | -6 | | ns |
| | | 3 V | -5 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-13 and Figure 5-14.

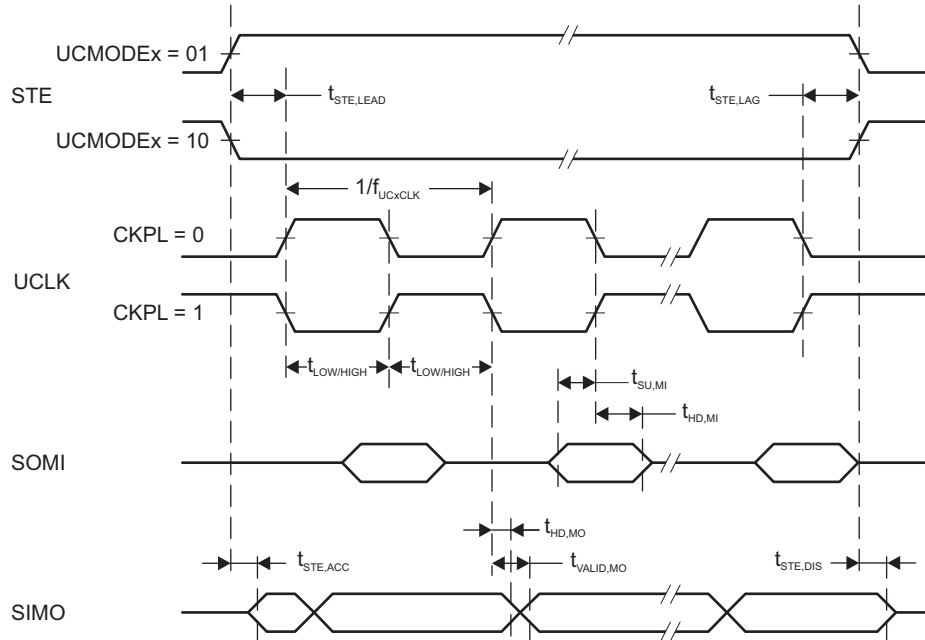


Figure 5-13. SPI Master Mode, CKPH = 0

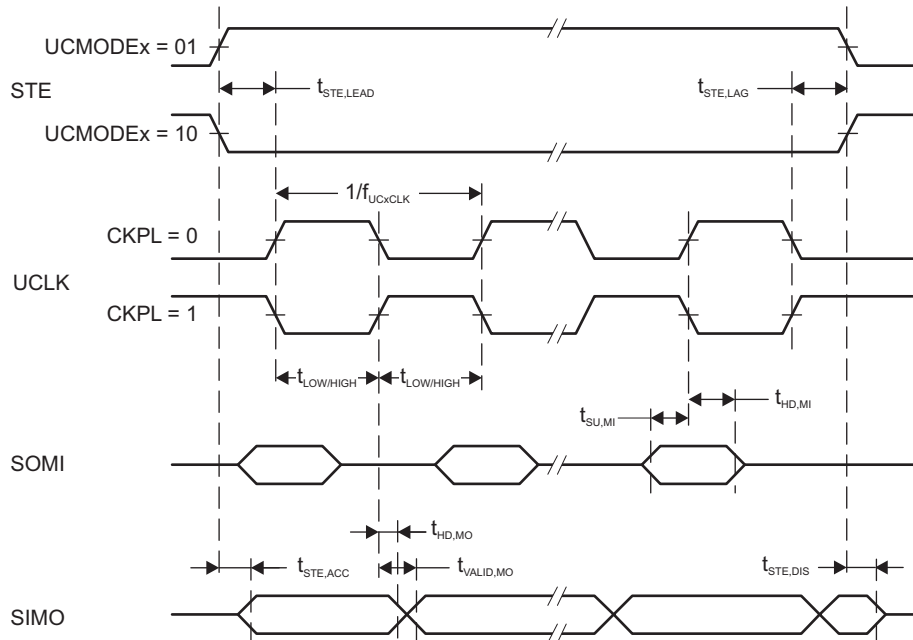


Figure 5-14. SPI Master Mode, CKPH = 1

Table 5-18 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-18. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE active to clock | | 2 V | 55 | | ns |
| | | | 3 V | 45 | | |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | | 2 V | 20 | | ns |
| | | | 3 V | 20 | | |
| t _{STE,ACC} | STE access time, STE active to SOMI data out | | 2 V | | 65 | ns |
| | | | 3 V | | 40 | |
| t _{STE,DIS} | STE disable time, STE inactive to SOMI high impedance | | 2 V | | 40 | ns |
| | | | 3 V | | 35 | |
| t _{SU,SI} | SIMO input data setup time | | 2 V | 8 | | ns |
| | | | 3 V | 6 | | |
| t _{HD,SI} | SIMO input data hold time | | 2 V | 12 | | ns |
| | | | 3 V | 12 | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 2 V | | 68 | ns |
| | | | 3 V | | 42 | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 5 | | ns |
| | | | 3 V | 5 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).

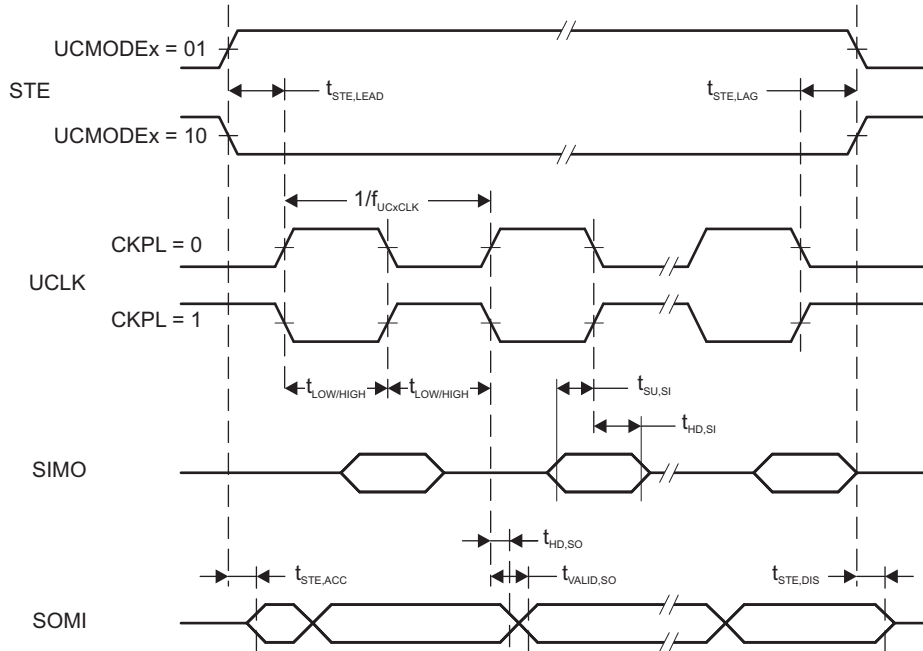


Figure 5-15. SPI Slave Mode, CKPH = 0

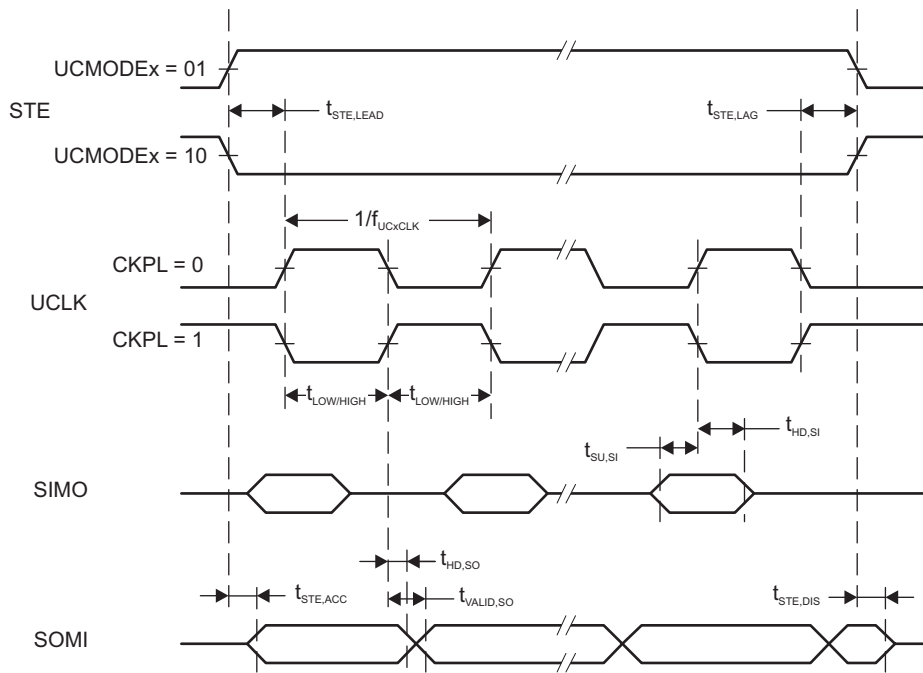


Figure 5-16. SPI Slave Mode, CKPH = 1

Table 5-19 lists the characteristics of the eUSCI in I²C mode.

Table 5-19. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|--|-----------------|------------|-----|-----|------|
| f _{eUSCI} eUSCI input clock frequency | Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ±10% | | | | 16 | MHz |
| f _{SCL} SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} Hold time (repeated) START | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 4.0 0.6 | | | μs |
| t _{SU,STA} Setup time for a repeated START | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 4.7 0.6 | | | μs |
| t _{HD,DAT} Data hold time | | 2 V, 3 V | 0 | | | ns |
| t _{SU,DAT} Data setup time | | 2 V, 3 V | 250 | | | ns |
| t _{SU,STO} Setup time for STOP | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 4.0 0.6 | | | μs |
| t _{SP} Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 50 | | 600 | ns |
| | UCGLITx = 1 | | 25 | 300 | | |
| | UCGLITx = 2 | | 12.5 | 150 | | |
| | UCGLITx = 3 | | 6.3 | 75 | | |
| t _{TIMEOUT} Clock low time-out | UCCLTOx = 1 | 2 V, 3 V | | 27 | | ms |
| | UCCLTOx = 2 | | | 30 | | |
| | UCCLTOx = 3 | | | 33 | | |

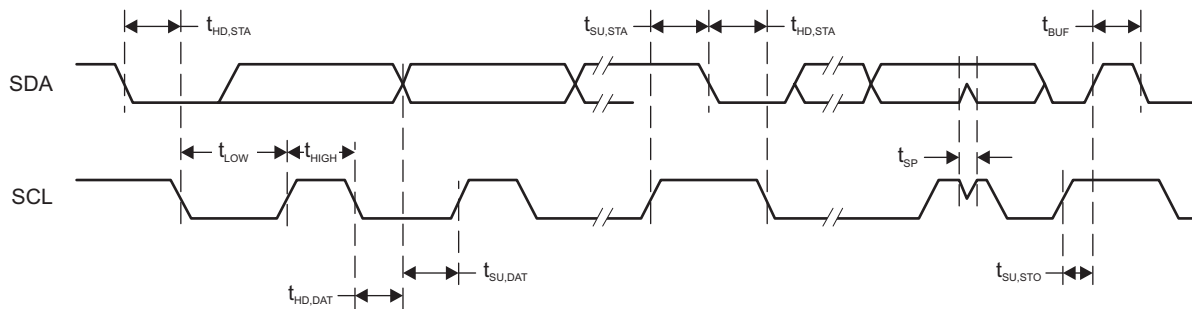


Figure 5-17. I²C Mode Timing

5.11.8 ADC

Table 5-20 lists the characteristics of the ADC power supply and input range conditions.

Table 5-20. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-------|-----|------------------|------|
| DV _{CC} | ADC supply voltage | | 2.0 | | 3.6 | V |
| V _(Ax) | Analog input voltage range | All ADC pins | 0 | | DV _{CC} | V |
| I _{ADC} | Operating supply current into DV _{CC} terminal, reference current not included, repeat-single-channel mode | f _{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b | 2 V | 185 | | μA |
| | | 3 V | | 207 | | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad | 2.2 V | 2.5 | 3.5 | pF |
| R _I | Input MUX ON resistance | DV _{CC} = 2 V, 0 V ≤ V _{Ax} ≤ DV _{CC} | | | 36 | kΩ |

Table 5-21 lists the ADC 10-bit timing parameters.

Table 5-21. ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|---|---|--------------|------|---------------------------------|------|-----|
| f _{ADCCLK} | For specified performance of ADC linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz | |
| f _{ADCOSC} | Internal ADC oscillator (MODOSC) | ADCDIV = 0, f _{ADCCLK} = f _{ADCOSC} | 2 V to 3.6 V | 3.8 | 4.8 | 5.8 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f _{ADCOSC} = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | μs |
| | | External f _{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0 | 2 V to 3.6 V | | 12 × 1 / f _{ADCCLK} | | |
| t _{ADCON} | Turnon settling time of the ADC | The error in a conversion started after t _{ADCON} is less than ±0.5 LSB. Reference and input signal are already settled. | | | 100 | ns | |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 36000 Ω, C _I = 3.5 pF. Approximately 8 Tau (τ) are required for an error of less than ±0.5 LSB. ⁽¹⁾ | 3 V | 2.0 | | μs | |

(1) $t_{\text{Sample}} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

Table 5-22 lists the ADC 10-bit linearity parameters.

Table 5-22. ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------|---|---|-----------------|-------|------|------|-------|
| E _I | Integral linearity error (10-bit mode) | V _{ref+} reference | 2.4 V to 3.6 V | -2 | | 2 | LSB |
| | Integral linearity error (8-bit mode) | | 2.0 V to 3.6 V | -2 | | 2 | |
| E _D | Differential linearity error (10-bit mode) | V _{ref+} reference | 2.4 V to 3.6 V | -1 | | 1 | LSB |
| | Differential linearity error (8-bit mode) | | 2.0 V to 3.6 V | -1 | | 1 | |
| E _O | Offset error (10-bit mode) | V _{ref+} reference | 2.4 V to 3.6 V | -6.5 | | 6.5 | mV |
| | Offset error (8-bit mode) | | 2.0 V to 3.6 V | -6.5 | | 6.5 | |
| E _G | Gain error (10-bit mode) | V _{ref+} as reference | 2.4 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| | Gain error (8-bit mode) | V _{ref+} as reference | 2.0 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| E _T | Total unadjusted error (10-bit mode) | V _{ref+} as reference | 2.4 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| | Total unadjusted error (8-bit mode) | V _{ref+} as reference | 2.0 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| V _{SENSOR} | See ⁽¹⁾ | ADCON = 1, INCH = 0Ch, T _A = 0°C | 3 V | | 913 | | mV |
| TC _{SENSOR} | See ⁽²⁾ | ADCON = 1, INCH = 0Ch | 3 V | | 3.35 | | mV/°C |
| t _{SENSOR} (sample) | Sample time required if channel 12 is selected ⁽³⁾ | ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, AM and all LPMs above LPM3 | 3 V | | 30 | | μs |
| | | ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, LPM3 | 3 V | | 100 | | |

- (1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for 30°C and 85°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, } ^\circ\text{C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor on time, t_{SENSOR(on)}.

5.11.9 CapTlvate

Table 5-23 lists the characteristics of the CapTlvate module.

Table 5-23. CapTlvate Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|---|-----|------|-----|---------------|
| V_{REG} | Reference voltage output | | 1.5 | 1.55 | 1.6 | V |
| C_{REG} | External buffer capacitor | $ESR \leq 200 \text{ m}\Omega$ | 0.8 | 1 | 1.2 | μF |
| $C_{ELECTRODE}$ | Maximum capacitance of all external electrodes on all CapTlvate blocks | Running a conversion at 4 MHz | | | 300 | pF |
| $t_{WAKEUP,COLD}$ | Voltage regulator wake-up time | LDO completely off then turned on | | 700 | | μs |
| $t_{WAKEUP,WARM}$ | Voltage regulator wake-up time | LDO in low-power mode then turned on | | 260 | | μs |
| f_{CAPCLK} | CapTlvate oscillator frequency, nominal | $T_A = 25^\circ\text{C}$, CAPCLK0, FREQSHFT = 00b | | 16 | | MHz |
| DC_{CAPCLK} | CapTlvate oscillator duty cycle | Excluding first clock cycle, $DC = t_{high} \times f$ | 40% | 50% | 60% | |

Table 5-24 lists the signal-to-noise ratio of the CapTlvate module.

Table 5-24. CapTlvate Signal-to-Noise Ratio Characteristics

over operating free-air temperature range from -40°C to 105°C ambient (T_A), unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|---|-----|------|-----|------|
| SNR | Signal-to-noise ratio ⁽¹⁾ | $T_A = 25^\circ\text{C}$, $C_t > 0.5 \text{ pF}$, $C_p < 20 \text{ pF}$, >2.5% change in capacitance ⁽²⁾ | 5:1 | 36:1 | | |
| | | $T_A = 0^\circ\text{C}$, $C_t > 0.5 \text{ pF}$, $C_p < 20 \text{ pF}$, >2.5% change in capacitance ⁽²⁾ | | 28:1 | | |
| | | $T_A = -40^\circ\text{C}$, $C_t > 0.5 \text{ pF}$, $C_p < 20 \text{ pF}$, >2.5% change in capacitance ⁽²⁾ | | 19:1 | | |

- (1) SNR is defined as the ratio of the measured change in electrode capacitance due to a touch compared with the measured change in capacitance due to the device noise floor. For additional detail on SNR in capacitive sensing applications and how to measure it in your system, see [Sensitivity, SNR, and Design Margin in Capacitive Touch Applications](#).
- (2) C_t represents the increase or decrease in electrode capacitance due to a touch. C_p represents the inherent parasitic capacitance of the sensing electrode that is present when no touch is applied. Therefore, the touch signal is defined as C_t/C_p , expressed as a percent change in capacitance. Increasing C_t or decreasing C_p increases signal.

5.11.10 FRAM

Table 5-25 lists the characteristics of the FRAM.

Table 5-25. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------|------------------|--|-----|--------|
| Read and write endurance | | 10 ¹⁵ | | | cycles |
| t _{Retention} Data retention duration | T _J = 25°C | 100 | | | years |
| | T _J = 70°C | 40 | | | |
| | T _J = 85°C | 10 | | | |
| I _{WRITE} Current to write into FRAM | | | I _{READ} ⁽¹⁾ | | nA |
| I _{ERASE} Erase current | | | N/A ⁽²⁾ | | nA |
| t _{WRITE} Write time | | | t _{READ} ⁽³⁾ | | ns |
| t _{READ} Read time | NWAITSx = 0 | | 1 / f _{SYSTEM} ⁽⁴⁾ | | ns |
| | NWAITSx = 1 | | 2 / f _{SYSTEM} ⁽⁴⁾ | | |

- (1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption parameter I_{AM,FRAM}.
- (2) FRAM does not require a special erase sequence.
- (3) Writing into FRAM is as fast as reading.
- (4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.11.11 Debug and Emulation

Table 5-26 lists the characteristics of the 2-wire SBW interface.

Table 5-26. JTAG, Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-18)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 8 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.028 | | 15 | μs |
| t _{SU, SBWTDIO} | SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire) | 2 V, 3 V | 4 | | | ns |
| t _{HD, SBWTDIO} | SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot, Spy-Bi-Wire) | 2 V, 3 V | 19 | | | ns |
| t _{Valid, SBWTDIO} | SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot, Spy-Bi-Wire) | 2 V, 3 V | | | 31 | ns |
| t _{SBW, En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2 V, 3 V | | | 110 | μs |
| t _{SBW, Ret} | Spy-Bi-Wire return to normal operation time ⁽²⁾ | 2 V, 3 V | 15 | | 100 | μs |
| R _{Internal} | Internal pull-down resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

- (1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) Maximum t_{SBW,Ret} time after pulling or releasing the TEST/SBWTCK pin low until the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode is selected.

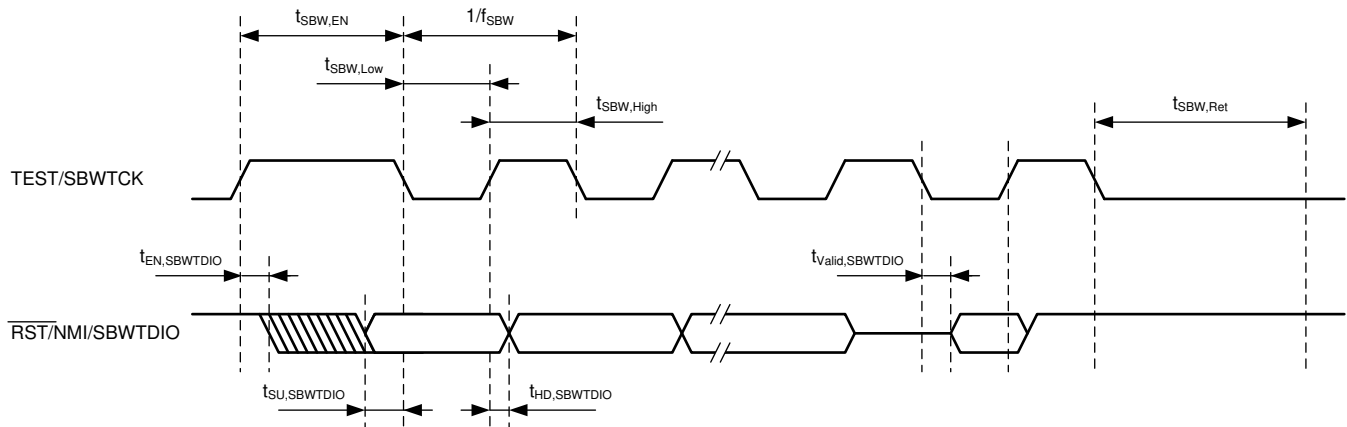


Figure 5-18. JTAG Spy-Bi-Wire Timing

Table 5-27 lists the characteristics of the 4-wire JTAG interface.

Table 5-27. JTAG, 4-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-19)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|---|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency ⁽¹⁾ | 2 V, 3 V | 0 | | 10 | MHz |
| t _{TCK,Low} | TCK low clock pulse duration | 2 V, 3 V | 15 | | | ns |
| t _{TCK,High} | TCK high clock pulse duration | 2 V, 3 V | 15 | | | ns |
| t _{SU,TMS} | TMS setup time (before rising edge of TCK) | 2 V, 3 V | 11 | | | ns |
| t _{HD,TMS} | TMS hold time (after rising edge of TCK) | 2 V, 3 V | 3 | | | ns |
| t _{SU,TDI} | TDI setup time (before rising edge of TCK) | 2 V, 3 V | 13 | | | ns |
| t _{HD,TDI} | TDI hold time (after rising edge of TCK) | 2 V, 3 V | 5 | | | ns |
| t _{Z-Valid,TDO} | TDO high impedance to valid output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| t _{Valid,TDO} | TDO to new valid output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| t _{Valid-Z,TDO} | TDO valid to high-impedance output time (after falling edge of TCK) | 2 V, 3 V | | | 26 | ns |
| t _{JTAG,Ret} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| R _{internal} | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

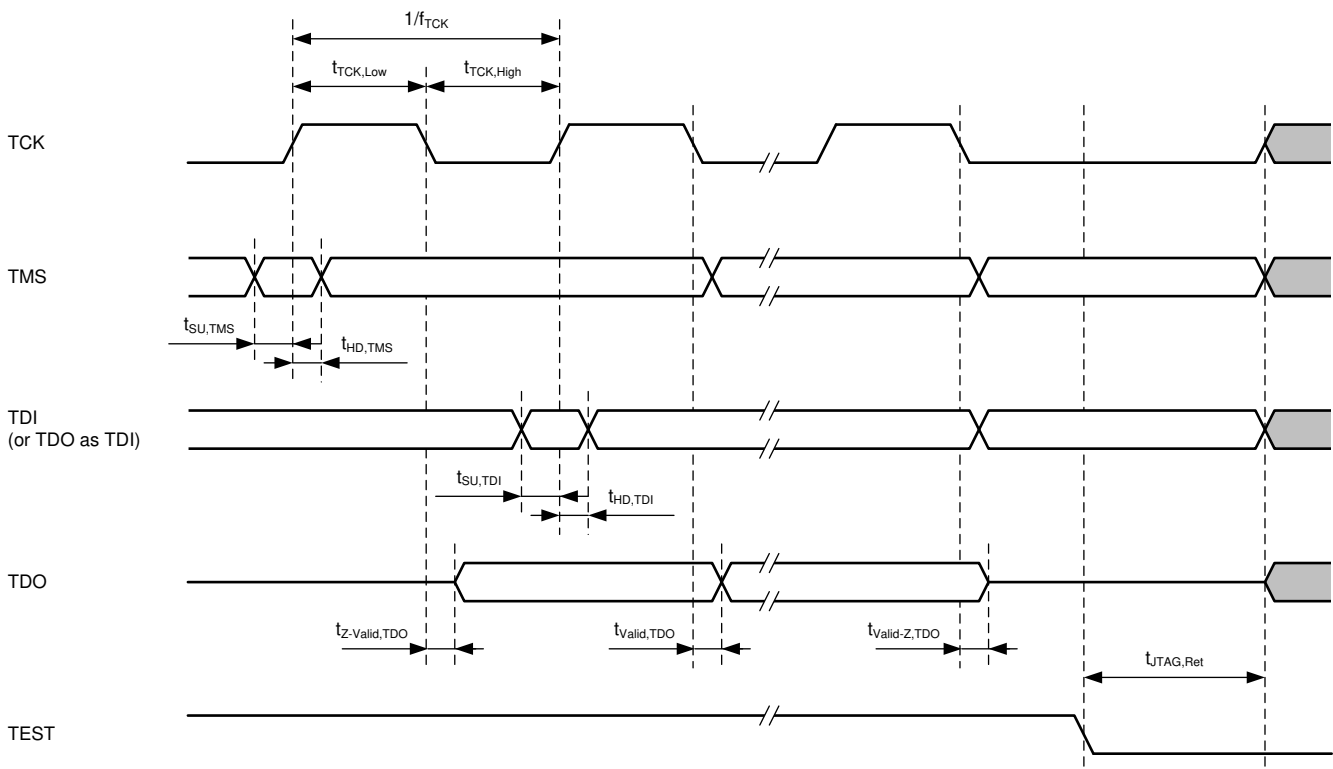


Figure 5-19. JTAG 4-Wire Timing

6 Detailed Description

6.1 Overview

The MSP430FR2522 and MSP430FR2512 ultra-low-power MCUs are FRAM-based MCUs with integrated high-performance charge-transfer CapTIvate technology in ultra-low-power high-reliability high-flexibility MCUs. The MSP430FR2522 and MSP430FR2512 MCUs feature up to 8 self-capacitance or 16 mutual-capacitance electrodes, proximity sensing, and high accuracy up to 1-fF detection. The MCUs also include two 16-bit timers, eUSCs that support UART, SPI, and I²C, a hardware multiplier, an RTC module, and a high-performance 10-bit ADC.

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

6.3 Operating Modes

The MSP430 has one active mode and several software-selectable low-power modes of operation (see [Table 6-1](#)). An interrupt event can wake the MCU from low-power mode LPM0, LPM3 or LPM4, service the request, and restore the MCU back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

NOTE

XT1CLK and VLOCLK can be active during LPM4 mode if requested by low-frequency peripherals, such as RTC, WDT, and CapTIvate.

Table 6-1. Operating Modes

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|--------------------------------|--------------------------------------|-----------------------|-----------------|--------------------------------------|---------------------|---------------------------------------|-------------------|
| | | ACTIVE MODE (FRAM ON) | CPU OFF | STANDBY | OFF | ONLY RTC | SHUTDOWN |
| Maximum system clock | | 16 MHz | 16 MHz | 40 kHz | 0 | 40 kHz | 0 |
| Power consumption at 25°C, 3 V | | 126 µA/MHz | 40 µA/MHz | 1.7 µA/button average with 8-Hz scan | 0.49 µA without SVS | 0.73 µA with RTC counter only in LFXT | 16 nA without SVS |
| Wake-up time | | N/A | Instant | 10 µs | 10 µs | 350 µs | 350 µs |
| Wake-up events | | N/A | All | All | CapTivate I/O | RTC I/O | I/O |
| Power | Regulator | Full Regulation | Full Regulation | Partial Power Down | Partial Power Down | Partial Power Down | Power Down |
| | SVS | On | On | Optional | Optional | Optional | Optional |
| | Brownout | On | On | On | On | On | On |
| Clock ⁽¹⁾ | MCLK | Active | Off | Off | Off | Off | Off |
| | SMCLK | Optional | Optional | Off | Off | Off | Off |
| | FLL | Optional | Optional | Off | Off | Off | Off |
| | DCO | Optional | Optional | Off | Off | Off | Off |
| | MODCLK | Optional | Optional | Off | Off | Off | Off |
| | REFO | Optional | Optional | Optional | Off | Off | Off |
| | ACLK | Optional | Optional | Optional | Off | Off | Off |
| | XT1CLK | Optional | Optional | Optional | Off | Optional | Off |
| | VLOCLK | Optional | Optional | Optional | Off | Optional | Off |
| CapTivate MODCLK | Optional | Optional | Optional | Off | Off | Off | |
| Core | CPU | On | Off | Off | Off | Off | Off |
| | FRAM | On | On | Off | Off | Off | Off |
| | RAM | On | On | On | On | Off | Off |
| | Backup memory ⁽²⁾ | On | On | On | On | On | Off |
| Peripherals | Timer0_A3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer1_A3 | Optional | Optional | Optional | Off | Off | Off |
| | WDT | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_A0 | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_B0 | Optional | Optional | Optional | Off | Off | Off |
| | CRC | Optional | Optional | Off | Off | Off | Off |
| | ADC | Optional | Optional | Optional | Off | Off | Off |
| | RTC | Optional | Optional | Optional | Off | Optional | Off |
| CapTivate | Optional | Optional | Optional | Off | Off | Off | |
| I/O | General-purpose digital input/output | On | Optional | State Held | State Held | State Held | State Held |

(1) The status shown for LPM4 applies to internal clocks only.

(2) Backup memory contains 32 bytes of register space in peripheral memory. See [Table 6-20](#) and [Table 6-35](#) for its memory allocation.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-2](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-2. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|--|------------------|--------------|-------------|
| System Reset Power up, Brownout, Supply supervisor External reset RST Watchdog time-out, Key violation FRAM uncorrectable bit error detection Software POR, BOR FLL unlock error | SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG | Reset | FFFEh | 63, Highest |
| System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM bit error detection | VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG | Nonmaskable | FFFCh | 62 |
| User NMI External NMI Oscillator fault | NMIIFG OFIFG | Nonmaskable | FFFAh | 61 |
| Timer0_A3 | TA0CCR0 CCIFG0 | Maskable | FFF8h | 60 |
| Timer0_A3 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TAOIFG (TA0IV) | Maskable | FFF6h | 59 |
| Timer1_A3 | TA1CCR0 CCIFG0 | Maskable | FFF4h | 58 |
| Timer1_A3 | TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV) | Maskable | FFF2h | 57 |
| RTC | RTCIFG | Maskable | FFF0h | 56 |
| Watchdog timer interval mode | WDTIFG | Maskable | FFEEh | 55 |
| eUSCI_A0 receive or transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV) | Maskable | FFECCh | 54 |
| eUSCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB0IV) | Maskable | FFEAh | 53 |
| ADC | ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIFG, ADCTOVIFG, ADCOVIFG (ADCIV) | Maskable | FFE8h | 52 |
| P1 | P1IFG.0 to P1IFG.7 (P1IV) | Maskable | FFE6h | 51 |
| P2 | P2IFG.0 to P2IFG.6 (P2IV) | Maskable | FFE4h | 50 |
| CapTivate | (See CapTivate Design Center for details) | Maskable | FFE2h | 49, Lowest |
| Reserved | Reserved | Maskable | FFE0h–FF88h | |

Table 6-3. Signatures

| SIGNATURE | WORD ADDRESS |
|-----------------|--------------|
| BSL Signature2 | 0FF86h |
| BSL Signature1 | 0FF84h |
| JTAG Signature2 | 0FF82h |
| JTAG Signature1 | 0FF80h |

6.5 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using either the UART serial interface or the I²C interface. Access to the MCU memory through the BSL is protected by a user-defined password. Use of the BSL requires four pins (see [Table 6-4](#) and [Table 6-5](#)). The BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. This device can support the blank device detection automatically to invoke the BSL with bypass this special entry sequence for saving time and on board programmable. For the complete description of the feature of the BSL, see the [MSP430 FRAM Device Bootloader \(BSL\) User's Guide](#).

Table 6-4. UART BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| $\text{TEST}/\text{SBWTCK}$ | Entry sequence signal |
| P1.4 | Data transmit |
| P1.5 | Data receive |
| DVCC | Power supply |
| DVSS | Ground supply |

Table 6-5. I²C BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|---------------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| $\text{TEST}/\text{SBWTCK}$ | Entry sequence signal |
| P1.2 | Data transmit and receive |
| P1.3 | Clock |
| DVCC | Power supply |
| DVSS | Ground supply |

6.6 JTAG Standard Interface

The MSP low-power microcontrollers support the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The $\text{TEST}/\text{SBWTCK}$ pin enables the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. [Table 6-6](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For details on using the JTAG interface, see [MSP430 Programming With the JTAG Interface](#).

Table 6-6. JTAG Pin Requirements and Function

| DEVICE SIGNAL | DIRECTION | JTAG FUNCTION |
|---|-----------|-----------------------------|
| P1.4/.../TCK | IN | JTAG clock input |
| P1.5/.../TMS | IN | JTAG state control |
| P1.6/.../TDI/TCLK | IN | JTAG data input, TCLK input |
| P1.7/.../TDO | OUT | JTAG data output |
| $\text{TEST}/\text{SBWTCK}$ | IN | Enable JTAG pins |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN | External reset |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

6.7 Spy-Bi-Wire Interface (SBW)

The MSP low-power microcontrollers support the 2-wire SBW interface. SBW can be used to interface with MSP development tools and device programmers. [Table 6-7](#) lists the SBW interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For details on using the SBW interface, see the [MSP430 Programming With the JTAG Interface](#).

Table 6-7. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | SBW FUNCTION |
|---|-----------|-----------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN, OUT | Spy-Bi-Wire data input and output |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

6.8 FRAM

The FRAM can be programmed using the JTAG port, SBW, the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

6.9 Memory Protection

The device features memory protection for user access authority and write protection, including options to:

- Secure the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Enable write protection to prevent unwanted write operation to FRAM contents by setting the control bits in the System Configuration 0 register. For detailed information, see the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10.1 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as [Equation 1](#) by using ADC sampling 1.5-V reference without any external components support.

$$\text{DVCC} = (1023 \times 1.5 \text{ V}) \div 1.5\text{-V reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered, when EXTREFEN = 1 on PMMCTL2 register, and it can be output to P1.1../A1/VREF+ , meanwhile the ADC channel 1 can also be selected to monitor this voltage. For more detailed information, see the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

6.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and an on-chip asynchronous high-speed clock (MODOSC). The clock system is designed for cost-effective designs with minimal external components. A fail-safe mechanism is included for XT1. The clock system module offers the following clock signals.

- **Main Clock (MCLK):** The system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- **Sub-Main Clock (SMCLK):** The subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- **Auxiliary Clock (ACLK):** This clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. [Table 6-8](#) lists the clock distribution used in this device.

Table 6-8. Clock Distribution

| | CLOCK SOURCE SELECT BITS | MCLK | SMCLK | ACLK | MODCLK | XT1CLK | VLOCLK | EXTERNAL PIN |
|-----------------|--------------------------|--------------|--------------------|--------------------|------------|--------------|-------------|-------------------|
| Frequency Range | | DC to 16 MHz | DC to 16 MHz | DC to 40 kHz | 5 MHz ±10% | DC to 40 kHz | 10 kHz ±50% | – |
| CPU | N/A | Default | – | – | – | – | – | – |
| FRAM | N/A | Default | – | – | – | – | – | – |
| RAM | N/A | Default | – | – | – | – | – | – |
| CRC | N/A | Default | – | – | – | – | – | – |
| I/O | N/A | Default | – | – | – | – | – | – |
| TA0 | TASSEL | – | 10b | 01b | – | – | 11b | 00b (TA0CLK pin) |
| TA1 | TASSEL | – | 10b | 01b | – | – | – | 00b (TA1CLK pin) |
| eUSCI_A0 | UCSSEL | – | 10b or 11b | 01b | – | – | – | 00b (UCA0CLK pin) |
| eUSCI_B0 | UCSSEL | – | 10b or 11b | 01b | – | – | – | 00b (UCB0CLK pin) |
| WDT | WDTSSEL | – | 00b | 01b | – | – | 10b | – |
| ADC | ADCSSEL | – | 10b or 11b | 01b | 00b | – | – | – |
| CapTivate | CAPTSSEL | – | – | 00b | – | – | 01b | – |
| RTC | RTCSS | – | 01b ⁽¹⁾ | 01b ⁽¹⁾ | – | 10b | 11b | – |

(1) Controlled by the RTCKSEL bit in the SYSCFG2 register

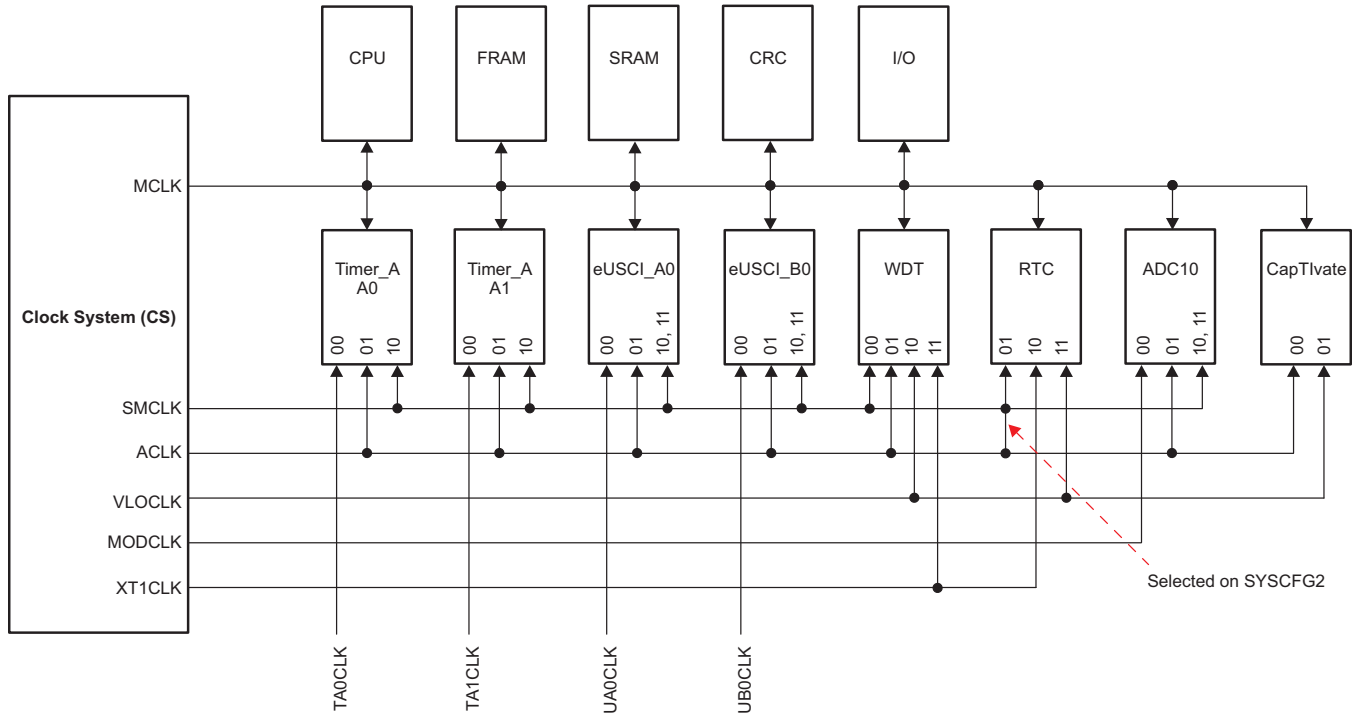


Figure 6-1. Clock Distribution Block Diagram

6.10.3 General-Purpose Input/Output Port (I/O)

Up to 15 I/O ports are implemented.

- P1 implements 8 bits, and P2 implements 7 bits.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPMx.5 wake-up input capability are available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise as a pair.
- CapTivate functionality is supported on all CAPx.y pins.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. [Table 6-9](#) lists the system clocks that can be used to source the WDT.

Table 6-9. WDT Clocks

| WDTSEL | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|--------|--|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | Reserved |

6.10.5 System (SYS) Module

The SYS module handles many of the system functions within the device. These features include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application. [Table 6-10](#) summarizes the interrupts that are managed by the SYS module.

Table 6-10. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|-----------------|--|------------|----------|
| SYSRSTIV, System Reset | 015Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG RST/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wakeup (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | Reserved | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog time-out (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | Uncorrectable FRAM bit error detection | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | FLL unlock (PUC) | 24h | |
| Reserved | 22h, 26h to 3Eh | | Lowest | |
| SYSSNIV, System NMI | 015Ch | No interrupt pending | 00h | |
| | | SVS low-power reset entry | 02h | Highest |
| | | Uncorrectable FRAM bit error detection | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah | |
| | | Reserved | 0Ch | |
| | | Reserved | 0Eh | |
| | | Reserved | 10h | |
| | | VMAIFG vacant memory access | 12h | |
| | | JMBINIFG JTAG mailbox input | 14h | |
| | | JMBOUTIFG JTAG mailbox output | 16h | |
| | | Correctable FRAM bit error detection | 18h | |
| | | Reserved | 1Ah to 1Eh | |
| SYSUNIV, User NMI | 015Ah | No interrupt pending | 00h | |
| | | NMIIFG NMI pin or SVS _H event | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h to 1Eh | |

6.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.10.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I²C communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA. The eUSCI_A and eUSCI_B are connected either from P1 port or P2 port, it can be selected from the USCIRAMP of SYSCFG3 or USCIBRMP bit of SYSCFG2. [Table 6-11](#) lists the pin configurations that are required for each eUSCI mode.

Table 6-11. eUSCI Pin Configurations

| | PIN (USCIARMP = 0) | UART | SPI |
|---------------------------|---------------------------|---------------------------|-----------------------|
| eUSCI_A0 | P1.4 | TXD | SIMO |
| | P1.5 | RXD | SOMI |
| | P1.6 | – | SCLK |
| | P1.7 | – | STE |
| | PIN (USCIARMP = 1) | UART | SPI |
| | P2.0 | TXD | SIMO |
| | P2.1 | RXD | SOMI |
| | P1.6 | – | SCLK |
| | P1.7 | – | STE |
| | eUSCI_B0 | PIN (USCIBRMP = 0) | I²C |
| P1.0 | | – | STE |
| P1.1 | | – | SCLK |
| P1.2 | | SDA | SIMO |
| P1.3 | | SCL | SOMI |
| PIN (USCIBRMP = 1) | | I²C | SPI |
| P2.3 | | – | STE |
| P2.4 | | – | SCLK |
| P2.5 | | SDA | SIMO |
| P2.6 | | SCL | SOMI |

6.10.8 Timers (Timer0_A3, Timer1_A3)

The Timer0_A3 and Timer1_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each timer supports multiple captures or compares, PWM outputs, and interval timing (see [Figure 6-2](#)). Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both Timer0_A3 and Timer1_A3 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up mode, they can be used to set the overflow value of the counter.

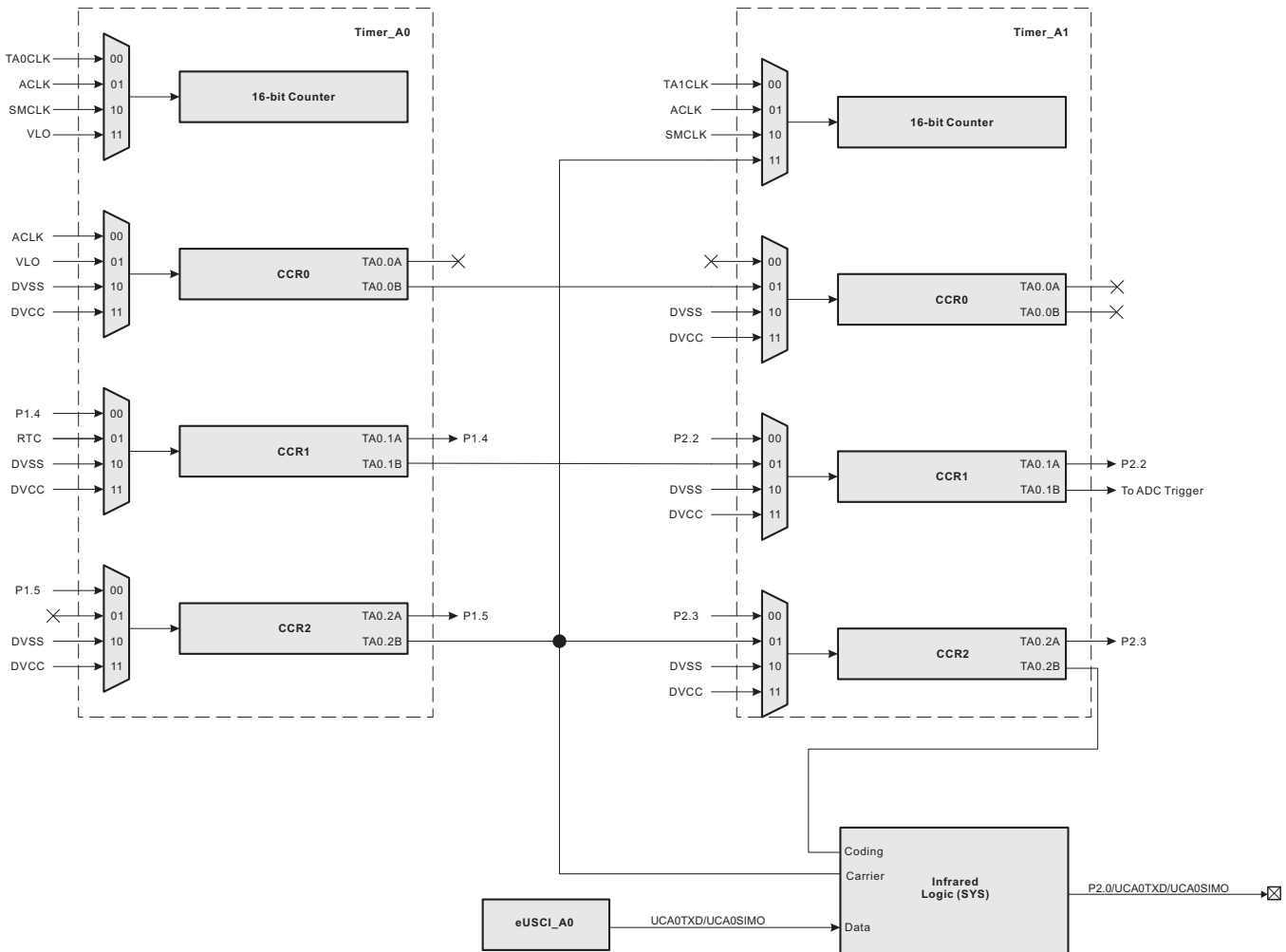


Figure 6-2. Timer0_A3 and Timer1_A3 Signal Connections

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#).

6.10.9 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The MPY module supports signed multiplication, unsigned multiplication, signed multiply-and-accumulate, and unsigned multiply-and-accumulate operations.

6.10.10 Backup Memory (BAKMEM)

The BAKMEM supports data retention during LPM3.5. This device provides up to 32 bytes that are retained during LPM3.5.

6.10.11 Real-Time Clock (RTC)

The RTC is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module can periodically wake up the CPU from LPM0, LPM3, or LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. RTC also can be sourced from ACLK controlled by RTCCLK in SYSCFG2. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_B3 CCI1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

Table 6-12. RTC Clock Source

| RTCSS | CLOCK SOURCE |
|-------|--|
| 00 | Reserved |
| 01 | SMCLK or ACLK is selected ⁽¹⁾ |
| 10 | XT1CLK |
| 11 | VLOCLK |

(1) Controlled by the RTCCLK bit of the SYSCFG2 register

6.10.12 10-Bit Analog-to-Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and 4 internal inputs (see [Table 6-13](#)).

Table 6-13. ADC Channel Connections

| ADCINCHx | ADC CHANNELS | EXTERNAL PIN |
|----------|----------------------------|--------------|
| 0 | A0/Veref+ | P1.0 |
| 1 | A1 ⁽¹⁾ | P1.1 |
| 2 | A2/Veref- | P1.2 |
| 3 | A3 | P1.3 |
| 4 | A4 | P2.2 |
| 5 | A5 | P2.3 |
| 6 | A6 | P2.4 |
| 7 | A7 | P2.5 |
| 8 | Not used | N/A |
| 9 | Not used | N/A |
| 10 | Not used | N/A |
| 11 | Not used | N/A |
| 12 | On-chip temperature sensor | N/A |
| 13 | Reference voltage (1.5 V) | N/A |

(1) When A7 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be measured by the A1 channel.

Table 6-13. ADC Channel Connections (continued)

| ADCINCHx | ADC CHANNELS | EXTERNAL PIN |
|----------|--------------|--------------|
| 14 | DVSS | N/A |
| 15 | DVCC | N/A |

The analog-to-digital conversion can be started by software or a hardware trigger. [Table 6-14](#) lists the trigger sources that are available.

Table 6-14. ADC Trigger Signal Connections

| ADC SHSx | | TRIGGER SOURCE |
|----------|---------|------------------------------|
| BINARY | DECIMAL | |
| 00 | 0 | ADCSC bit (software trigger) |
| 01 | 1 | RTC event |
| 10 | 2 | TA1.1B |
| 11 | 3 | Reserved |

6.10.13 CapTivate Technology

The CapTivate module detects the capacitance changed with a charge-transfer method and is functional in AM, LPM0, LPM3 and LPM4. The CapTivate module can periodically wake the CPU from LPM0, LPM3 or LPM4 based on a CapTivate timer source such as ACLK or VLO clock. The CapTivate module also can work on wake-on-touch state machine mode for better power saving without periodically woke up the CPU. The CapTivate module supports the following touch-sensing capability:

- The MSP430FR2522 supports up to 16 CapTivate buttons composed of 2 CapTivate blocks. The MSP430FR2512 supports up to 4 CapTivate buttons composed of 1 CapTivate block. Each block consists of 4 I/Os, and these blocks scan in parallel of 2 electrodes.
- Each block can be individually configured in self or mutual mode. Each CapTivate I/O can be used for either self or mutual electrodes.
- Supports a wake-on-touch state machine.
- Supports synchronized conversion on a zero-crossing event trigger.
- Processing logic to perform filter calculation and threshold detection.

To learn more about MSP MCUs featuring CapTivate technology, see the [CapTivate™ Technology Guide](#).

6.10.14 Embedded Emulation Module (EEM)

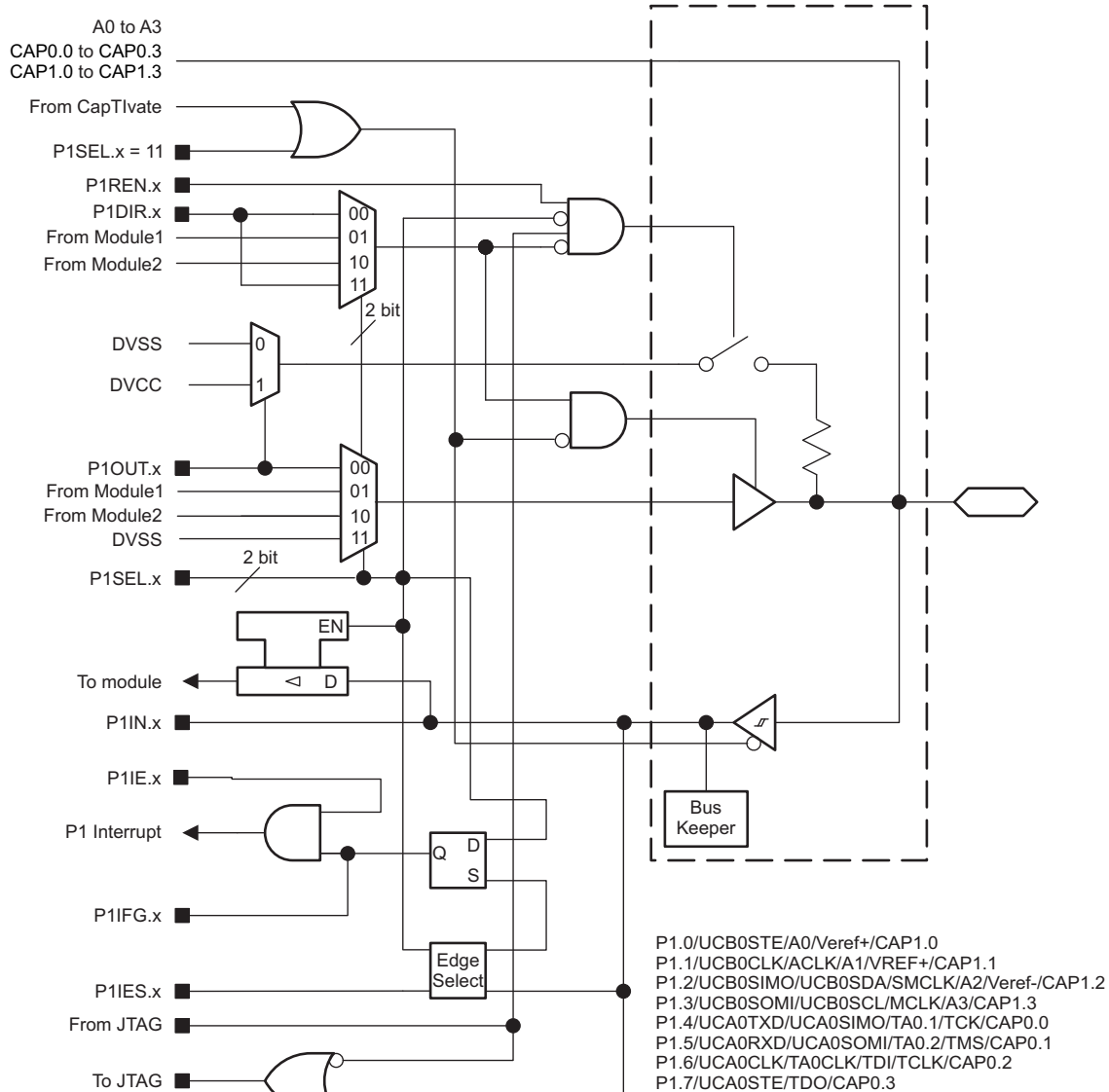
The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level
- EEM version: S

6.11 Input/Output Diagrams

6.11.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-15 summarizes the selection of pin function.



NOTE: CapTlvate channel 1 is available on the MSP430FR2522 only.

Figure 6-3. Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

NOTE

CapTlvate shared with alternative functions

The CapTlvate function and alternative functions are powered by different power supplies (1.5 V and 3.3 V, respectively).

To prevent pad damage when changing the function, TI recommends checking the external application circuit of each pad before enabling the alternative function.

Table 6-15. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | |
|---|---|-----------------------|---|-----------------------------------|--------------------------------|----------|
| | | | P1DIR.x | P1SELx | ANALOG FUNCTION ⁽²⁾ | JTAG |
| P1.0/UCB0STE/A0/ Veref+/CAP1.0 ⁽³⁾ | 0 | P1.0 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0STE | X | 01 | 0 | N/A |
| | | A0,Veref+ | X | ADCPCTLx = 1 (x = 0) from SYSCFG2 | | N/A |
| | | CAP1.0 ⁽³⁾ | X | P1SELx = 11, or from CapTlvate | | |
| P1.1/UCB0CLK/ACLK/ A1/VREF+/CAP1.1 ⁽³⁾ | 1 | P1.1 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0CLK | X | 01 | 0 | N/A |
| | | ACLK | 1 | 10 | 0 | N/A |
| | | A1,VREF+ | X | ADCPCTLx = 1 (x = 1) from SYSCFG2 | | N/A |
| | | CAP1.1 ⁽³⁾ | X | P1SELx = 11, or from CapTlvate | | |
| P1.2/UCB0SIMO/ UCB0SDA/SMCLK/A2/ Veref-/CAP1.2 ⁽³⁾ | 2 | P1.2 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0SIMO/UCB0SDA | X | 01 | 0 | N/A |
| | | SMCLK | 1 | 10 | 0 | N/A |
| | | A2, Veref- | X | ADCPCTLx = 1 (x = 2) from SYSCFG2 | | N/A |
| | | CAP1.2 ⁽³⁾ | X | P1SELx = 11, or from CapTlvate | | |
| P1.3/UCB0SOMI/ UCB0SCL/MCLK/A3/ CAP1.3 ⁽³⁾ | 3 | P1.3 (I/O) | I: 0; O: 1 | 00 | 0 | N/A |
| | | UCB0SOMI/UCB0SCL | X | 01 | 0 | N/A |
| | | MCLK | 1 | 10 | 0 | N/A |
| | | A3 | X | ADCPCTLx = 1 (x = 3) from SYSCFG2 | | N/A |
| | | CAP1.3 ⁽³⁾ | X | P1SELx = 11, or from CapTlvate | | |
| P1.4/UCA0TXD/ UCA0SIMO/TA0.1/ TCK/CAP0.0 | 4 | P1.4 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0TXD/UCA0SIMO | X | 01 | 0 | Disabled |
| | | TA0.CCI1A | 0 | 10 | 0 | Disabled |
| | | TA0.1 | 1 | | | |
| | | CAP0.0 | X | P1SELx = 11, or from CapTlvate | | Disabled |
| | | JTAG TCK | X | X | X | TCK |
| P1.5/UCA0RXD/ UCA0SOMI/TA0.2/ TMS/CAP0.1 | 5 | P1.5 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0RXD/UCA0SOMI | X | 01 | 0 | Disabled |
| | | TA0.CCI2A | 0 | 10 | 0 | Disabled |
| | | TA0.2 | 1 | | | |
| | | CAP0.1 | X | P1SELx = 11, or from CapTlvate | | Disabled |
| | | JTAG TMS | X | X | X | TMS |
| P1.6/UCA0CLK/ TA0CLK/TDI/TCLK/ CAP0.2 | 6 | P1.6 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0CLK | X | 01 | 0 | Disabled |
| | | TA0CLK | 0 | 10 | 0 | Disabled |
| | | CAP0.2 | X | P1SELx = 11, or from CapTlvate | | Disabled |
| | | JTAG TDI/TCLK | X | X | X | TDI/TCLK |
| P1.7/UCA0STE/TDO/ CAP0.3 | 7 | P1.7 (I/O) | I: 0; O: 1 | 00 | 0 | Disabled |
| | | UCA0STE | X | 01 | 0 | Disabled |
| | | CAP0.3 | X | P1SELx = 11, or from CapTlvate | | Disabled |
| | | JTAG TDO | X | X | X | TDO |

(1) X = don't care

(2) Setting the bits disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

(3) CapTlvate channel 1 is available on the MSP430FR2522 only.

6.11.2 Port P2 (P2.0 to P2.6) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-16 summarizes the selection of pin function.

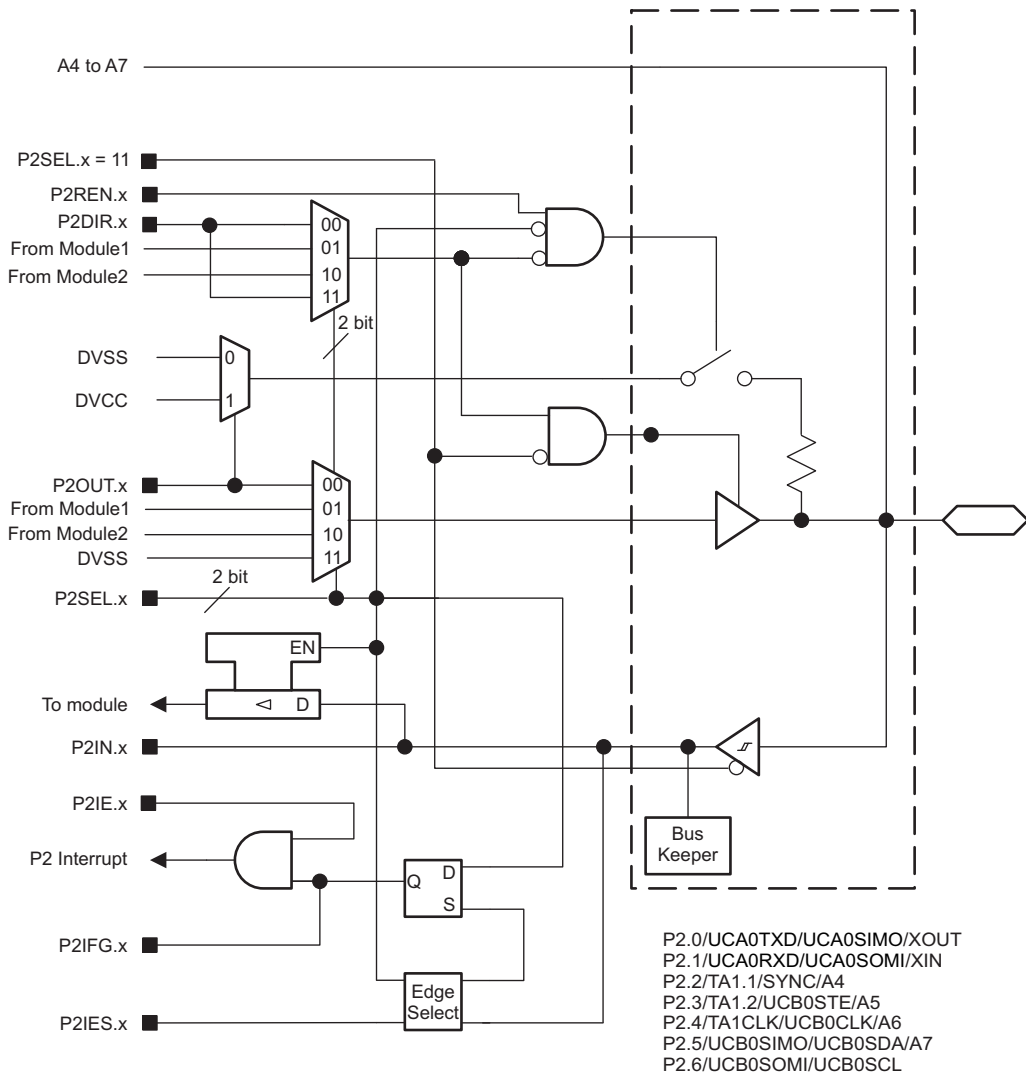


Figure 6-4. Port P2 (P2.0 to P2.6) Input/Output With Schmitt Trigger

Table 6-16. Port P2 (P2.0 to P2.6) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|--------------------------------|---|------------------|---|--------|---|
| | | | P2DIR.x | P2SELx | ANALOG FUNCTION ⁽²⁾ |
| P2.0/UCA0TXD/ UCA0SIMO/XOUT | 0 | P2.0 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCA0TXD/UCA0SIMO | X | 01 | 0 |
| | | XOUT | X | 10 | 0 |
| P2.1/UCA0RXD/ UCA0SOMI/XIN | 1 | P2.1 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCA0RXD/UCA0SOMI | X | 01 | 0 |
| | | XIN | X | 10 | 0 |
| P2.2/TA1.1/SYNC/A4 | 2 | P2.2 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | TA1.CCI1A | 0 | 01 | 0 |
| | | TA1.1 | 1 | | |
| | | SYNC | 0 | 10 | 0 |
| | | A4 | X | X | ADCPCTLx = 1 (x = 4) from SYSCFG2 ⁽²⁾ |
| P2.3/TA1.2/ UCB0STE/A5 | 3 | P2.3 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | TA1.CCI2A | 0 | 01 | 0 |
| | | TA1.2 | 1 | | |
| | | UCB0STE | X | 10 | 0 |
| | | A5 | X | X | ADCPCTLx = 1 (x = 5) from SYSCFG2 ⁽²⁾ |
| P2.4/TA1CLK/ UCB0CLK/A6 | 4 | P2.4 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | TA1CLK | 0 | 01 | 0 |
| | | UCB0CLK | X | 10 | 0 |
| | | A6 | X | X | ADCPCTLx = 1 (x = 6) from SYSCFG2 ⁽²⁾ |
| P2.5/UCB0SIMO/ UCB0SDA/A7 | 5 | P2.5 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCB0SIMO/UCB0SDA | X | 10 | 0 |
| | | A7 | X | X | ADCPCTLx = 1 (x = 7) from SYSCFG2 ⁽²⁾ |
| P2.6/UCB0SOMI/ UCB0SCL | 6 | P2.6 (I/O) | I: 0; O: 1 | 00 | 0 |
| | | UCB0SOMI/UCB0SCL | X | 10 | 0 |

(1) X = don't care

(2) Setting the bits disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12 Device Descriptors

Table 6-17 lists the Device IDs of the devices. Table 6-18 lists the contents of the device descriptor tag-length-value (TLV) structure for the devices.

Table 6-17. Device IDs

| DEVICE | DEVICE ID | |
|--------------|-----------|-------|
| | 1A05h | 1A04h |
| MSP430FR2522 | 83h | 10h |
| MSP430FR2512 | 83h | 1Ch |

Table 6-18. Device Descriptors

| DESCRIPTION | | MSP430FR25x2 | |
|---------------------------------------|---------------------------------------|--------------|-----------------|
| | | ADDRESS | VALUE |
| Information Block | Info length | 1A00h | 06h |
| | CRC length | 1A01h | 06h |
| | CRC value ⁽¹⁾ | 1A02h | Per unit |
| | | 1A03h | Per unit |
| | Device ID | 1A04h | See Table 6-17. |
| | | 1A05h | |
| | Hardware revision | 1A06h | Per unit |
| Firmware revision | 1A07h | Per unit | |
| Die Record | Die record tag | 1A08h | 08h |
| | Die record length | 1A09h | 0Ah |
| | Lot wafer ID | 1A0Ah | Per unit |
| | | 1A0Bh | Per unit |
| | | 1A0Ch | Per unit |
| | | 1A0Dh | Per unit |
| | Die X position | 1A0Eh | Per unit |
| | | 1A0Fh | Per unit |
| | Die Y position | 1A10h | Per unit |
| | | 1A11h | Per unit |
| Test result | 1A12h | Per unit | |
| | 1A13h | Per unit | |
| ADC calibration | ADC calibration tag | 1A14h | Per unit |
| | ADC calibration length | 1A15h | Per unit |
| | ADC gain factor | 1A16h | Per unit |
| | | 1A17h | Per unit |
| | ADC offset | 1A18h | Per unit |
| | | 1A19h | Per unit |
| | ADC 1.5-V reference, temperature 30°C | 1A1Ah | Per unit |
| | | 1A1Bh | Per unit |
| ADC 1.5-V reference, temperature 85°C | 1A1Ch | Per unit | |
| | 1A1Dh | Per unit | |

(1) The CRC value covers the check sum from 0x1A04h to 0x1AF5h by applying the CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$.

Table 6-18. Device Descriptors (continued)

| DESCRIPTION | | MSP430FR25x2 | |
|-------------------------------|---|--------------|----------|
| | | ADDRESS | VALUE |
| Reference and DCO Calibration | Calibration tag | 1A1Eh | 12h |
| | Calibration length | 1A1Fh | 04h |
| | 1.5-V reference factor | 1A20h | Per unit |
| | | 1A21h | Per unit |
| | DCO tap setting for 16 MHz, temperature 30°C ⁽²⁾ | 1A22h | Per unit |
| | | 1A23h | Per unit |

(2) This value can be directly loaded into DCO bits in CSCTL0 registers to get accurate 16-MHz frequency at room temperature, especially when the MCU exits from LPM3 and below. TI suggests using the predivider to decrease the frequency if the temperature drift might result an overshoot beyond 16 MHz.

6.13 Memory

6.13.1 Memory Organization

Table 6-19 summarizes the memory organization of the devices.

Table 6-19. Memory Organization

| | ACCESS | MSP430FR2522 MSP430FR2512 |
|--|---|--|
| Memory (FRAM) Main: interrupt vectors and signatures Main: code memory | Read/Write (Optional Write Protect) ⁽¹⁾ | 7.25KB FFFFh to FF80h FFFFh to E300h |
| RAM | Read/Write | 2KB 27FFh to 2000h |
| Information Memory (FRAM) | Read/Write (Optional Write Protect) ⁽²⁾ | 256B 18FFh to 1800h |
| Bootloader (BSL1) Memory (ROM) | Read only | 2KB 17FFh to 1000h |
| Bootloader (BSL2) Memory (ROM) | Read only | 1KB FFFFh to FFC0h |
| CapTivate Libraries and Driver Libraries (ROM) | Read only | 12KB 6FFFh to 4000h |
| Peripherals | Read/Write | 4KB 0FFFh to 0000h |

(1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more details

(2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more details

6.13.2 Peripheral File Map

Table 6-20 lists the available peripherals and the register base address for each.

Table 6-20. Peripherals Summary

| MODULE NAME | BASE ADDRESS | SIZE |
|--|--------------|-------|
| Special Functions (See Table 6-21) | 0100h | 0010h |
| PMM (See Table 6-22) | 0120h | 0020h |
| SYS (See Table 6-23) | 0140h | 0040h |
| CS (See Table 6-24) | 0180h | 0020h |
| FRAM (See Table 6-25) | 01A0h | 0010h |
| CRC (See Table 6-26) | 01C0h | 0008h |
| WDT (See Table 6-27) | 01CCh | 0002h |
| Port P1, P2 (See Table 6-28) | 0200h | 0020h |
| RTC (See Table 6-29) | 0300h | 0010h |
| Timer0_A3 (See Table 6-30) | 0380h | 0030h |
| Timer1_A3 (See Table 6-31) | 03C0h | 0030h |
| MPY32 (See Table 6-32) | 04C0h | 0030h |
| eUSCI_A0 (See Table 6-33) | 0500h | 0020h |
| eUSCI_B0 (See Table 6-34) | 0540h | 0030h |
| Backup Memory (See Table 6-35) | 0660h | 0020h |
| ADC (See Table 6-36) | 0700h | 0040h |
| CapTivate (See CapTivate Design Center for details) | 0A00h | 0200h |

Table 6-21. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|-----------------------|---------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 6-22. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| PMM control 2 | PMMCTL2 | 04h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 control 0 | PM5CTL0 | 10h |

Table 6-23. SYS Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|-------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |
| System configuration 0 | SYSCFG0 | 20h |
| System configuration 1 | SYSCFG1 | 22h |
| System configuration 2 | SYSCFG2 | 24h |

Table 6-24. CS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |
| CS control 7 | CSCTL7 | 0Eh |
| CS control 8 | CSCTL8 | 10h |

Table 6-25. FRAM Registers (Base Address: 01A0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| FRAM control 0 | FRCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

Table 6-26. CRC Registers (Base Address: 01C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 6-27. WDT Registers (Base Address: 01CCh)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|------------------------|---------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 6-28. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|-------------------------------|---------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pulling enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pulling enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Ch |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 6-29. RTC Registers (Base Address: 0300h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|---------|--------|
| RTC control | RTCCTL | 00h |
| RTC interrupt vector | RTCIV | 04h |
| RTC modulo | RTCMOD | 08h |
| RTC counter | RTCCNT | 0Ch |

Table 6-30. Timer0_A3 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

Table 6-31. Timer1_A3 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 6-32. MPY32 Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

Table 6-33. eUSCI_A0 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|-------------------------------|-------------|--------|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA0BR0 | 06h |
| eUSCI_A control rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | IUCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | IUCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

Table 6-34. eUSCI_B0 Registers (Base Address: 0540h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|------------------------|-----------|--------|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |

Table 6-34. eUSCI_B0 Registers (Base Address: 0540h) (continued)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B receive address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB0I2CSA | 20h |
| eUSCI_B interrupt enable | UCB0IE | 2Ah |
| eUSCI_B interrupt flags | UCB0IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB0IV | 2Eh |

Table 6-35. Backup Memory Registers (Base Address: 0660h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|----------------------|----------|--------|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |
| Backup memory 4 | BAKMEM4 | 08h |
| Backup memory 5 | BAKMEM5 | 0Ah |
| Backup memory 6 | BAKMEM6 | 0Ch |
| Backup memory 7 | BAKMEM7 | 0Eh |
| Backup memory 8 | BAKMEM8 | 10h |
| Backup memory 9 | BAKMEM9 | 12h |
| Backup memory 10 | BAKMEM10 | 14h |
| Backup memory 11 | BAKMEM11 | 16h |
| Backup memory 12 | BAKMEM12 | 18h |
| Backup memory 13 | BAKMEM13 | 1Ah |
| Backup memory 14 | BAKMEM14 | 1Ch |
| Backup memory 15 | BAKMEM15 | 1Eh |

Table 6-36. ADC Registers (Base Address: 0700h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| ADC control 0 | ADCCTL0 | 00h |
| ADC control 1 | ADCCTL1 | 02h |
| ADC control 2 | ADCCTL2 | 04h |
| ADC window comparator low threshold | ADCLO | 06h |
| ADC window comparator high threshold | ADCHI | 08h |
| ADC memory control 0 | ADCMCTL0 | 0Ah |
| ADC conversion memory | ADCMEM0 | 12h |
| ADC interrupt enable | ADCIE | 1Ah |
| ADC interrupt flags | ADCIFG | 1Ch |
| ADC interrupt vector word | ADCIV | 1Eh |

6.14 Identification

6.14.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entries in [Section 6.12](#).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entries in [Section 6.12](#).

6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in [MSP430 Programming With the JTAG Interface](#).

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital-to-analog circuits on the board and to achieve high analog accuracy.

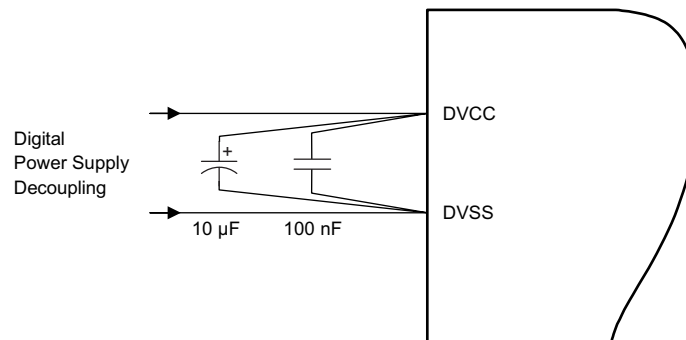


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If the XIN and XOUT pins are not used, they must be terminated according to [Section 4.6](#).

Figure 7-2 shows a typical connection diagram.

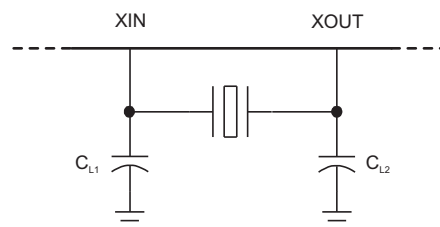


Figure 7-2. Typical Crystal Connection

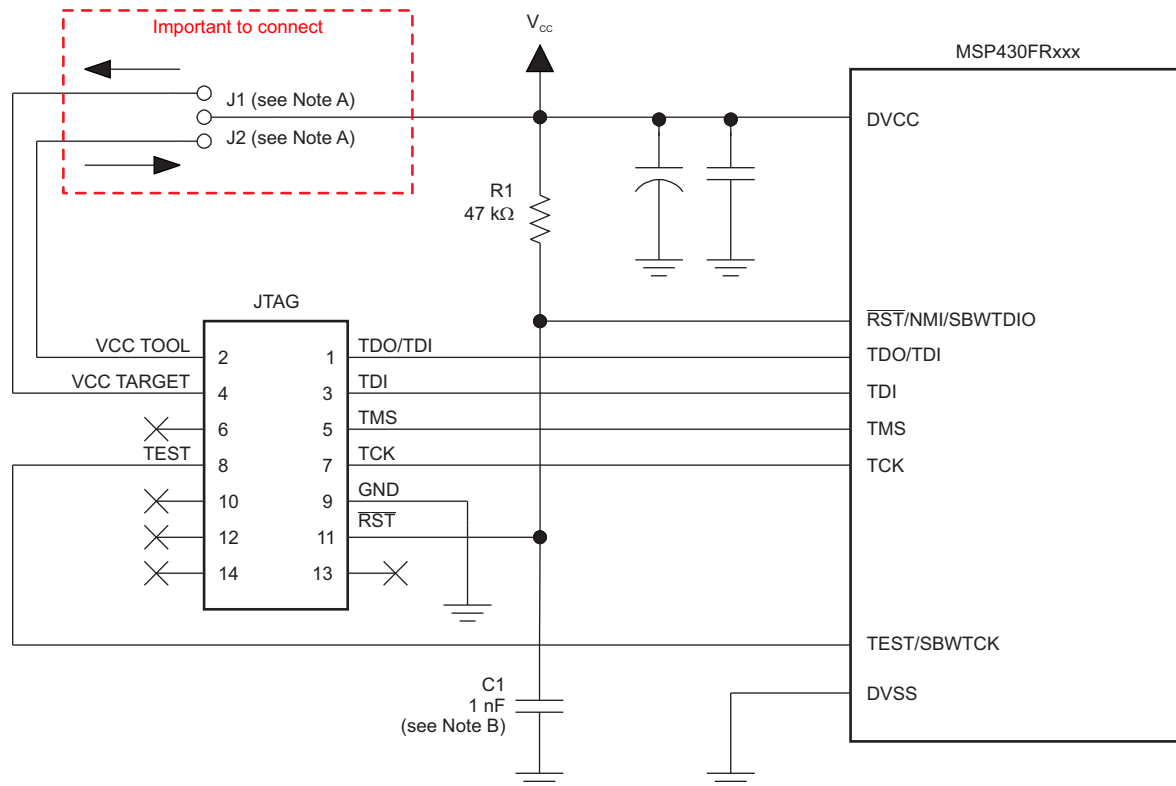
See [MSP430 32-kHz Crystal Oscillators](#) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [Figure 7-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [Figure 7-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

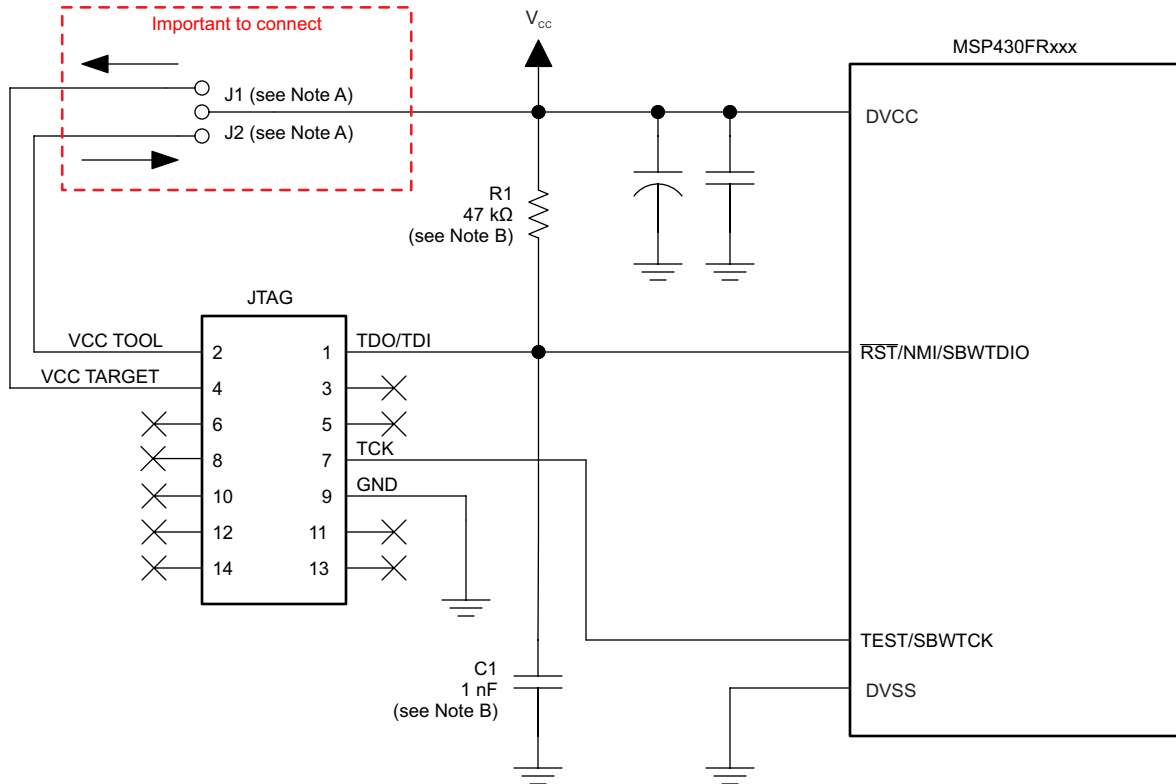
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC} sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC} sense feature detects the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [Figure 7-3](#) and [Figure 7-4](#) show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the [MSP430 Hardware Tools User's Guide](#).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST}}/\text{NMI}/\text{SBWTIO}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}/\text{NMI}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}/\text{NMI}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}/\text{NMI}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}/\text{NMI}$ pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k Ω pullup resistor to the RST/NMI pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the [MP430FR4xx and MP430FR2xx Family User's Guide](#) for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.6](#).

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See [MSP430 32-kHz Crystal Oscillators](#) for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See [MSP430 System-Level ESD Considerations](#) for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in [Section 5.1](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

[Figure 7-5](#) shows the recommended decoupling circuit when an external voltage reference is used.

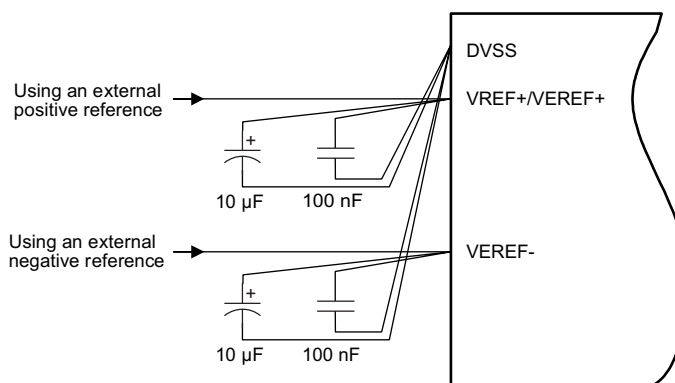


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.1](#) combined with the connections shown in [Figure 7-5](#) prevent this.

Quickly switching digital signals and noisy power supply lines can corrupt the conversion results, so keep the ADC input trace shielded from those digital and power supply lines. Putting the MCU in low-power mode during the ADC conversion improves the ADC performance in a noisy environment. If the device includes the analog power pair inputs (AVCC and AVSS), TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

[Figure 7-5](#) shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the [MSP430FR4xx and MSP430FR2xx Family User's Guide](#).

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- μ F capacitor buffers the reference pin and filters any low-frequency ripple. A bypass capacitor of 100 nF filters out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

7.2.2 CapTIvate Peripheral

This section provides a brief introduction to the CapTIvate technology with examples of PCB layout and performance from the design kit. A more detailed description of the CapTIvate technology and the tools needed to be successful, application development tools, hardware design guides, and software library, can be found in the [CapTIvate™ Technology Guide](#).

7.2.2.1 Device Connection and Layout Fundamentals

To learn more on how to design the CapTIvate Technology, see the [Capacitive Touch Design Flow for MSP430™ MCUs With CapTIvate™ Technology](#) application report.

7.2.2.2 Measurements

The following measurements are taken from the [CapTivate Technology Design Center](#), using the [CAPTIVATE-PHONE](#) and [CAPTIVATE-BSWP](#) panels. Unless otherwise stated, the settings used are the out-of-box settings, which can be found in the example projects. The intent of these measurements is to show performance in a configuration that is readily available and reproducible.



Figure 7-6. CAPTIVATE-PHONE and CAPTIVATE-BSWP Panels

7.2.2.2.1 SNR

The [Sensitivity, SNR, and Design Margin in Capacitive Touch Applications](#) application report provides a specific view for analyzing the signal-to-noise ratio of each element.

7.2.2.2.2 Sensitivity

To show sensitivity, in terms of farads, the internal reference capacitor is used as the change in capacitance. In the mutual-capacitance case, the 0.1-pF capacitor is used. In the self-capacitance case, the 1-pF reference capacitor is used. For simplicity, the results for only button 1 on both the CAPTIVATE-PHONE and CAPTIVATE-BSWP panels are reported in [Table 7-1](#).

Table 7-1. Button Sensitivity

| CONVERSION COUNT | CONVERSION GAIN | CAPTIVATE-PHONE BUTTON 1 | | CAPTIVATE-BSWP BUTTON 1 | |
|------------------|-----------------|----------------------------|--------------------------|----------------------------|------------------------|
| | | CONVERSION TIME (μ s) | COUNTS FOR 0.1-pF CHANGE | CONVERSION TIME (μ s) | COUNTS FOR 1-pF CHANGE |
| 100 | 100 | 25 | 6 | 50 | 8 |
| 200 | 200 | 50 | 10 | 100 | 16 |
| 200 | 100 | 50 | 21 | 100 | 31 |
| 800 | 400 | 200 | 70 | 400 | 112 |
| 800 | 200 | 200 | 140 | 400 | 202 |
| 800 | 100 | 200 | 257 | 400 | 333 |

An alternative measure in sensitivity is the ability to resolve capacitance change over a wide range of base capacitance. [Table 7-2](#) shows example conversion times (for a self-mode measurement of discrete capacitors) that can be used to achieve the desired resolution for a given parasitic load capacitance.

Table 7-2. Button Sensitivity

| CAPACITANCE Cp (pF) ⁽¹⁾ | CONVERSION COUNT/GAIN | CONVERSION TIME (μs) | COUNTS FOR 0.130-pF CHANGE | COUNTS FOR 0.260-pF CHANGE | COUNTS FOR 0.520-pF CHANGE |
|------------------------------------|-----------------------|----------------------|----------------------------|----------------------------|----------------------------|
| 23 | 400/100 | 200 | 10 | 23 | 35 |
| 50 | 550/100 | 275 | 11 | 24 | 37 |
| 78 | 650/100 | 325 | 11 | 23 | 36 |
| 150 | 850/100 | 425 | 11 | 22 | 35 |
| 150 ⁽²⁾ | 1200/200 | 600 | 11 | 23 | 37 |
| 200 ⁽²⁾ | 1200/150 | 600 | 13 | 26 | 41 |

(1) These measurements were taken with the CapTIvate MCU processor board with the 470-Ω series resistors replaced with 0-Ω resistors.

(2) 0-V discharge voltage is used.

7.2.2.3 Power

The low-power mode LPM3 and LPM4 specifications in [Section 5.7](#) are derived from the CapTIvate technology design kit as indicated in the notes.

7.3 CapTIvate Technology Evaluation

[Table 7-3](#) lists tools that demonstrate the use of the MSP430FR25x2 devices. See [CapTIvate Evaluation Tools](#) to get started with evaluating the CapTIvate technology in various real-world application scenarios. Consult these evaluation tool designs for additional guidance regarding schematics, layout, and software implementation.

Table 7-3. Evaluation Tools

| DESIGN NAME | LINK |
|---|---|
| MSP430 CapTIvate™ Touch Keypad BoosterPack Plug-in Module | http://www.ti.com/tool/boostxl-capkeypad |

8 Device and Documentation Support

8.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with your development, visit the [MSP430™ ultra-low-power sensing & measurement MCUs overview](#).

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

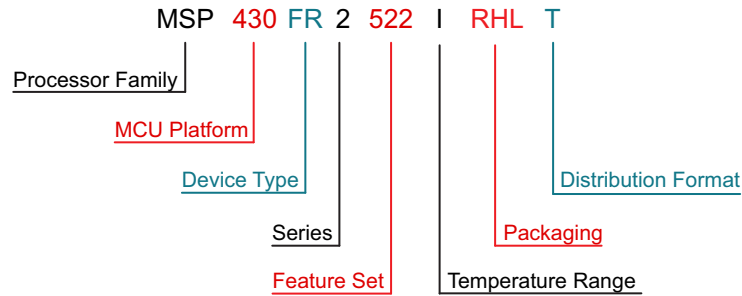
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 8-1](#) provides a legend for reading the complete device name.



| | |
|----------------------------|---|
| Processor Family | MSP = Mixed-signal processor XMS = Experimental silicon |
| MCU Platform | 430 = MSP430 16-bit low-power platform |
| Device Type | FR = FRAM |
| Series | 2 = Up to 16 MHz without LCD |
| Feature Set | 522 = 2 CapTIvate blocks, 8KB of FRAM, 2KB of RAM, up to 8 CapTIvate I/Os 512 = 1 CapTIvate block, 8KB of FRAM, 2KB of RAM, up to 4 CapTIvate I/Os |
| Temperature Range | I = -40°C to 85°C |
| Packaging | www.ti.com/packaging |
| Distribution Format | T = Small reel R = Large reel No marking = Tube or tray |

Figure 8-1. Device Nomenclature

8.3 Tools and Software

Table 8-1 lists the debug features supported by these microcontrollers. See the [Code Composer Studio IDE for MSP430 MCUs User's Guide](#) for details on the available features.

Table 8-1. Hardware Features

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT | EEM VERSION |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|-------------|
| MSP430xv2 | Yes | Yes | 3 | Yes | Yes | No | No | No | S |

Design Kits and Evaluation Modules

[MSP-TS430RHL20 20-Pin Target Development Board for MSP430FR2x MCUs](#)

The MSP-TS430RHL20 is a stand-alone ZIF socket target board used to program and debug the MSP430 in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol. The development board supports all MSP430FR252x and MSP430FR242x Flash parts in a 20-pin VQFN package (TI package code: RHL).

[MSP-FET + MSP-TS430RHL20 FRAM Microcontroller Development Kit Bundle](#)

The MSP-FET430RHL20-BNDL bundle combines two debugging tools that support the 20-pin RHL package for the MSP430FR2422 microcontroller (for example, MSP430FR2422RHL). These two tools include MSP-TS430RHL20 and MSP-FET.

Software

[MSP430Ware™ Software](#)

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

[MSP430FR2422 Code Examples](#)

C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

[MSP Driver Library](#)

Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

[MSP EnergyTrace™ Technology](#)

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

[ULP \(Ultra-Low Power\) Advisor](#)

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

[FRAM Embedded Software Utilities for MSP Ultra-Low-Power Microcontrollers](#)

The FRAM Utilities is designed to grow as a collection of embedded software utilities that leverage the ultra-low-power and virtually unlimited write endurance of FRAM. The utilities are available for MSP430FRxx FRAM microcontrollers and provide example code to help start application development. Included utilities include Compute Through Power Loss (CTPL). CTPL is utility API set that enables ease of use with LPMx.5 low-power modes and a powerful shutdown mode that allows an application to save and restore critical system components when a power loss is detected.

[IEC60730 Software Package](#)

The IEC60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

[Fixed Point Math Library for MSP](#)

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

[Floating Point Math Library for MSP430](#)

Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

Development Tools

[Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using CCS with an MSP MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP microcontroller.

[Command-Line Programmer](#)

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – that lets users quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer.

MSP-GANG Production Programmer

The MSP Gang Programmer can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices.

8.4 Documentation Support

The following documents describe the MSP430FR25x2 microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, [MSP430FR2522](http://ti.com)). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

[MSP430FR2522 Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430FR2512 Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

User's Guides

[MSP430FR4xx and MSP430FR2xx Family User's Guide](#)

Detailed description of all modules and peripherals available in this device family.

[MSP430 FRAM Device Bootloader \(BSL\) User's Guide](#)

The BSL can program memory during MSP430 MCU project development and updates. The BSL can be activated by a utility that sends commands using a serial protocol. The BSL enables the user to control the activity of the MSP430 device and to exchange data using a personal computer or other device.

[MSP430 Programming With the JTAG Interface](#)

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

[MSP430 Hardware Tools User's Guide](#)

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller.

Application Reports

[MSP430 32-kHz Crystal Oscillators](#)

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

[MSP430 System-Level ESD Considerations](#)

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses different ESD topics to help board designers and OEMs understand and design robust system-level designs. A few real-world system-level ESD protection design examples and their results are also discussed.

8.5 Related Links

[Table 8-2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FR2522 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR2512 | Click here | Click here | Click here | Click here | Click here |

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 Trademarks

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8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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8.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

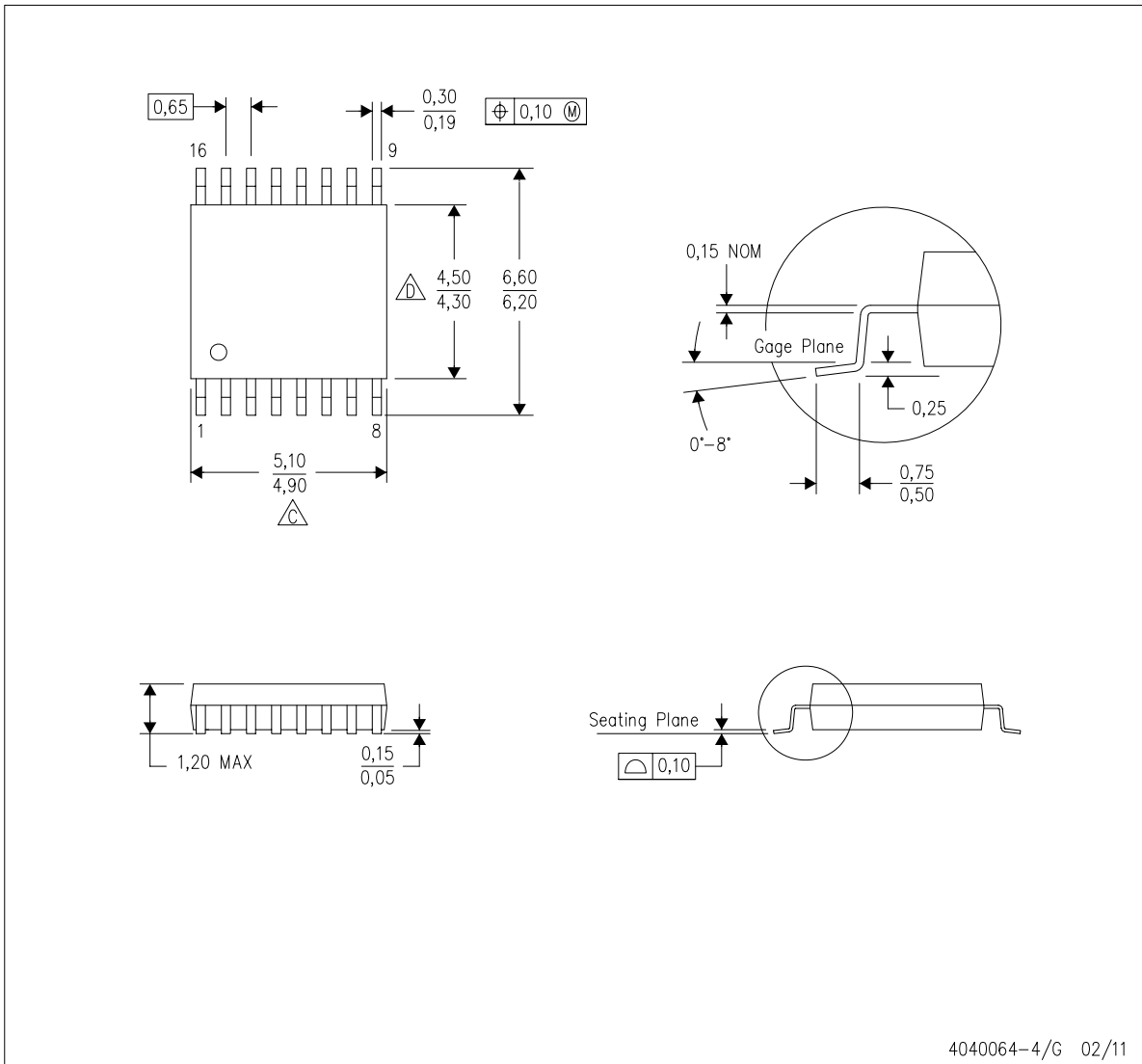
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



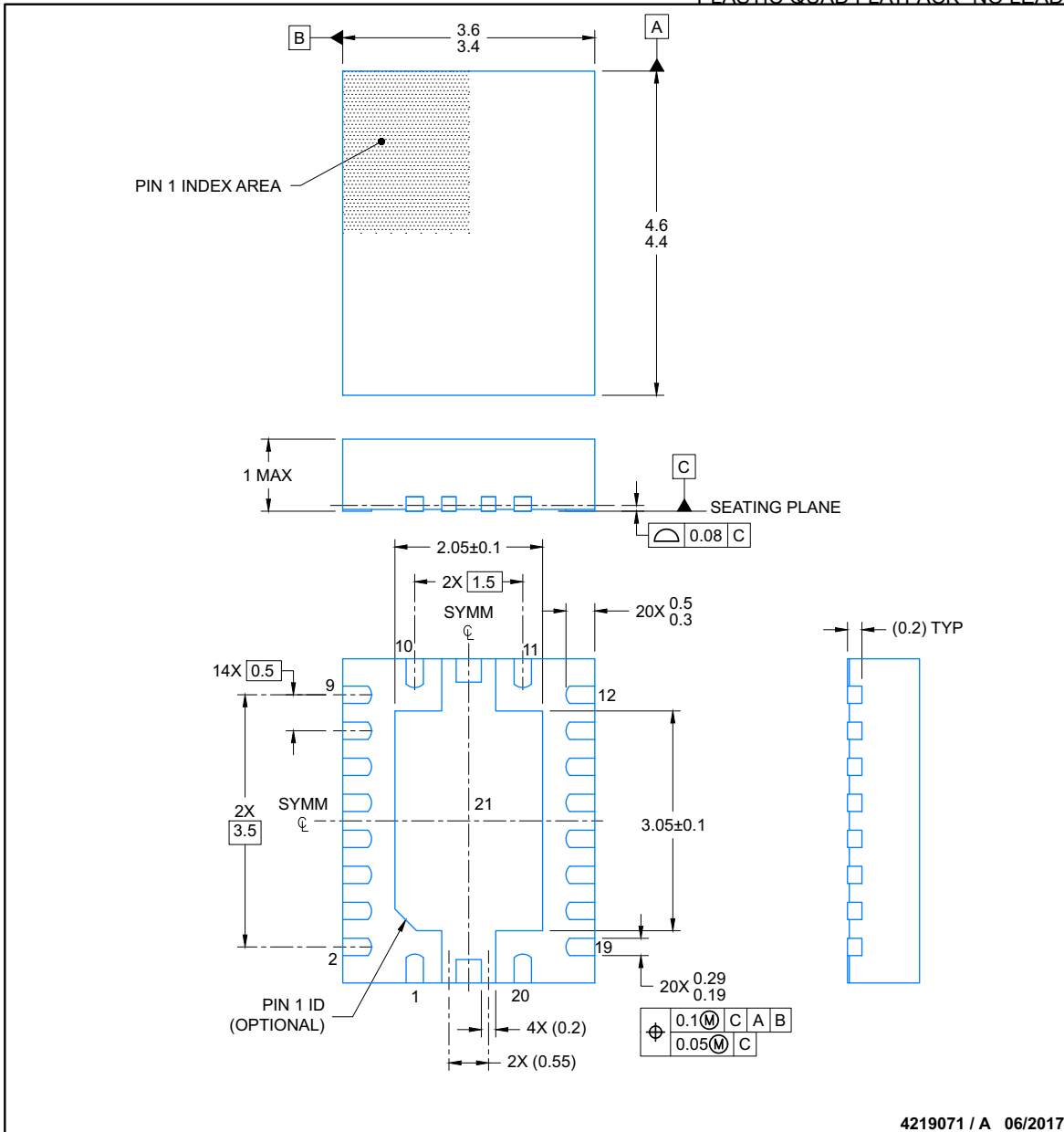
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PACKAGE OUTLINE

RH1 0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



4219071 / A 06/2017

NOTES:

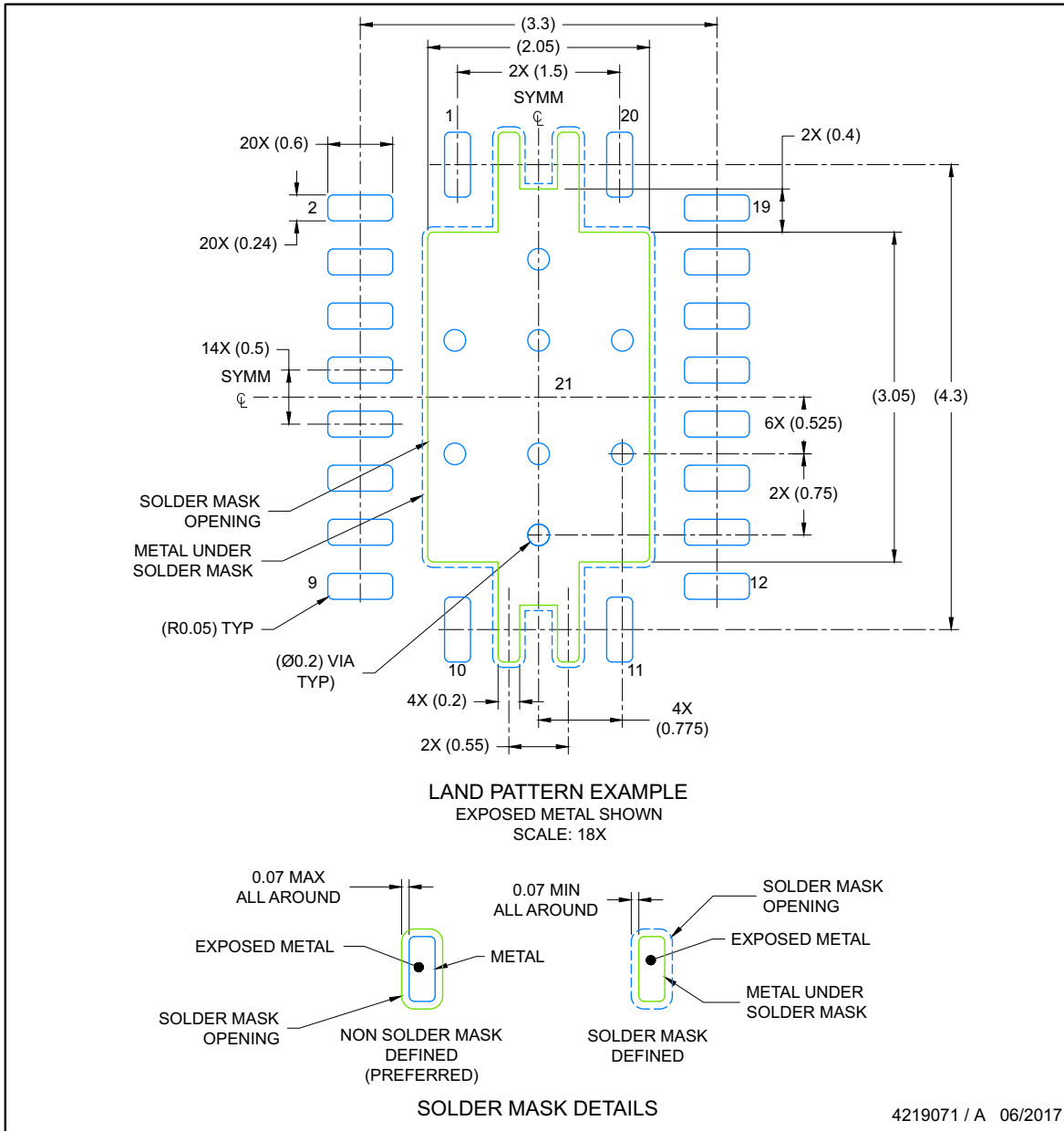
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHL0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



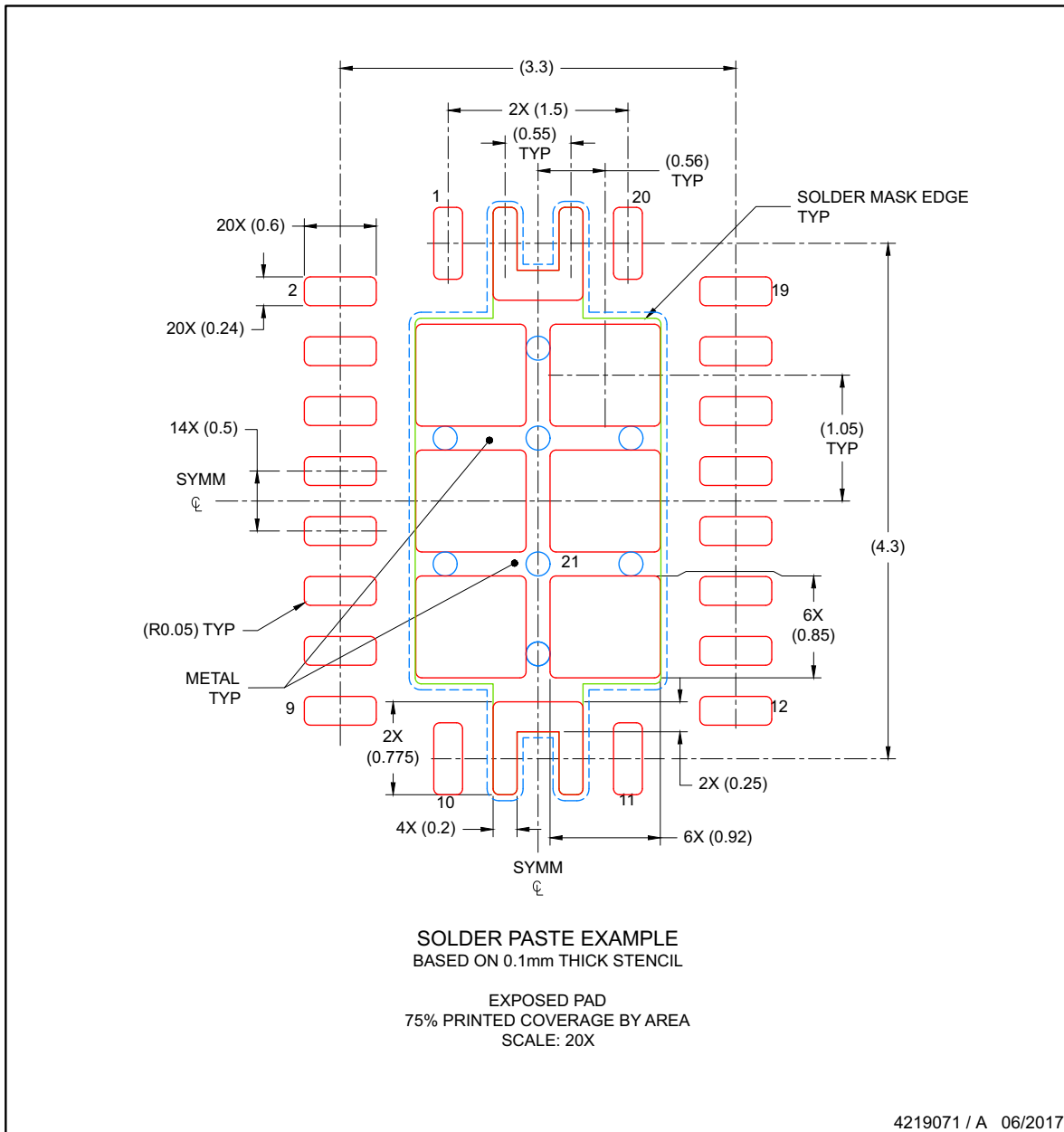
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

RHL0020A

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FR2512IPW16 | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FR2512 | Samples |
| MSP430FR2512IPW16R | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FR2512 | Samples |
| MSP430FR2512IRHLR | ACTIVE | VQFN | RHL | 20 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2512 | Samples |
| MSP430FR2512IRHLT | ACTIVE | VQFN | RHL | 20 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2512 | Samples |
| MSP430FR2522IPW16 | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FR2522 | Samples |
| MSP430FR2522IPW16R | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FR2522 | Samples |
| MSP430FR2522IRHLR | ACTIVE | VQFN | RHL | 20 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2522 | Samples |
| MSP430FR2522IRHLT | ACTIVE | VQFN | RHL | 20 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FR2522 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

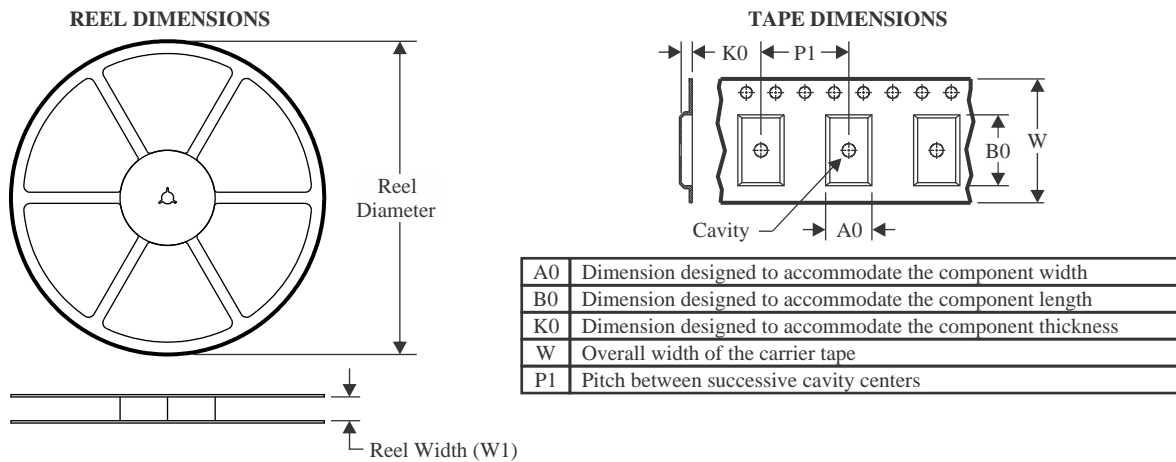
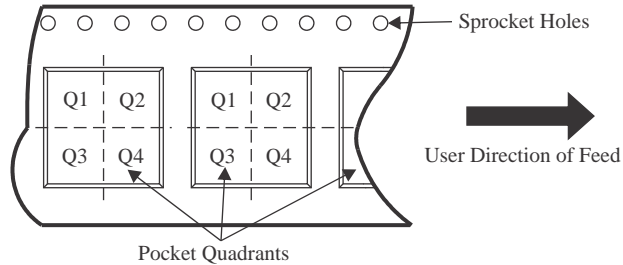
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

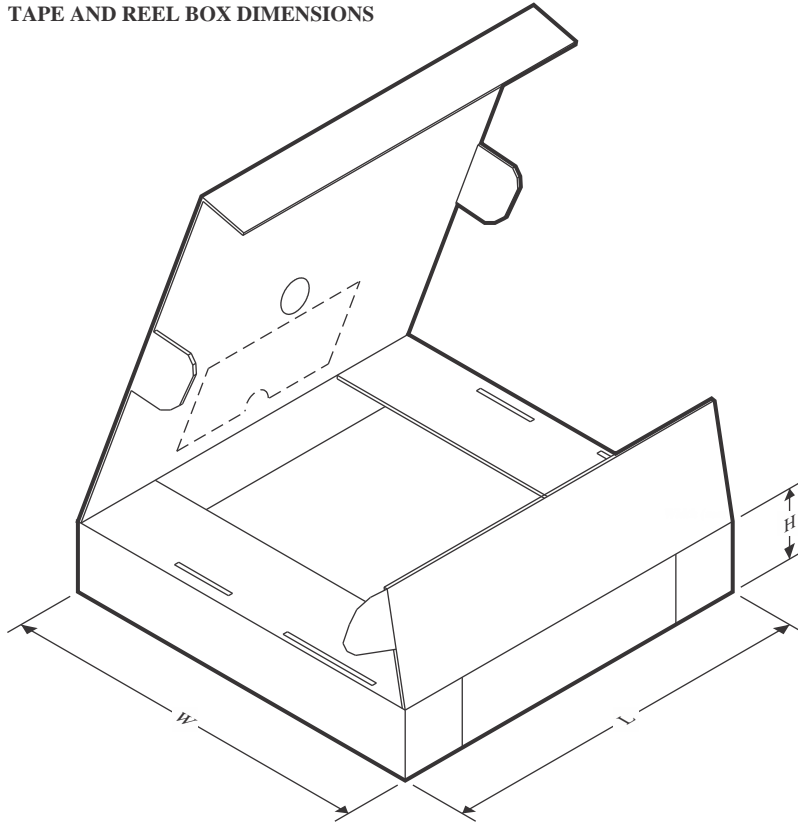
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


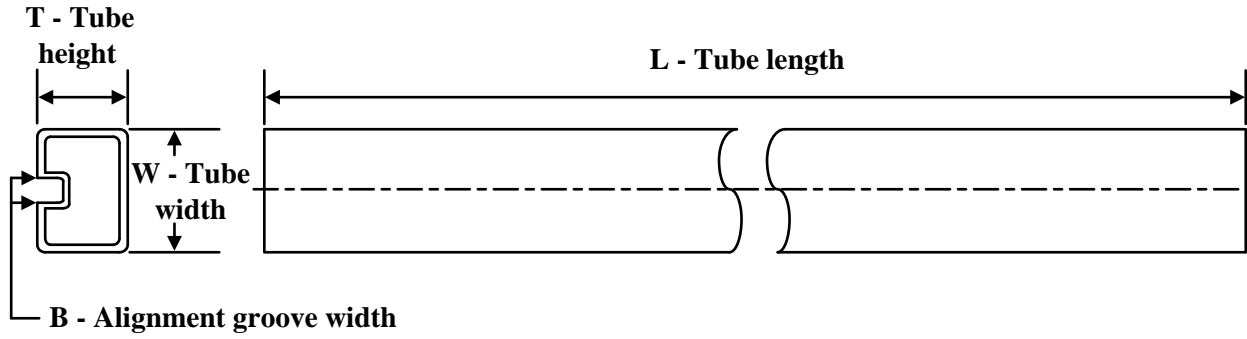
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR2512IPW16R | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430FR2512IRHLR | VQFN | RHL | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| MSP430FR2512IRHLT | VQFN | RHL | 20 | 250 | 180.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| MSP430FR2522IPW16R | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430FR2522IRHLR | VQFN | RHL | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| MSP430FR2522IRHLT | VQFN | RHL | 20 | 250 | 180.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR2512IPW16R | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2512IRHLR | VQFN | RHL | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2512IRHLT | VQFN | RHL | 20 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2522IPW16R | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2522IRHLR | VQFN | RHL | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2522IRHLT | VQFN | RHL | 20 | 250 | 210.0 | 185.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MSP430FR2512IPW16 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430FR2522IPW16 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

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