



**THE DATASHEET OF  
FAN7171M-F085**



# 600 V / 4 A, High-Side Automotive Gate Driver IC

## FAN7171-F085



SOIC8  
CASE 751EB

### Description

The FAN7171-F085 is a monolithic high-side gate drive IC that can drive high-speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

onsemi's high-voltage process and common-mode noise-canceling techniques provide stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -9.8$  V (typical) for  $V_{BS} = 15$  V.

The UVLO circuit prevents malfunction when  $V_{BS}$  is lower than the specified threshold voltage.

The high-current and low-output voltage-drop feature make this device suitable for sustaining switch drivers and energy-recovery switch drivers in automotive motor drive inverters, switching power supplies, and high-power DC-DC converter applications.

### Features

- Floating Channel for Bootstrap Operation to +600 V
- 4 A Sourcing and 4 A Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Cancelling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In-phase with Input Signal
- Under-Voltage Lockout for  $V_{BS}$
- 25 V Shunt Regulator on  $V_{DD}$  and  $V_{BS}$
- 8-SOIC Package, Case 751EB (JEDEC MS-012, 0.150 inch Narrow Body)
- Automotive Qualified to AEC Q100 for Ambient Operating Temperature from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### Applications

- Common Rail Injection Systems
- DC-DC Converter
- Motor Drive (Electric Power Steering, Fans)

### Related Product Resources

- FAN7171-F085 Product Folder
- AN-6076 Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC
- AN-8102 200 Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications
- AN-9052 Design Guide for Selection of Bootstrap Components
- AN-4171 FAN7085 High-Side Gate Driver- Internal Recharge Path Design Considerations

### ORDERING INFORMATION

Device	Package	Shipping†
FAN7171M-F085	Case 751EB (Pb-Free / Halogen Free)	Tube
FAN7171MX-F085		Tape & Reel
FAN7171MX-F085-1		Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. These devices passed wave soldering test by JESD22A-111.
2. A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as onsemi has officially announced in Aug 2014.



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**Table 1. PIN DESCRIPTIONS**

Pin #	Name	Description
1	V <sub>DD</sub>	Supply Voltage
2	IN	Logic Input for High–Side Gate Driver Output
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	V <sub>S</sub>	High–Voltage Floating Supply Return
7	HO	High–Side Driver Output
8	V <sub>B</sub>	High–Side Floating Supply

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Symbol	Characteristics	Min.	Max.	Unit
V <sub>S</sub>	High–Side Floating Offset Voltage	V <sub>B</sub> –V <sub>SHUNT</sub>	V <sub>B</sub> +0.3	V
V <sub>B</sub>	High–Side Floating Supply Voltage (Note 3)	–0.3	625.0	V
V <sub>HO</sub>	High–Side Floating Output Voltage	V <sub>S</sub> –0.3	V <sub>B</sub> +0.3	V
V <sub>DD</sub>	Low–Side and Logic Supply Voltage (Note 3)	–0.3	V <sub>SHUNT</sub>	V
V <sub>IN</sub>	Logic Input Voltage	–0.3	V <sub>DD</sub> +0.3	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Slew Rate		±50	V/ns
P <sub>D</sub>	Power Dissipation (Notes 4, 5, 6)		0.625	W
θ <sub>JA</sub>	Thermal Resistance		200	°C/W
T <sub>J</sub>	Junction Temperature	–55	150	°C
T <sub>STG</sub>	Storage Temperature	–55	150	°C
T <sub>A</sub>	Operating Ambient Temperature	–40	125	°C
ESD	Human Body Model (HBM)		2000	V
	Charge Device Model (CDM)		500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This IC contains a shunt regulator on V<sub>DD</sub> and V<sub>BS</sub> with a normal breakdown voltage of 25 V. Please note that this supply pin should not be driven by a low–impedance voltage source greater than the V<sub>SHUNT</sub> specified in the Electrical Characteristics section.
- Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR–4 glass epoxy material).
- Refer to the following standards:  
 JESD51–2: Integral circuits thermal test method environmental conditions, natural convection, and  
 JESD51–3: Low effective thermal conductivity test board for leaded surface–mount packages.
- Do not exceed power dissipation (P<sub>D</sub>) under any circumstances.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristics	Min.	Max.	Unit
V <sub>BS</sub>	High–Side Floating Supply Voltage	V <sub>S</sub> +10	V <sub>S</sub> +20	V
V <sub>S</sub>	High–Side Floating Supply Offset Voltage (DC)	6–V <sub>DD</sub>	600	V
	High–Side Floating Supply Offset Voltage (Transient)	–15 (~170)		
		–7 (~400)		
V <sub>HO</sub>	High–Side Output Voltage	V <sub>S</sub>	V <sub>B</sub>	V
V <sub>IN</sub>	Logic Input Voltage	GND	V <sub>DD</sub>	V
V <sub>DD</sub>	Supply Voltage	10	20	V
T <sub>PULSE</sub>	Minimum Input Pulse Width (Note 7)	80	–	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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7. Input pulses shorter than the minimum recommendation can cause abnormal output. Short input pulses can be turn on pulses (i.e., rising edge to the adjacent falling edge), turn off pulses (i.e., falling edge to the adjacent rising edge) but also parasitic pulses induced by noise. Refer to Figure 24 and Figure 25. Value guaranteed by design.

**Table 4. ELECTRICAL CHARACTERISTICS**

( $V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND. The  $V_O$  and  $I_O$  parameters are relative to  $V_S$  and are applicable to the respective output HO)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>POWER SUPPLY SECTION</b>						
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN} = 0\text{ V or }5\text{ V}$		25	70	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$f_{IN} = 20\text{ kHz}$ , No Load		35	100	$\mu\text{A}$
<b>BOOTSTRAPPED SUPPLY SECTION</b>						
$V_{BSUV+}$	$V_{BS}$ Supply Under-Voltage Positive-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	8.2	9.2	10.2	V
$V_{BSUV-}$	$V_{BS}$ Supply Under-Voltage Negative-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	7.5	8.5	9.5	V
$V_{BSHYS}$	$V_{BS}$ Supply UVLO Hysteresis Voltage	$V_{BS} = \text{Sweep}$		0.6		V
$I_{LK}$	Offset Supply Leakage Current	$V_B = V_S = 600\text{ V}$			50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN} = 0\text{ V or }5\text{ V}$		60	120	$\mu\text{A}$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$C_{LOAD} = 1\text{ nF}$ , $f_{IN} = 20\text{ kHz}$ , RMS Value		0.73	2.80	mA
<b>SHUNT REGULATOR SECTION</b>						
$V_{SHUNT}$	$V_{DD}$ and $V_{BS}$ Shunt Regulator Clamping Voltage	$I_{SHUNT} = 5\text{ mA}$	23	25		V
<b>INPUT LOGIC SECTION (IN)</b>						
$V_{IH}$	Logic "1" Input Voltage		2.5			V
$V_{IL}$	Logic "0" Input Voltage				0.8	V
$I_{IN+}$	Logic Input High Bias Current	$V_{IN} = 5\text{ V}$		45	125	$\mu\text{A}$
$I_{IN-}$	Logic Input Low Bias Current	$V_{IN} = 0\text{ V}$			2	$\mu\text{A}$
$R_{IN}$	Input Pull-down Resistance		40	110		k $\Omega$
<b>GATE DRIVER OUTPUT SECTION (HO)</b>						
$V_{OH}$	High Level Output Voltage ( $V_{BIAS} - V_O$ )	No Load			1.5	V
$V_{OL}$	Low Level Output Voltage	No Load			35	mV
$I_{O+}$	Output High, Short-Circuit Pulsed Current (Note 8)	$V_{HO} = 0\text{ V}$ , $V_{IN} = 5\text{ V}$ , $PW \leq 10\ \mu\text{s}$	3.0	4.0		A
$I_{O-}$	Output Low, Short-Circuit Pulsed Current (Note 8)	$V_{HO} = 15\text{ V}$ , $V_{IN} = 0\text{ V}$ , $PW \leq 10\ \mu\text{s}$	3.0	4.0		A
$V_S$	Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO			-9.8	-7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. These parameters guaranteed by design.

**Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS**

( $V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $V_S = \text{GND} = 0\text{ V}$ ,  $C_L = 1000\text{ pF}$ , and  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{ON}$	Turn-On Propagation Delay	$V_S = 0\text{ V}$		150	210	ns
$t_{OFF}$	Turn-Off Propagation Delay	$V_S = 0\text{ V}$		150	210	ns

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**Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS** (continued)

( $V_{BIAS} (V_{DD}, V_{BS}) = 15\text{ V}$ ,  $V_S = \text{GND} = 0\text{ V}$ ,  $C_L = 1000\text{ pF}$ , and  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_R$	Turn-On Rise Time			25	50	ns
$t_F$	Turn-Off Fall Time			15	45	ns

TYPICAL PERFORMANCE CHARACTERISTICS

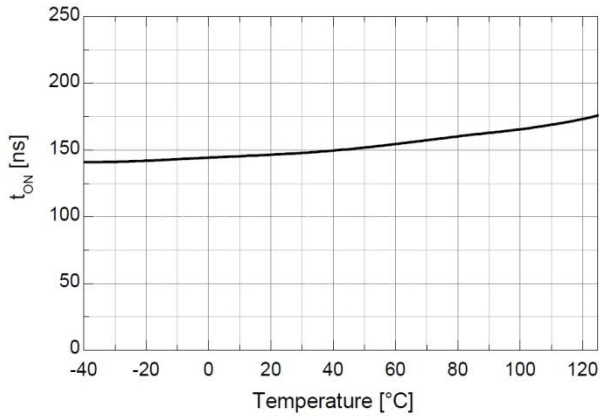


Figure 4. Turn-On Propagation Delay vs. Temperature

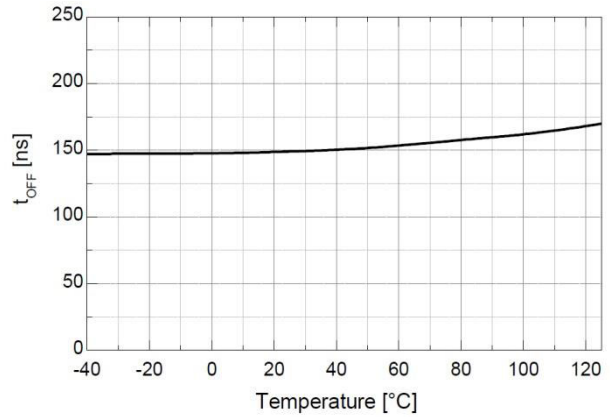


Figure 5. Turn-Off Propagation Delay vs. Temperature

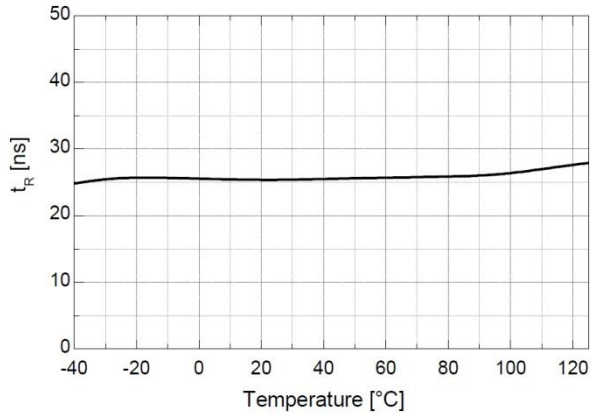


Figure 7. Turn-On Rise Time vs. Temperature

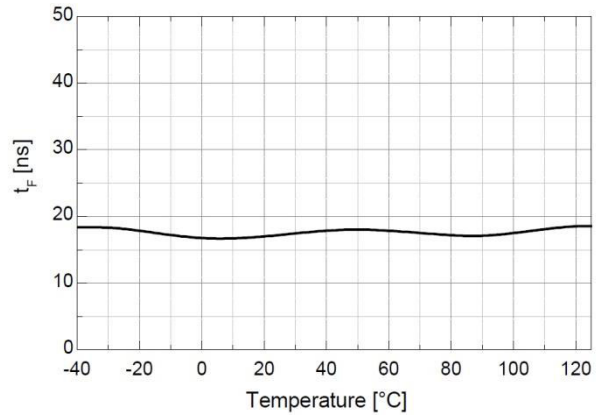


Figure 6. Turn-Off Fall Time vs. Temperature

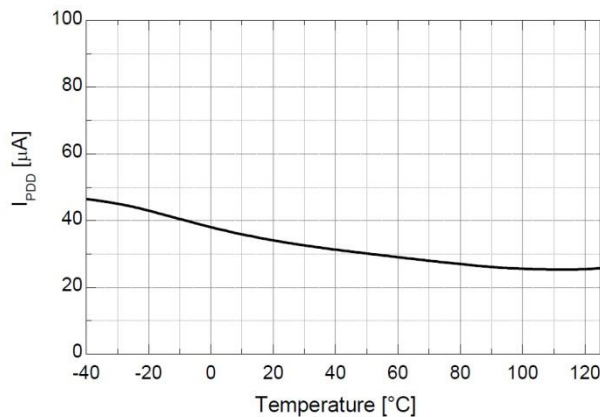


Figure 9. Operating V<sub>DD</sub> Supply Current vs. Temperature

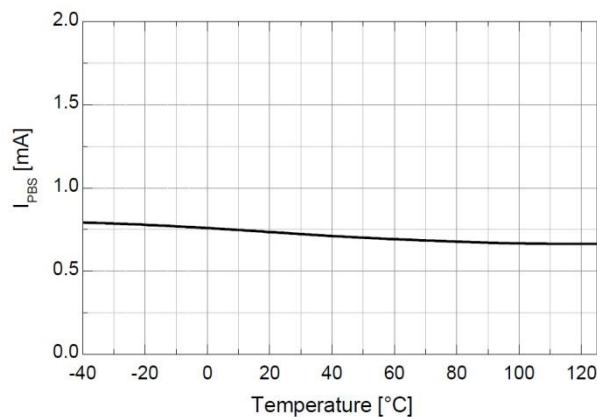


Figure 8. Operating V<sub>BS</sub> Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

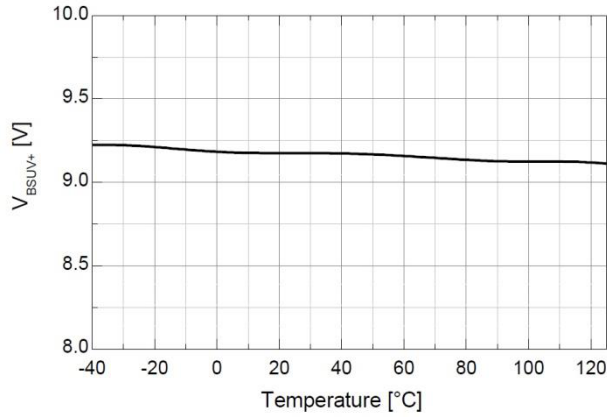


Figure 10. V<sub>BS</sub> UVLO+ vs. Temperature

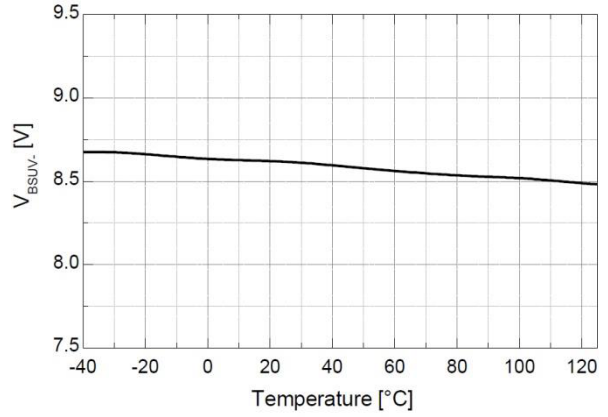


Figure 11. V<sub>BS</sub> UVLO- vs. Temperature

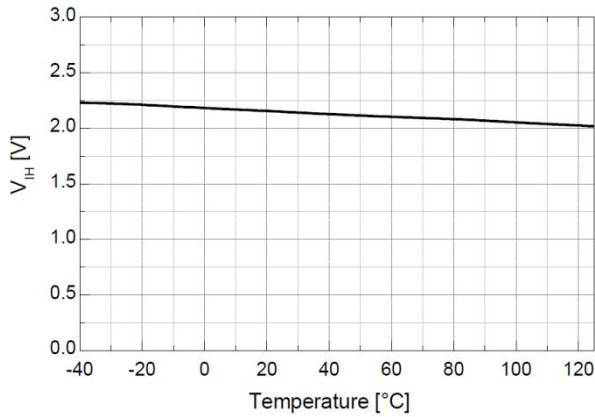


Figure 13. Logic High Input Voltage vs. Temperature

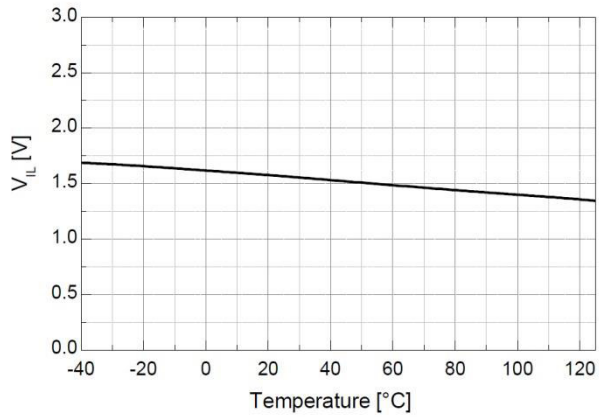


Figure 12. Logic Low Input Voltage vs. Temperature

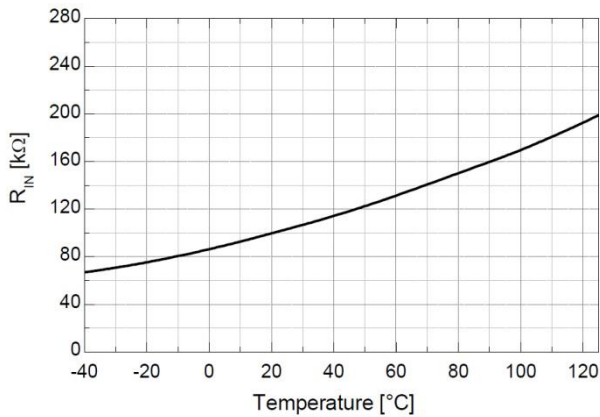


Figure 15. Input Pull-Down Resistance vs. Temperature

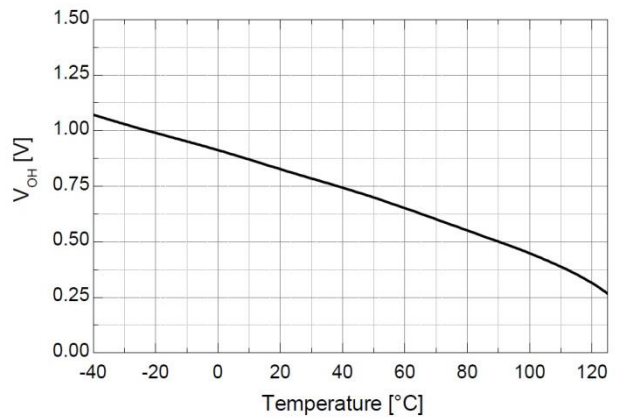


Figure 14. High-Level output Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

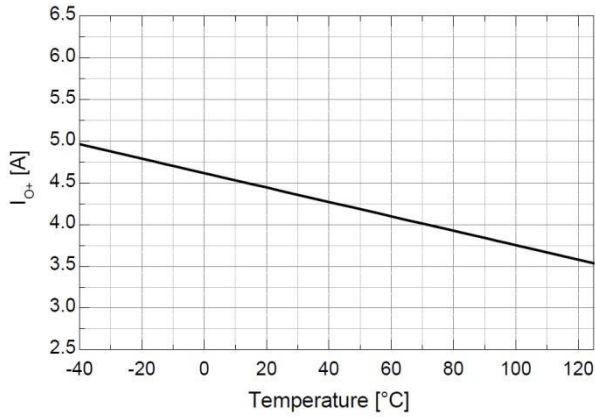


Figure 16. Output High, Short-Circuit Pulsed Current vs. Temperature

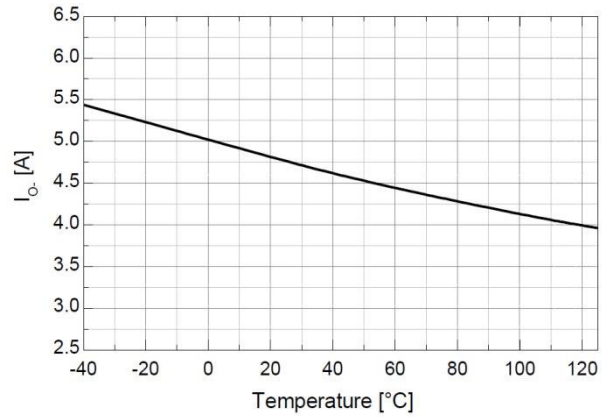


Figure 17. Output Low, Short-Circuit Pulsed Current vs. Temperature

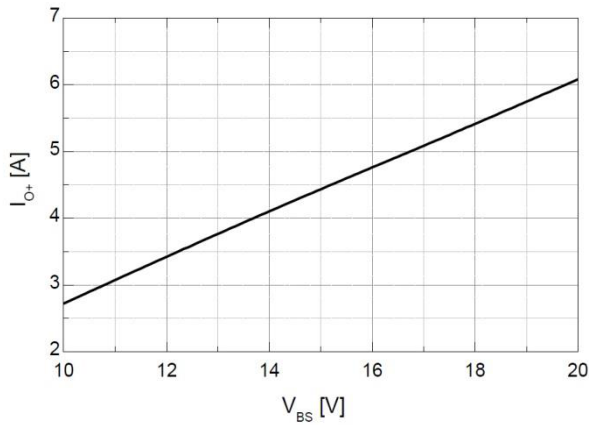


Figure 19. Output High, Short-Circuit Pulsed Current vs. Supply Voltage

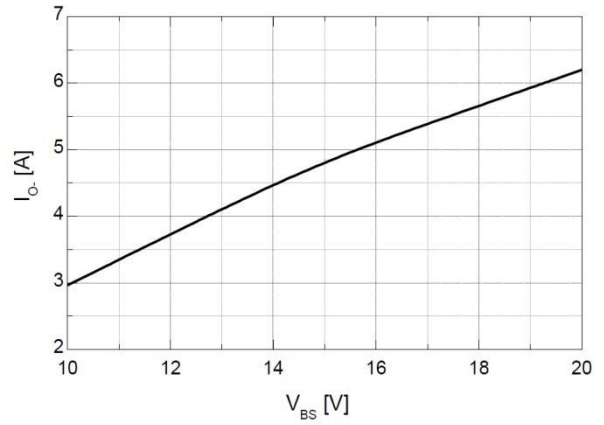


Figure 18. Output Low, Short-Circuit Pulsed Current vs. Supply Voltage

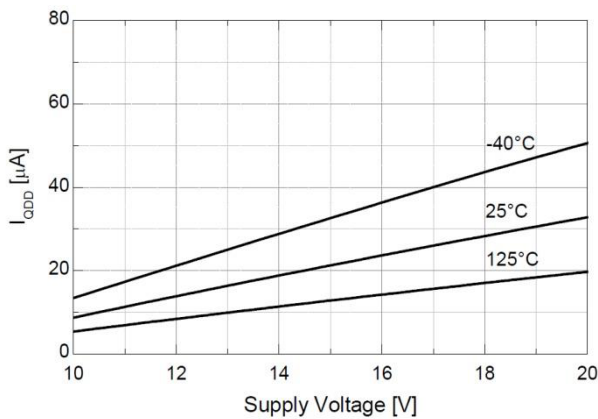


Figure 21. Quiescent  $V_{DD}$  Supply Current vs. Supply Voltage

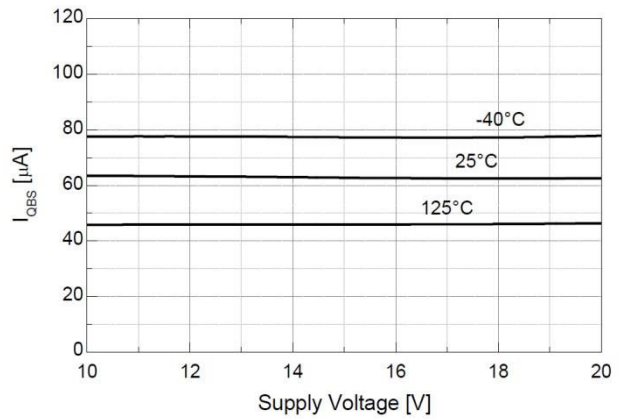


Figure 20. Quiescent  $V_{BS}$  Supply Current vs. Supply Voltage

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## SWITCHING TIME DEFINITIONS

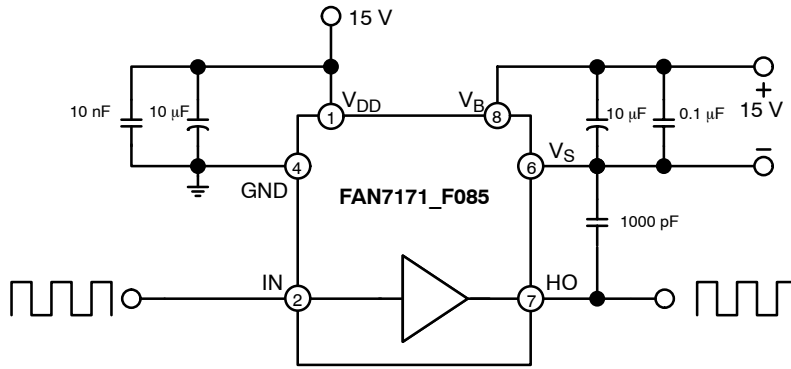


Figure 22. Switching Time Test Circuit ( Referenced 8-SOIC)

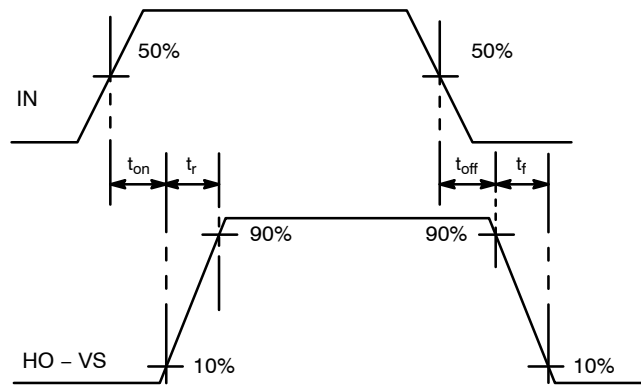


Figure 23. Switching Time Waveform Definitions

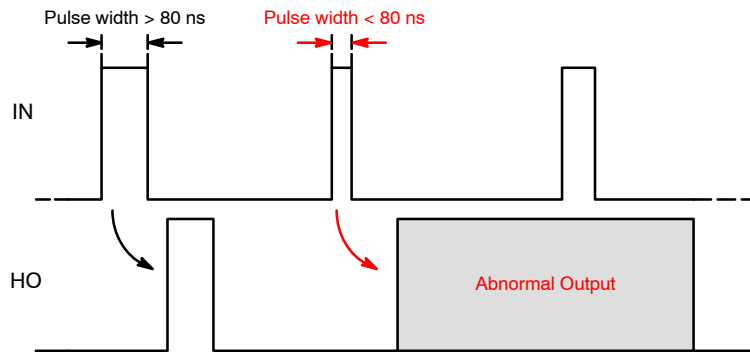


Figure 24. Output Waveform with Short Turn On Input Pulse Width

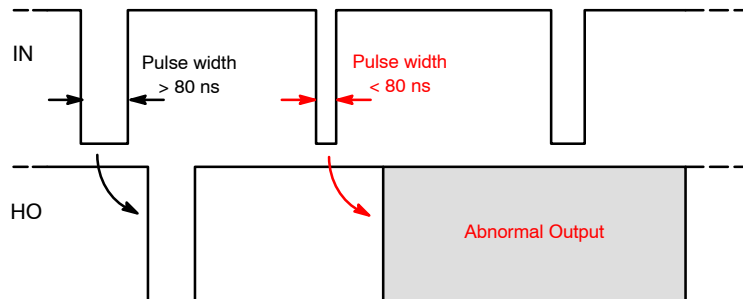


Figure 25. Output Waveform with Short Turn Off Input Pulse Width

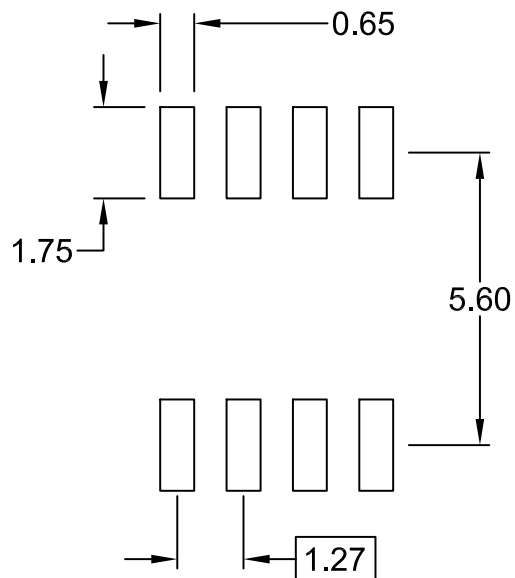
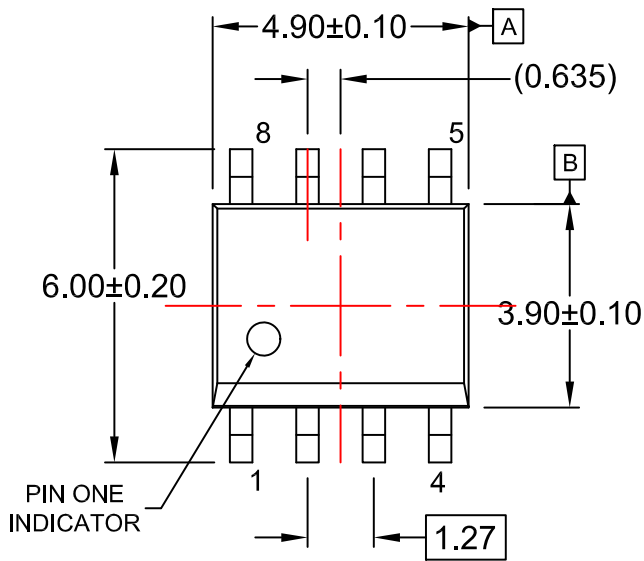
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®

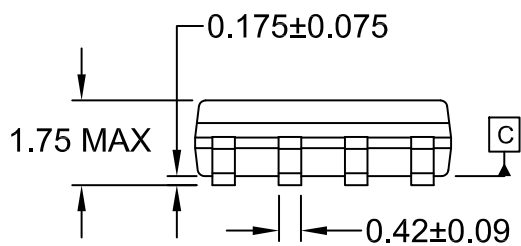


**SOIC8**  
**CASE 751EB**  
**ISSUE A**

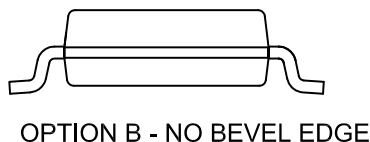
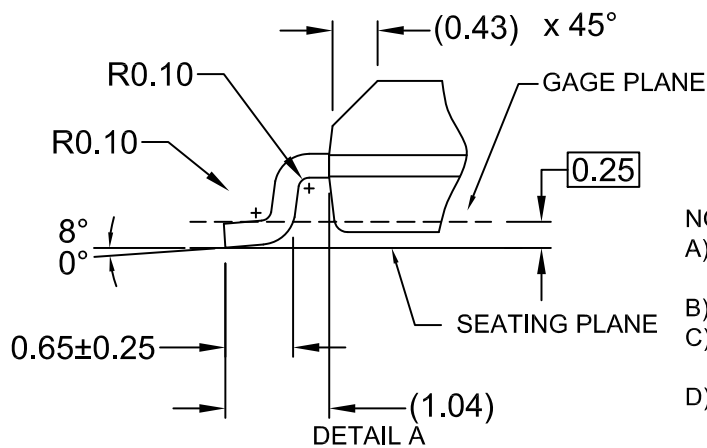
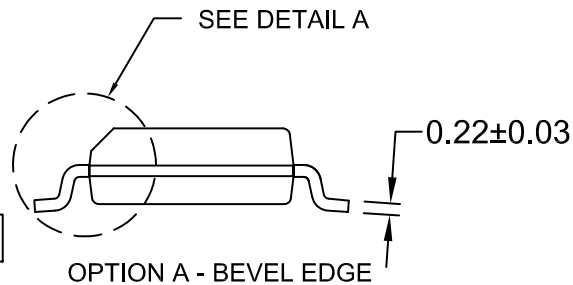
DATE 24 AUG 2017



⊕ 0.25 (M) C B A



⌒ 0.10



**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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