THE DATASHEET OF

DS17287-5

DS17285/DS17287/ DS17485/DS17487/ DS17885/DS17887

Real-Time Clocks

General Description

The DS17285, DS17485, DS17885, DS17287, DS17487, and DS17887 real-time clocks (RTCs) are designed to be successors to the industry-standard DS12885 and DS12887. The DS17285, DS17485, and DS17885 (hereafter referred to as the DS17x85) provide a real-time clock/calendar, one time-of-day alarm, three maskable interrupts with a common interrupt output, a programmable square wave, and 114 bytes of battery-backed NV SRAM. The DS17x85 also incorporates a number of enhanced functions including a silicon serial number, power-on/off control circuitry, and 2k, 4k, or 8kbytes of battery-backed NV SRAM. The DS17287, DS17487, and DS17887 (hereafter referred to as the DS17x87) integrate a quartz crystal and lithium energy source into a 24-pin encapsulated DIP package. The DS17x85 and DS17x87 power-control circuitry allows the system to be powered on by an external stimulus such as a keyboard or by a time-and-date (wake-up) alarm. The $\overline{PWR}$ output pin is triggered by one or either of these events, and is used to turn on an external power supply. The $\overline{PWR}$ pin is under software control, so that when a task is complete, the system power can then be shut down.

For all devices, the date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. It also operates in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to a backup supply. A lithium coin cell battery can be connected to the V_{BAT} input pin on the DS17x85 to maintain time and date operation when primary power is absent. The DS17x85 and DS17x87 include a V_{BAUX} input used to power auxiliary functions such as $\overline{PWR}$ control. The device is accessed through a multiplexed byte-wide interface.

Applications

- Embedded Systems
- Utility Meters
- Security Systems
- Network Hubs, Bridges, and Routers

Features

- Incorporates Industry-Standard DS12887 PC Clock Plus Enhanced Functions
- RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Through 2099
- Optional +3.0V or +5.0V Operation
- SMI Recovery Stack
- 64-Bit Silicon Serial Number
- Power-Control Circuitry Supports System Power-On from Date/Time Alarm or Key Closure
- Crystal Select Bit Allows Operation with 6pF or 12.5pF Crystal
- 12-Hour or 24-Hour Clock with AM and PM in 12-Hour Mode
- 114 Bytes of General-Purpose, Battery-Backed NV SRAM
- Extended Battery-Backed NV SRAM
  - 2048 Bytes (DS17285/DS17287)
  - 4096 Bytes (DS17485/DS17487)
  - 8192 Bytes (DS17885/DS17887)
- RAM Clear Function
- Interrupt Output with Six Independently Maskable Interrupt Flags
- Time-of-Day Alarm Once per Second to Once per Day
- End of Clock Update Cycle Flag
- Programmable Square-Wave Output
- Automatic Power-Fail Detect and Switch Circuitry
- Available in PDIP, SO, or TSOP Package (DS17285, DS17485, DS17885)
- Optional Encapsulated DIP (EDIP) Package with Integrated Crystal and Battery (DS17287, DS17487, DS17887)
- Optional Industrial Temperature Range Available
- Underwriters Laboratory (UL) Recognized

Ordering Information, Pin Configurations, and Typical Operating Circuit appear at end of data sheet.

19-5222; Rev 2; 5/16

maxim integrated™

Absolute Maximum Ratings

Voltage Range on V_{CC} Pin Relative to Ground ...-0.3V to +6.0V
Operating Temperature Range (Noncondensing)
Commercial.....0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature Range
EDIP ..... -40°C to +85°C
PDIP, SO, TSOP..... -55°C to +125°C

Lead Temperature (soldering, 10s) .....+260°C
(**Note:** EDIP is hand or wave-soldered only.)
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(**V_{CC} = +4.5V to +5.5V, or V_{CC} = +2.7V to +3.7V, T_A = Over the operating temperature range, unless otherwise noted.** Typical values are with T_A = +25°C, V_{CC} = 5.0V or 3.0V and V_{BAT} = 3.0V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 3)	V_{CC}	(-5)	4.5	5.0	5.5	V
		(-3)	2.7	3.0	3.7	
V_{BAT} Input Voltage	V_{BAT}	(Note 3)	2.5	3.0	3.7	V
V_{BAUX} Input Voltage (Note 3)	V_{BAUX}	(-5)	2.5	3.0	5.2	V
		(-3)			3.7	
Input Logic 1 (Note 3)	V_{IH}	(-5)	2.2		V_{CC} + 0.3	V
		(-3)	2.0		V_{CC} + 0.3	
Input Logic 0 (Note 3)	V_{IL}	(-5)	-0.3		+0.8	V
		(-3)	-0.3		+0.6	
V_{CC} Power-Supply Current (Note 4)	I_{CC1}	(-5)		25	50	mA
		(-3)		15	30	
V_{CC} Standby Current (Notes 4, 5)	I_{CCS}	(-5)		1.0	3.0	mA
		(-3)		0.5	2.0	
Input Leakage	I_{IL}		-1.0		+1.0	µA
I/O Leakage	I_{OL}	(Note 6)	-1.0		+1.0	µA
Output Logic 1 Voltage (Note 3)	V_{OH}	(-5), -1.0mA	2.4			V
		(-3), -0.4mA	2.4			
Output Logic 0 Voltage AD0–AD7, $\overline{IRQ}$, SQW (Note 3)	V_{OL}	(-5), +2.1mA			0.4	V
		(-3), +0.8mA			0.4	
Output Logic 0 Voltage $\overline{PWR}$ (Note 3)	V_{OL}	(-5), +10mA			0.4	V
		(-3), +4mA			0.4	
Power-Fail Voltage (Note 3)	V_{PF}	(-5)	4.25	4.37	4.5	V
		(-3)	2.5	2.6	2.7	
VRT Trip Point	VRT_{TRIP}	(Note 3)		1.3		V

DC Electrical Characteristics

(V_{CC} = 0V, V_{BAT} = 3.0V, T_A = Over the operating range, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BAT} or V_{BAUX} Current (Oscillator On); T_A = +25°C, V_{BAT} = 3.0V	I_{BAT}	(Note 7)		500	700	nA
V_{BAT} or V_{BAUX} Current (Oscillator Off)	I_{BATDR}	(Note 7)		50	400	nA

AC Electrical Characteristics

(**V_{CC} = +4.5V to +5.5V**, T_A = Over the operating range, unless otherwise noted.) (Note 2)

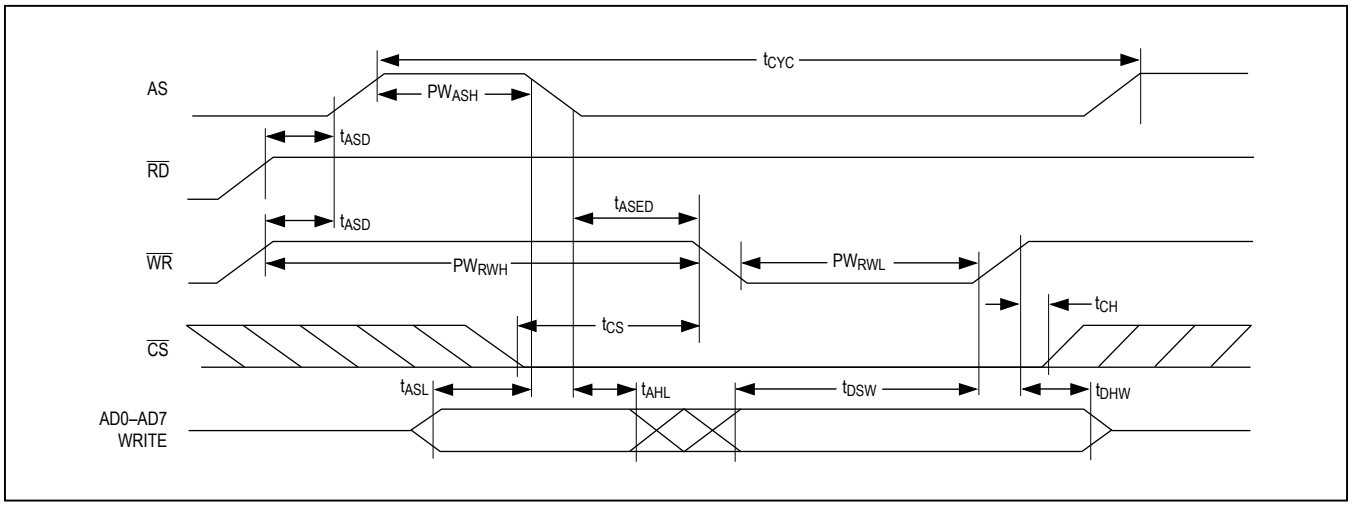
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}		240		DC	ns
Pulse Width, $\overline{RD}$ or $\overline{WR}$ Low	PW_{RWL}		120			ns
Pulse Width, $\overline{RD}$ or $\overline{WR}$ High	PW_{RWH}		80			ns
Input Rise and Fall	t_R, t_F				30	ns
Chip-Select Setup Time Before $\overline{RD}$ or $\overline{WR}$	t_{CS}		20			ns
Chip-Select Hold Time	t_{CH}		0			ns
Read-Data Hold Time	t_{DHR}		10		50	ns
Write-Data Hold Time	t_{DHW}		0			ns
Address Setup Time to ALE Fall	t_{ASL}		20			ns
Address Hold Time to ALE Fall	t_{AHL}		10			ns
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}		25			ns
Pulse Width ALE High	PW_{ASH}		40			ns
Delay Time ALE Low to $\overline{RD}$ Low	t_{ASED}		30			ns
Output Data Delay Time from $\overline{RD}$	t_{DDR}	(Note 8)	20		120	ns
Data Setup Time	t_{DSW}		30			ns
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}				2	µs

AC Electrical Characteristics

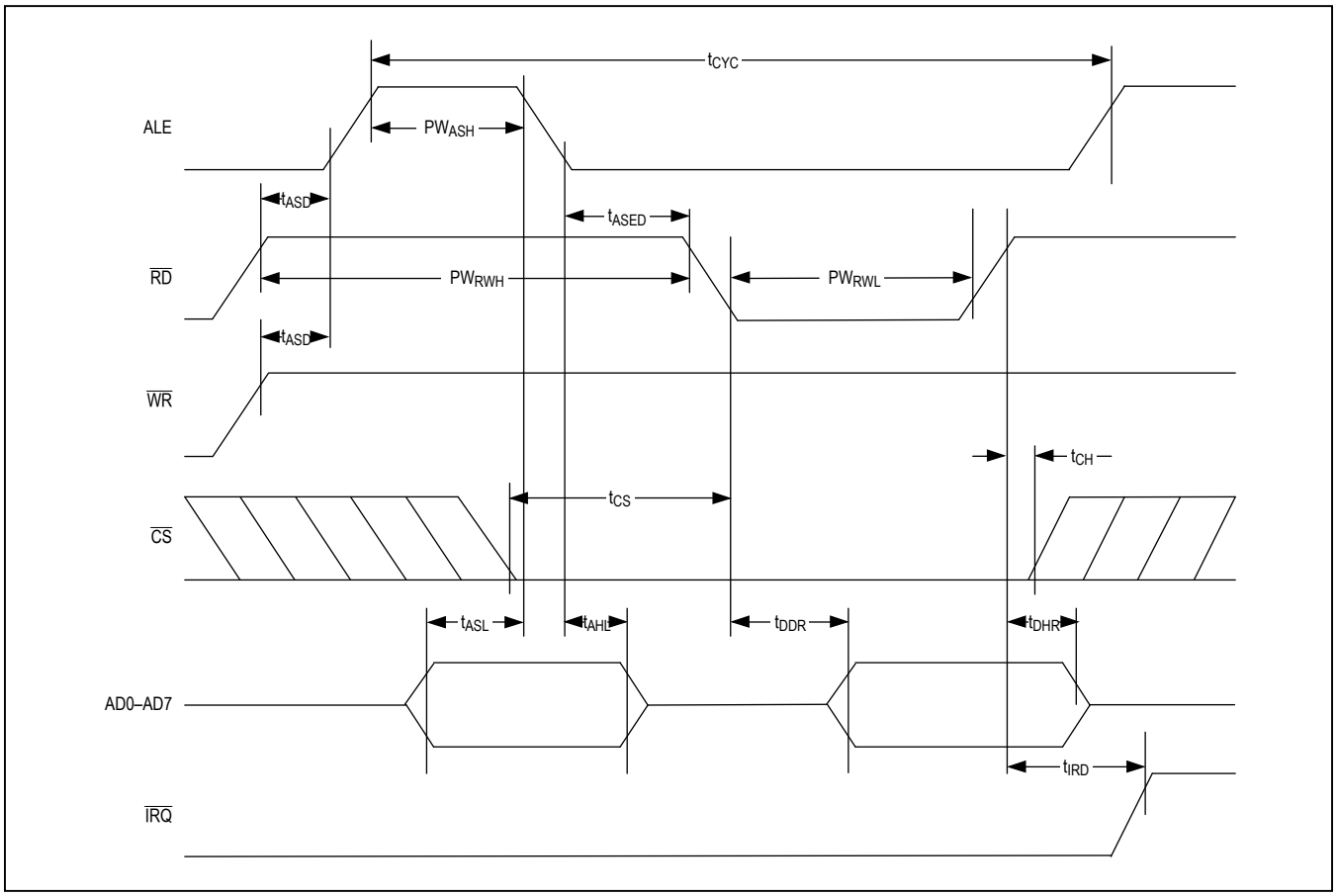
(V_{CC} **= +2.7V to +3.7V**, T_A = Over the operating range, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}		360		DC	ns
Pulse Width, $\overline{RD}$ or $\overline{WR}$ Low	PW_{RWL}		200			ns
Pulse Width, $\overline{RD}$ or $\overline{WR}$ High	PW_{RWH}		150			ns
Input Rise and Fall	t_R, t_F				30	ns
Chip-Select Setup Time Before $\overline{RD}$ or $\overline{WR}$	t_{CS}		20			ns
Chip-Select Hold Time	t_{CH}		0			ns
Read-Data Hold Time	t_{DHR}		10		90	ns
Write-Data Hold Time	t_{DHW}		0			ns
Address Setup Time to ALE Fall	t_{ASL}		40			ns
Address Hold Time to ALE Fall	t_{AHL}		10			ns
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	t_{ASD}		30			ns
Pulse Width ALE High	PW_{ASH}		40			ns
Delay Time ALE Low to $\overline{RD}$ Low	t_{ASED}		30			ns
Output Data Delay Time from $\overline{RD}$	t_{DDR}	(Note 8)	20		200	ns
Data Setup Time	t_{DSW}		70			ns
$\overline{IRQ}$ Release from $\overline{RD}$	t_{IRD}				2	µs

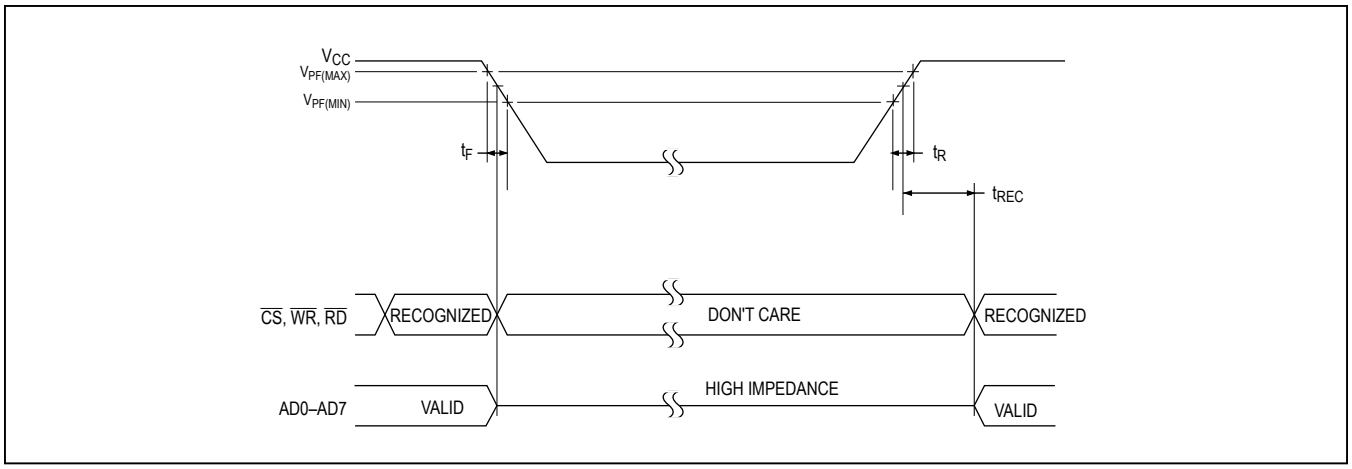
Write Timing



Read Timing



Power-Up/Power-Down Timing



Power-Up/Power-Down Characteristics

(T_A = -40°C to +85°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}	(Note 9)	20		150	ms
V_{CC} Fall Time, $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Fall Time, $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_R		0			µs

Data Retention (DS17x87 Only)

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data Retention	t_{DR}	(Note 9)	10			Years

Capacitance

(T_A = +25°C) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins Except X1	C_{IN}	(Note 10)			12	pF
Capacitance on $\overline{IRQ}$, SQW, and DQ0–DQ7 Pins	C_{IO}	(Note 10)			12	pF

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels:	0 to 3.0V
Output Load Including Scope and Jig:	50pF + 1TTL Gate
Input and Output Timing Measurement Reference Levels:	Input/Output: V_{IL} max and V_{IH} min
Input Pulse Rise and Fall Times:	5ns

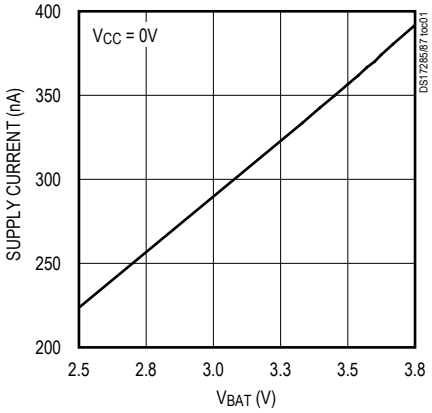
WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode can cause loss of data.

Note 1: RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. However, post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibrations not used to prevent damage to the crystal.
Note 2: Limits at -40°C are guaranteed by design and not production tested.
Note 3: All voltages are referenced to ground.
Note 4: All outputs are open.
Note 5: Specified with $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = V_{CC}, ALE, AD0–AD7 = 0.
Note 6: Applies to the AD0–AD7 pins, $\overline{IRQ}$, and SQW when each is in a high-impedance state.
Note 7: Measured with a 32.768kHz crystal attached to X1 and X2.
Note 8: Measured with a 50pF capacitance load plus 1TTL gate.
Note 9: If the oscillator is disabled in software, or if the countdown chain is in reset, t_{REC} is bypassed, and the part becomes immediately accessible.
Note 10: Guaranteed by design. Not production tested.

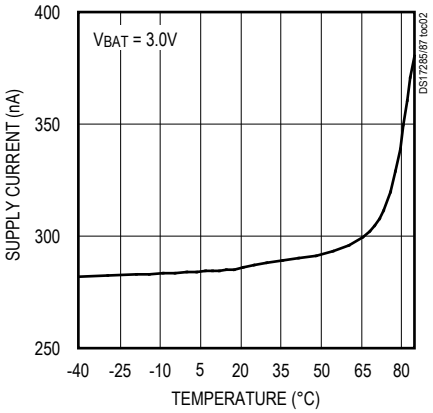
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

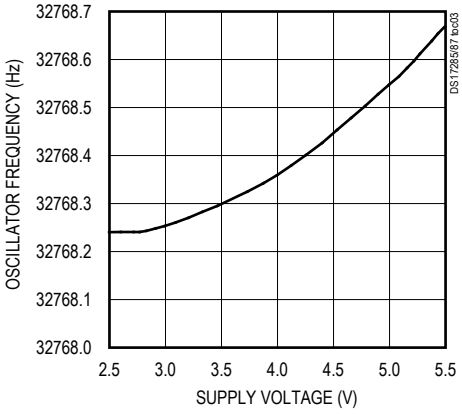
SUPPLY CURRENT vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



Pin Description

PIN		NAME	FUNCTION
24	28		
1	8	$\overline{PWR}$	Active-Low Power-On Reset. This open-drain output pin is intended for use as an on/off control for the system power. With V_{CC} voltage removed from the device, $\overline{PWR}$ can be automatically activated from a kickstart input by the $\overline{KS}$ pin or from a wake-up interrupt. Once the system is powered on, the state of $\overline{PWR}$ can be controlled by bits in the control registers. The $\overline{PWR}$ pin can be connected through a pullup resistor to a positive supply. For 5V operation, the voltage of the pullup supply should be no greater than 5.7V. For 3V operation, the voltage on the pullup supply should be no greater than 3.9V.
2, 3	9, 10	X1, X2	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF or 12.5pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is left unconnected if an external oscillator is connected to pin X1. These pins are missing (N.C.) on the EDIP package.
4–11	12–17, 19, 20	AD0–AD7	Multiplexed Bidirectional Address/Data Bus. The addresses are presented during the first portion of the bus cycle and latched into the device by the falling edge of ALE. Write data is latched by the rising edge of $\overline{WR}$. In a read cycle, the device outputs data during the latter portion of the $\overline{RD}$ low. The read cycle is terminated and the bus returns to a high-impedance state as $\overline{RD}$ transitions high.
12, 16	21, 22, 26	GND	Ground

Pin Description (continued)

PIN		NAME	FUNCTION
24	28		
13	23	$\overline{CS}$	Active-Low Chip-Select Input. This pin must be asserted low during a bus cycle for the device to be accessed. $\overline{CS}$ must be kept in the active state during $\overline{RD}$ and $\overline{WR}$. Bus cycles that take place without asserting $\overline{CS}$ latch addresses, but no access occurs.
14	24	ALE	Address Latch Enable Input, Active High. This input pin is used to demultiplex the address/data bus. The falling edge of ALE causes the address to be latched within the device.
15	25	$\overline{WR}$	Active-Low Write Input. This pin defines the period during which data is written to the addressed register.
17	27	$\overline{RD}$	Active-Low Read Input. This pin identifies the period when the device drives the bus with read data. It is an enable signal for the output buffers of the device.
18	28	$\overline{KS}$	Active-Low Kickstart Input. When V_{CC} is removed from the device, the system can be powered on in response to an active-low transition on the $\overline{KS}$ pin, as might be generated from a key closure. V_{BAUX} must be present and auxiliary-battery-enable bit (ABE) must be set to 1 if the kickstart function is used, and the $\overline{KS}$ pin must be pulled up to the V_{BAUX} supply. While V_{CC} is applied, the $\overline{KS}$ pin can be used as an interrupt input. If not used, $\overline{KS}$ must be grounded and ABE set to 0.
19	1	$\overline{IRQ}$	Active-Low Interrupt Request. This pin is an active-low output that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the application software must clear all enabled flag bits contributing to the pin's active state. When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{IRQ}$ bus, provided that they are all open drain. The $\overline{IRQ}$ pin requires an external pullup resistor to V_{CC}.
20	2	V_{BAT}	Connection for Primary Battery. This supply input is used to power the normal clock functions when V_{CC} is absent. Diodes placed in series between V_{BAT} and the battery can prevent proper operation. If V_{BAT} is not required, the pin must be grounded. UL recognized to ensure against reverse charging current when used with a lithium battery (www.maximintegrated.com/qa/info/ul). This pin is missing (N.C.) on the EDIP package.

Pin Description (continued)

PIN		NAME	FUNCTION
24	28		
21	3	$\overline{RCLR}$	Active-Low RAM Clear Input. This pin is used to clear (set to logic 1) all the 114 bytes of general-purpose RAM but does not affect the RAM associated with the real time clock or extended RAM. $\overline{RCLR}$ may be invoked while the part is powered from any supply. The $\overline{RCLR}$ function is designed to be used via a human interface (shorting to ground manually or by a switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pullup resistor on this pin.
22	4	V_{BAUX}	Auxiliary Battery Input. Required for kickstart and wake-up functions. This input also supports clock/calendar and user RAM if V_{BAT} is at lower voltage or is not used. A standard +3V lithium cell or other energy source can be used. Diodes placed in series between V_{BAUX} and the battery may prevent proper operation. UL recognized to ensure against reverse charging current when used with a lithium battery (www.maximintegrated.com/qa/info/ul/). For 3V V_{CC} operation, V_{BAUX} must be held between +2.5V and +3.7V. For 5V V_{CC} operation, V_{BAUX} must be held between +2.5V and +5.2V. If V_{BAUX} is not used it should be grounded and the auxiliary-battery-enable bit bank 1, register 4BH, should = 0.
23	5	SQW	Square-Wave Output. When V_{CC} rises above V_{PF}, bits DV1 and E32k are set to 1. This condition enables a 32kHz square-wave output. A square wave is output if either SQWE = 1 or E32k = 1. If E32k = 1, then 32kHz is output regardless of the other control bits. If E32k = 0, then the output frequency is dependent on the control bits in Register A. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 3. The SQW signal can be turned on and off using the SQWE bit in Register B or the E32k bit in extended register 4Bh. A 32kHz square wave is also available when V_{CC} is less than V_{PF} if E32k = 1, ABE = 1, and voltage is applied to the V_{BAUX} pin. When disabled, SQW is high impedance when V_{CC} is below V_{PF}.
24	6, 7	V_{CC}	DC Power Pin for Primary Power Supply. When V_{CC} is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below V_{PF} reads and writes are inhibited.
2, 3, 16, 20 (DS17x87 only)	11, 18	N.C.	No Connection

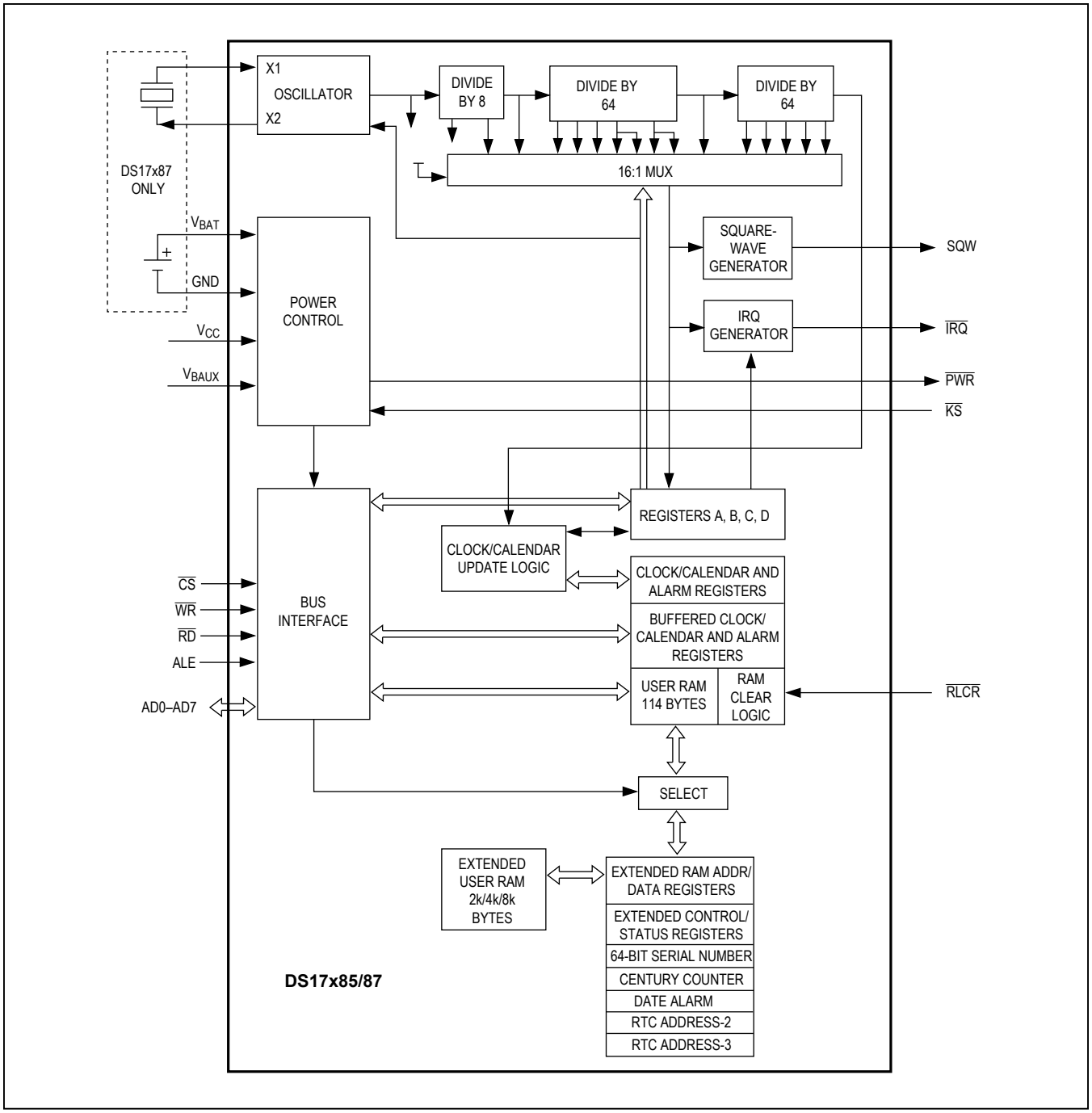


Figure 1. Functional Diagram

Detailed Description

The DS17x85 is a successor to the DS1285 real-time clock (RTC). The device provides 18 bytes of real-time clock/calendar, alarm, and control/status registers and 114 bytes of nonvolatile battery-backed RAM. The device also provides additional extended RAM in either 2k/4k/8kbytes (DS17285/DS17485/DS17885). A time-of-day alarm, six maskable interrupts with a common interrupt output, and a programmable square-wave output are available. It also operates in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power-supply failure is detected, the device automatically switches to a backup supply. The backup supply input supports a primary battery, such as a lithium coin cell. The device is accessed by a multiplexed address/data bus.

Oscillator Circuit

The DS17x85 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal, and Figure 2 shows a functional schematic of the oscillator circuit. The oscillator is controlled by an enable bit in the control register. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

An external 32.768kHz oscillator can also drive the DS17x85. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 3 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Clock Accuracy (DS17287, DS17487, and DS17887)

The encapsulated DIP (EDIP) modules are trimmed at the factory to ±1 minute per month accuracy at 25°C.

Table 1. Crystal Specifications* (DS17x85 Only)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		6 or 12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.*

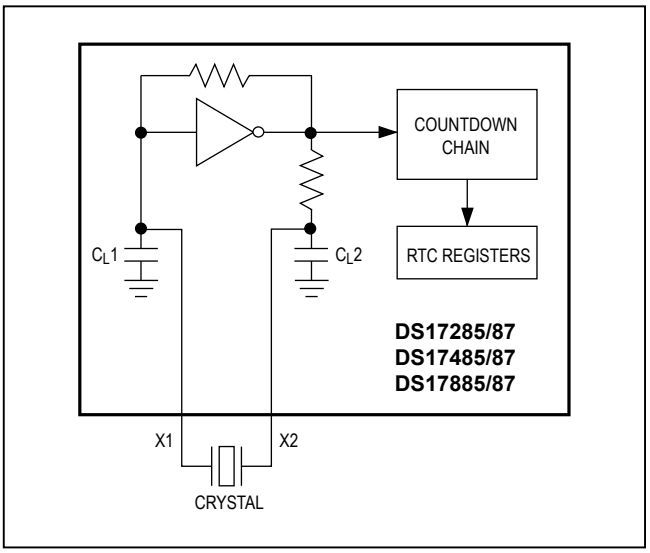


Figure 2. Oscillator Circuit Showing Internal Bias Network

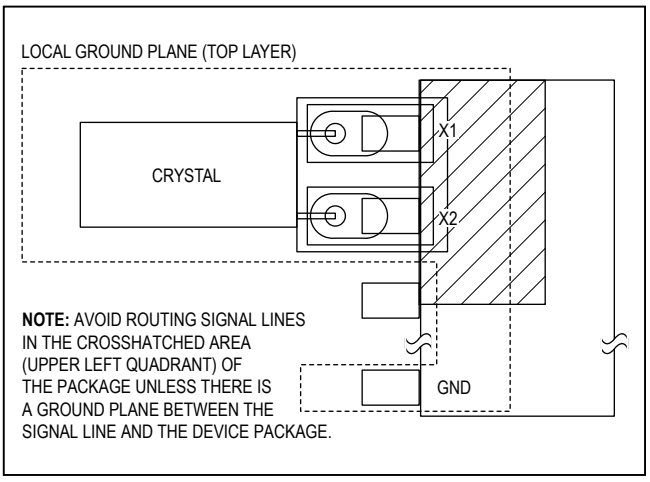


Figure 3. Layout Example

Power-Down/Power-Up Considerations

The RTC function continues to operate, and all the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. V_{BAT} or V_{BAUX} must remain within the minimum and maximum limits when V_{CC} is not applied. When V_{CC} falls below V_{PF}, the device inhibits all access, putting the part into a low-power mode. When V_{CC} is applied and exceeds V_{PF} (power-fail trip point), the device becomes accessible after t_{REC}, if the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time period allows the system to stabilize after power is applied. If the oscillator is not enabled, the oscillator enable bit is enabled on powerup, and the device becomes immediately accessible.

Power Control

The power control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the device inhibits read and write access. If V_{PF} is less than V_{BAT}, the device power is switched from V_{CC} to the higher of V_{BAT} or V_{BAUX} when V_{CC} drops below V_{PF}. If V_{PF} is greater than the higher of V_{BAT} or V_{BAUX}, the device power is switched from V_{CC} to the higher of V_{BAT} or V_{BAUX} when V_{CC} drops below the higher backup source. The registers are maintained from the V_{BAT} or V_{BAUX} source until V_{CC} is returned to nominal levels. After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC}.

Table 2. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < (V_{BAT} \mid V_{BAUX})$	No	V_{BAT} or V_{BAUX}
$V_{CC} < V_{PF}$, $V_{CC} > (V_{BAT} \mid V_{BAUX})$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < (V_{BAT} \mid V_{BAUX})$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > (V_{BAT} \mid V_{BAUX})$	Yes	V_{CC}

Time, Calendar, and Alarm Locations

The time and calendar information is obtained by reading the appropriate register bytes. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the 12 time, calendar, and alarm bytes can be either binary or binary-coded decimal (BCD) format. Tables 3A and 3B show the BCD and binary formats of the 12 time, date, and alarm registers, control registers A to D, plus the two extended registers that reside in bank 1 only (bank 0 and bank 1 switching is explained later in this text).

The day-of-week register increments at midnight, incrementing from 1 through 7. The day-of-week register is used by the daylight saving function, and so the value 1 is defined as Sunday. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years.

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 12 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 12 time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 12 data bytes. Tables 3A and 3B show the BCD and binary formats of the 12 time, calendar, and alarm locations.

The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is logic 1. The time, calendar, and alarm bytes are always accessible because they are double-buffered. Once per second, the eight bytes are advanced by one second and checked for an alarm condition.

If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm enable bit is high. In this mode, the "0" bits in the alarm registers and the corresponding time registers must always be written to 0 (see Table 3A and 3B). Writing the 0 bits in the alarm and/or time registers to 1 can result in undefined operation.

The second use condition is to insert a "don't care" state in one or more of the alarm bytes. The don't care code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the don't care condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with don't care codes in the hours and minute alarm bytes. An alarm is generated every second with don't care codes in the hours, minutes, and seconds alarm bytes.

All 128 bytes can be directly written or read except for the following:

1) Registers C and D are read-only.
2) Bit 7 of register A is read-only.
3) The MSB of the seconds byte is read-only.

Table 3A. Time, Calendar, and Alarm Data Modes—BCD Mode (DM = 0)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Seconds			Seconds				Seconds Alarm	00–59
02h	0	10 Minutes			Minutes				Minutes	00–59
03h	0	10 Minutes			Minutes				Minutes Alarm	00–59
04h	$\overline{AM}$/PM	0	0	10 Hour	Hours				Hours	1–12 + $\overline{AM}$/PM
	0		10 Hour							00–23
05h	$\overline{AM}$/PM	0	0	10 Hour	Hours				Hours Alarm	1–12 + $\overline{AM}$/PM
	0		10 Hour							00–23
06h	0	0	0	0	0	Day			Day	01–07
07h	0	0	10 Date		Date				Date	01–31
08h	0	0	0	10 Month	Month				Month	01–12
09h	10 Year				Year				Year	00–99
0Ah	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0Bh	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0Ch	IRQF	PF	AF	UF	0	0	0	0	Control	—
0Dh	VRT	0	0	0	0	0	0	0	Control	—
Bank 1, 48h	10 Century				Century				Century	00–99
Bank 1, 49h	10 Date				Date				Date Alarm	01–31

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but can be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Table 3B. Time, Calendar, and Alarm Data Modes—Binary Mode (DM = 1)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	0	0	Seconds						Seconds	00–3B
01h	0	0	Seconds						Seconds Alarm	00–3B
02h	0	0	Minutes						Minutes	00–3B
03h	0	0	Minutes						Minutes Alarm	00–3B
04h	$\overline{AM}$/PM	0	0	0	Hours				Hours	1–0C + AM/PM
	0			Hours						00–17
05h	$\overline{AM}$/PM	0	0	0	Hours				Hours Alarm	1–0C + AM/PM
	0			Hours						00–17
06h	0	0	0	0	0	Day			Day	01–07
07h	0	0	0	Date					Date	01–1F
08h	0	0	0	0	Month				Month	01–0C
09h	0	Year							Year	00–63
0Ah	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0Bh	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0Ch	IRQF	PF	AF	UF	0	0	0	0	Control	—
0Dh	VRT	0	0	0	0	0	0	0	Control	—
Bank 1, 48h	10 Century				Century				Century	00–63
Bank 1, 49h	10 Date				Date				Date Alarm	01–1F

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but can be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Control Registers

The four control registers (A, B, C, and D) reside in both bank 0 and bank 1. These registers are accessible at all times, even during the update cycle.

Register A (0Ah)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7: Update In Progress (UIP). This bit is a status flag that can be monitored. When the UIP bit is 1, the update transfer will soon occur. When UIP is 0, the update transfer does not occur for at least 244µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only. Writing the SET bit in Register B to 1 inhibits any update transfer and clears the UIP status bit.

Bits 6, 5, and 4: DV2, DV1, and DV0. These bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 01X is the only combination of bits that turns the oscillator on and allows the RTC to keep time. A pattern of 11X enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 01X is written to DV0, DV1, and DV2. DV0 is used to select bank 0 or bank 1 as defined in Table 5. When DV0 is set to 0, bank 0 is selected. When DV0 is set to 1, bank 1 is selected.

Bits 3 to 0: Rate Selector Bits (RS3 to RS0). These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1) Enable the interrupt with the PIE bit;
2) Enable the SQW output pin with the SQWE or E32k bits;
3) Enable both at the same time and the same rate; or
4) Enable neither.

Table 4 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits.

Table 4. Periodic Interrupt Rate and Square-Wave Output Frequency

EXT REG B	SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
E32K	RS3	RS2	RS1	RS0		
0	0	0	0	0	None	None
0	0	0	0	1	3.90625ms	256Hz
0	0	0	1	0	7.8125ms	128Hz
0	0	0	1	1	122.070Fs	8.192kHz
0	0	1	0	0	244.141Fs	4.096kHz
0	0	1	0	1	488.281Fs	2.048kHz
0	0	1	1	0	976.5625Fs	1.024kHz
0	0	1	1	1	1.953125ms	512Hz
0	1	0	0	0	3.90625ms	256Hz
0	1	0	0	1	7.8125ms	128Hz
0	1	0	1	0	15.625ms	64Hz
0	1	0	1	1	31.25ms	32Hz
0	1	1	0	0	62.5ms	16Hz
0	1	1	0	1	125ms	8Hz
0	1	1	1	0	250ms	4Hz
0	1	1	1	1	500ms	2Hz
1	X	X	X	X	*	32.768kHz

**RS3 to RS0 determine periodic interrupt rates as listed for E32K = 0.*

Register B (0Bh)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7: SET. When the SET bit is 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to 1, any update transfer is inhibited, and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit and is not affected by any internal functions of the DS17x85.

Bit 6: Periodic Interrupt Enable (PIE). This bit is a read/write bit that allows the periodic interrupt flag (PF) bit in Register C to drive the $\overline{IRQ}$ pin low. When PIE is set to 1, periodic interrupts are generated by driving the $\overline{IRQ}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{IRQ}$ output from being driven by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal DS17x85 functions.

Bit 5: Alarm Interrupt Enable (AIE). This bit is a read/write bit that, when set to 1, permits the alarm flag (AF) bit in Register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a don't care alarm code of binary 11XXXXXX. When the AIE bit is set to 0, the AF bit does not initiate the $\overline{IRQ}$ signal. The internal functions of the DS17x285/87 do not affect the AIE bit.

Bit 4: Update-Ended Interrupt Enable (UIE). This bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert $\overline{IRQ}$. The SET bit going high clears the UIE bit.

Bit 3: Square-Wave Enable (SQWE). When this bit is set to 1 and E32k = 0, a square-wave signal at the frequency set by RS3–RS0 is driven out on the SQW pin. When the SQWE bit is set to 0 and E32k = 0, the SQW pin is held low. SQWE is a read/write bit. SQWE is set to 1 when V_{CC} is powered up.

Bit 2: Data Mode (DM). This bit indicates whether time and calendar information is in binary or BCD format. The program sets the DM bit to the appropriate format and can be read as required. This bit is not modified by internal functions. A 1 in DM signifies binary data, while a 0 in DM specifies binary-coded decimal (BCD) data.

Bit 1: 24/12 Control (24/12). This bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions.

Bit 0: Daylight Saving Enable (DSE). This bit is a read/write bit that enables two daylight saving adjustments when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59AM to 3:00:00AM. On the last Sunday in October when the time first reaches 1:59:59AM, it changes to 1:00:00AM. When DSE is enabled, the internal logic tests for the first/last Sunday condition at midnight. If the DSE bit is not set when the test occurs, the daylight saving function does not operate correctly. These adjustments do not occur when the DSE bit is zero. This bit is not affected by internal functions.

Register C (0Ch)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

Bit 7: Interrupt Request Flag (IRQF). This bit is set to 1 when any of the following are true:

PF = PIE = 1 WF = WIE = 1

AF = AIE = 1 KF = KSE = 1

UF = UIE = 1 RF = RIE = 1

Any time the IRQF bit is 1, the $\overline{IRQ}$ pin is driven low. Flag bits PF, AF, and UF are cleared after reading Register C.

Bit 6: Periodic Interrupt Flag (PF). This is a read-only bit that is set to 1 when an edge is detected on the selected tap of the divider chain. The RS3–RS0 bits establish the periodic rate. PF is set to 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{IRQ}$ signal is active and sets the IRQF bit. Reading Register C clears this bit.

Bit 5: Alarm Interrupt Flag (AF). A 1 in this bit indicates that the current time has matched the alarm time. If the AIE bit is also 1, the $\overline{IRQ}$ pin goes low and a 1 appears in the IRQF bit. Reading Register C clears this bit.

Bit 4: Update-Ended Interrupt Flag (UF). This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be 1, which asserts $\overline{IRQ}$. Reading Register C clears this bit.

Bits 3 to 0: Unused. These unused bits always read 0 and cannot be written.

Register D (0Dh)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

Register D (0Dh)

Bit 7: Valid RAM and Time (VRT). This bit indicates the condition of the battery connected to the V_{BAT} and V_{BAUX} pin. If either supply is above the internal voltage threshold, VRT_{TRIP}, the bit will be high. This bit is not writeable and should always be a 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable.

Bits 6 to 0: Unused. These bits cannot be written and, when read, always read 0.

Nonvolatile RAM

The user RAM bytes are not dedicated to any special function within the DS17x85. They can be used by the processor program as battery-backed memory and are fully available during the update cycle.

The user RAM is divided into two separate memory banks. When the bank 0 is selected, the 14 real-time clock registers and 114 bytes of user RAM are accessible. When bank 1 is selected, an additional 2kbytes, 4kbytes, or 8kbytes of user RAM are accessible through the extended RAM address and data registers.

Interrupts

The RTC includes six separate, fully automatic sources of interrupt for a processor:

1) Alarm Interrupt
2) Periodic Interrupt
3) Update-Ended Interrupt
4) Wake-Up Interrupt
5) Kickstart Interrupt
6) RAM Clear Interrupt

The conditions that generate each of these independent interrupt conditions are described in detail in other sections of this data sheet. This section describes the overall control of the interrupts.

The application software can select which interrupts, if any, are to be used. There are 6 bits, including 3 bits in Register B and 3 bits in Extended Register 4B, that enable the interrupts. The extended register locations are described later. Writing logic 1 to an interruptenable bit permits that interrupt to be initiated when the event occurs. A logic 0 in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the event initiating the interrupt condition might have occurred much earlier. Therefore, there are cases where the software should clear these earlier generated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C or in Extended Register 4A. These flag bits are set regardless of the setting of the corresponding enable bit located either in Register B or in Extended Register 4B. The flag bits can be used in a polling mode without enabling the corresponding enable bits.

However, care should be taken when using the flag bits of Register C as they are automatically cleared to 0 immediately after they are read. Double latching is implemented on these bits so that set bits remain stable throughout the read cycle. All bits that were set are cleared when read and new interrupts that are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each used flag bit should be examined when read to ensure that no interrupts are lost.

The flag bits in Extended Register 4A are not automatically cleared following a read. Instead, each flag bit can be cleared to 0 only by writing 0 to that bit.

When using the flag bits with fully enabled interrupts, the $\overline{IRQ}$ line is driven low when an interrupt flag bit is set and its corresponding enable bit is also set. $\overline{IRQ}$ is held low as long as at least one of the six possible interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is 1 whenever the $\overline{IRQ}$ pin is being driven low as a result of one of the six possible active sources. Therefore, determination that the DS17x85/DS17x87 initiated an interrupt is accomplished by reading Register C and finding IRQF = 1. IRQF remains set until all enabled interrupt flag bits are cleared to 0.

Oscillator Control Bits

A pattern of 01X in bits 4 to 6 of Register A turns the oscillator on and enables the countdown chain. A pattern of 11X (DV2 = 1, DV1 = 1, DV0 = X) turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 to 6 keep the oscillator off.

When the DS17x87 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system.

Square-Wave Output Selection

Thirteen of the 15 divider taps are made available to a 1-of-16 multiplexer, as shown in Figure 1. The square wave and periodic interrupt generators share the output of the multiplexer. The RS0–RS3 bits in Register A establish the output frequency of the multiplexer. These frequencies are listed in Table 4. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square-wave enable bit (SQWE).

If E32K = 0, the square-wave output is determined by the RS3 to RS0 bits. If E32K = 1, a 32kHz square wave is output on the SQW pin, regardless of the RS3 to RS0 bits' state. If E32K = ABE = 1 and a valid voltage is applied to V_{BAUX}, a 32kHz square wave is output on SQW when V_{CC} is below V_{TP}.

Periodic Interrupt Selection

The periodic interrupt causes the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits that select the squarewave frequency (see Table 4). Changing the Register A bits affects both the square-wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE and E32k bits control the square-wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

Update Cycle

The DS17x85 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, and alarm bytes is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers, and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a don't care code is present in all alarm locations.

There are three methods that can handle access of the RTC that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress (UIP) bit in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1 ($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

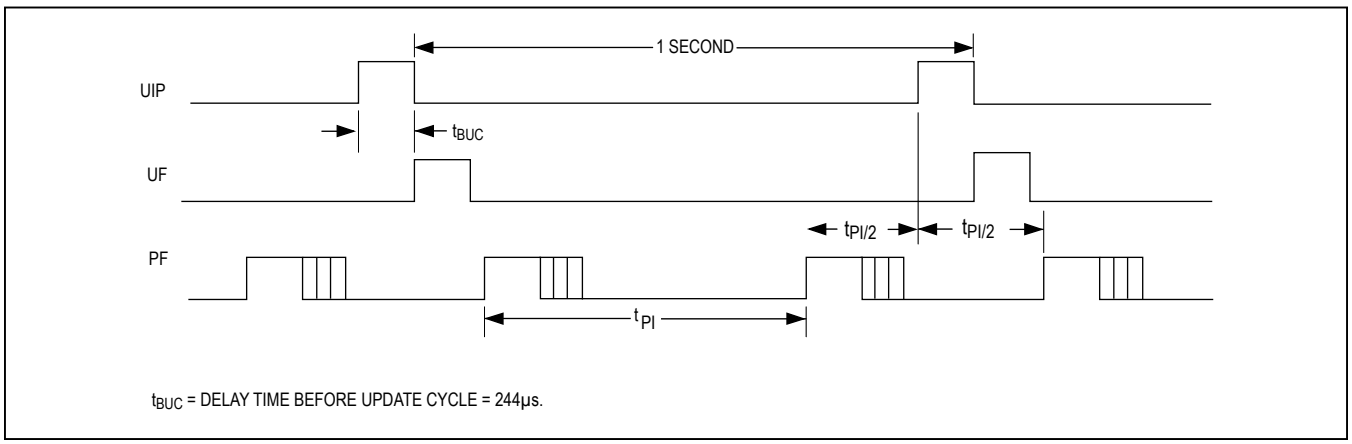


Figure 4. UIP and Periodic Interrupt Timing

Extended Functions

The extended functions provided by the DS17x85/DS17x87 that are new to the RAMified RTC family are accessed by a software-controlled bank-switching scheme, as illustrated in Table 5. In bank 0, the clock/calendar registers and 50 bytes of user RAM are in the same locations as for the DS1287. As a result, existing routines implemented within BIOS, DOS, or application software packages can gain access to the DS17x85/DS17x87 clock registers with no changes. Also in bank 0, an extra 64 bytes of RAM are provided at addresses just above the original locations for a total of 114 directly addressable bytes of user RAM.

When bank 1 is selected, the clock/calendar registers and the original 50 bytes of user RAM still appear as bank 0. However, the extended registers that provide control and status for the extended functions are accessed in place of the additional 64 bytes of user RAM. The major extended functions controlled by the extended registers are listed below:

- 64-Bit Silicon Serial Number
- Century Counter
- RTC Write Counter
- Date Alarm
- Auxiliary Battery Control/Status
- Wake-Up
- Kickstart
- RAM Clear Control/Status
- Extended RAM Access

The bank selection is controlled by the state of the DV0 bit in register A. To access bank 0 the DV0 bit should be written to a 0. To access bank 1, DV0 should be written to 1. Register locations designated as reserved in the bank 1 map are reserved for future use by Dallas Semiconductor. Bits in these locations cannot be written and return a 0 if read.

Silicon Serial Number

A unique 64-bit lasered serial number is located in bank 1, registers 40h–47h. This serial number is divided into three parts. The first byte in register 40h contains a model number to identify the device type of the DS17x85/DS17x87. Registers 41h–46h contain a unique binary number. Register 47h contains a CRC byte used to validate the data in registers 40h–46h. The CRC polynomial is $X^8 + X^5 + X^4 + 1$. See Figure 5. All 8 bytes of the serial number are read-only registers. The DS17x85/DS17x87 is manufactured such that no two devices contain an identical number in locations 41h–47h.

DEVICE	MODEL NUMBER
DS17285/87	72h
DS17485/87	74h
DS17885/87	78h

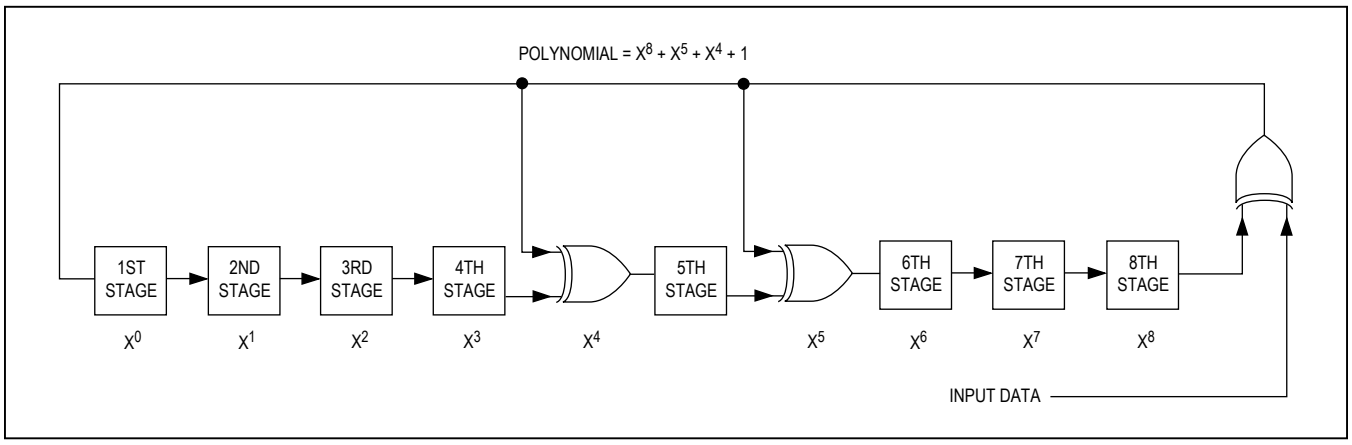


Figure 5. CRC Polynomial

Table 5. Extended Bank Register Bank Definition

Bank 0 DV0 = 0		Bank 1 DV0 = 1	
00h	Timekeeping and Control	00h	Timekeeping and Control
0Dh		0Dh	
0Eh	50 Bytes – User RAM	0Eh	50 Bytes – User RAM
3Fh		3Fh	
40h	64 Bytes – User RAM	40h	Model Number Byte
		41h	1st Byte Serial Number
		42h	2nd Byte Serial Number
		43h	3rd Byte Serial Number
		44h	4th Byte Serial Number
		45h	5th Byte Serial Number
		46h	6th Byte Serial Number
		47h	CRC Byte
		48h	Century Byte
		49h	Date Alarm
		4Ah	Extended Control Register 4A
		4Bh	Extended Control Register 4B
		4Ch	Reserved
		4Dh	Reserved
		4Eh	RTC Address – 2
		4Fh	RTC Address – 3
		50h	Extended RAM Address LSB
		51h	Extended RAM Address MSB
		52h	Reserved
		53h	Extended RAM Data Port
		54h	Reserved
		55h	Reserved
		56h	Reserved
		57h	Reserved
		58h	Reserved
		59h	Reserved
		5Ah	Reserved
		5Bh	Reserved
		5Ch	Reserved
		5Dh	Reserved
		5Eh	RTC Write Counter
		5Fh	Reserved
7Fh		7Fh	

Note: *Reserved bits can be written to any value, but always read back as zeros.*

Century Counter

A register has been added in bank 1, location 48H, to keep track of centuries. The value is read in either binary or BCD according to the setting of the DM bit.

RTC Write Counter

An 8-bit counter located in extended register bank 1, 5Eh, counts the number of times the RTC is written to. This counter is incremented on the rising edge of the WR signal every time that the $\overline{CS}$ signal qualifies it. This counter is a read-only register and rolls over after 256 RTC write pulses. This counter can be used to determine if and how many RTC writes have occurred since the last time this register was read.

Auxiliary Battery

The V_{BAUX} input is provided to supply power from an auxiliary battery for the DS17x85/DS17x87 kickstart, wake-up, and SQW output in the absence of V_{CC} functions. This power source must be available to use these auxiliary functions when no V_{CC} is applied to the device.

The auxiliary battery enable (ABE; bank 1, register 04BH) bit in Extended Control Register 4B is used to turn the auxiliary battery on and off for the above functions in the absence of V_{CC}. When set to 1, V_{BAUX} battery power is enabled; when cleared to 0, V_{BAUX} battery power is disabled to these functions.

In the DS17x85/DS17x87, this auxiliary battery can be used as the primary backup power source for maintaining the clock/calendar, user RAM, and extended external RAM functions. This occurs if the V_{BAT} pin is at a lower voltage than V_{BAUX}. If the DS17x85 is to be backed up using a single battery with any auxiliary functions enabled, then V_{BAUX} should be used and V_{BAT} should be grounded. If V_{BAUX} is not to be used, it should be grounded and ABE should be cleared to 0.

Wake-Up/Kickstart

The DS17x85/DS17x87 incorporates a wake-up feature that powers on the system at a predetermined date and time through activation of the $\overline{PWR}$ output pin. In addition, the kickstart feature allows the system to be powered up in response to a low-going transition on the $\overline{KS}$ pin, without operating voltage applied to the V_{CC} pin.

As a result, system power can be applied upon such events as a key closure or modem ring-detect signal.

To use either the wake-up or the kickstart functions, the DS17x85/DS17x87 must have an auxiliary battery connected to the V_{BAUX} pin, the oscillator must be running, and the countdown chain must not be in reset (Register A DV2, DV1, DV0 = 01X). If DV2 and DV1 are not in this required state, the $\overline{PWR}$ pin is not driven low in response to a kickstart or wake-up condition while in battery-backed mode.

The wake-up feature is controlled through the wake-up interrupt-enable bit in Extended Control Register 4B (WIE, bank 1, 04BH). Setting WIE to 1 enables the wake-up feature, clearing WIE to 0 disables it. Similarly, the kickstart interrupt-enable bit in Extended Control Register 4B (KSE, bank 1, 04BH) controls the kickstart feature.

A wake-up sequence occurs as follows: When wake-up is enabled through WIE = 1 while the system is powered down (no V_{CC} voltage), the clock/calendar monitors the current date for a match condition with the date alarm register (bank 1, register 049H). With the date alarm register, the hours, minutes, and seconds alarm bytes in the clock/calendar register map (bank 0, registers 05H, 03H, and 01H) are also monitored. As a result, a wake-up occurs at the date and time specified by the date, hours, minutes, and seconds alarm register values. This additional alarm occurs regardless of the programming of the AIE bit (bank 0, register B, 0BH). When the match condition occurs, the $\overline{PWR}$ pin is automatically driven low. This output can be used to turn on the main system power supply that provides V_{CC} voltage to the DS17x85/DS17x87 as well as the other major components in the system. Also at this time, the wake-up flag (WF, bank 1, register 04AH) is set, indicating that a wake-up condition has occurred.

A kickstart sequence occurs when kickstarting is enabled through KSE = 1. While the system is powered down, the $\overline{KS}$ input pin is monitored for a low-going transition of minimum pulse width t_{KSPW}. When such a transition is detected, the $\overline{PWR}$ line is pulled low, as it is for a wake-up condition. Also at this time, the kickstart flag (KF, bank 1, register 04AH) is set, indicating that a kickstart condition has occurred.

The timing associated with both the wake-up and kickstarting sequences is illustrated in the *Wake-Up/Kickstart Timing Diagram* (Figure 6). The timing associated with these functions is divided into five intervals, labeled 1 to 5 on the diagram.

The occurrence of either a kickstart or wake-up condition causes the $\overline{PWR}$ pin to be driven low, as described above. During interval 1, if the supply voltage on the DS17x85/DS17x87 V_{CC} pin rises above the greater of V_{BAT} or V_{PF} before the power-on timeout period (t_{POTO}) expires, then $\overline{PWR}$ remains at the active-low level. If V_{CC} does not rise above the greater of V_{BAT} or V_{PF} in this time, then the $\overline{PWR}$ output pin is turned off and returns to its high-impedance level. In this event, the $\overline{IRQ}$ pin also remains tri-stated. The interrupt flag bit (either WF or KF) associated with the attempted power-on sequence remains set until cleared by software during a subsequent system power-on.

If V_{CC} is applied within the timeout period, then the system power-on sequence continue as shown in intervals 2 to 5 in the timing diagram. During interval 2, $\overline{PWR}$ remains active and $\overline{IRQ}$ is driven to its active-low level, indicating that either WF or KF was set in initiating the power-on. In the diagram $\overline{KS}$ is assumed to be pulled up to the V_{BAUX} supply. Also at this time, the PAB bit is automatically cleared to 0 in response to a successful power-on. The $\overline{PWR}$ line remains active as long as the PAB remains cleared to 0.

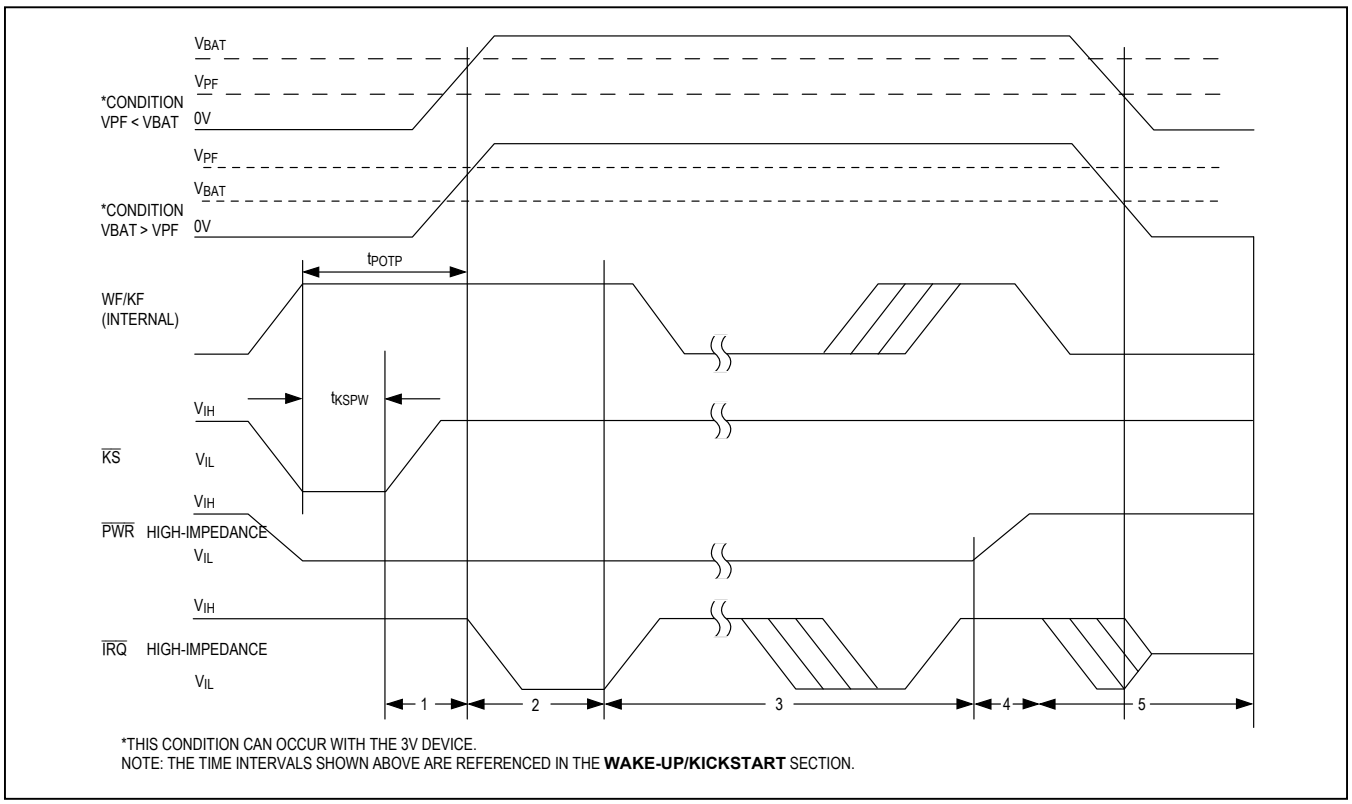


Figure 6. Wake-Up/Kickstart Timing Diagram

Table 6. Wake-Up/Kickstart Timing

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Kickstart-Input Pulse Width	t_{KSPW}		2			µs
Wake-Up/Kickstart Power-On Timeout	t_{POTO}		2			s

Note: *Wake-up/kickstart timeout is generated only when the oscillator is enabled and the countdown chain is not reset.*

At the beginning of interval 3, the system processor has begun code execution and clears the interrupt condition of WF and/or KF by writing zeros to both of these control bits. As long as no other interrupt within the DS17x85/DS17x87 is pending, the IRQ line is taken inactive once these bits are reset. Execution of the application software can proceed. During this time, the wake-up and kickstart functions can be used to generate status and interrupts. WF is set in response to a date, hours, minutes, and seconds match condition. KF is set in response to a low-going transition on $\overline{KS}$. If the associated interrupt-enable bit is set (WIE and/or KSE), the $\overline{IRQ}$ line is driven active low in response to enabled event. In addition, the other possible interrupt sources within the DS17885/DS17887 can cause $\overline{IRQ}$ to be driven low. While system power is applied, the on-chip logic always attempts to drive the $\overline{PWR}$ pin active in response to the enabled kickstart or wake-up condition. This is true even if $\overline{PWR}$ was previously inactive as the result of power being applied by some means other than wake-up or kickstart.

The system can be powered down under software control by setting the PAB bit to logic 1. This causes the open-drain $\overline{PWR}$ pin to be placed in a high-impedance state, as shown at the beginning of interval 4 in the timing diagram. As V_{CC} voltage decays, the $\overline{IRQ}$ output pin is placed in a high-impedance state when V_{CC} goes below V_{PF}. If the system is to be again powered on in response to a wake-up or kickstart, then the WF and KF flags should be cleared, and WIE and/or KSE should be enabled prior to setting the PAB bit.

During interval 5, the system is fully powered down. Battery backup of the clock calendar and NV RAM is in effect and $\overline{IRQ}$ is tri-stated, and monitoring of wake-up and kickstart takes place. If PRS = 1, $\overline{PWR}$ stays active; otherwise, if PRS = 0, $\overline{PWR}$ is high impedance.

RAM Clear

The DS17x85/DS17x87 provide a RAM clear function for the 114 bytes of user RAM. When enabled, this function can be performed regardless of the condition of the V_{CC} pin.

The RAM clear function is enabled or disabled through the RAM clear-enable bit (RCE; bank 1, register 04BH). When this bit is set to logic 1, the 114 bytes of user RAM is cleared (all bits set to 1) when an active-low transition is sensed on the RCLR pin. This action has no effect on either the clock/calendar settings or the contents of the extended RAM. The RAM clear flag (RF, bank 1, register 04AH) is set when the RAM clear operation has been completed. If V_{CC} is present at the time of the RAM clear and RIE = 1, the $\overline{IRQ}$ line is also driven low upon completion. Writing a zero to the RF bit clears the interrupt condition. The $\overline{IRQ}$ line then returns to its inactive high level, provided there are no other pending interrupts. Once the RCLR pin is activated, all read/write accesses are locked out for a minimum recover time, specified as t_{REC} in *Electrical Characteristics*.

When RCE is cleared to 0, the RAM clear function is disabled. The state of the RCLR pin has no effect on the contents of the user RAM, and transitions on the RCLR pin have no effect on RF.

Extended RAM

The DS17x85/DS17x87 provide 2k, 4k, or 8k x 8 of onchip SRAM that is controlled as nonvolatile storage sustained from a lithium battery. On power-up, the RAM is taken out of write-protect status by the internal power-OK signal (POK) generated from the write-protect circuitry. The on-chip SRAM is accessed through the eight multiplexed address/data lines AD7 to AD0. Three on-chip latch registers control access to the SRAM. Two registers are used to hold the SRAM address, and the other register is used to hold read/write data.

Access to the extended RAM is controlled by three of the registers shown in Table 5. The extended registers in bank 1 must first be selected by setting the DV0 bit in register A to logic 1. The address of the RAM location to be accessed must be loaded into the extended RAM address registers located at 50h and 51h. The least significant address byte should be written to location 50h, and the most significant bits (right-justified) should be loaded in location 51h. Data in the addressed location can be read by performing a read operation from location 53h, or written to by performing a write operation to location 53h. Data in any addressed location can be read or written repeatedly without changing the address in location 50h and 51h.

To read or write consecutive extended RAM locations, a burst mode feature can be enabled to increment the extended RAM address. To enable the burst mode feature, set the BME bit in the Extended Control Register 4Ah to logic 1. With burst mode enabled, write the extended RAM starting address location to registers 50h and 51h. Then read or write the extended RAM data from/to register 53h. The extended RAM address locations are automatically incremented on the rising edge of $\overline{RD}$ or $\overline{WR}$ only when register 53h is being accessed. See the *Burst Mode Timing Waveform*.

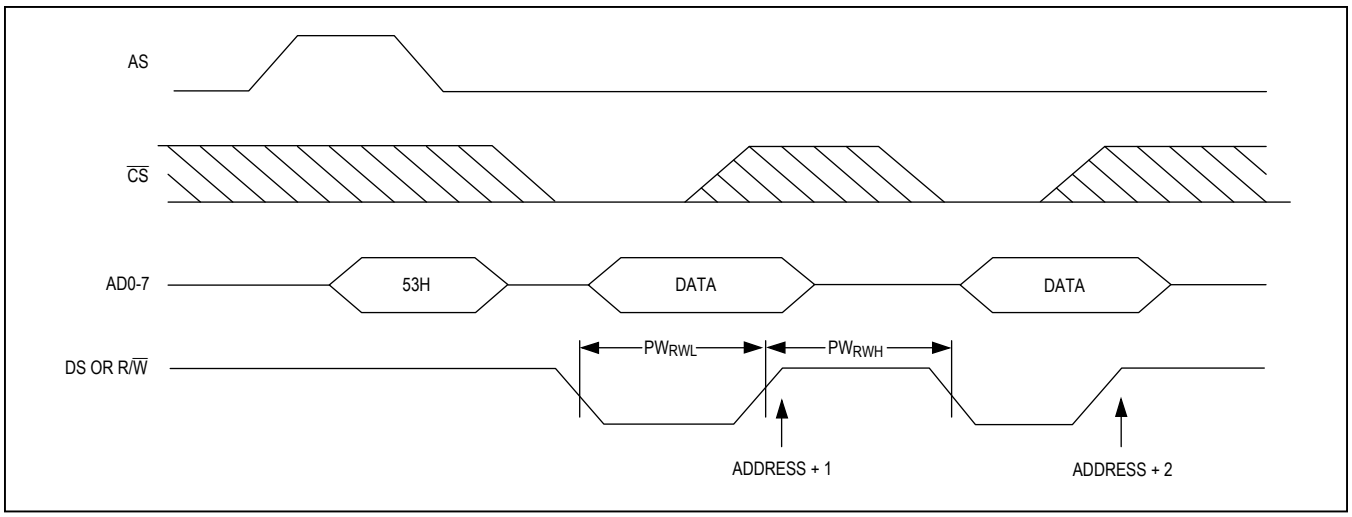


Figure 7. Burst Mode Timing Waveform

Extended Control Registers

Two extended control registers are provided to supply control and status information for the extended functions offered by the DS17x85/DS17x87. These are designated as Extended Control Registers 4A and 4B, and are located in register bank 1, locations 04AH and 04BH, respectively. The functions of the bits within these registers are described as follows.

Extended Control Register (4Ah)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT2	INCR	BME	*	PAB	RF	WF	KF

Bit 7: Valid RAM and Time 2 (VRT2). This status bit gives the condition of the auxiliary battery. It is set to logic 1 condition when the external lithium battery is connected to the V_{BAUX}. If this bit is read as logic 0, the external battery should be replaced.

Bit 6: Increment in Progress Status (INCR). This bit is set to 1 when an increment to the time/date registers is in progress and the alarm checks are being made. INCR is set to 1 at 122µs before the update cycle starts and is cleared to 0 at the end of each update cycle.

Bit 5: Burst Mode Enable (BME). The burst mode enable bit allows the extended user RAM address registers to automatically increment for consecutive reads and writes. When BME is set to logic 1, the automatic incrementing is enabled and when BME is set to a logic 0, the automatic incrementing is disabled.

Bit 3: Power Active-Bar Control (PAB). When this bit is 0, the $\overline{PWR}$ pin is in the active low state. When this bit is 1, the $\overline{PWR}$ pin is in the high-impedance state. The user can write this bit to logic 1 or 0. If either WF and WIE = 1 or KF and KSE = 1, the PAB bit is cleared to 0.

Bit 2: RAM Clear Flag (RF). This bit is set to logic 1 when a high-to-low transition occurs on the RCLR input if RCE = 1. Writing this bit to logic 0 clears it. This bit can also be written to logic 1 to force an interrupt condition.

Bit 1: Wake-Up Alarm Flag (WF). This bit is set to 1 when a wake-up alarm condition occurs or when the user writes it to 1. WF is cleared by writing it to 0.

Bit 0: Kickstart Flag (KF). This bit is set to 1 when a kickstart condition occurs or when the user writes it to 1. This bit is cleared by writing it to logic 0.

Extended Control Register (4Bh)

MSB **LSB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ABE	E32k	CS	RCE	PRS	RIE	WIE	KSE

Bit 7: Auxiliary Battery Enable (ABE). When written to logic 1, this bit enables the V_{BAUX} pin for extended functions.

Bit 6: Enable 32.768kHz Output (E32k). When written to logic 1, this bit enables the 32.768kHz oscillator frequency to be output on the SQW pin. E32k is set to 1 when V_{CC} is powered up.

Bit 5: Crystal Select (CS). When CS is set to 0, the oscillator is configured for operation with a crystal that has a 6pF specified load capacitance. When CS = 1, the oscillator is configured for a 12.5pF crystal. CS is disabled in the DS17x87 module and should be set to CS = 0.

Bit 4: RAM Clear Enable (RCE). When set to 1, this bit enables a low level on RCLR to clear all 114 bytes of user RAM. When RCE = 0, RCLR and the RAM clear function are disabled.

Bit 3: PAB Reset Select (PRS). When set to 0, the $\overline{PWR}$ pin is set high impedance when the DS17x85 goes into power fail. When set to 1, the $\overline{PWR}$ pin remains active upon entering power fail.

Bit 2: RAM Clear Interrupt Enable (RIE). When RIE is set to 1, the $\overline{IRQ}$ pin is driven low when a RAM clear function is completed.

Bit 1: Wake-Up Alarm Interrupt Enable (WIE). When V_{CC} voltage is absent and WIE is set to 1, the $\overline{PWR}$ pin is driven active low when a wake-up condition occurs, causing the WF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If WIE is set while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to WF being set to 1. When WIE is cleared to 0, the WF bit has no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

Bit 0: Kickstart Interrupt Enable (KSE). When V_{CC} voltage is absent and KSE is set to 1, the $\overline{PWR}$ pin is driven active low when a kickstart condition occurs ($\overline{KS}$ pulsed low), causing the KF bit to be set to 1. When V_{CC} is then applied, the $\overline{IRQ}$ pin is also driven low. If KSE is set to 1 while system power is applied, both $\overline{IRQ}$ and $\overline{PWR}$ are driven low in response to KF being set to 1. When KSE is cleared to 0, the KF bit has no effect on the $\overline{PWR}$ or $\overline{IRQ}$ pins.

System Maintenance Interrupt (SMI) Recovery Stack

An SMI recovery register stack is located in the extended register bank, locations 4Eh and 4Fh. This register stack, shown below, can be used by the BIOS to recover from an SMI occurring during an RTC read or write.

The RTC address is latched on the falling edge of the ALE signal. Each time an RTC address is latched, the register address stack is pushed. The stack is only four registers deep, holding the three previous RTC addresses in addition to the current RTC address being accessed. Figure 8 illustrates how the BIOS could recover the RTC address when an SMI occurs.

1) The RTC address is latched.
2) An SMI is generated before an RTC read or write occurs.
3) RTC address 0Ah is latched and the address from 1 is pushed to the “RTC Address–1” stack location. This step is necessary to change the bank select bit, DV0 = 1.
4) RTC address 4Eh is latched and the address from 1 is pushed to location 4Eh, “RTC Address–2” while 0Ah is pushed to the “RTC Address–1” location. The data in this register, 4Eh, is the RTC address lost due to the SMI.

	RTC ADDRESS
	RTC ADDRESS-1
4Eh	RTC ADDRESS-2
4Fh	RTC ADDRESS-3

SMI Recovery Stack

7	6	5	4	3	2	1	0
DV0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

REGISTER BIT DEFINITION

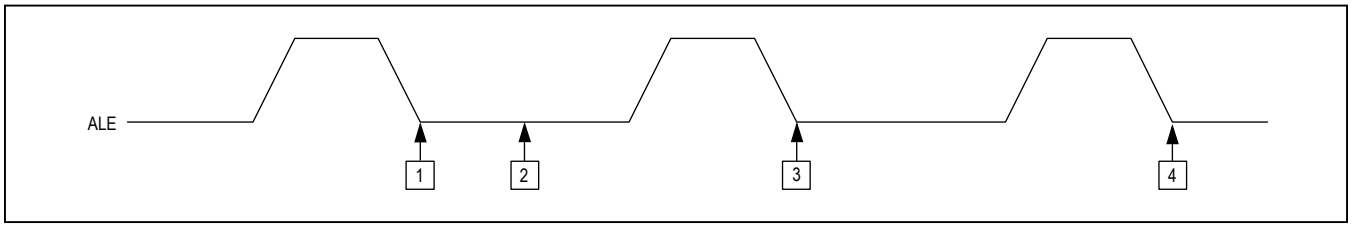
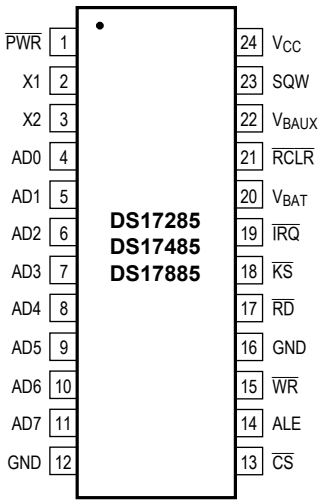


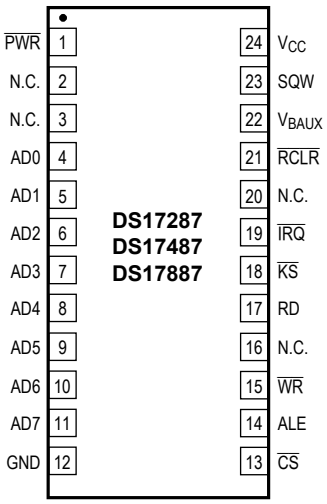
Figure 8. ALE Waveform

Pin Configurations

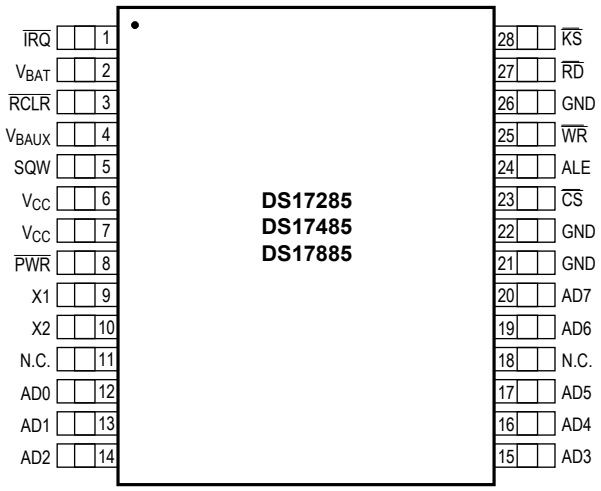
TOP VIEW



SO, PDIP



EDIP



TSOP

Ordering Information

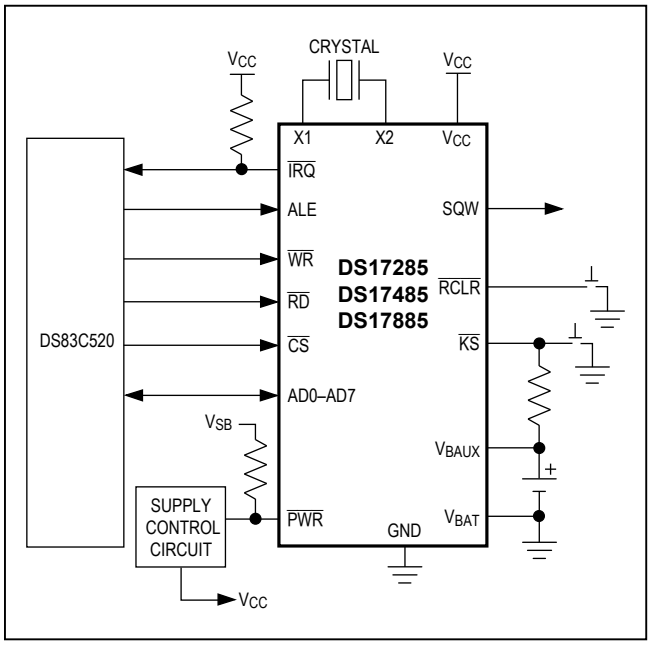
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK*
DS17285-3+	0°C to +70°C	24 PDIP	DS17285-3
DS17285-5+	0°C to +70°C	24 PDIP	DS17285-5
DS17285E-3+	0°C to +70°C	28 TSOP	DS17285E3
DS17285E-5+	0°C to +70°C	28 TSOP	DS17285E5
DS17285EN-3+	-40°C to +85°C	28 TSOP	DS17285E3
DS17285S-3+	0°C to +70°C	24 SO (300 mils)	DS17285S-3
DS17285S-5+	0°C to +70°C	24 SO (300 mils)	DS17285S-5
DS17285SN-3+	-40°C to +85°C	24 SO (300 mils)	DS17285SN3
DS17285SN-5+	-40°C to +85°C	24 SO (300 mils)	DS17285SN5
DS17287-3+	0°C to +70°C	24 EDIP	DS17287-3
DS17287-5+	0°C to +70°C	24 EDIP	DS17287-5
DS17485-3+	0°C to +70°C	24 PDIP	DS17485-3
DS17485-5+	0°C to +70°C	24 PDIP	DS17485-5
DS17485E-3+	0°C to +70°C	28 TSOP	DS17485E3
DS17485E-5+	0°C to +70°C	28 TSOP	DS17485E5
DS17485S-3+	0°C to +70°C	24 SO (300 mils)	DS17485S-3
DS17485S-5+	0°C to +70NC	24 SO (300 mils)	DS17485S-5
DS17485SN-5+	-40°C to +85°C	24 SO (300 mils)	DS17485SN5
DS17487-3+	0°C to +70°C	24 EDIP	DS17487-3
DS17487-3IND+	-40°C to +85°C	24 EDIP	DS17487-3 REAL TIME IND
DS17487-5+	0°C to +70°C	24 EDIP	DS17487-5
DS17487-5IND+	-40°C to +85°C	24 EDIP	DS17487-5 REAL TIME IND
DS17885-3+	0°C to +70°C	24 PDIP	DS17885-3
DS17885-5+	0°C to +70°C	24 PDIP	DS17885-5
DS17885E-3+	0°C to +70°C	28 TSOP	DS17885E3
DS17885E-5+	0°C to +70°C	28 TSOP	DS17885E5
DS17885EN-3+	-40°C to +85°C	28 TSOP	DS17885E3
DS17885S-3+	0°C to +70°C	24 SO (300 mils)	DS17885S-3
DS17885S-5+	0°C to +70°C	24 SO (300 mils)	DS17885S-5
DS17885SN-3+	-40°C to +85°C	24 SO (300 mils)	DS17885SN3
DS17887-3+	0°C to +70°C	24 EDIP	DS17887-3
DS17887-3IND+	-40°C to +85°C	24 EDIP	DS17887-3 REAL TIME IND
DS17887-5+	0°C to +70°C	24 EDIP	DS17887-5
DS17887-5IND+	-40°C to +85°C	24 EDIP	DS17887-5 REAL TIME IND

+Denotes a lead(Pb)-free/RoHS-compliant package.

**A "+" anywhere on the top mark denotes a lead(Pb)-free package. An "N" or "IND" denotes an industrial temperature range package.*

***Note:** A "-5" suffix denotes a V_{CC} = 5V±10% device, and a "-3" suffix denotes a V_{CC} = 3V±10% device.*

Typical Operating Circuit



Thermal Information

PACKAGE	THETA-JA (°C/W)	THETA-JC (°C/W)
DIP	75	30
SO	105	22

Chip Information

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	DOCUMENT NO.
24 PDIP (600 mils)	21-0044
24 SO (300 mils)	21-0042
24 EDIP (740 mils)	21-0241
28 TSOP (465 mils)	21-0273

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/06	Initial release of revised data sheet template	—
1	4/10	Updated the storage temperature ranges, added the lead temperature, and updated the soldering temperature for all packages in the *Absolute Maximum Ratings*; removed the leaded parts from the *Ordering Information* table; updated the Document No. for the Package Information table.	2, 29, 30
2	5/16	Updated *Package Information* table	30

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