# THE DATASHEET OF

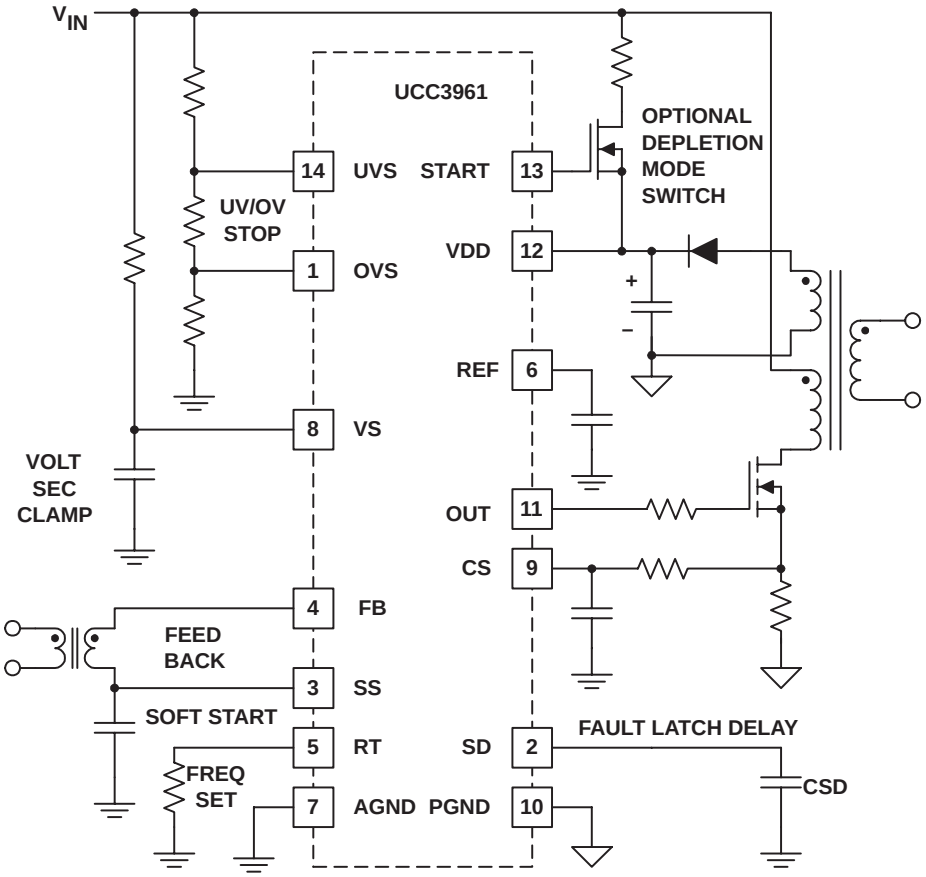
# CY8C4245AZI-473

# UCC2961, UCC3961
# ADVANCED PRIMARY-SIDE STARTUP CONTROLLER

SLUS431A – MAY 2000 – REVISED DECEMBER 2000

- Operates with Secondary–Side PWM Control
- Isolated PWM Command through a Pulse Transformer
- Initial Free-Running Soft-Startup with Duty-Cycle Clamping
- Up to 400-kHz Synchronizable Switching Frequency
- High-Current FET Drive (1.5-A Sink, 0.75-A Source)
- Multi-Mode Overcurrent Protection with Restart, Latching, or Cycle-by-Cycle Current Limiting
- Programmable Volt-Second Clamp for Transformer Reset
- Undervoltage Lockout with 2-V Hysteresis
- Low-Current Startup with Optional Disconnect
- Programmable Overvoltage and Undervoltage Protection
- 8–pin Version Also Available (UCC3960)

## typical application diagram




UDG–99039

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## description

The UCC3961 advanced primary-side startup controller is a unique solution that provides all the primary-side functions required for a single-ended, isolated, switch-mode power converter incorporating secondary-side PWM control. It is usable with a wide range of secondary control circuits and is especially well suited for systems where sophisticated handling of overload conditions is required.

Secondary-side control assumes that output voltage and current measurements are interfaced directly to an output ground-referenced PWM stage that develops the power switch command for the supply. This digital PWM command can then be transmitted to the primary-side power switch through a simple and low-cost isolating pulse transformer. With secondary-side control, it is much easier to monitor and control the system load with tightly coupled analog control loops. Load-oriented features such as output current sharing and synchronous rectification are implemented more easily.

The UCC3961 provides all the circuitry required on the primary side of a secondary-side controlled power supply. It features a free running 60-kHz to 360-kHz oscillator which is synchronizable to the secondary-side PWM signal and also has the ability to accept start/stop PWM commands from the isolating pulse-edge transformer (PET). The use of an extremely small and low-cost pulse transformer allows for higher converter bandwidth. This also eliminates the loop-gain variations due to initial accuracy and aging of an opto-coupler feedback element or the size penalty of a gate transformer. It also includes an undervoltage lockout circuit with 2-V hysteresis, a low-current startup with active low during UVLO, a soft-start capability, a 5-V reference and a high-current power output.

Advanced features of UCC3961 allows implementation of initial startup with optional high-voltage disconnect after starting, and input voltage monitoring with turnoff for either undervoltage or overvoltage conditions. Other features include power-switch current protection, pulse-by-pulse current limiting, shutdown after a programmable delay and continuous input volt*second clamp. The UCC3961 also provides a multi purpose, bidirectional shutdown pin (SD), that can be used in conjunction with the devices on the START pin, to modify the converters behavior in overload conditions. The possible configurations include continuous-peak current limiting, delayed or immediate shutdown with full cycle soft restart or fully latched overcurrent shutdown.

In a non-typical use, the UCC3961 can accommodate an analog feedback signal through an opto-isolator where the UCC3961 then can operate in voltage-mode control mode with primary-side peak current limiting.

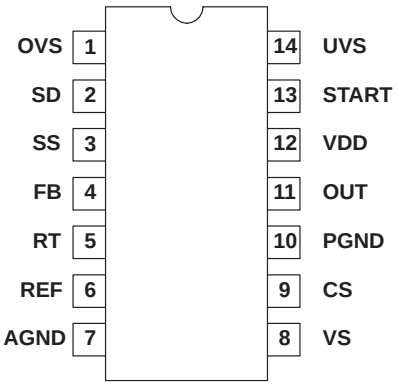
The UCC3961 and the UCC2961 are available in the 14-pin SOIC (D) and PDIP (P) packages. For applications where only startup and control are desired, a simplified version of this product is offered in an 8-pin package as the UCC2960 and UCC3960.

**AVAILABLE OPTIONS**

| TA | PACKAGED DEVICES | |
|---|---|---|
| | SOIC–14 SMALL OUTLINE (D) | PDIP–14 PLASTIC DIP (N) |
| –40°C to 85°C | UCC2961D | UCC2961N |
| 0°C to 70°C | UCC3961D | UCC3961N |

† The SOIC (D) packages are available taped and reeled. Add an R suffix to the device type (e.g., UCC2961DR) to order quantities of 2500 devices per reel.

**D OR N PACKAGES**
**(TOP VIEW)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡**

| | | |
|---|---|---|
| Input voltage, $V_{I(VDD)}$ | | 19 V |
| Input current, $I_{I(VDD)}$ | | 25 V |
| Output current §, $I_O$ | | –1.5 A / 2 A |
| Output voltage: | REF, START | –0.3 V to VDD+0.3 V |
| Input voltage: | OVS, SD, SS, RT, VS, CS, UVS | –0.3 V to VDD+0.3 V |
| | FB | –7.0 V to VDD+0.3 V |
| Operating junction temperature range, $T_J$ | | –55°C to 150°C |
| Storage temperature range, $T_{stg}$ | | –65°C to 150°C |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | | 300°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 µs. All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

§ 4nF load with 4-Ω series resistor.

## electrical characteristics $V_{DD}$ = 12 V, RT = 53.3 kΩ, $C_{VDD}$ = 1 μF, $C_{REF}$ = 0.1 μF, $C_{SS}$ = 0.01 μF, $R_{OUT}$ = 4 Ω, $C_{OUT}$ = 1 nF and $T_A = T_J$ (unless otherwise stated)

### supply section (VDD)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Clamp voltage | $I_{VDD}$ = 10 mA | 16 | 17.5 | 19 | V |
| Operating current | No load, $C_{OUT}$ = 0 | 1.8 | 2.3 | 2.8 | mA |
| Starting current | VDD = 9 V | 100 | 150 | 200 | μA |

### undervoltage lockout section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Start threshold voltage | | 9.5 | 10 | 10.5 | V |
| Hysteresis voltage | | 1.7 | 2 | 2.3 | V |

### voltage reference section (REF)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Reference voltage | | 4.75 | 5.0 | 5.25 | V |
| Load regulation voltage | $I_{REF}$ = 0 mA to –2.5 mA | | 3 | 5 | mV |
| Line regulation voltage | $V_{DD}$ = 10 V to 12 V | | 1 | 5 | mV |
| Short-circuit current | | 8 | 10 | 16 | mA |

### overvoltage sense section (OVS)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Threshold voltage | | 3.68 | 4 | 4.32 | V |
| Input bias current | | | | 0.2 | μA |

### undervoltage sense section (UVS)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Threshold voltage | | 3.68 | 4 | 4.32 | V |
| Input bias current | | | | 0.2 | μA |

### soft start section (SS)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Discharge current | SD = 4.5 V pulsed | 3 | 5 | 7 | μA |
| Charge current | SD = 4.5 V pulsed | –5 | –7 | –10 | μA |
| Low–threshold voltage | | 0.9 | 1 | 1.1 | V |
| Clamp threshold | | 4.5 | 5 | 5.5 | V |
| On resistance | $V_{DD}$ = 7.5 V | 600 | 800 | 1000 | Ω |

### shutdown section (SD)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Threshold voltage | | 3.68 | 4 | 4.32 | V |
| Discharge current | | 0.4 | 0.6 | 0.8 | μA |
| Charge current | | –4 | –6 | –8 | μA |
| On resistance | $V_{DD}$ = 7.5 V | 2.5 | 3.3 | 5 | kΩ |

NOTES: 1. OUT Low, nominal of 0.7 V reflects the 3 Ω DMOS ON resistance plus 4 Ω $R_{SERIES}$.
2. OUT High (VDD–OUT), nominal of 0.56 V reflects the 10W HVPMOS ON resistance plus 4W $R_{SERIES}$.

## electrical characteristics $V_{DD}$ = 12 V, RT = 53.3 kΩ, $C_{VDD}$ = 1 μF, $C_{REF}$ = 0.1 μF, $C_{SS}$ = 0.01 μF, $R_{OUT}$ = 4 Ω, $C_{OUT}$ = 1 nF and $T_A = T_J$ (unless otherwise stated) (continued)

### current sense section (CS)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Threshold | Pulse-by-pulse | 0.9 | 1 | 1.1 | V |
| | Immediate | 1.3 | 1.4 | 1.5 | V |
| Input bias | CS = 1.1 V pulsed | | | 0.2 | μA |
| Delay time CS to OUT | | 60 | 100 | 140 | ns |
| On resistance | | 600 | 800 | 1000 | Ω |

### oscillator section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Frequency | | 135 | 150 | 165 | kHz |
| Frequency change with voltage | $V_{DD}$ = 10 V to 12 V | | 0.02 | 0.2 | %/V |
| Minimum duty cycle | | | 0% | | |
| Maximum duty cycle | | 69% | 72% | 75% | |

### volt-second section (VS)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Threshold | | 3.68 | 4 | 4.32 | V |
| Input bias | | | | 0.2 | μA |
| On resistance | | 600 | 800 | 1000 | Ω |

### output section (OUT)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Low-level output voltage | $I_{OUT}$ = 100 mA (dc) | See Note 1 | | 0.7 | 1.0 | V |
| High-level output voltage | $I_{OUT}$ = –40 mA (dc) | See Note 2 | | 0.56 | 1.0 | V |
| Low-level output voltage during UVLO | $I_{OUT}$ = 20 mA (dc), | $V_{DD}$ = 7.5 V | | | 1.5 | V |
| Rise time | | | | 30 | 60 | ns |
| Fall time | | | | 15 | 30 | ns |

### bias regulator section (START)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Bias regulator | $V_{DD}$ – START = 0.5 V | | 11.7 | 12.1 | 12.5 | V |
| Override voltage | $V_{DD}$ – START = 1.0 V, | See Note 3 | | 12.2 | | V |

### feedback section (FB)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| input bias current | FB = 4.5 V, | SS = 0 V | | | 0.4 | μA |
| Negative compliance voltage | IFB = –100 mA, | SS = 0 V | –6.8 | –7.2 | –7.6 | V |
| Delay time, FB–SS to OUT, rising edge | FB–SS Pulsed = 2 V, | FB = SS | 40 | 70 | 100 | ns |
| Delay time, FB–SS to OUT, falling edge | FB–SS Pulsed = 2 V, | FB = SS | 50 | 85 | 120 | ns |

NOTES: 1. OUT Low, nominal of 0.7 V reflects the 3 Ω DMOS ON resistance plus 4 Ω $R_{SERIES}$.
2. OUT High (VDD–OUT), nominal of 0.56 V reflects the 10 Ω HVPMOS ON resistance plus 4 Ω $R_{SERIES}$.
3. The override $V_{DD}$ voltage for shutting off the bias regulation is 100 mV higher than the bias regulator voltage.

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 7 | | This pin is the reference point for grounding all analog functions and must be kept as clean as possible from all switching noise. It should be connected to PGND in only one location as close to the IC as practical. |
| CS | 9 | I | Pulse-by-pulse and shutdown overcurrent sense input pin |
| FB | 4 | I | Control input for the signal from a secondary–side PWM controller |
| OUT | 11 | O | Drive pin for the MOSFET power switch |
| OVS | 1 | I | This pin is used with an external resistor divider of VIN to terminate operation if a voltage is sensed above the internal 4 V threshold. Activation sets the shutdown latch that requires recycling the voltage on VDD to restart. |
| PGND | 10 | | This power ground for the PWM output stage conducts any current transients from the power switch gate drive. It should be closely bypassed to VDD and connected to AGND in only one location as close to the IC as possible. |
| REF | 6 | O | This is a 5-V output usable with external loads of up to 10 mA. This voltage is also the source for all internal analog threshold settings and should be bypassed with a minimum of 0.1-µF capacitance to AGND. |
| RT | 5 | I | Sets the free-running startup oscillator frequency |
| SD | 2 | I | Input to the shutdown circuit |
| SS | 3 | I | The pin implements the primary-side soft-start function. This is the connection point for an external capacitor that determines the rate of increase in commanded pulse width for the power switch at startup. It also serves as the ac ground return for the feedback pulse transformer to provide a tracking bias for the FB input. |
| START | 13 | O | Used to develop a regulated 12 V at VDD and thereby minimize or eliminate continuous current drain |
| UVS | 14 | I | This pin is used with an external resistor divider of Vin to terminate operation if a voltage is sensed below the internal 4-V threshold. Activation maintains the circuit in shutdown with the soft-start capacitor clamped low. |
| VDD | 12 | I | Power input connection for all control circuitry |
| VS | 8 | I | Volt-second clamp |

## detailed descriptions

### current sense (CS)

This is the pulse-by-pulse and shutdown overcurrent sense input pin. This current-sense pin triggers a pulse-by-pulse termination anytime a 1.0-V threshold is exceeded while a signal in excess of 1.375 V on this pin initiates a complete shutdown. Each activation of pulse-by-pulse termination also sends a current pulse to the SD pin where an external capacitor can be used to provide a delayed shutdown. Since the CS pin can be noise sensitive, it is good practice to insert a small low-pass RC filter between this pin and the current sensor.

### feedback (FB)

This is the control input for the signal from a secondary-side PWM controller whose pulse-width command has been differentiated by the feedback pulse-edge transformer into positive *start* and negative *stop* pulses. These signals are used to turn on and turn off the primary power switch and must have an amplitude of at least $V_{SS}$ ±2.0V (4 V peak-to-peak) for at least 25 ns per pulse and no more than 200 ns per pulse. The maximum amplitude allowed on this pin is $V_{SS}$ ± 7.0 V.

### output drive (OUT)

This is the drive pin for the MOSFET power switch and sinks (1.5 A) and sources (0.75 A) fast, high-current gate-drive pulses. During shutdown, this pin is self–biased to an active low state. A minimum of 4 W should be added in series with the output to ensure that the on-chip driver safe operating area is not exceeded. (Data from the IRF820/830/840 family of MOSFETs, commonly available in the TO–220 package, is used to derive this value. The gate charge needed to provide full enhancement was used to establish an equivalent capacitance of up to 4000 pF.)

**timing resistor (RT)**

A resistor from this pin to AGND establishes a current,

$$I_{SET} = \frac{2\ V}{RT}$$

that is mirrored internally for several functions. It establishes the free-running startup switching frequency with an internal capacitor according to the relationship,

$$fs = \frac{8.0 \times 10^9}{RT}$$

The startup oscillator has a rise and fall time set to limit the duty-cycle of the power switch to a maximum of 72%, a limit that is maintained even after the feedback signal takes command. The range of RT is 22.2 kΩ to 133 kΩ, giving a free-run frequency range range of 60 kHz to 360 kHz, respectively. Variations in the free-running oscillator frequency overtemperature are very small. The typical temperature coefficient is –40 Hz per degree Celsius, measured at 150 kHz.

**shutdown (SD)**

This pin is the input to the shutdown circuit. Like OVS, this pin also sets the shutdown latch when a threshold above 4 V is exceeded. The primary intent of this input is to allow the use of an external capacitor to program a delay between the onset of current limiting and the issuance of a shutdown command by integrating current pulses that appear on this pin with each activation of the CS input. This pin is pulled low with a current sink of 0.33/RT when there is no CS signal. The shutdown function can be disabled by connecting SD pin to AGND.

**soft-start (SS)**

The pin implements the primary-side soft-start function. This is the connection point for an external capacitor that determines the rate of increase in commanded pulse width for the power switch at startup. It also serves as the ac ground return for the feedback pulse transformer to provide a tracking bias for the FB input.

**start bias regulator (START)**

In conjunction with an external depletion-mode N-channel FET, such as the Supertex DN2530, this pin can be used to develop a regulated voltage of 12 V at VDD and thereby minimize or eliminate continuous current drain when starting from a variable high voltage source. If this function is unused, this pin can be left open.

**power (VDD)**

This is the power input connection for all the control circuitry and, in addition, conducts all the gate charge current for the power FET. It should be closely bypassed with at least 1.0-μF to PGND and 1.0-μF to AGND. This pin is internally shunt regulated to clamp at 17.5V to protect the internal components so if a voltage source above this value is possible, external current limiting must be provided.

**volt-second clamp (VS)**

This pin provides a volt–second clamp for the operation of the transformer–driving power switch with the aid of an external capacitor to ground and a high value resistor to the transformer's voltage source (Vin). With the initiation of each power pulse, the circuit releases an internal grounding clamp across the capacitor allowing it to charge with a current from the resistor proportional to the input voltage. If this pin reaches 4 V prior to output termination from other control functions, then this ends the power pulse.

$$T_{VS} = 1.61 \times R_{VS} \times C_{VS}$$

$$R_{VS} > 100\ \Omega$$

## pin descriptions (continued)

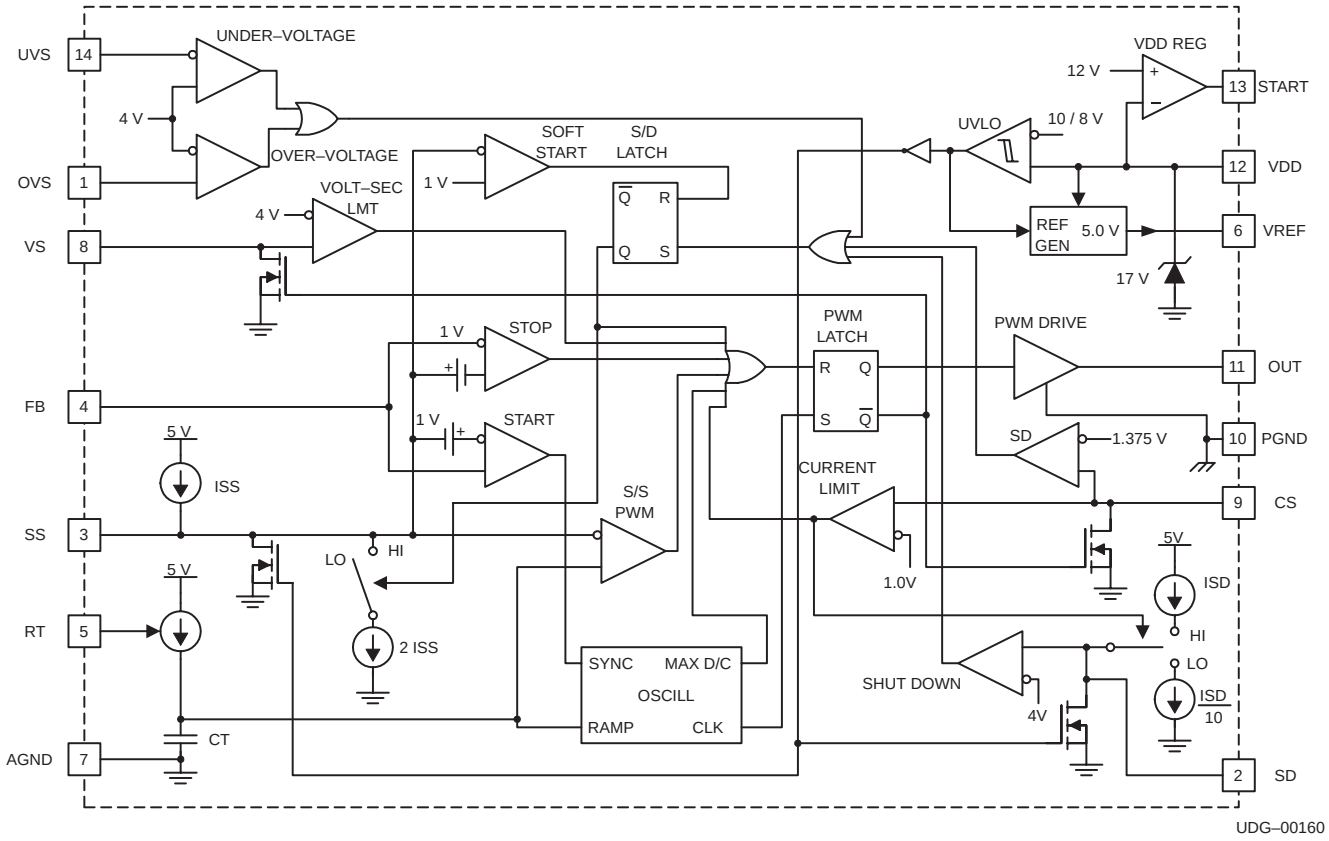



**Figure 1. Block Diagram**

## DETAILED DESCRIPTION

### start-up oscillator

The RT pin is connected to an internal 2.0 V nominal, unity-gain closed-loop amplifier that is referenced to a voltage divider off the 5.0-V reference. When a 22.2-kΩ resistor is connected from the RT pin to GND an approximate $I_{RT}$ = 90μA internal current is realized that charges the internal oscillator capacitor that is approximately 58 pF. $I_{RT}$ = 90μA produces a maximum free running oscillator frequency of 360 KHz at a 72% duty cycle. When a 133.3-kΩ resistor is connected from the RT pin to GND an approximate $I_{RT}$ = 15 mA internal current is realized that produces a minimum free running oscillator frequency of 60 KHz at approximately 72% duty cycle. This maximum duty cycle is setup by on-chip MOSFET current mirrors that are not programmable.

Any frequency between these two limits (6:1 maximum to minimum frequency) is obtainable by linearly scaling the RT resistance between the minimum 22.2-kΩ and maximum 133.3-kΩ values. The secondary-side PWM frequency should be fixed at (1 / 0.9) or 1.11 times the user programmed primary-side free running oscillator frequency for proper primary-side synchronization. Therefore, in all cases the recommended secondary-side synchronization frequency shall be 1.11 times higher than the selected primary-side free running startup frequency. Taking into consideration the two extreme limits for primary-side free running startup frequency, the secondary-side operating frequency should be set between 400 kHz and 67 kHz.

## DETAILED DESCRIPTION

### soft start

The soft-start section contains all the circuitry required to produce a user programmable slowly increasing PWM duty cycle, starting from 0% to a maximum of 72%. The soft-start cycle is triggered either by the initial primary-side startup procedure or after any one of three user-programmable fault conditions and one fixed-fault condition. The PWM duty cycle increases according to the charge rate of an user selectable external soft-start capacitor, connected from the SS pin to GND. The SS capacitor is charged by a nominal 7-μA internal current source.

Voltage comparators referenced to a 4.0-V threshold monitor the OVS pin, SD pin and the UVS pin and trigger a soft-start cycle when a fault condition is detected on any of these pins. Should the CS pin rise in voltage above 1.375 V a soft-star cycle is also triggered. The soft-start cycle disables the output driver OUT and holds it in the low state until the capacitor connected from the SS pin to GND is discharged below 1.0 V by an internal 5-μA current sink. After this discharge period the PMW output OUT is enabled and the duty cycle is allowed to slowly increase as before.

### synchronization

The SS pin and the FB pin accept the secondary side of a small-signal synchronization transformer. A series-blocking capacitor inserted in the primary-side of the synchronization transformer is intended to differentiate the square-wave gate drive output of the secondary-side PWM controller while preventing the transformer from saturation. The SS capacitor also provides an ac GND at the SS pin or the synchronization transformer secondary. The small signal synchronization transformer provides galvanic isolation between primary and secondary side and must have adequate voltage breakdown rating between the primary and secondary windings.

Two comparators, with an approximate 1.0-V offset each, are connected to the FB pin to provide plus and minus differential voltage comparison with a 2.0-V deadband between the FB and SS pins. The 2.0-V deadband prevents inductive backswing of the small signal transformer from giving false secondary-side pulse-edge detection.

Enough energy must be coupled into the comparator differential inputs to ensure reliable comparator switching. This requires sufficient voltage overdrive above the 1.0-V comparator threshold and a specified transformer circuit time constant to provide a minimum synchronization pulse width.

On receiving the first recognizable negative going voltage pulse (turnoff command) generated from the falling edge of the differentiated square-wave gate drive signal on the secondary-side, the PWM latch is reset and a synchronization latch is set. After this event all primary-side PMW driver output is slaved to the secondary-side driver output in both frequency and duty cycle. The triggering of a soft-start cycle by a fault condition resets the synchronization latch to again allow the internal startup oscillator to control the PWM latch.

### pulse-width modulation

The PWM section consists of a reset dominant SR latch with necessary logical gating on the SET input to allow control from the free running startup oscillator until feedback from the secondary-side PWM gate drive output is detected. After the occurrence of detectable feedback from the secondary-side gate driver, the control of the primary-side PWM latch is handed off to the secondary-side PWM controller. A nine-input OR gate on the PWM latch reset dominant input allows the numerous fault conditions to reset the PWM latch and control from either the startup oscillator or feedback from the secondary-side PWM output driver.

## DETAILED DESCRIPTION

### undervoltage lockout

The undervoltage lockout (UVLO) circuit enables normal operation after VDD exceeds the 10.0-V turnon threshold and permits operation until VDD falls below the 8-V turnoff threshold. While activated, the UVLO circuit holds the PWM gate driver output (OUT) and the internal-reference buffer amplifier output REF low. To ensure proper soft-start and to prevent false SD detection, internal N-channel MOSFET switches discharge external capacitors connected to the SS and SD pins during undervoltage conditions.

### voltage reference

The 5-V internal reference is connected to the REF pin and must be bypassed using a good quality, high-frequency capacitor. This 5-V reference is not available externally while the chip is disabled by the undervoltage lockout circuit.

### current sensing

The current sense (CS) circuit monitors the voltage across a ground referenced current sense resistor, connected between the source of the external power MOSFET and GND. The signal amplitude at the CS pin is compared to two thresholds (1.0 V, and 1.375 V respectively) by two independent voltage comparators.

A voltage level greater than 1.0 V, but less than 1.375 V, sets the reset dominant shutdown latch and resets the PWM latch. The SD latch is reset by the startup oscillator arriving at its 4.0 V compare threshold. When the SD latch is set, a scaled current, $I_{SD} = -(1/6) \times (I_{RT})$, charges an user-selected external capacitor connected between the SD pin and GND. When the SD latch is reset, a scaled current $I_{SD} = (1/10)*(1/6) \times (IRT)$, discharges the user-selected capacitor connected between the SD pin and GND.

A current-sense voltage greater than 1.375 V immediately triggers a SD event and also reset the PWM latch. During the off period of the PWM latch, any capacitance connected to the CS pin is discharged to GND potential by an internal 800-Ω device.

### volt-second clamp

The volt-second (VS) clamp circuit monitors the voltage at the VS pin produced by an external-series RC circuit. The resistor is connected from the HV primary-side power input, that is derived from the rectified line voltage, to the VS pin. The capacitor is from the VS pin to GND and being charged by the resistor during the on-time of the OUT driver. The resulting exponential voltage at the VS pin is monitored by a voltage comparator with a 4.0-V threshold. Should the voltage at the VS pin exceed 4.0-V, the PWM latch is reset, and as a result the output drive signal is terminated. This RC circuit can be tailored to prevent the power transformer from saturation by effectively limiting the applied maximum volt-second product across the primary winding. During the off period of the PWM output driver the VS capacitor is discharged to GND potential by an internal switch with 800Ω on resistance.

## DETAILED DESCRIPTION

### start regulator and VDD clamp

To facilitate the primary-side startup, a $V_{DD}$ = 12V voltage regulator may be implemented by using an external depletion-mode FET. The gate of this device is then connected to the START pin, the source terminal is attached to the VDD pin, and the drain is tied to the HV primary-side power input that is derived from the rectified line voltage. An auxiliary bootstrap winding off the main power transformer can be used to generate a bias voltage greater than 12 V, that effectively shuts down the 12-V regulator and increase the efficiency of the biasing solution during normal operation.

To ensure that the absolute-maximum voltage ratings of internal devices are not violated, an internal-shunt voltage regulator is provided to clamp the VDD pin at a nominal 17.5-V maximum voltage. Similarly to other shunt or Zener-like voltage regulator circuits, the current through the internal VDD clamp must be limited below the maximum current level indicated in the datasheet. In addition to limiting the current through the clamp circuit, the maximum power dissipation capability of the particular package used in the application must be considered.

### OUT driver

An internal output driver (OUT) is provided to drive the gate of an external N–channel power MOSFET. The output driver consists of a nominal 4.0-W ON-resistance P-channel MOSFET for turn-on, and a nominal 2.0-Ω ON resistance DMOS FET utilized during the turn–off of the external MOSFET transistor. An external series gate resistance is specified to maintain an acceptable safe operating area (SOA) for the DMOS device of the internal output driver. As discussed in the UVLO section of this datasheet, the undervoltage lockout (UVLO) circuit holds the PWM gate driver output low while UVLO conditions exists.

## APPLICATION INFORMATION

The evaluation circuit of UCC3961 as the primary-side startup circuit and UCC38C45 as the secondary-side controller is shown in Figure 2.

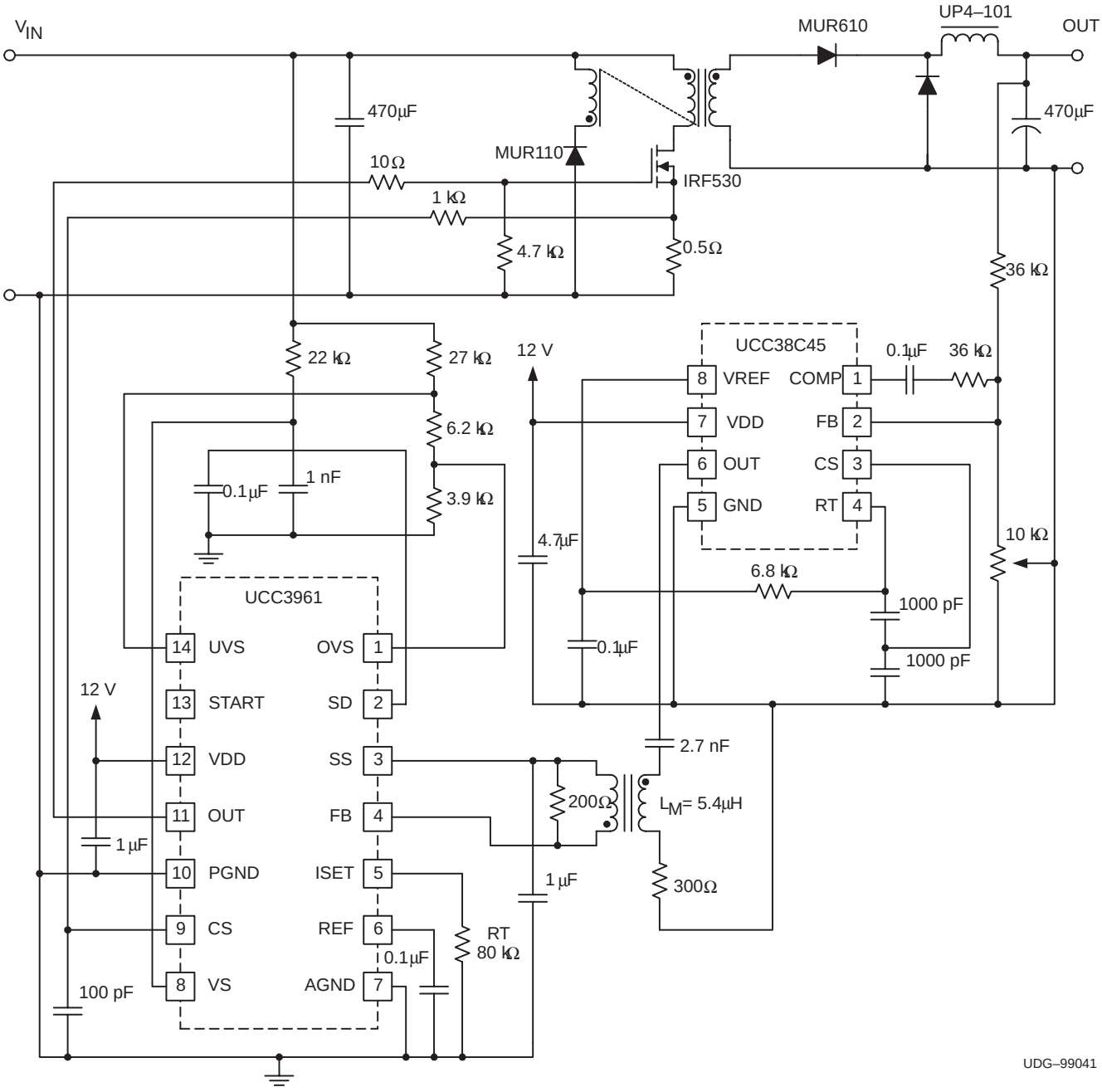



**Figure 2. Evaluation Circuit of UCC3961**

## APPLICATION INFORMATION

### pulse edge transmission circuit

The UCC3961 uses a pulse-edge-transmission (PET) circuit to transmit isolated gate-pulse information from the secondary-side controller. It is important for the PET circuit to have proper frequency response and adequately high damping (low Q-factor) in order to prevent excessive overshoot. The circuit is shown in Figure 3.

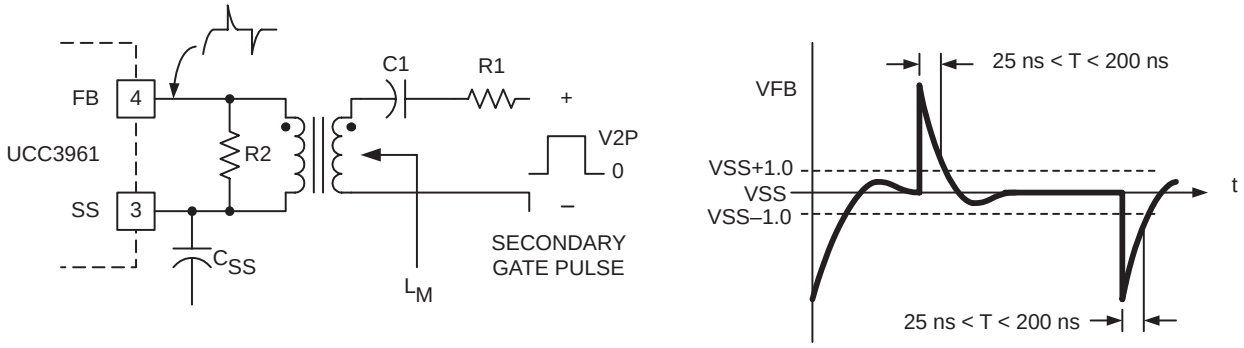



**Figure 3. Pulse Edge Transmission Circuit**

The pulse width measured at the FB pin must be between 25 ns when measured at 1 V above the soft-start voltage and and 200 ns when measured at 1 V below the soft-start voltage. The FB voltage must not be overdriven by more than 5 V above or 5 V below the soft-start voltage. In order to prevent false triggering, the FB voltage must not ring below the soft-start voltage by more than ±0.9 V. This can be met if the PET circuit has a resonant frequency of 880 kHz and a Q of 0.25. The following values meet the specifications for a 12-V secondary-gate pulse signal, over the full range of UCC3961 operating frequencies.

T1 1:1 turns ratio, LM = 5.4-µH, Ferronics 11–622J, N1 = N2 = 4 turns

R1 300 Ω

C1 2700 pF

R2 200 Ω

Pulse-edge-transmission (PET) circuits in standard surface-mount packages are available from Pulse Engineering (Part #PA0128, Part #PA0115) and from Cooper Electronic Technologies (Coiltronix), (Part #CTX01–15157).

## PARAMETER MEASUREMENT INFORMATION

### NORMAL OPERATING WAVEFORMS

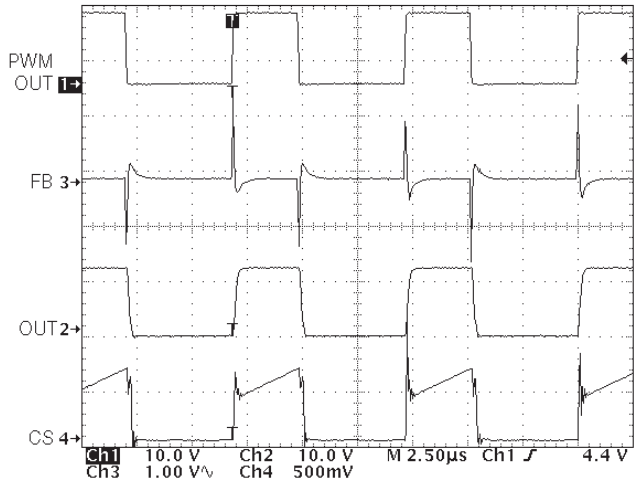



**Figure 4**

### OPERATING WAVEFORMS DURING OVERLOAD

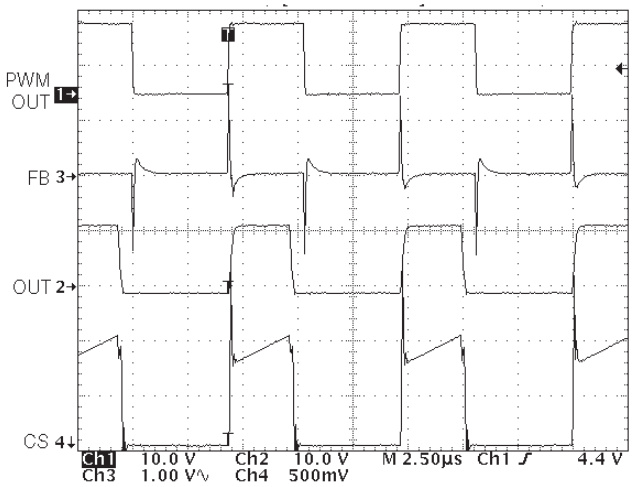



**Figure 5**

### OPERATING WAVEFORMS DURING NO LOAD

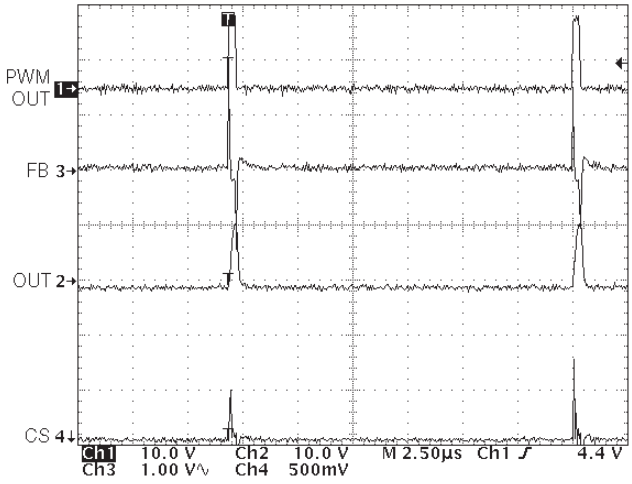



**Figure 6**

## ADDITIONAL REFERENCES

1. Dennis, Mark and Michael Madigan, *50-W Forward Converter with Synchronous Rectification and Secondary-Side Control*, SEM–1300, Topic 4, Texas Instruments Literature Number SLUP002.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC2961D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UCC2961D | Samples |
| UCC3961D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UCC3961D | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

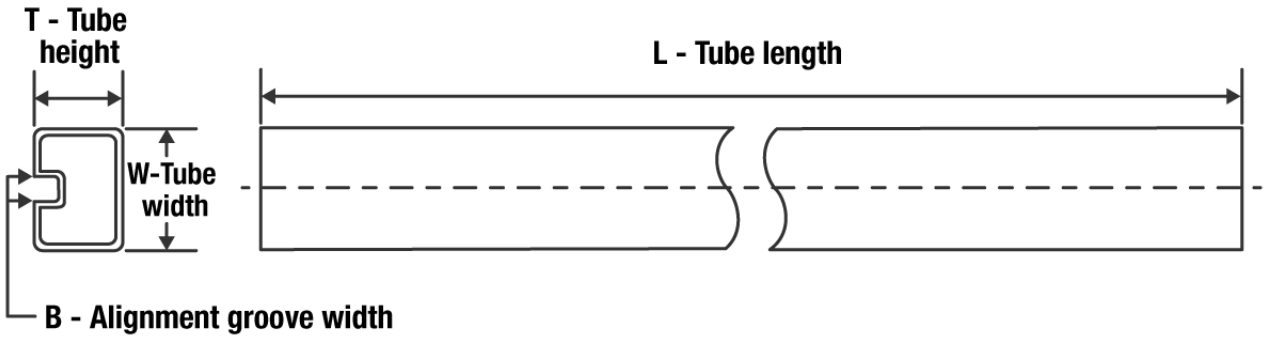
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCC2961D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| UCC3961D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

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