THE DATASHEET OF

CY25100SXC-065

CY25100

Field and Factory Programmable Spread Spectrum Clock Generator for EMI Reduction

Features

- Wide Operating Output (SSCLK) Frequency Range
  - 3 MHz to 200 MHz
- Programmable Spread Spectrum with nominal 31.5 kHz Modulation Frequency
  - Center Spread: ±0.25% to ±2.5%
  - Down Spread: –0.5% to –5.0%
- Input frequency range
  - External Crystal: 8 to 30 MHz Fundamental Crystals
  - External Reference: 8 to 166 MHz Clock
- Integrated Phase-Locked Loop (PLL)
- Field Programmable devices available
- Programmable Crystal Load Capacitor Tuning Array
- Low Cycle-to-cycle Jitter
- Spread Spectrum on/off function
- Powerdown or Output Enable function
- Commercial and Industrial temperature ranges
- 3.3 V operation
- 8-pin TSSOP and SOIC packages

Functional Description

The CY25100 is a Spread Spectrum Clock Generator (SSCG) IC used to reduce EMI found in today's high speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

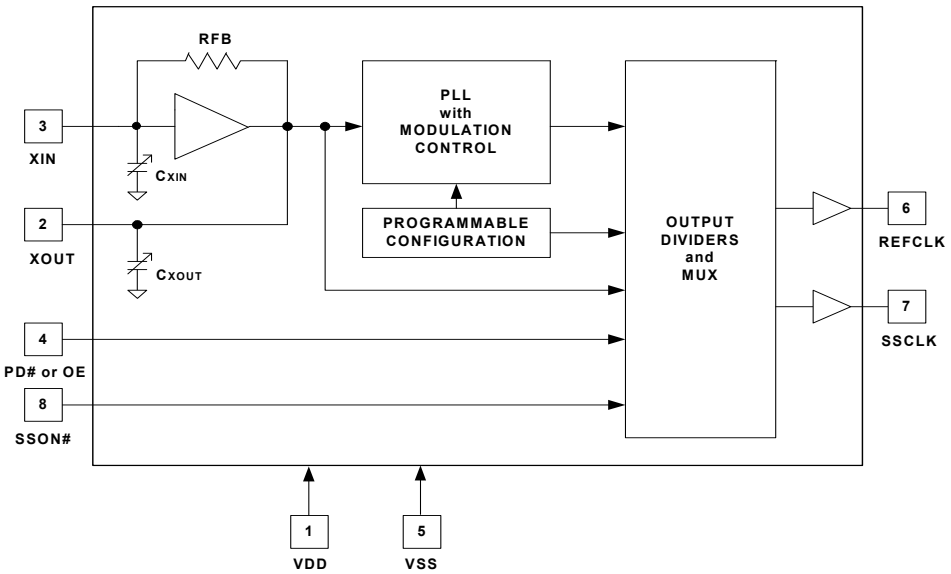
The CY25100 uses a factory or field-programmable configuration memory array to synthesize output frequency, spread percentage, crystal load capacitor, reference clock output on/off, spread spectrum on/off function, and PD#/OE options.

The spread percentage is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%.

The input to the CY25100 can either be a crystal or a clock signal. The CY25100 has two clock outputs: REFCLK and SSCLK. The non-spread spectrum REFCLK output has the same frequency as the input of the CY25100.

For a complete list of related documentation, click here.

Logic Block Diagram

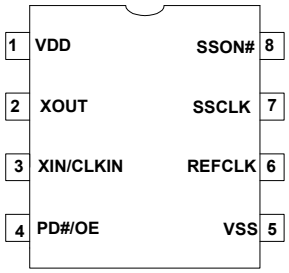


Contents

Pinouts

Figure 1. 8-pin SOIC/TSSOP pinout

CY25100



Pin Description

Pin	Name	Type	Description
1	VDD	Power	3.3 V power supply.
2	XOUT	Output	Crystal output. Leave this pin floating if external clock is connected to pin 3.
3	XIN/CLKIN	Input	Crystal input or reference clock input.
4	PD#/OE	Input	User has the option of choosing either PD# or OE function. Power Down pin: Active LOW. If PD# = 0, PLL and crystal oscillator circuit are powered down, and outputs are weakly pulled low. Output Enable pin: Active HIGH. If OE = 1, SSCLK and REFCLK are enabled.
5	VSS	Power	Power supply ground.
6	REFCLK	Output	Buffered reference output.
7	SSCLK	Output	Spread spectrum clock output.
8	SSON#	Input	Spread spectrum control: Active LOW. 0 = spread on. 1 = spread off.

User Specified Variables

Pin Function	Input Frequency	Total Crystal Load Capacitance	Output Frequency	Spread Percent (0.5% – 5%, 0.25% granularity)	Reference Output	Power Down or Output Enable
Pin Name	XIN and XOUT	XIN and XOUT	SSCLK	SSCLK	REFOUT	PD#/OE
Pin#	3 and 2	3 and 2	7	7	6	4
Unit	MHz	pF	MHz	% and Center- or Down-spread	On or Off	Select PD# or OE
	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED

Programming Description

Field Programmable CY25100

The CY25100 is programmed at the package level, and must be programmed prior to installation on a circuit board. Field programmable devices are denoted by an “F” in the ordering code, and are blank when shipped. The CY25100 is Flash technology based, which allows it to be reprogrammed up to 100 times. This allows fast and easy design changes and product updates, and eliminates issues with old and out of date inventory.

Samples and small prototype quantities can be programmed on the CY3672 programmer with the CY3690 (TSSOP package) or CY3691 (SOIC package) socket adapter.

CY3672 Programmer and CY3690/CY3691 Socket Adapters

The Cypress CY3672 programmer and the CY3690 or CY3691 socket adapter may be used to program field programmable versions of the CY25100. The CY3690 enables users to program the CY25100ZXCF and CY25100ZXIF (TSSOP). CY3691 provides the ability to program the CY25100SXCF and CY25100SXIF (SOIC). The CY3690 and CY3691 are separate orderable items, so the existing users of the CY3672 programmer need to order only the specific socket adapter to program the CY25100.

Factory Programmable CY25100

Factory programming by Cypress is available for high volume orders. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Product Functions

Input Frequency (XIN, Pin 3 and XOUT, Pin 2)

The input to the CY25100 can be a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signals is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (Pin 3 and Pin 2)

The CY25100 has internal load capacitors at Pin 3 (C_{XIN}) and Pin 2 (C_{XOUT}) C_{XIN} always equals C_{XOUT}, and they are programmable from 12 pF to 60 pF, in 0.5 pF increments.This feature eliminates the need for external crystal load capacitors.

The following formula is used to calculate the value of C_{XIN} and C_{XOUT} for matching the crystal load (C_L):

$C_{XIN} = C_{XOUT} = 2C_L – C_P$

where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance on each node of the crystal.

For example, if a crystal with C_L of 16 pF is used, and C_P is 2 pF, C_{XIN} and C_{XOUT} are calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) – 2 = 30$ pF

If using a driven reference, set C_{XIN} and C_{XOUT} to the minimum value 12 pF, connect the reference to XIN/CLKIN, and leave XOUT unconnected.

Output Frequency (SSCLK, Pin 7)

The modulated frequency at the SSCLK output is produced by synthesizing the input reference clock. The modulation can be stopped by SSON# digital control input (SSON# = HIGH, no modulation). If modulation is stopped, the clock frequency is the nominal value of the synthesized frequency without modulation (spread percentage = 0). The range of synthesized clock is from 3 to 200 MHz.

Spread Percentage (SSCLK, Pin 7)

The SSCLK spread can be programmed at any percentage value from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% for down spread.

Reference Output (REFOUT, Pin 6)

The reference clock output has the same frequency and the same phase as the input clock. This output can be programmed to be enabled (clock on) or disabled (High Z, clock off). If this output is not required, it is recommended that the disabled (High Z, Clock Off) option be selected.

Modulation Frequency

The modulation frequency is 31.5 kHz for all SSCLK frequencies from 3 to 200 MHz.

Power Down or Output Enable (PD# or OE, Pin 4)

The part can be programmed to include either PD# or OE function. PD# function powers down the oscillator and PLL. The OE function disables the outputs.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... –0.5 to +7.0 V
DC Input Voltage ..... –0.5 V to V_{DD} + 0.5 V
Storage Temperature (Non condensing) ..... –55 °C to +125 °C
Junction Temperature ..... –40 °C to +125 °C
Data Retention at Tj = 125 °C .....> 10 years
Package Power Dissipation ..... 350 mW
Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... ≥ 2000V

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ	Max	Unit
f_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	8	–	30	MHz
C_{LNOM}	Nominal Load Capacitance	Internal load caps	6	–	30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.13	3.30	3.45	V
T_A	Ambient Commercial Temperature	0	–	70	°C
	Ambient Industrial Temperature	–40	–	85	°C
C_{LOAD}	Maximum Load Capacitance at Pin 6 and Pin 7	–	–	15	pF
f_{REF}	External Reference Crystal (Fundamental tuned crystals only)	8	–	30	MHz
	External Reference Clock	8	–	166	MHz
f_{SSCLK}	SSCLK Output Frequency, C_{LOAD} = 15 pF	3	–	200	MHz
f_{REFCLK}	REFCLK Output Frequency, C_{LOAD} = 15 pF	8	–	166	MHz
f_{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
t_{PU}	Power Up Time for all V_{DD}'s to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$ V, $V_{DD} = 3.3$ V (source)	10	12	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$ V, $V_{DD} = 3.3$ V (sink)	10	12	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7 × V_{DD}	–	V_{DD}	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3 × V_{DD}	V
I_{IH}	Input High Current, PD#/OE and SSON# Pins	$V_{in} = V_{DD}$	–10	–	10	µA
I_{IL}	Input Low Current, PD#/OE and SSON# Pins	$V_{in} = V_{SS}$	–10	–	10	µA
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = 0, output pulldown resistor disabled	–10	–	10	µA
C_{XIN} or C_{XOUT}[1]	Programmable Capacitance at Pin 2 and Pin 3	Capacitance at minimum setting	–	12	–	pF
		Capacitance at maximum setting	–	60	–	pF
C_{IN}[1]	Input Capacitance at Pin 4 and Pin 8	Input pins excluding XIN and XOUT	–	5	7	pF
I_{VDD}	Supply Current	$V_{DD} = 3.45$ V, Fin = 30 MHz, REFCLK = 30 MHz, SSCLK = 66 MHz, $C_{LOAD} = 15$ pF, PD#/OE = SSON# = V_{DD}	–	25	35	mA
I_{DDS}	Standby Current	$V_{DD} = 3.45$ V, Device powered down with PD# = 0 V (driven reference pulled down)	–	15	30	µA

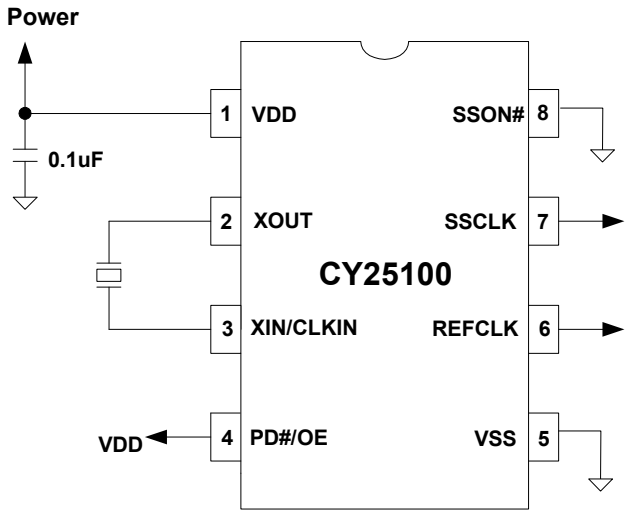
Thermal Resistance

Parameter [2]	Description	Test Conditions	8-pin SOIC	8-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	134	161	°C/W
θ_{JC}	Thermal resistance (junction to case)		49	31	°C/W

Notes
1. Guaranteed by characterization, not 100% tested.
2. These parameters are guaranteed by design and are not tested.

Application Circuit

Figure 2. Application Circuit Diagram [3, 4, 5]



Notes

3. Because the load capacitors (C_{XIN} and C_{XOUT}) are provided by the CY25100, no external capacitors are needed on the X_{IN} and X_{OUT} pins to match the crystal load capacitor (C_L). Only a single 0.1-µF bypass capacitor is required on the V_{DD} pin.
4. If an external clock is used, apply the clock to X_{IN} (pin 3) and leave X_{OUT} (pin 2) floating (unconnected).
5. If SSON# (pin 8) is LOW (V_{SS}), the frequency modulation is on at SSCLK (pin 7).

AC Electrical Characteristics

The AC Electrical Characteristics for part CY25100 is as follows. [6]

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$, Duty Cycle of CLKIN = 50% at input bias	40	50	60	%
SR1	Rising Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz; 20%–80% of V_{DD}	0.7	1.1	3.6	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz; 80%–20% of V_{DD}	0.7	1.1	3.6	V/ns
SR3	Rising Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz; 20%–80% of V_{DD}	1.0	1.6	4.0	V/ns
SR4	Falling Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz; 80%–20% of V_{DD}	1.2	1.6	4.0	V/ns
t_{CCJ1} [7]	Cycle-to-Cycle Jitter, SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK off	–	90	120	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK off	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK off	–	130	170	ps
t_{CCJ2} [7]	Cycle-to-Cycle Jitter, SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	105	140	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	200	260	ps
t_{CCJ3} [7]	Cycle-to-Cycle Jitter, REFCLK (Pin 6)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	80	100	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	135	180	ps
t_{STP}	Power down Time (pin 4 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	350	ns
t_{OE1}	Output Disable Time (pin 4 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
t_{OE2}	Output Enable Time (pin 4 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
t_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3.5	5	ms
t_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous), reference clock at correct frequency	–	2	3	ms

Notes

6. Guaranteed by characterization, not 100% tested.
7. Jitter is configuration dependent. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, spread percentage, temperature, and output load.

Switching Waveforms

Figure 3. Duty Cycle Timing (DC = t_{1A}/t_{1B})

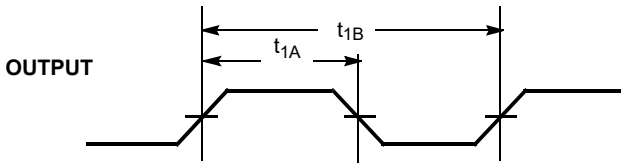
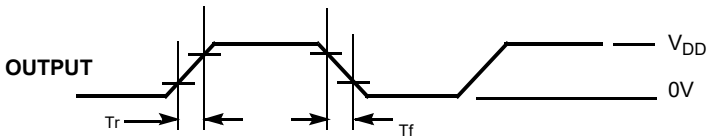


Figure 4. Output Rise/Fall Time (SSCLK and REFCLK)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)

Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 5. Power Down and Power Up Timing

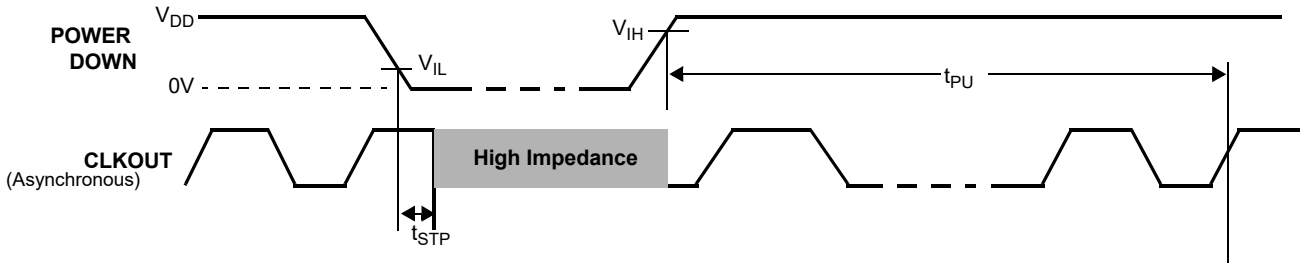
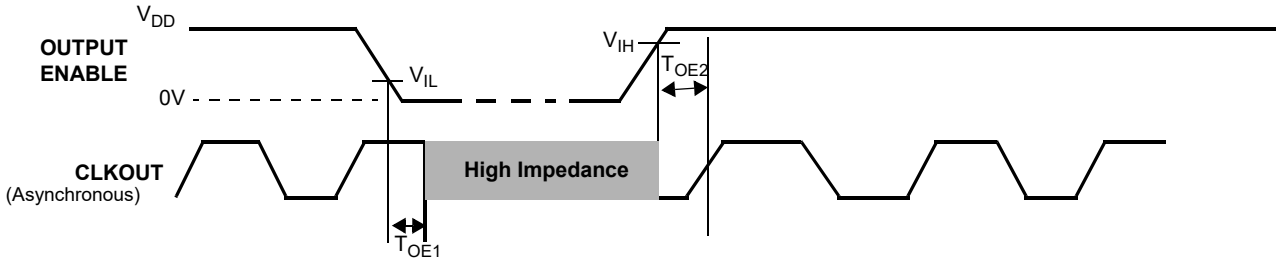
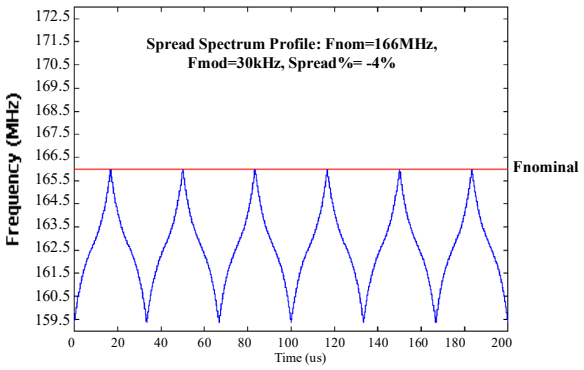


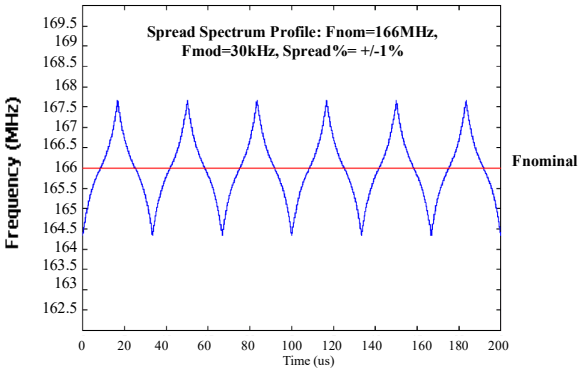
Figure 6. Output Enable/Disable Timing

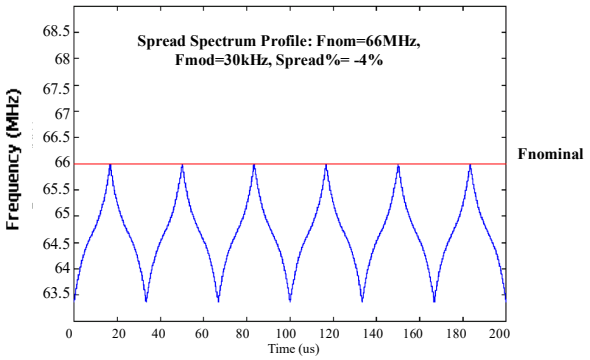


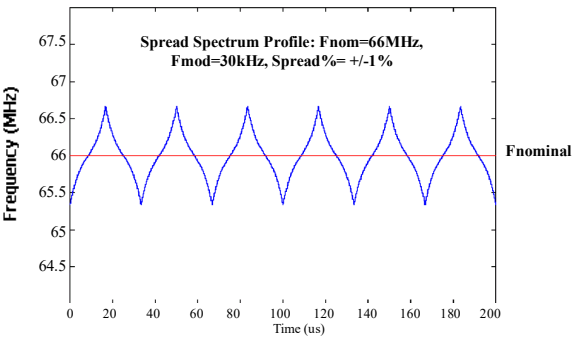
Informational Graphs

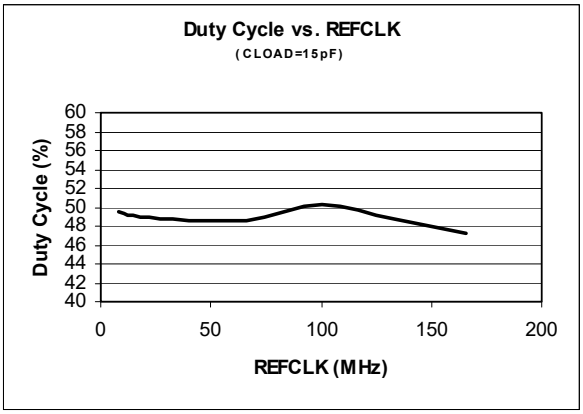
The Informational Graphs are as follows. [8]

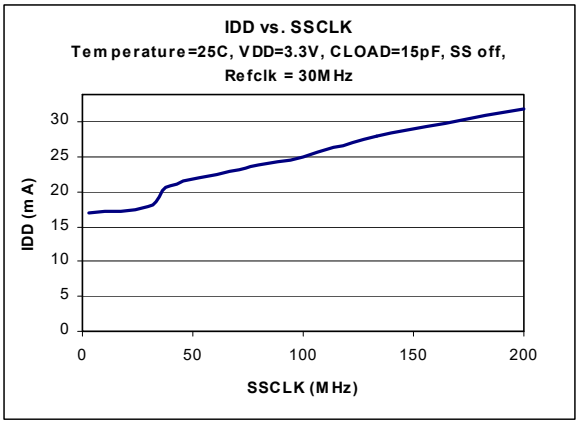










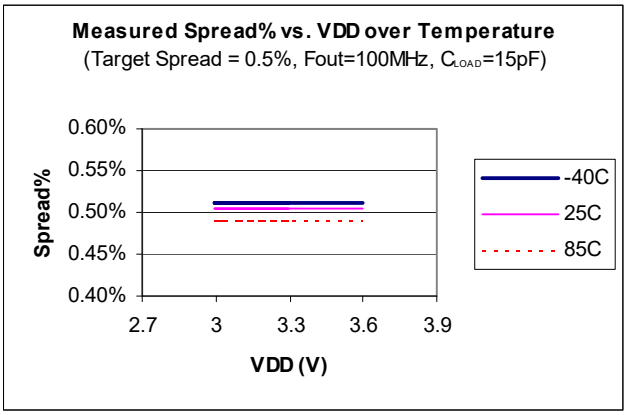


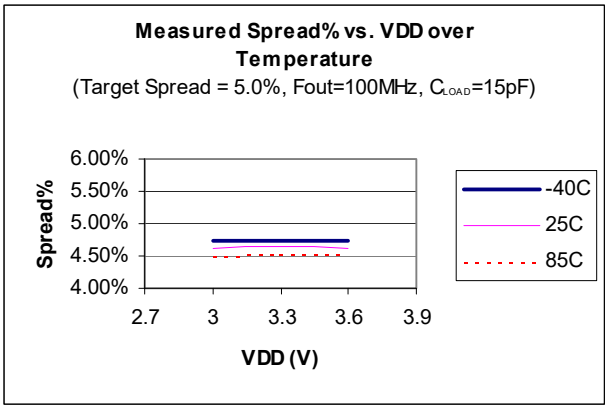
Note

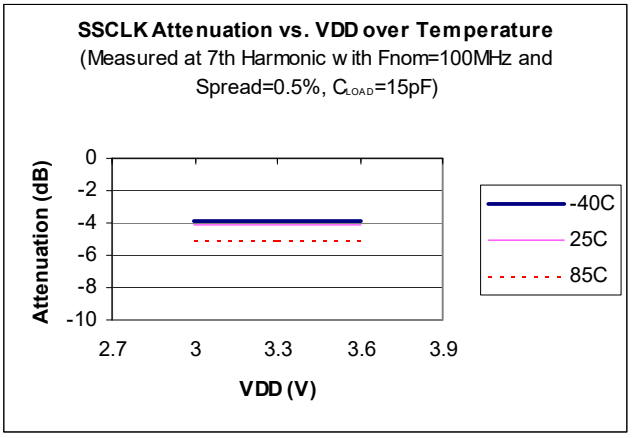
8. The Informational Graphs are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to DC Electrical Characteristics on page 6 and AC Electrical Characteristics on page 8 for device specifications.

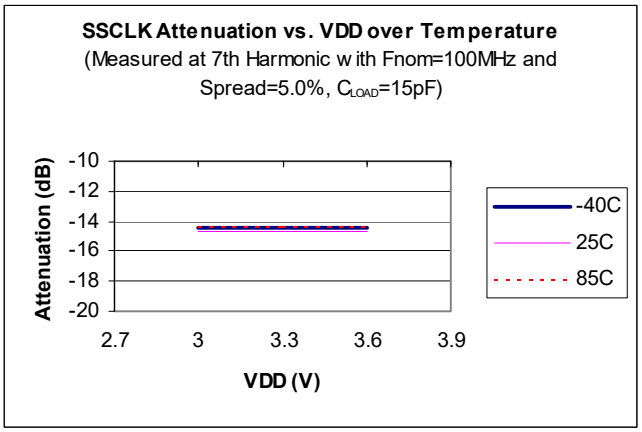
Informational Graphs (continued)

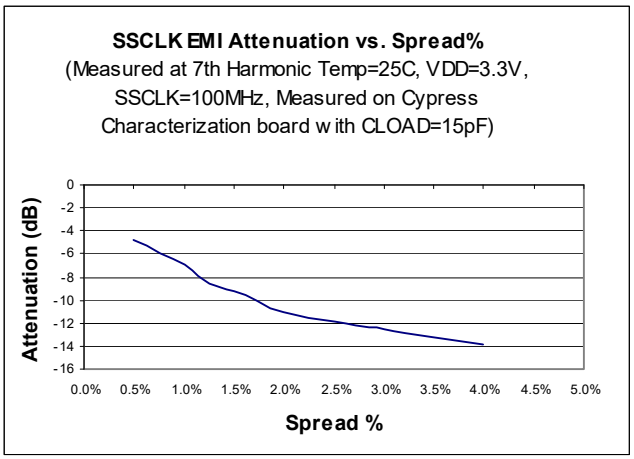
The Informational Graphs are as follows. [8]

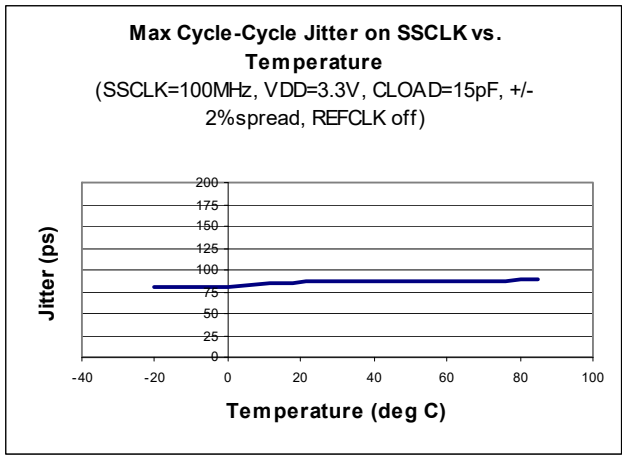












Ordering Information

Ordering Code	Package Description	Product Flow
Pb-free		
CY25100SXCF	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25100SXCFT	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100SXIF	8-pin SOIC	Industrial, –40 °C to 85 °C
CY25100SXIFT	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C
CY25100ZXCF	8-pin TSSOP	Commercial, 0 °C to 70 °C
CY25100ZXCFT	8-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100ZXIF	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZXIFT	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C
Programmer		
CY3675-CLKMAKER1	Programmer	

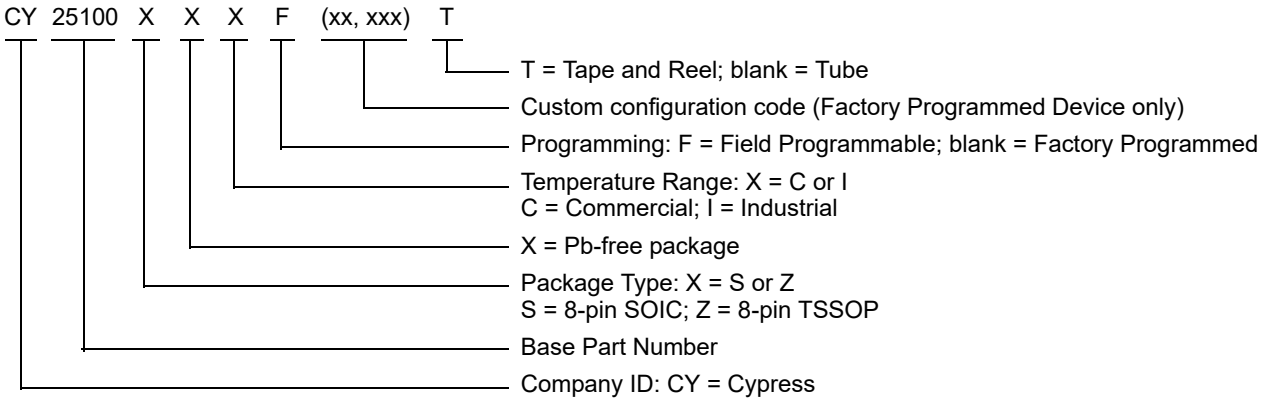
Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code	Package Description	Product Flow
CY25100ZIxxx[9, 10]	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZIxxxT[9, 10]	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C
Pb-free		
CY25100SXCxxx[9]	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25100SXCxxxT[9]	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100SXIxxx[9]	8-pin SOIC	Industrial, –40 °C to 85 °C
CY25100SXIxxxT[9]	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C
CY25100ZXCxx[9]	8-pin TSSOP	Commercial, 0 °C to 70 °C
CY25100ZXCxxT[9]	8-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100ZXIxx[9]	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZXIxxT[9]	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C

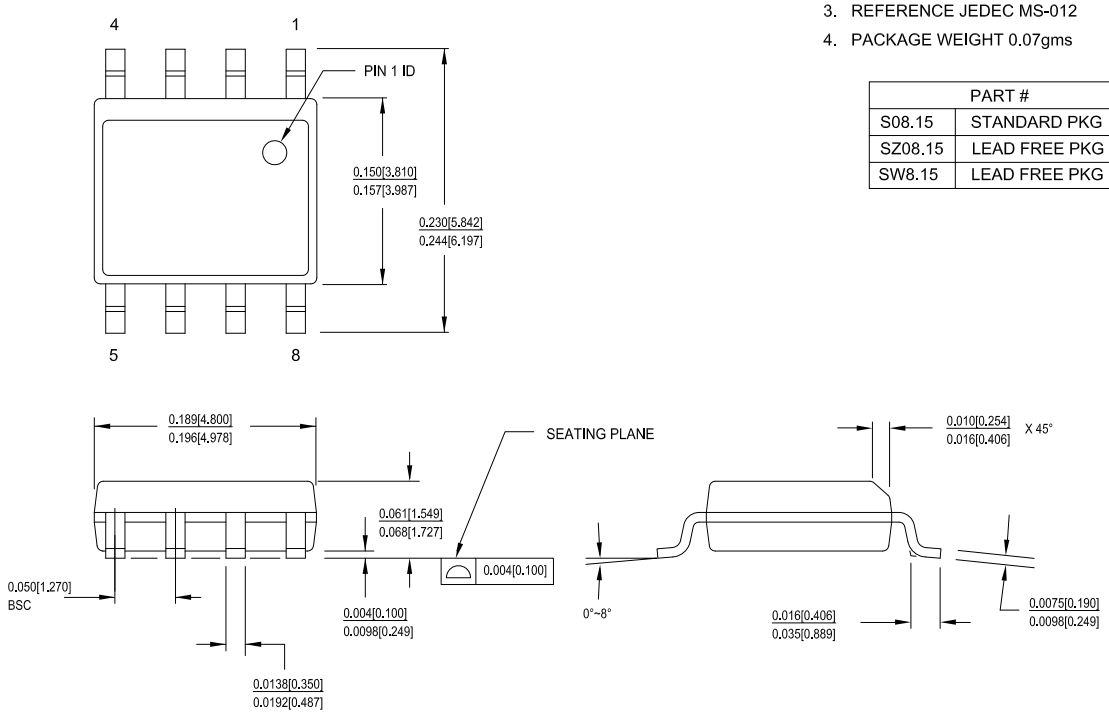
Note
9. Ordering codes with “xxx” or “xx” are factory-programmed configurations. “xxx” or “xx” denotes the specific device configuration. “w” denotes the revision. Factory programming is available for high-volume orders. For more details, contact your local Cypress field application engineer or Cypress Sales Representative.
10. Not recommended for new designs. New designs should use Pb-free devices.

Ordering Code Definitions



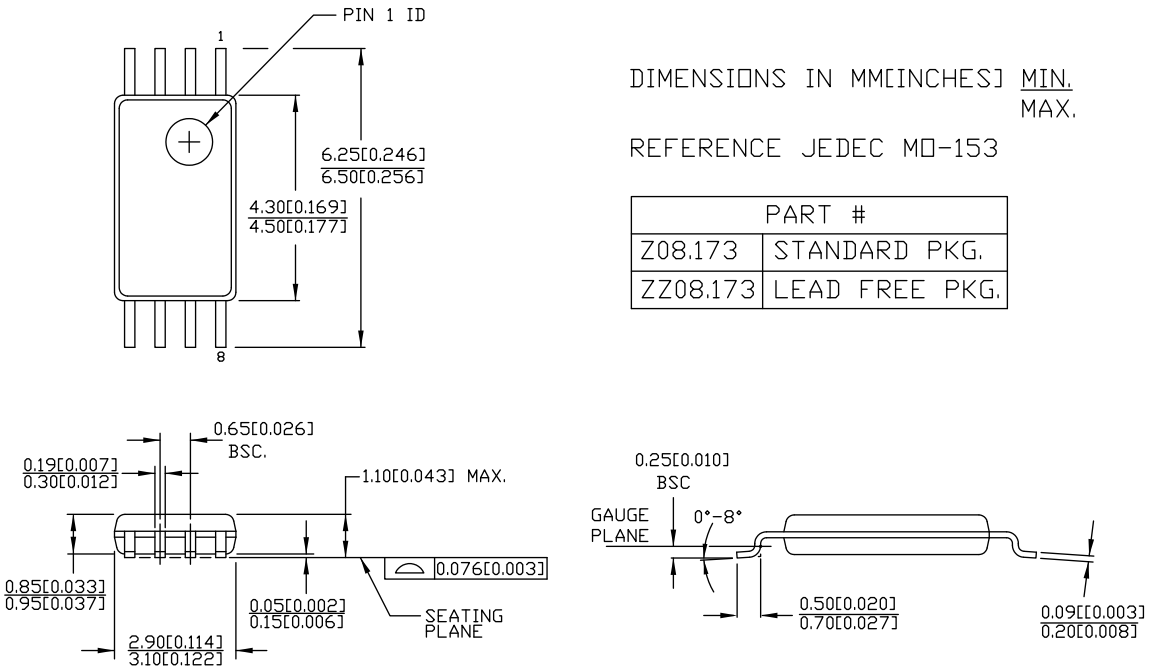
Package Diagrams

Figure 7. 8-pin SOIC (150 Mils) S08.15/SZ08.15/SW815 Package Outline, 51-85066



Package Diagrams (continued)

Figure 7. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



Acronyms

Acronym	Description
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FAE	Field Application Engineer
JEDEC	Joint Electron Devices Engineering Council
OE	Output Enable
PCB	Printed Circuit Board
PD	Power Down
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generator
TSSOP	Thin Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY25100, Field and Factory Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07499				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	126578	CKN	06/27/2003	New data sheet.
*A	128753	IJATMP	08/29/2003	Updated Programming Description: Added Field Programmable CY25100. Added CyberClocks™ Online Software. Added CY3672 Programmer and CY3690/CY3691 Socket Adapters. Added Factory Programmable CY25100. Removed “Custom Configuration Request Procedure”. Updated Ordering Information: Updated part numbers. Added Note 9 and referred the same note in “Part Number” column.
*B	130342	RGL	12/02/2003	Updated Application Circuit: Updated Figure 2. Updated Ordering Information: No change in part numbers. Updated details in “Package Description” column corresponding to MPNs CY3690 and CY3691. Updated Package Diagrams: spec 51-85066 – Changed revision from *B to *C. spec 51-85093 – Changed revision from ** to *A.
*C	204121	RGL	02/11/2004	Added Industrial Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Note 9.
*D	215392	RGL	03/31/2004	Updated Ordering Information: Updated part numbers.
*E	2513909	AESA	06/10/2008	Updated Ordering Information: Updated part numbers. Replaced “Lead free” with “Pb-Free”. Added Note 10 and referred the same note in corresponding MPNs. Added “Pb-Free” in header. Updated details in “Package Description” column (Removed Pb-Free). Updated to new template.
*F	2601881	KVM / PYRS	11/06/2008	Updated AC Electrical Characteristics: Changed minimum value of SR3 parameter from 1.2 V/ns to 1.0 V/ns. Updated Ordering Information: Updated part numbers. Removed reference of Note 9 from Parameter column. Referred Note 9 in ‘xxx’ parts.
*G	2742910	KVM	07/23/2009	General text cleanup across the document. Replaced “CY3672 FTG” with “CY3672” in all instances across the document. Removed “Benefits”. Updated Pin Description: Added a column “Type” and added corresponding details of all pins. Updated Programming Description: Updated CyberClocks™ Online Software: Updated description. Updated Product Functions: Updated Modulation Frequency: Updated description.

Document History Page (continued)

Document Title: CY25100, Field and Factory Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07499				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G (cont.)	2742910	KVM	07/23/2009	Updated DC Electrical Characteristics: Added minimum values for I_{IH} and I_{IL} parameters. Updated details in “Condition” column corresponding to I_{OZ} parameter. Updated AC Electrical Characteristics: Standardized timing parameter names to upper case in “Parameter” column. Updated Ordering Information: Updated part numbers. Updated Note 9. Updated Note 10.
*H	2897317	KVM	03/22/2010	Updated Ordering Information: Updated part numbers. Added Possible Configurations: Moved ‘xxx’ parts under Possible Configurations. Updated Package Diagrams: spec 51-85066 – Changed revision from *C to *D. spec 51-85093 – Changed revision from *A to *B.
*I	3366141	PURU	09/12/2011	Updated Logic Block Diagram. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85066 – Changed revision from *D to *E. spec 51-85093 – Changed revision from *B to *C. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*J	4108421	CINM	08/30/2013	Updated Package Diagrams: spec 51-85066 – Changed revision from *E to *F. spec 51-85093 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*K	4581659	TAVA	11/28/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams: spec 51-85093 – Changed revision from *D to *E.
*L	5516747	PSR / PAWK	11/10/2016	Updated Programming Description: Removed “CyberClocks™ Online Software”. Added Thermal Resistance. Updated Package Diagrams: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*M	6015682	PAWK	02/01/2018	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85066 – Changed revision from *H to *I. Updated to new template.

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