THE DATASHEET OF

BU90T82-ZE2

LVDS Interface LSI

27bit LVDS Dual-out Transmitter

BU90T82

General Description

The BU90T82 transmitter operates from 10MHz to 174MHz wide clock range, and 27bits data of parallel CMOS level inputs (R/G/B24bits and VSYNC, HSYNC, DE) are converted to eight channels of LVDS data stream. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less.
The BU90T82 has low swing mode to be able to expect further low power and low EMI.
Flexible Input/Output mode support various application interfaces.

Key Specifications

- Supply Voltage Range VDD 1.62 to 1.98 V
  VDDIO 1.62 to 3.60 V
- Operating Frequency 10 to 174 MHz
- Operating Temperature Range -40 to +85 ℃

•Package

	(Typ)	(Typ)	(Max)
SBGA072T070A	7.0mm×7.0mm×1.2mm		

•Applications

- Security camera, Digital camera
- Tablet
- Flat Panel Display

Features

- 27bits data of parallel LVCMOS level inputs are converted to 4 or 8 channels of LVDS data stream.
- The maximum data rate is 1218Mbps/Lane
- Support clock frequency from 10MHz up to 174MHz
- Flexible Input/Output mode
  1. Single in / Single LVDS out
  2. Single in / Dual LVDS out
  3. Double edge Single in / Dual LVDS out
  4. Single in / Distribution LVDS out
- Power down mode
- Clock edge selectable
- 6bit/8bit mode selectable
- LVDS output mapping selectable (VESA/JIEDA)
- Support reduced swing LVDS for low EMI
- Support LVDS Outputs pin reverse function
- Support spread spectrum clock generator input

Block Diagram

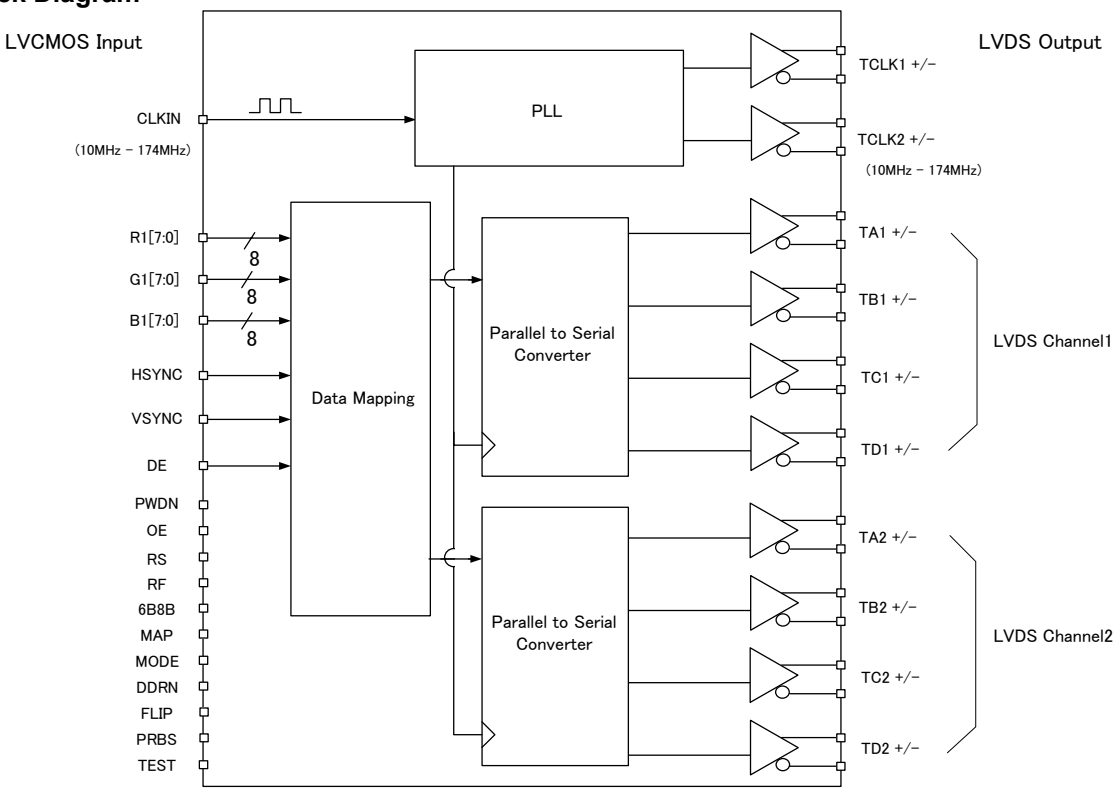


Figure 1. Block Diagram

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

	1	2	3	4	5	6	7	8	9	
A	TA1+	TB1+	TC1+	TCLK1+	TD1+	TA2+	TB2+	TC2+	TCLK2+	A
B	TA1-	TB1-	TC1-	TCLK1-	TD1-	TA2-	TB2-	TC2-	TCLK2-	B
C	PRBS	FLIP	TEST	GND	VDD	GND	VDD	TD2-	TD2+	C
D	R11	R10	VDD				GND	PWDN	OE	D
E	R13	R12	GND				MODE	MAP	DDRN	E
F	R15	R14	GND				6B8B	RS	CLKIN	F
G	R17	R16	VDD	GND	VDD	GND	VDDIO	RF	DE	G
H	G10	G12	G14	G16	B10	B12	B14	B16	VSYNC	H
J	G11	G13	G15	G17	B11	B13	B15	B17	HSYNC	J
	1	2	3	4	5	6	7	8	9	

Figure 2. Pin Configuration (Top View)

Pin Description

Pin name	Pin NO.	Type	Descriptions
TA1+/-, TB1+/-, TC1+/-,TD1+/-	A1,B1,A2,B2,A3,B3,A5,B5	LVDS output	LVDS Data output (Channel1)
TCLK1+/-	A4,B4		LVDS Clock output (Channel1)
TA2+/-, TB2+/-, TC2+/-,TD2+/-	A6,B6,A7,B7,A8,B8,C9,C8	LVDS output	LVDS Data output (Channel2)
TCLK2+/-	A9,B9		LVDS Clock output (Channel2)
R1[7:0]	G1,G2,F1,F2,E1,E2,D1,D2	LVCMOS input	Pixel data input
G1[7:0]	J4,H4,J3,H3,J2,H2,J1,H1		
B1[7:0]	J8,H8,J7,H7,J6,H6,J5,H5		
DE	G9	LVCMOS input	Control data input
HSYNC	J9		
VSYNC	H9		
CLKIN	F9	LVCMOS input	Clock input
PWDN	D8	LVCMOS input	Power Down H : Normal operation L : Power down (all LVDS output signal are Hi-z)
OE	D9		LVDS Output Enable. H: Output enable L: Output disable(all LVDS output signal are Hi-z)
RF	G8		Input CLK Triggering Edge Select. H : Rising edge L : Falling edge
RS	F8		LVDS Swing Mode Select H: 350mV L: 200mV
MAP	E8		LVDS Output Data Mapping Select H: JEIDA L: VESA
MODE	E7		LVDS Output Mode Select H: Single in / Single out L: Single in / Dual out (MODE=H, DDRN=L Distribution out)
DDRN	E9		Input CLK Triggering Edge Select. H: DDR function disable L: DDR function enable (It is possible only at Dual-out mode) (MODE=H, DDRN=L Distribution out)
6B8B	F7		6bit/8bit Mode Select H : 6bit mode (TD1+/-, TD2+/- outputs are Hi-z) L : 8bit mode
FLIP	C2		LVDS Output Pin Reverse Select. H: Reverse L/Open: Normal
TEST	C3		TEST Mode Select (Normal operation is Low)
PRBS	C1		PRBS Data Output (Normal operation is Low)
VDD	C5,C7,D3,G3,G5	Power	Power Supply for Internal Core
VDDIO	G7		Power Supply for I/O
GND	C4,C6,D7,E3,F3,G4,G6	Ground	Ground Pins

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating		Units
		Min	Max	
Supply Voltage	VDDIO	-0.3	4.0	V
	VDD	-0.3	2.1	V
Input Voltage	V_{IN}	-0.3	VDDIO+0.3	V
Output Voltage	V_{OUT}	-0.3	VDD+0.3	V
Storage Temperature Range	Tstg	-55	125	℃
Power Dissipation(Note1)	P_d	0.86		W

(Note1) Package power when IC mounting on the PCB board.
The size of PCB board : 114.5×101.5×1.6(mm^3)
The material of PCB board : The FR4 glass epoxy board.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol			Rating			Units
				Min	Typ	Max	
Supply Voltage	VDD			1.62	1.8	1.98	V
	VDDIO			1.62	1.8 / 2.5 / 3.3	3.6	V
Operating Temperature Range	Ta			-40	-	85	℃
Operating Frequency	MODE=L Dual-Out	Single Edge (DDRN=H)	Input	20	-	174	MHz
			LVDS Output	10	-	87	MHz
		Double Edge (DDRN=L)	Input	10	-	174	MHz
			LVDS Output	10	-	174	MHz
	MODE=H Single-Out, Distribution-Out		Input	10	-	174	MHz
			LVDS Output	10	-	174	MHz

DC Characteristics

Table 1. LVCMOS DC Specifications（VDDIO=1.62V~3.6V, VDD=1.62~1.98V, Ta=-40℃~+85℃）

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V_{IH}	High Level Input Voltage	VDDIO×0.65	-	VDDIO	V	-
V_{IL}	Low Level Input Voltage	GND	-	VDDIO×0.35	V	
I_{inc}	Input Current	-10	-	+10	μA	0V≤V_{IN}≤VDDIO (exclude TEST, FLIP pins)
I_{RDN}	Pull-Down Resister	-	50	-	kΩ	TEST, FLIP pins

Table 2. LVDS Transmitter DC Specifications（VDDIO=1.62V~3.6V, VDD=1.62V~1.98V, Ta=-40℃~+85℃）

Symbol	Parameter	Limits			Units	Conditions	
		Min	Typ	Max			
V_{OD}	Differential Output Voltage	250	350	450	mV	RL=100Ω	RS = H
		140	200	300	mV		RS = L
ΔV_{OD}	Change in VOD between complementary output states	-	-	35	mV	RL=100Ω	
V_{OC}	Common Mode Voltage	1.125	1.25	1.375	V		
ΔV_{OC}	Change in VOC between complementary output states	-	-	35	mV		
I_{os}	Output Short Circuit Current	-	100	150	mA	V_{OUT}=GND	
I_{oz}	Output TRI-STATE Current	-10	-	+10	μA	PWDN=L, V_{OUT}=0V to VDD	

AC Characteristics

Table 3. Switching Characteristics（VDDIO=2.5V, VDD=1.8V, Ta=25℃, RL=100Ω, CL=5pF）

Symbol	Parameter		Limits			Units
			Min	Typ	Max	
t_{TCP}	Input CLK Period (Figure-4,5)		5.75	-	100	ns
t_{TCH}	CLK IN High Time (Figure -4,5)		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCL}	CLK IN Low Time (Figure -4,5)		$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TS}	LVCMOS Data Set up to CLK IN (Figure -4,5)		0.8	-	-	ns
t_{TH}	LVCMOS Data Hold from CLK IN (Figure -4,5)		0.8	-	-	ns
t_{LVT}	LVDS Transition Time (Figure -3)		-	0.6	1.5	ns
t_{TCOP}	CLK OUT Period (Figure -6)		5.75	-	100	ns
T_{TSUP}	Differential Output Setup Time	CLKOUT(NOTE2)=174MHz	-	-	120	ps
T_{THLD}	Differential Output Hold time	CLKOUT(NOTE2)=174MHz	-	-	120	ps
t_{TCD}	CLK IN to TCLK+/- Delay (Figure-4,5)	MODE=L,DDRN=H	$3.5t_{TCOP}$	-	$9.5t_{TCOP}$	ns
		Others	$6.5t_{TCOP}$	-	$12.5t_{TCOP}$	ns
t_{TOP1}	Output Data Position 1 (Figure -6)		$-T_{THLD}$	0	$+T_{TSUP}$	ns
t_{TOP0}	Output Data Position 0 (Figure -6)		$\frac{t_{TCOP}}{7} - T_{THLD}$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TOP6}	Output Data Position 6 (Figure -6)		$2\frac{t_{TCOP}}{7} - T_{THLD}$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TOP5}	Output Data Position 5 (Figure -6)		$3\frac{t_{TCOP}}{7} - T_{THLD}$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TOP4}	Output Data Position 4 (Figure -6)		$4\frac{t_{TCOP}}{7} - T_{THLD}$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TOP3}	Output Data Position 3 (Figure -6)		$5\frac{t_{TCOP}}{7} - T_{THLD}$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TOP2}	Output Data Position 2 (Figure -6)		$6\frac{t_{TCOP}}{7} - T_{THLD}$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + T_{TSUP}$	ns
t_{TPLL}	Phase Locked Loop Set Time (Figure -7)		-	-	10	ms
t_{DEINT}	DE input Period (Figure –10)		$4t_{TCP}$	$t_{TCP}*(2n)$(Note3)	-	ns
t_{DEH}	DE High time (Figure -10)		$2t_{TCP}$	$t_{TCP}*(2m)$(Note3)	-	ns
t_{DEL}	DE Low time (Figure -10)		$2t_{TCP}$	-	-	ns

(Note2) CLKOUT: LVDS Output clock frequency.
(Note3) m, n= integer、refer to Figure 10 (DE Input Timing Diagrams)

AC Timing Diagrams

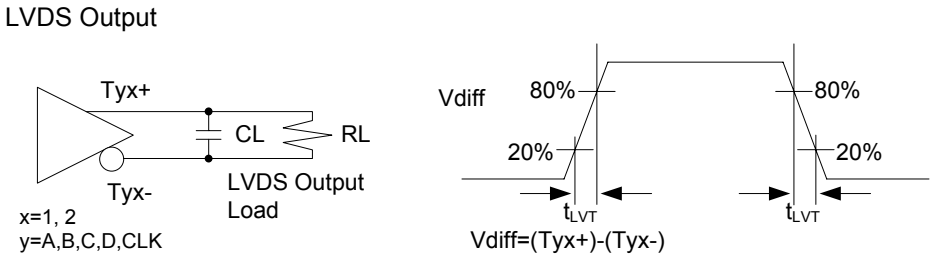


Figure 3. LVDS Output AC Timing Diagrams

AC Timing Diagrams

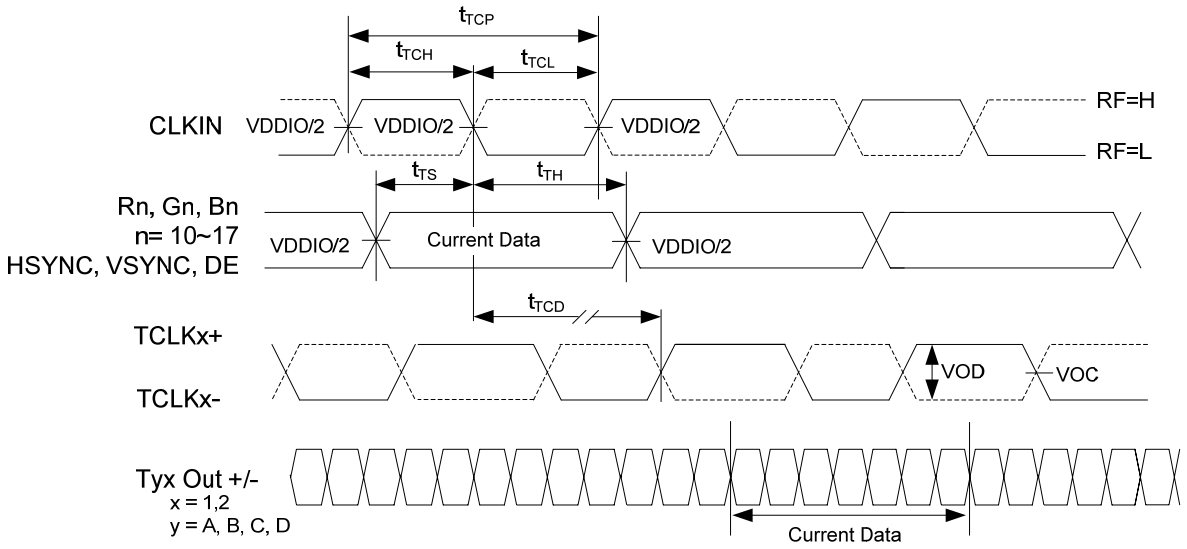


Figure 4. LVCMOS Input AC Timing Diagrams (DDR function OFF)

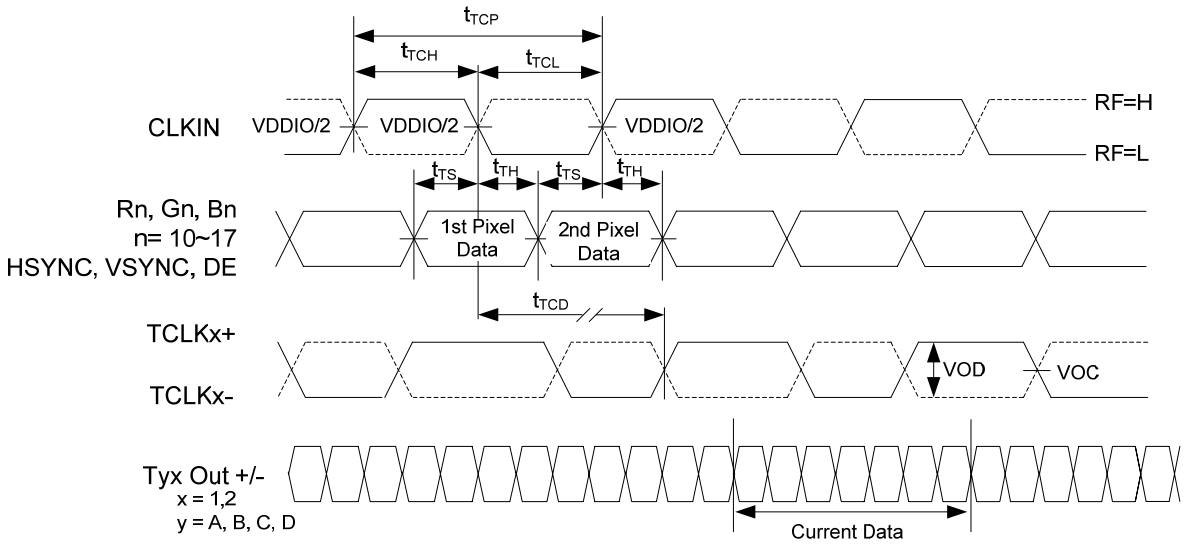


Figure 5. LVCMOS Input AC Timing Diagrams (DDR function ON)

LVDS Output AC Timing Diagrams

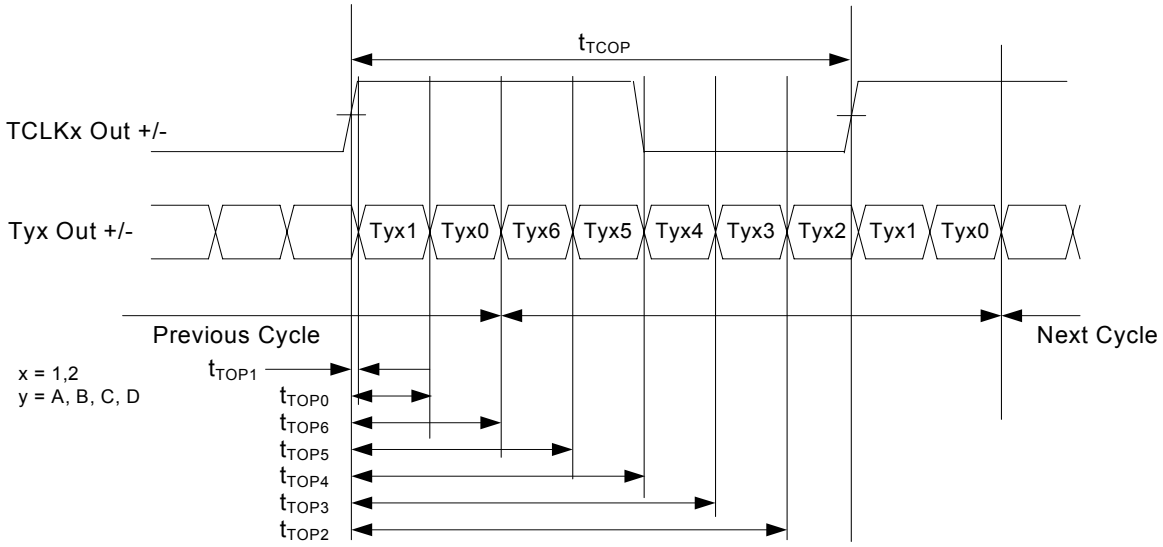


Figure 6. LVDS Output AC Timing Diagrams

Phase Locked Loop Set Time

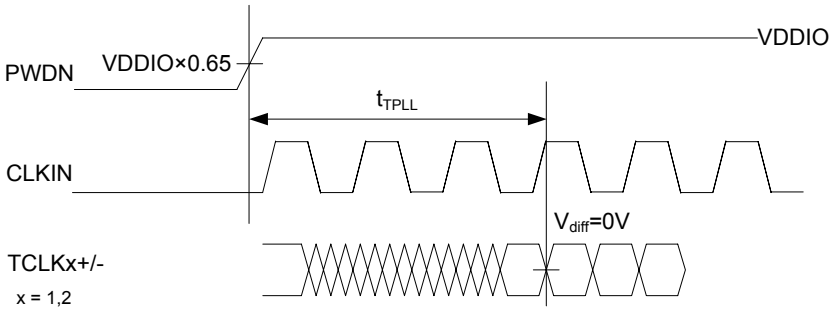


Figure 7. Phase Locked Loop Set Time

Supply Current

Table 4. Supply Current

VDDIO=2.5V, VDD=1.8V, Temp=25℃, 6B8B = L, RS=H, RL=100Ω,CL=5pF

Symbol	Parameter	Limits			Units	Conditions	
		Min	Typ	Max			
Gray Scale Pattern (i_{tccG})	Supply current	-	95	-	mA	Single-in/Single-out MODE=H, DDRN=H	CLKIN=174MHz
		-	128	-	mA	Double edge Single-in/Dual-out MODE=L, DDRN=L	CLKIN =174MHz
		-	101	-	mA	Single-in/Dual-out MODE=L, DDRN=H	CLKIN =174MHz
		-	126	-	mA	Single-in/Distribution-out MODE=H, DDRN=L	CLKIN =174MHz
Worst case Pattern (i_{tccw})		-	108	-	mA	Single-in/Single-out MODE=H, DDRN=H	CLKIN =174MHz
		-	139	-	mA	Double edge Single-in/Dual-out MODE=L, DDRN=L	CLKIN =174MHz
		-	111	-	mA	Single-in/Dual-out MODE=L, DDRN=H	CLKIN =174MHz
		-	131	-	mA	Single-in/Distribution-out MODE=H, DDRN=L	CLKIN =174MHz
i_{tccS}	Transmitter Power Down Supply Current	-	-	10	μA	PWDN=L	

Gray Scale Pattern

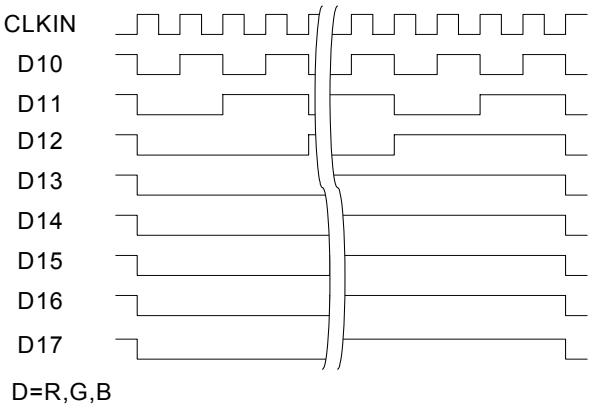


Figure 8-(1). Gray Scale Pattern

Worst Case Pattern (Maximum Power condition)

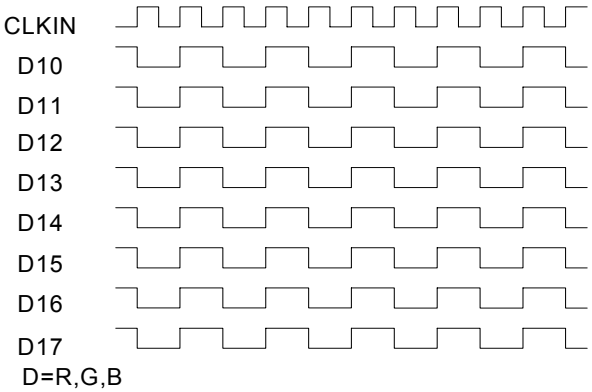


Figure 8-(2). Worst Case Pattern

LVCMOS Data Inputs Pixel Map Table

Table 5. LVCMOS Data Inputs Pixel Map Table

TFT Panel Data				BU90T82 Input
	24Bit	18Bit (Map=L)	18Bit (Map=H)	
LSB	R10	R10	-	R10
	R11	R11	-	R11
	R12	R12	R10	R12
	R13	R13	R11	R13
	R14	R14	R12	R14
	R15	R15	R13	R15
	R16	-	R14	R16
MSB	R17	-	R15	R17
LSB	G10	G10	-	G10
	G11	G11	-	G11
	G12	G12	G10	G12
	G13	G13	G11	G13
	G14	G14	G12	G14
	G15	G15	G13	G15
	G16	-	G14	G16
MSB	G17	-	G15	G17
LSB	B10	B10	-	B10
	B11	B11	-	B11
	B12	B12	B10	B12
	B13	B13	B11	B13
	B14	B14	B12	B14
	B15	B15	B13	B15
	B16	-	B14	B16
MSB	B17	-	B15	B17
	VSYNC	VSYNC	VSYNC	VSYNC
	HSYNC	HSYNC	HSYNC	HSYNC
	DE	DE	DE	DE

Output Mode Select on MODE, DDRN Pins

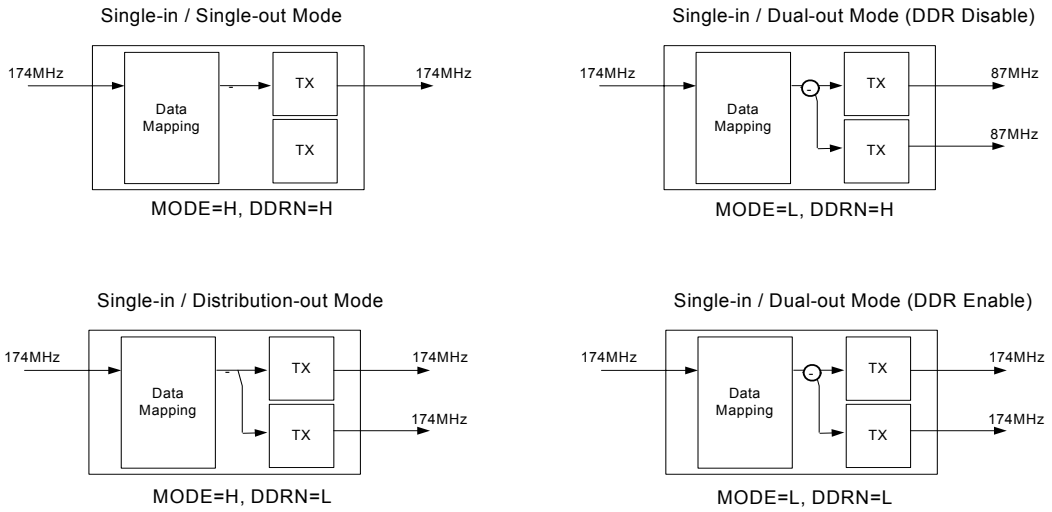
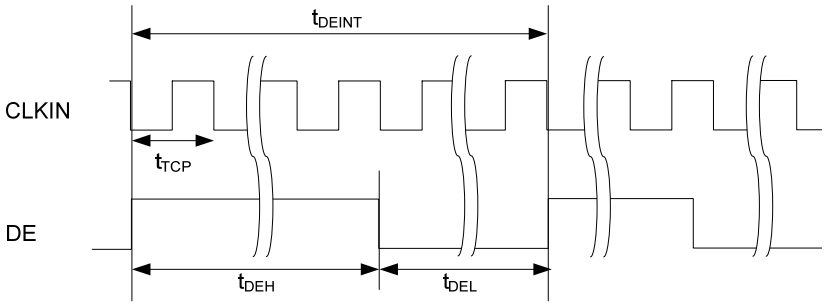


Figure 9. Output Mode Select on MODE,DDRN Pins

Table 6. Input DE Signal

In	Out	MODE Pin select	DDRN Pin select	Input DE Signal
Single	Single	H	H	Optional
Single	Dual	L	H	Require(Figure 10, 12)
Single	Distribution	H	L	Optional
Single	Dual (DDR function ON)	L	L	Optional

DE Input Timing Diagrams



In Single-in/Dual out mode、the period between rising edges of DE(t_{deint}), high time of DE(t_{DEH})
$t_{DEH} = t_{TCP} * (2m)$
$t_{DEINT} = t_{TCP} * (2n)$
m, n=integer

Figure 10. Single-in / Dual-out mode DE Input Timing Diagrams (MODE=L,DDRN=H)

Single-in / Single-out Mode (MODE=H; DDRN=H)

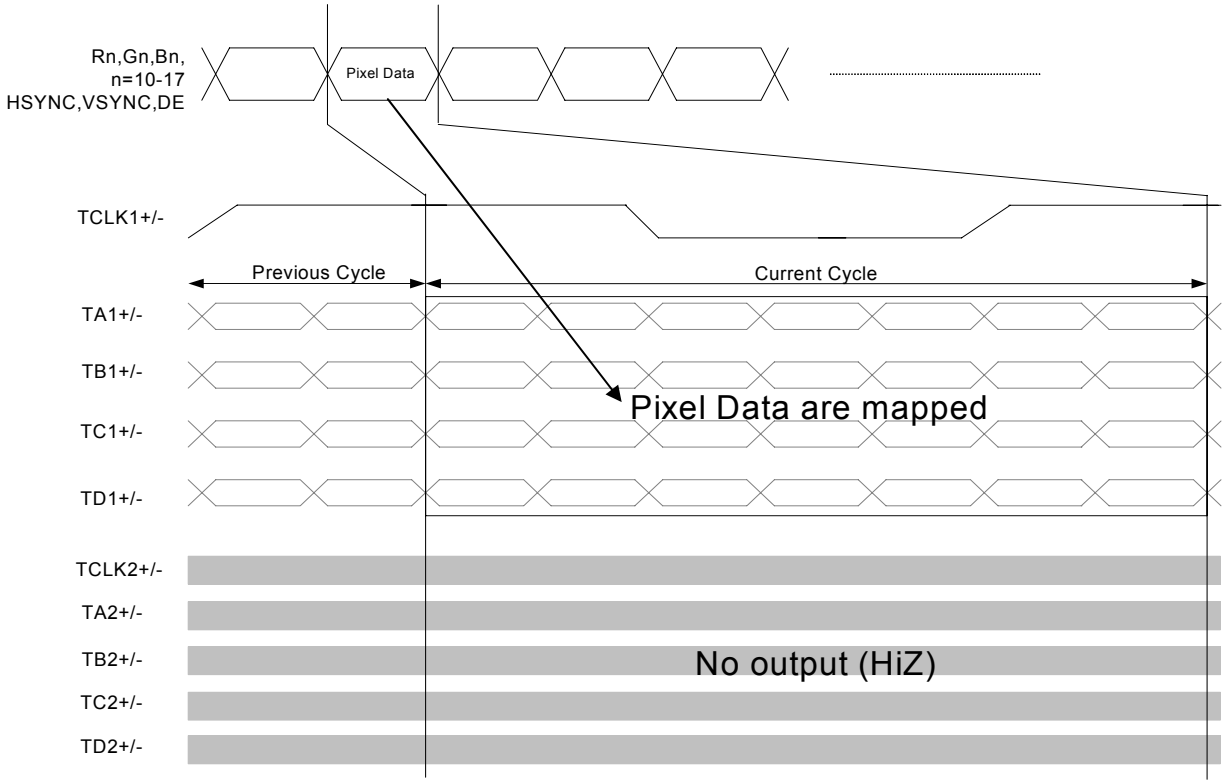


Figure 11. Single-In/Single-out Mode (FLIP=L)

Single-in / Dual-out Mode (MODE=L; DDRN=H)

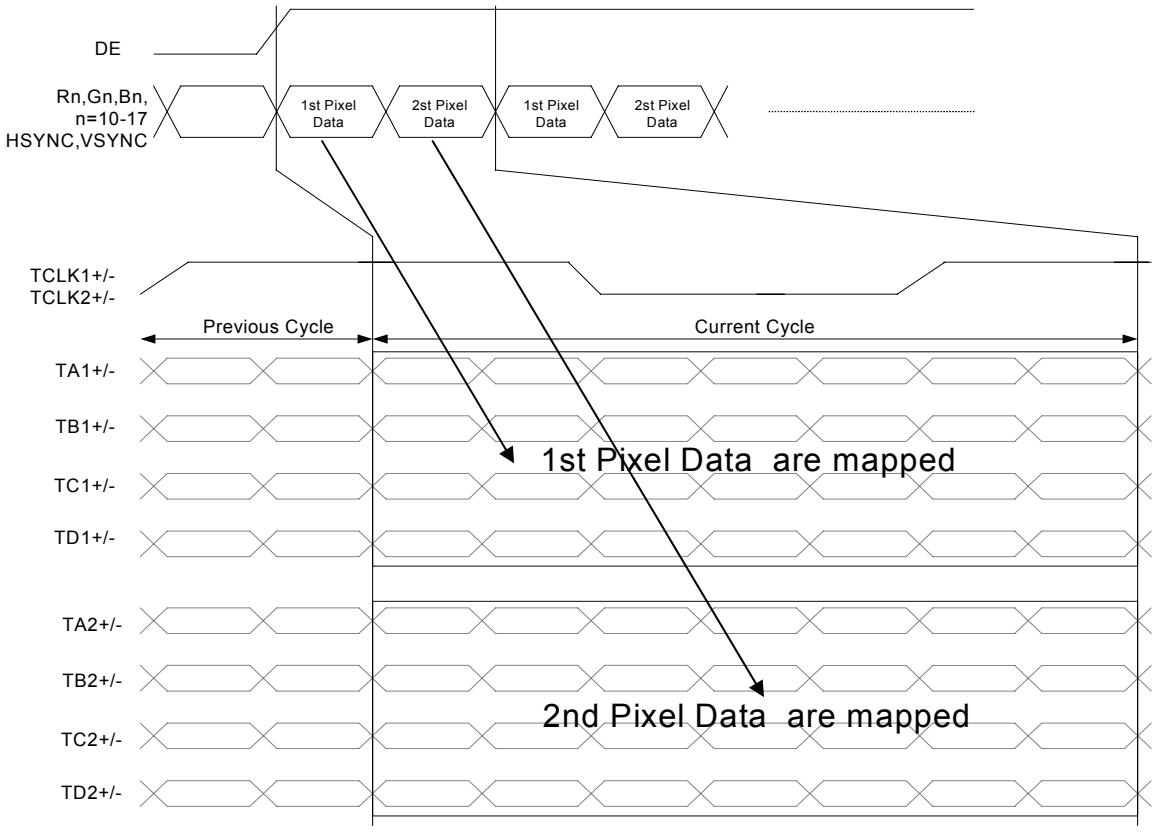


Figure 12. Single-In/Dual-out Mode (FLIP=L)

Single-in / Distribution-out Mode (MODE=H; DDRN=L)

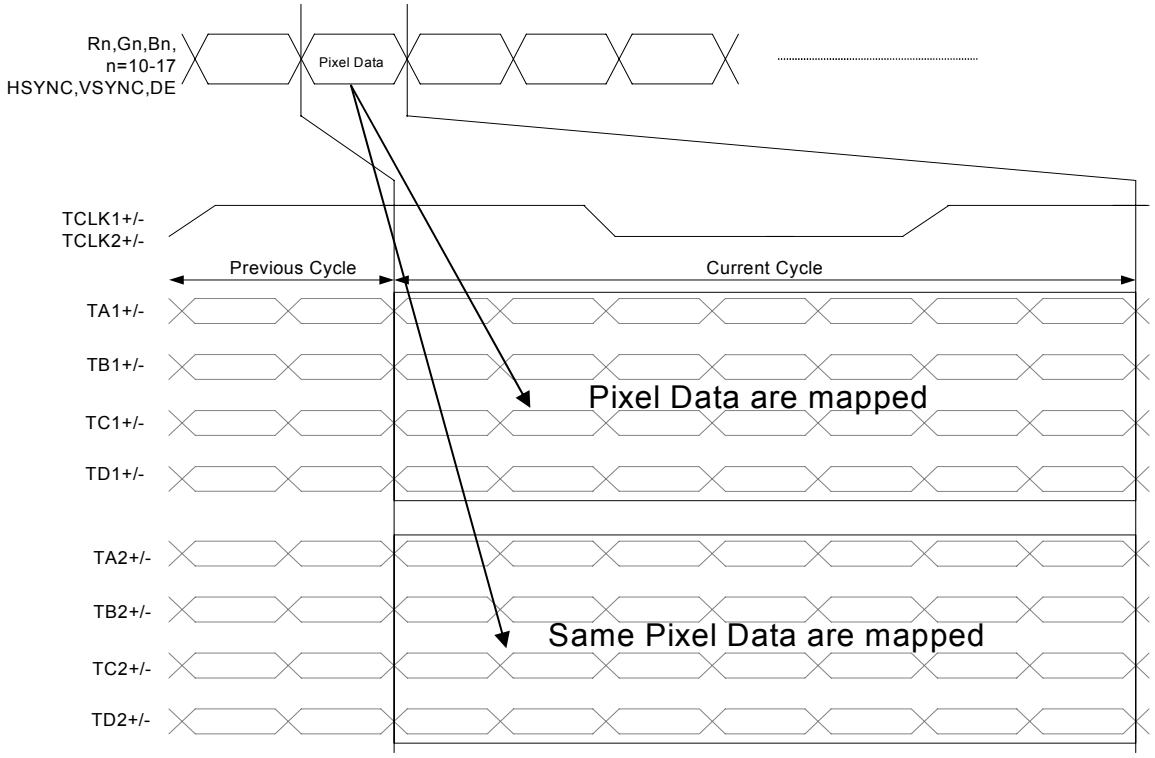


Figure 13. Single-In/Distribution-out Mode (FLIP=L)

Single-in / DDR Dual-out Mode (MODE=L; DDRN=L)

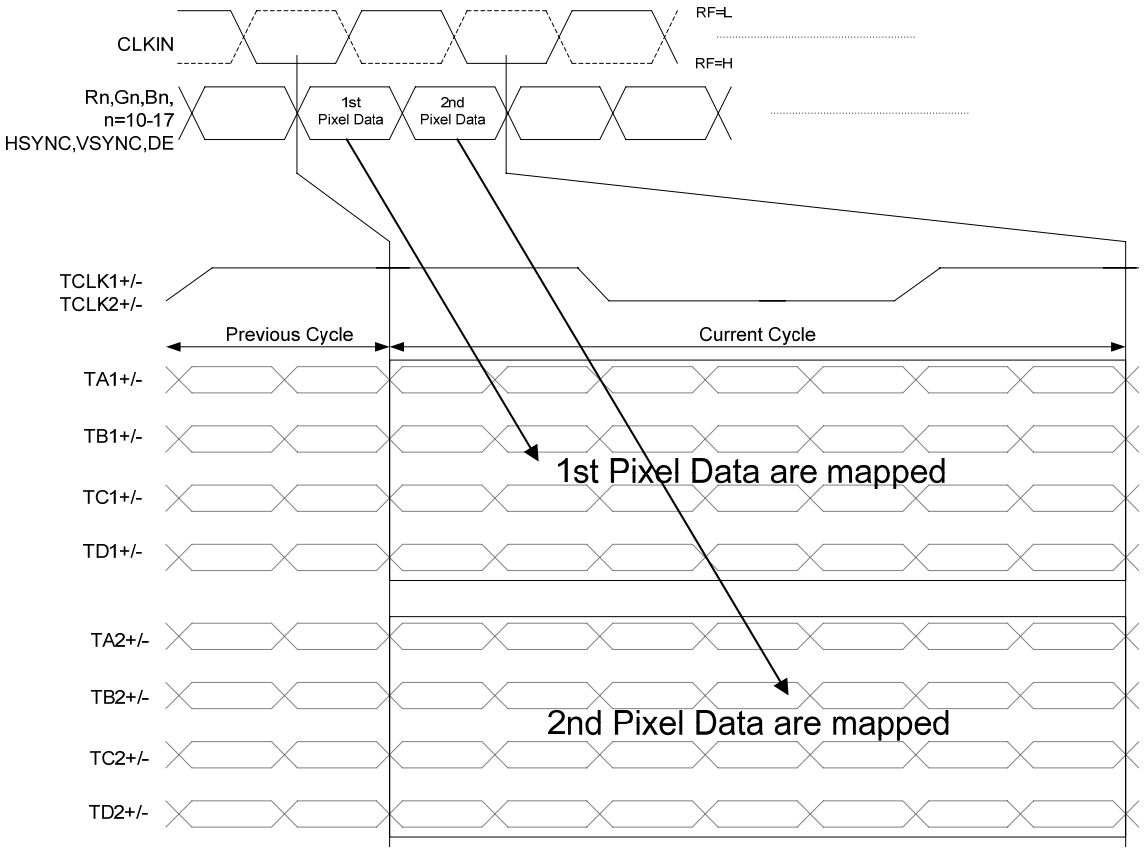


Figure 14. Single-In/DDR Dual-out Mode (FLIP=L)

LVDS Output Data mapping Table (6B8B = L)

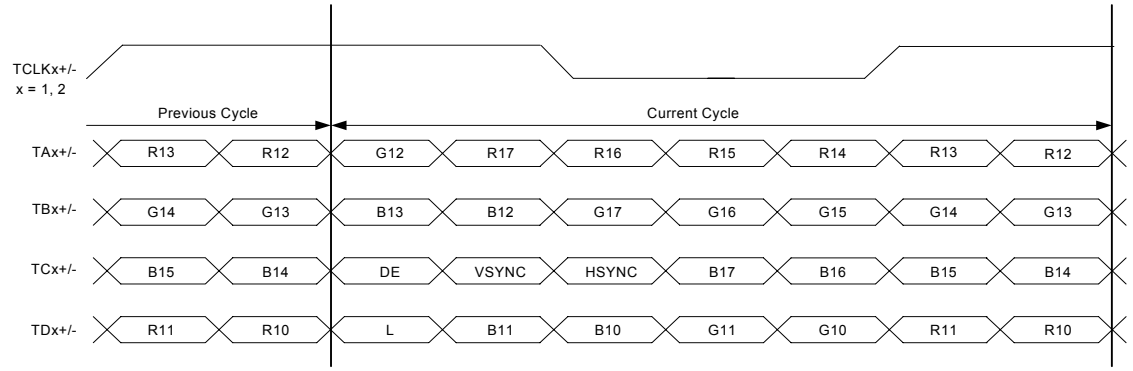


Figure 15-(1). 8bit mode LVDS output mapping (MAP=H: JEIDA)

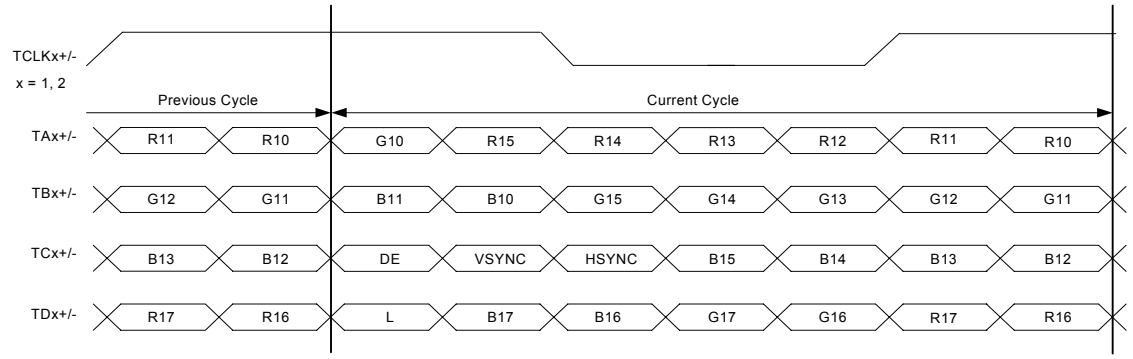


Figure 15-(2). 8bit mode LVDS output mapping (MAP=L; VESA)

LVDS Output Data mapping Table (6B8B = H)

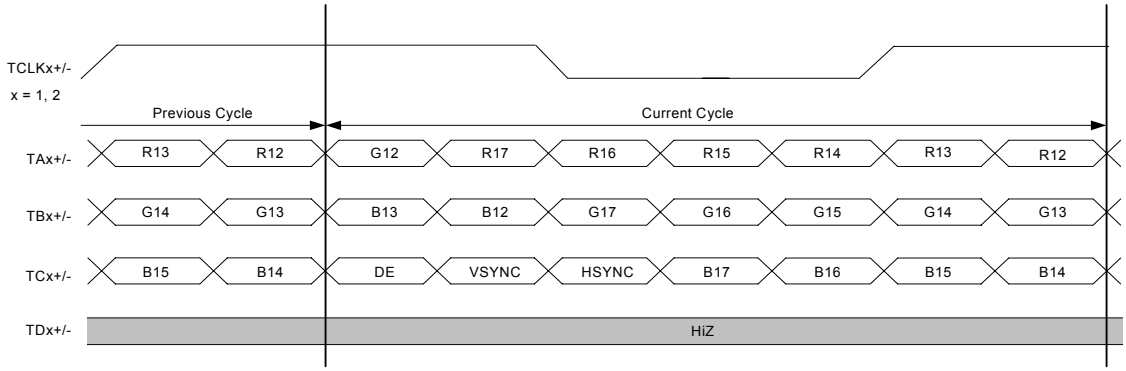


Figure 16-(1). 6bit mode LVDS output mapping (MAP=H; JEIDA)

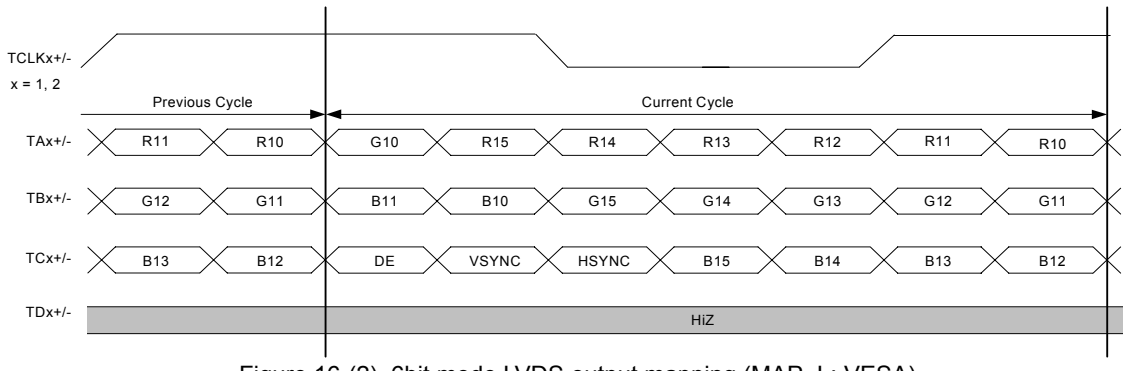


Figure 16-(2). 6bit mode LVDS output mapping (MAP=L; VESA)

LVDS Data Output Table for Function of FLIP pin

Table 7. LVDS Data Output Pin Name

Pin No	Output Data											
	Single Out				Dual Out				Distribute Out			
	8bit		6bit		8bit		6bit		8bit		6bit	
	FLIP=L	FLIP=H	FLIP=L	FLIP=H	FLIP=L	FLIP=H	FLIP=L	FLIP=H	FLIP=L	FLIP=H	FLIP=L	FLIP=H
A1	TA1+	-	TA1+	-	TA1+	TD2-	TA1+	-	TA1+	TD1-	TA1+	-
B1	TA1-	-	TA1-	-	TA1-	TD2+	TA1-	-	TA1-	TD1+	TA1-	-
A2	TB1+	-	TB1+	-	TB1+	TCLK2-	TB1+	TCLK2-	TB1+	TCLK1-	TB1+	TCLK1-
B2	TB1-	-	TB1-	-	TB1-	TCLK2+	TB1-	TCLK2+	TB1-	TCLK1+	TB1-	TCLK1+
A3	TC1+	-	TC1+	-	TC1+	TC2-	TC1+	TC2-	TC1+	TC1-	TC1+	TC1-
B3	TC1-	-	TC1-	-	TC1-	TC2+	TC1-	TC2+	TC1-	TC1+	TC1-	TC1+
A4	TCLK1+	-	TCLK1+	-	TCLK1+	TB2-	TCLK1+	TB2-	TCLK1+	TB1-	TCLK1+	TB1-
B4	TCLK1-	-	TCLK1-	-	TCLK1-	TB2+	TCLK1-	TB2+	TCLK1-	TB1+	TCLK1-	TB1+
A5	TD1+	-	-	-	TD1+	TA2-	-	TA2-	TD1+	TA1-	-	TA1-
B5	TD1-	-	-	-	TD1-	TA2+	-	TA2+	TD1-	TA1+	-	TA1+
A6	-	TD1-	-	-	TA2+	TD1-	TA2+	-	TA1+	TD1-	TA1+	-
B6	-	TD1+	-	-	TA2-	TD1+	TA2-	-	TA1-	TD1+	TA1-	-
A7	-	TCLK1-	-	TCLK1-	TB2+	TCLK1-	TB2+	TCLK1-	TB1+	TCLK1-	TB1+	TCLK1-
B7	-	TCLK1+	-	TCLK1+	TB2-	TCLK1+	TB2-	TCLK1+	TB1-	TCLK1+	TB1-	TCLK1+
A8	-	TC1-	-	TC1-	TC2+	TC1-	TC2+	TC1-	TC1+	TC1-	TC1+	TC1-
B8	-	TC1+	-	TC1+	TC2-	TC1+	TC2-	TC1+	TC1-	TC1+	TC1-	TC1+
A9	-	TB1-	-	TB1-	TCLK2+	TB1-	TCLK2+	TB1-	TCLK1+	TB1-	TCLK1+	TB1-
B9	-	TB1+	-	TB1+	TCLK2-	TB1+	TCLK2-	TB1+	TCLK1-	TB1+	TCLK1-	TB1+
C9	-	TA1-	-	TA1-	TD2+	TA1-	-	TA1-	TD1+	TA1-	-	TA1-
C8	-	TA1+	-	TA1+	TD2-	TA1+	-	TA1+	TD1-	TA1+	-	TA1+

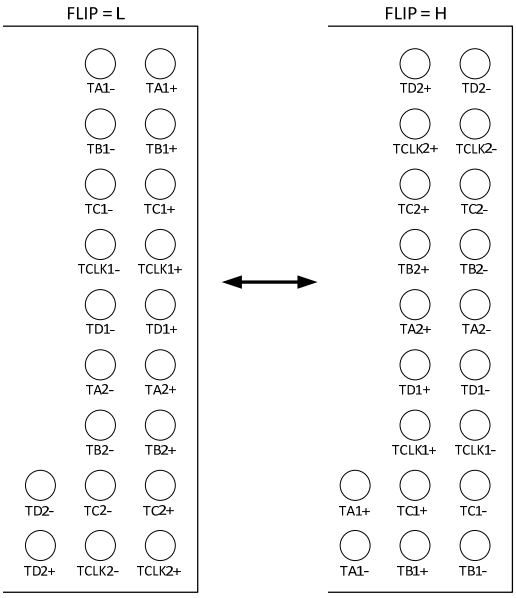


Figure 17. LVDS Data Output for Function of FLIP pin

Typical Application Circuit (24bit・Single-out mode)

example
BU90T82: LVCMOS Data Input (24bit) / rising edge / 350mV swing output / VESA mapping / Single-out

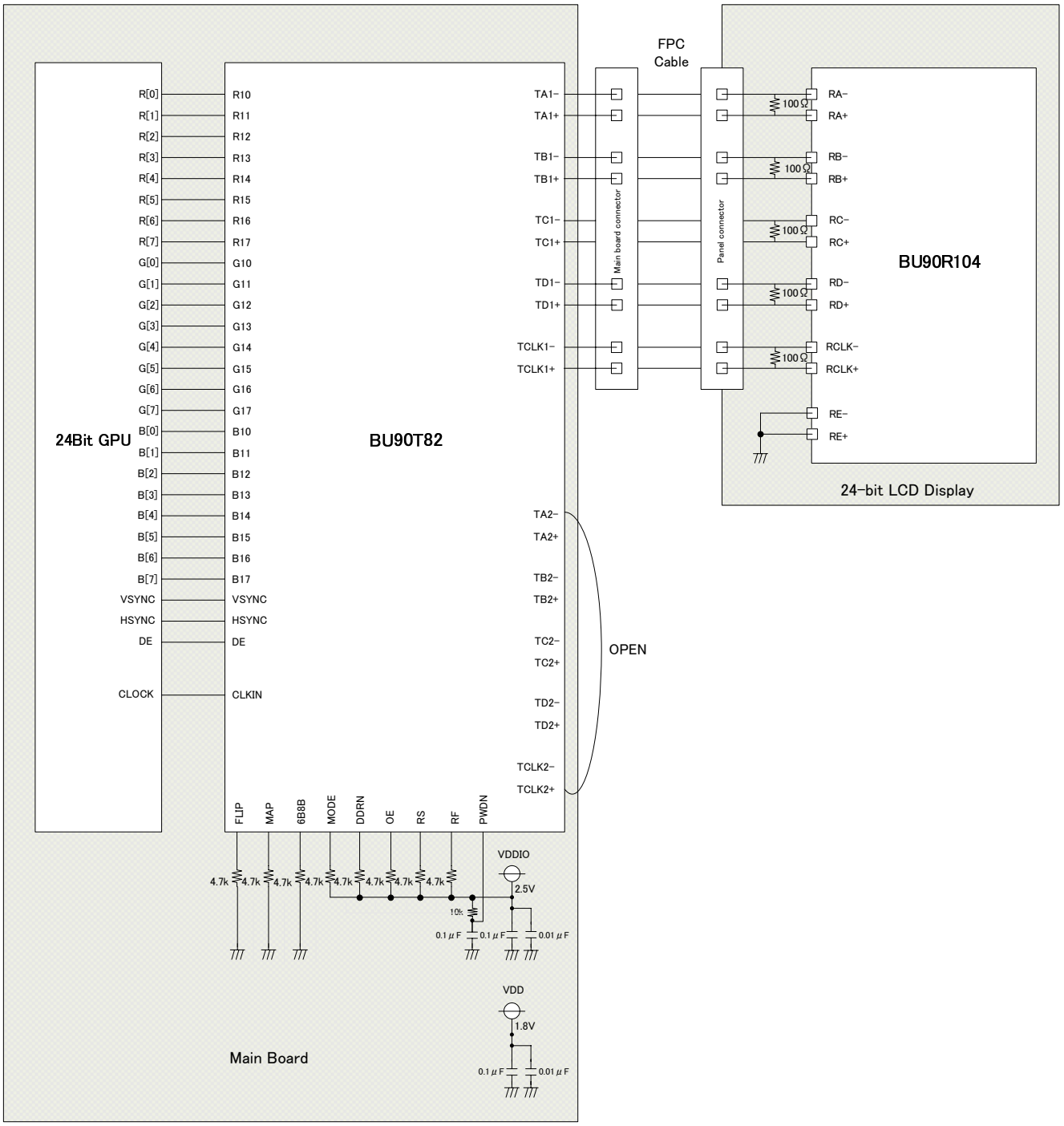


Figure 18. Application Circuit (24bit Single-out mode)

Typical Application Circuit (18bit・Single-out mode)

example
BU90T82: LVCMOS Data Input (18bit) / rising edge /350mV swing output / VESA mapping /Single-out

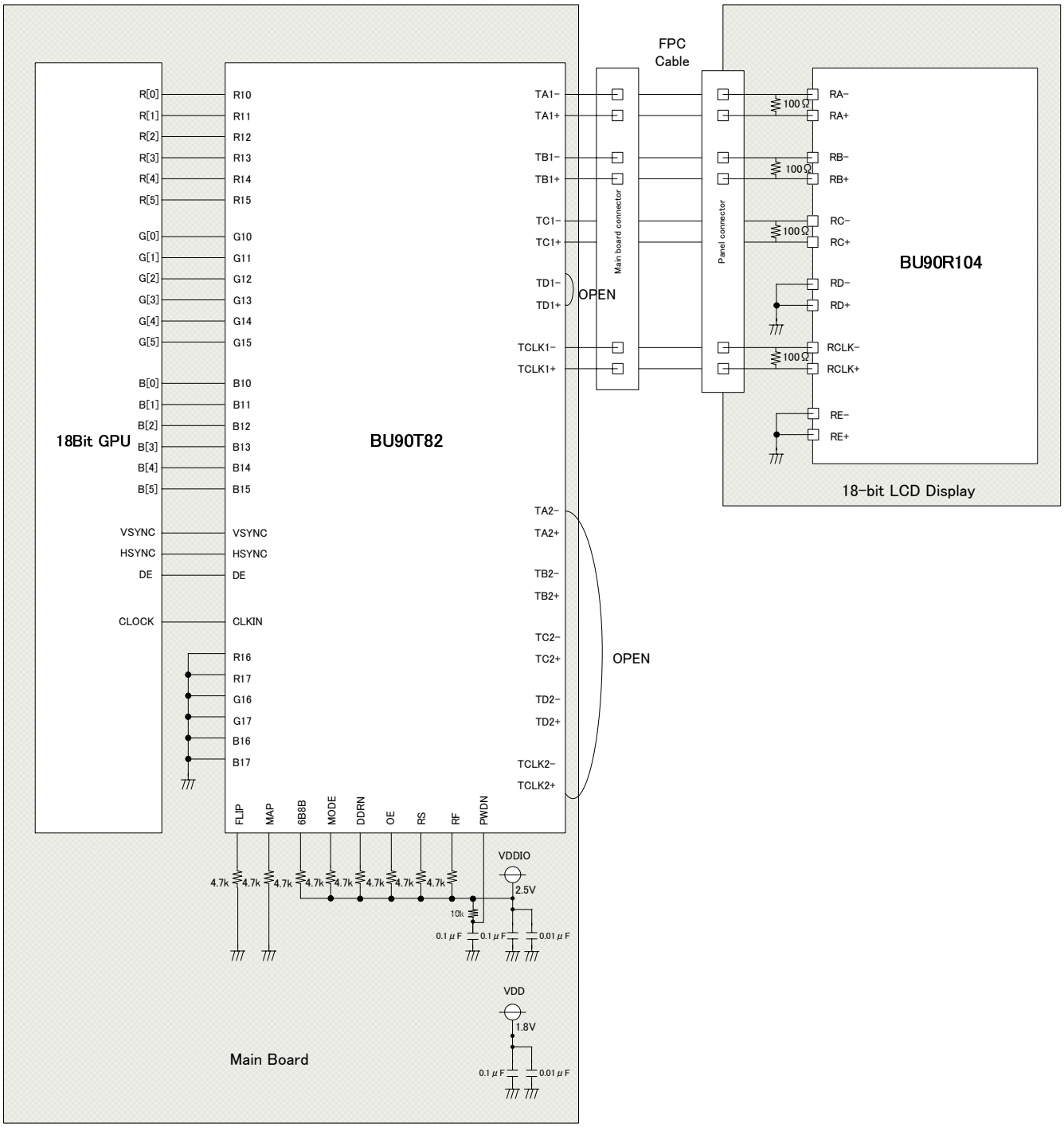


Figure 19. Application Circuit (18bit Single-out mode)

Typical Application Circuit (24bit・Distribution-out mode)

example
BU90T82: LVCMOS Data Input (24bit) / rising edge / 350mV swing output / VESA mapping

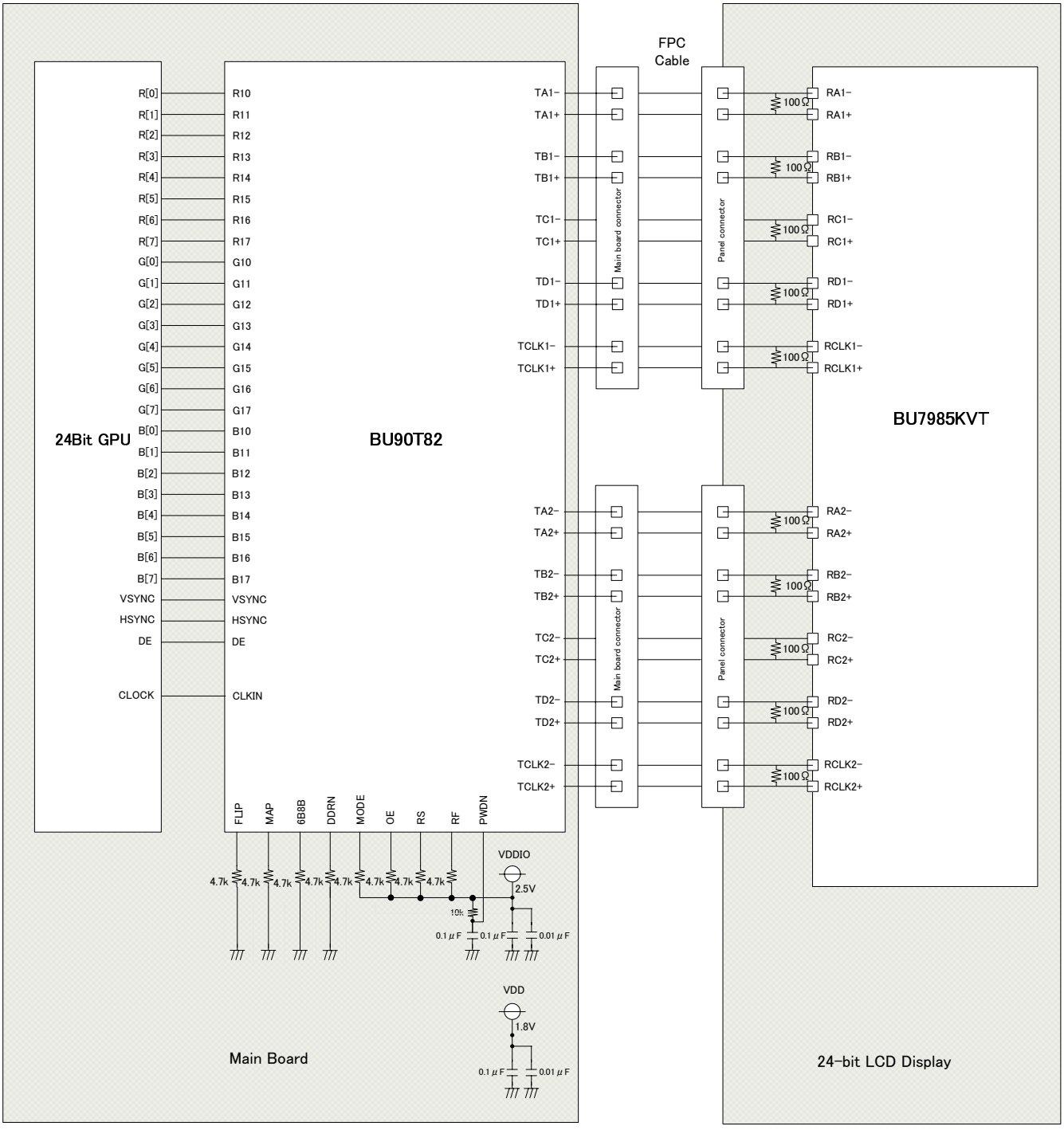


Figure 20. Application Circuit (24bit Distribution-out mode)

Typical Application Circuit (24bit・Dual-out mode)

example
BU90T82: LVCMOS Data Input (24bit) / rising edge / 350mV swing output / VESA mapping / Dual-out

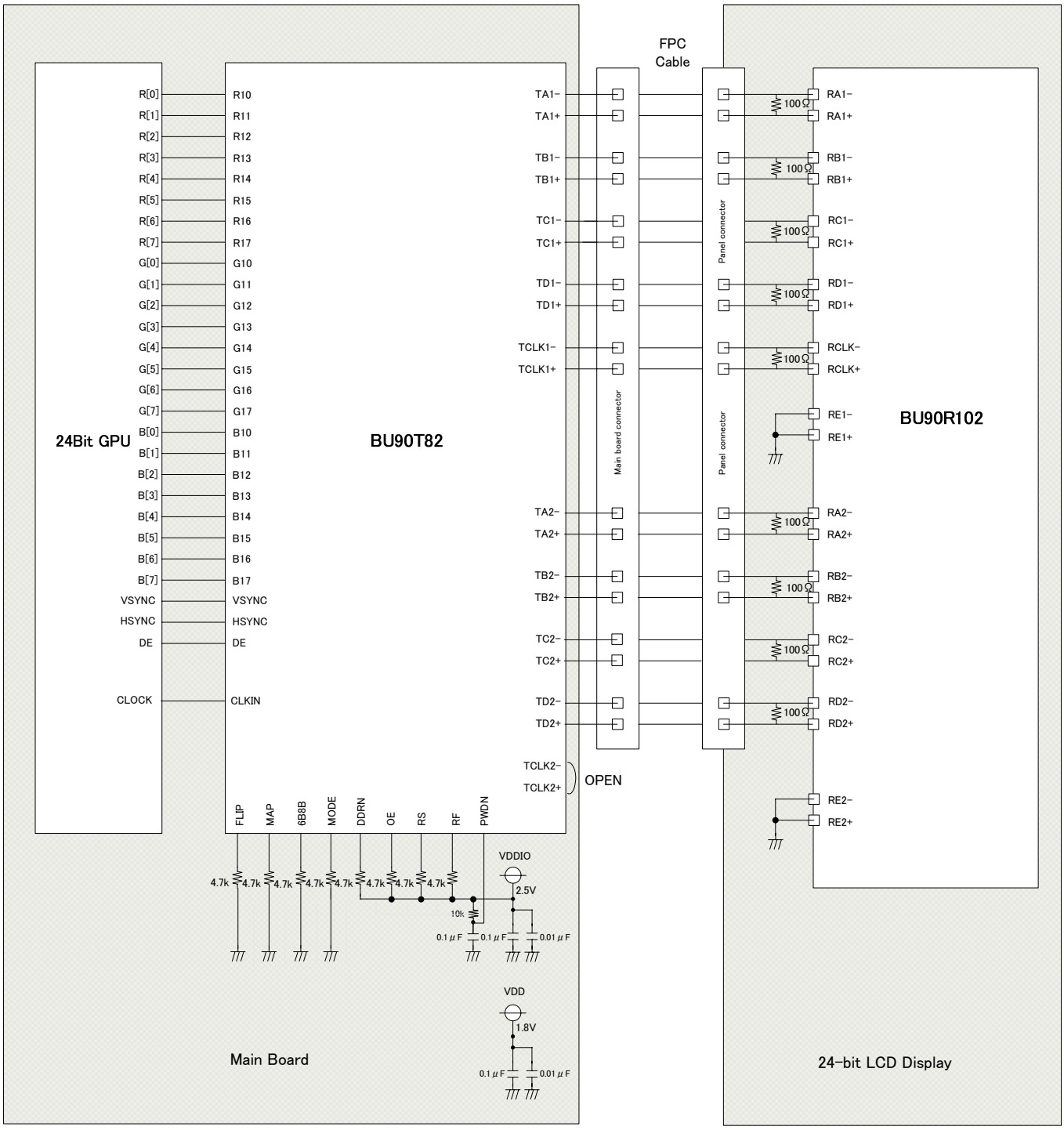


Figure 21. Application Circuit (24bit Dual-out mode)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line

Operational Notes – continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC

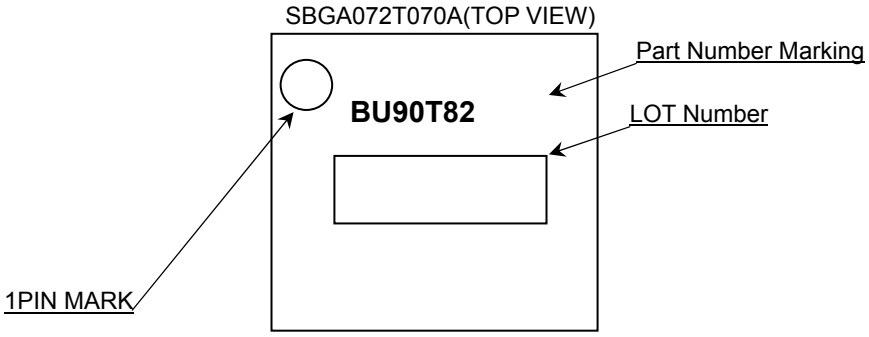
Ordering part number

B U 9 0 T 8 2 - E 2

Part No.

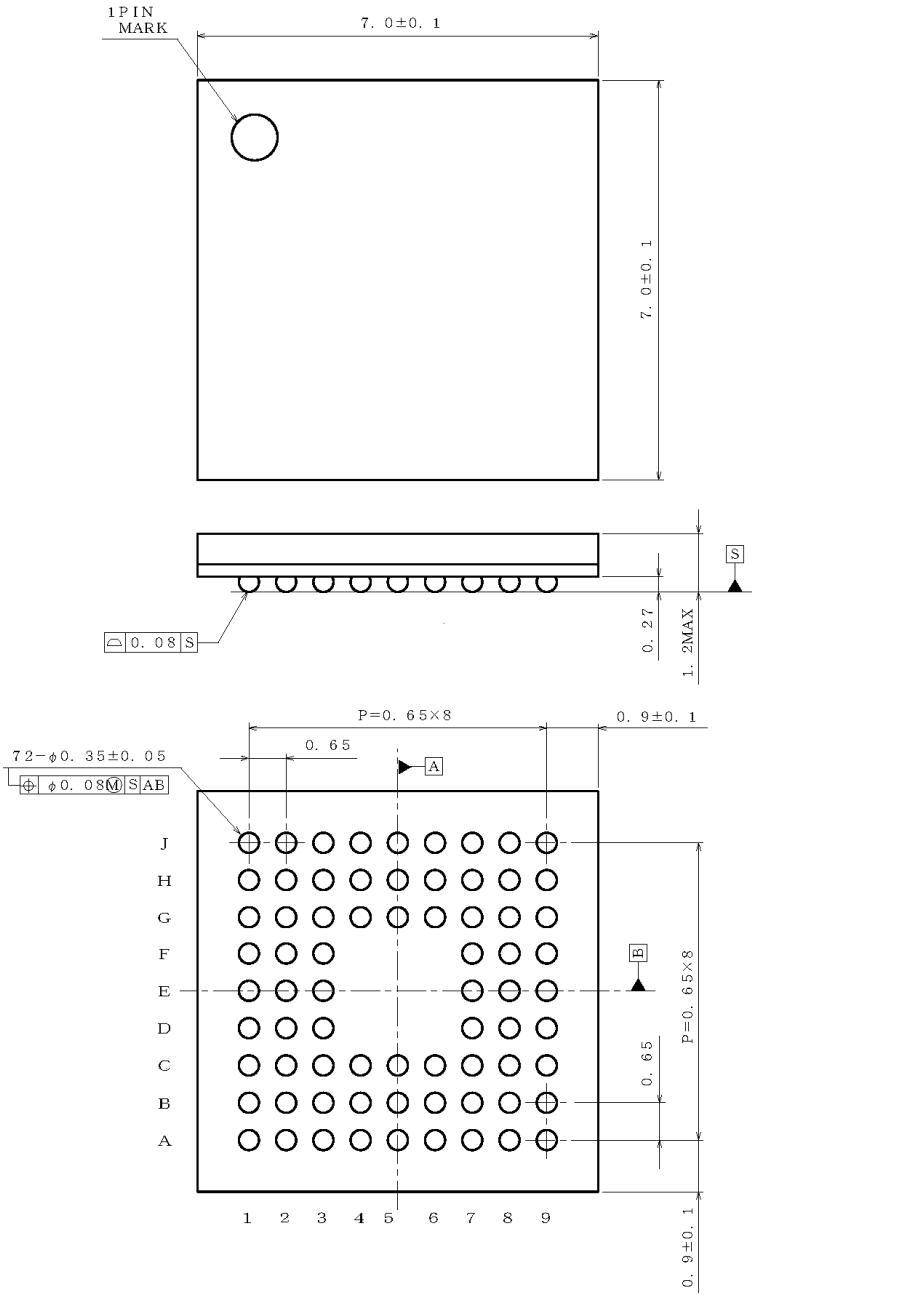
Packaging and forming specification
E2:Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	SBGA072T070A

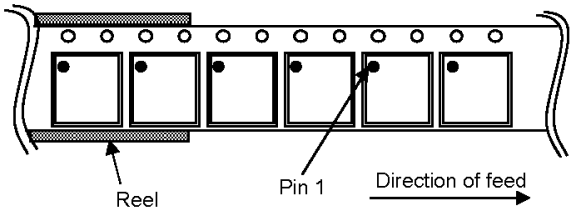


(UNIT : mm)

PKG : SBGA072T070A
Drawing No. EX001−0037

< Tape and Reel Information >

Tape	Embossed carrier tape with dry pack
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
30.Jul.2014	001	New Release
23.Mar.2015	002	Page 2: Added Contents; Page 7: Modified CLKIN to TCLK+/- Delay Time
06.Jul.2016	003	Page 6: Change supply voltage, size of mounting PCB in absolute maximum ratings Add spec of pull-down resistor Page 7: Change t_{TCP} to t_{TCOP} in Table 3. CLKIN to TCLK+/- Delay, output data position. Page 8: Modify RF setting in Figure 4, 5 Page 17-20: Figure 18,19,20,21. Modify Application Circuit Page 24: Modify BGA ball assign in physical dimension

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View BU90T82-ZE2 on WIN SOURCE
- Rohm Semiconductor Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management