



**THE DATASHEET OF
BGA7L1BN6E6327XTSA1**



BGA7L1BN6

Silicon Germanium Low Noise Amplifier for LTE

Data Sheet

Revision 3.1, 2017-03-03

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Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 3.1, 2017-03-03	
all	Initial final version

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Features

- Insertion power gain: 13.6 dB
- Low noise figure: 0.75 dB
- Low current consumption: 4.9 mA
- Insertion Loss in bypass mode: -2.2 dB
- Operating frequencies: 716 - 960 MHz
- Two-state control: Bypass- and High gain-Mode
- Supply voltage: 1.5 V to 3.6 V
- Digital on/off switch (1V logic high level)
- Ultra small TSNP-6-2 leadless package (footprint: 0.7 x 1.1 mm²)
- B7HF Silicon Germanium technology
- RF output internally matched to 50 Ω
- Only 1 external SMD component necessary
- Pb-free (RoHS compliant) package



Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

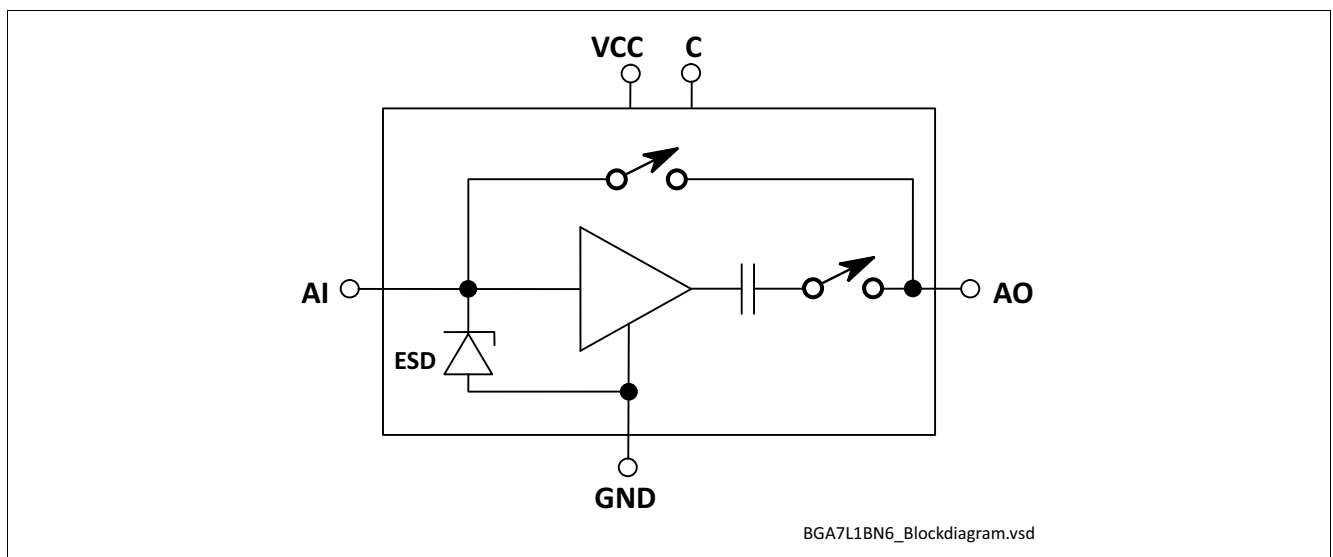


Figure 1 Block Diagram

Product Name	Marking	Package
BGA7L1BN6	K	TSNP-6-2

Description

The BGA7L1BN6 is a front-end low noise amplifier for LTE which covers a wide frequency range from 716 MHz to 960 MHz. The LNA provides 13.6 dB gain and 0.75 dB noise figure at a current consumption of 4.9 mA in the application configuration described in [Chapter 3](#). In bypass mode the LNA provides an insertion loss of -2.2dB. The BGA7L1BN6 is based upon Infineon Technologies' B7HF Silicon Germanium technology. It operates from 1.5 V to 3.6 V supply voltage. The device features a single-line two-state control (Bypass- and High gain-Mode). OFF-state can be enabled by powering down Vcc.

Pin Definition and Function**Table 1 Pin Definition and Function**

Pin No.	Name	Function
1	GND	Ground
2	VCC	DC supply
3	AO	LNA output
4	GND	Ground
5	AI	LNA input
6	C	Control

1 Maximum Ratings

Table 2 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	V_{CC}	-0.3	–	5.0	V	1)
Voltage at pin AI	V_{AI}	-0.3	–	0.9	V	–
Voltage at pin AO	V_{AO}	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin C	V_C	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at GND pins	V_{GND}	-0.3	–	0.3	V	–
Current into pin VCC	I_{CC}	–	–	50	mA	–
RF input power	P_{IN}	–	–	+25	dBm	–
Total power dissipation, $T_S < 148\text{ °C}^2)$	P_{tot}	–	–	250	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-65	–	150	°C	–

1) All voltages refer to GND-Node unless otherwise noted

2) T_S is measured on the ground lead at the soldering point

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 Electrical Characteristics

Table 3 Electrical Characteristics:¹⁾ $T_A = 25\text{ °C}$, $V_{CC} = 2.8\text{ V}$, $V_{C,ON} = 2.8\text{ V}$, $V_{C,BYP} = 0\text{ V}$, $f = 716 - 960\text{ MHz}$

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	–	3.6	V	–
Supply current	I_{CC}	–	4.9	5.9	mA	High gain mode
		–	87	120	μA	Bypass mode
		–	110	150	μA	Bypass mode / $V_{CC} = 5.0\text{ V}$
Control voltage	V_C	1.0	–	V_{CC}	V	High gain mode
		0	–	0.4	V	Bypass mode
Insertion power gain $f = 840\text{ MHz}$	$ S_{21} ^2$	12.1	13.6	15.1	dB	High gain mode
		-3.2	-2.2	-1.2	dB	Bypass mode
Noise figure ²⁾ $Z_S = 50\ \Omega$	NF	–	0.75	1.3	dB	High gain mode
		–	1.8	2.8	dB	Bypass mode
Input return loss $f = 840\text{ MHz}$	RL_{in}	9	12	–	dB	High gain mode
		6	9	–	dB	Bypass mode
Output return loss $f = 840\text{ MHz}$	RL_{out}	10	13	–	dB	High gain mode
		5	8	–	dB	Bypass mode
Reverse isolation	$1/ S_{12} ^2$	17	21	–	dB	High gain mode
		-3.2	-2.2	–	dB	Bypass mode
Power gain settling time ³⁾	t_S	–	3	6	μs	Bypass- to HG-mode
		–	0.2	0.3	μs	HG- to Bypass-mode
Inband input 1dB-compression point, $f = 840\text{ MHz}$	IP_{1dB}	-3	-1	–	dBm	High gain mode
		+2	+6	–	dBm	Bypass mode
Inband input 3 rd -order intercept point ⁴⁾ $f_1 = 840\text{ MHz}$, $f_2 = f_1 + 1\text{ MHz}$	IIP_3	0	+5	–	dBm	High gain mode
		+13	+18	–	dBm	Bypass mode
Phase shift	PS	-5	0	5	°	High gain mode and bypass mode
Stability	k	> 1	–	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in chapter 3

2) PCB losses are subtracted

3) To be within 1 dB of the final gain

4) High gain mode: Input power = -30 dBm for each tone / Bypass mode: Input power = -10 dBm for each tone

3 Application Information

Application Board Configuration

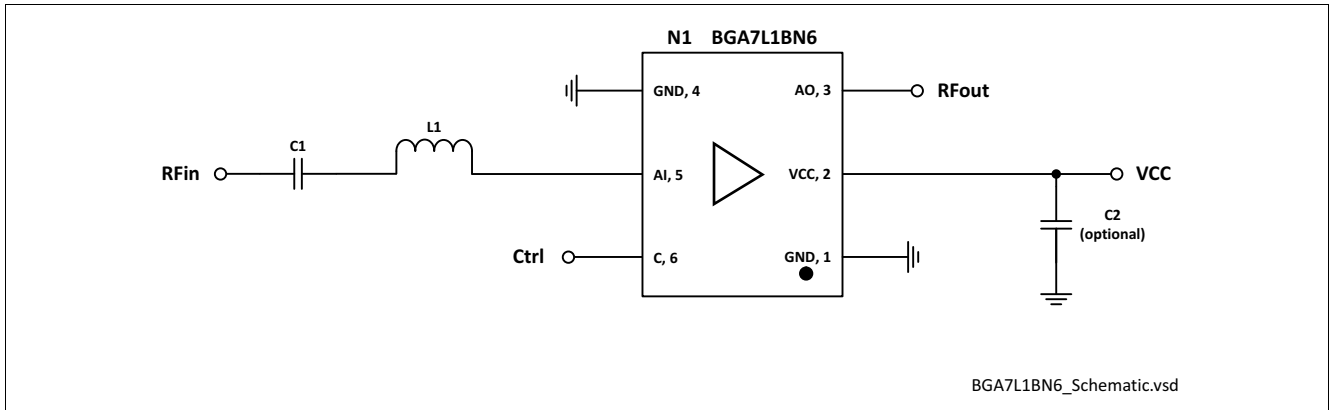


Figure 2 Application Schematic BGA7L1BN6

Table 4 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1	1nF	0402	Various	DC block ¹⁾
C2 (optional)	≥ 1nF	0402	Various	RF bypass ²⁾
L1	11nH	0402	Murata LQW type	Input matching
N1	BGA7L1BN6	TSNP-6-2	Infineon	SiGe LNA

1) DC block might be necessary due to internal LNA bias voltage @ AI (LNA Analog Input pin). The DC block can be realized with pre-filter (e.g. SAW)

2) RF bypass recommended to mitigate power supply noise

Note: No external DC blocking capacitor at RFout is required in typical applications as long as no DC is applied.

A list of all application notes is available at <http://www.infineon.com/ltelna>

4 Package Information

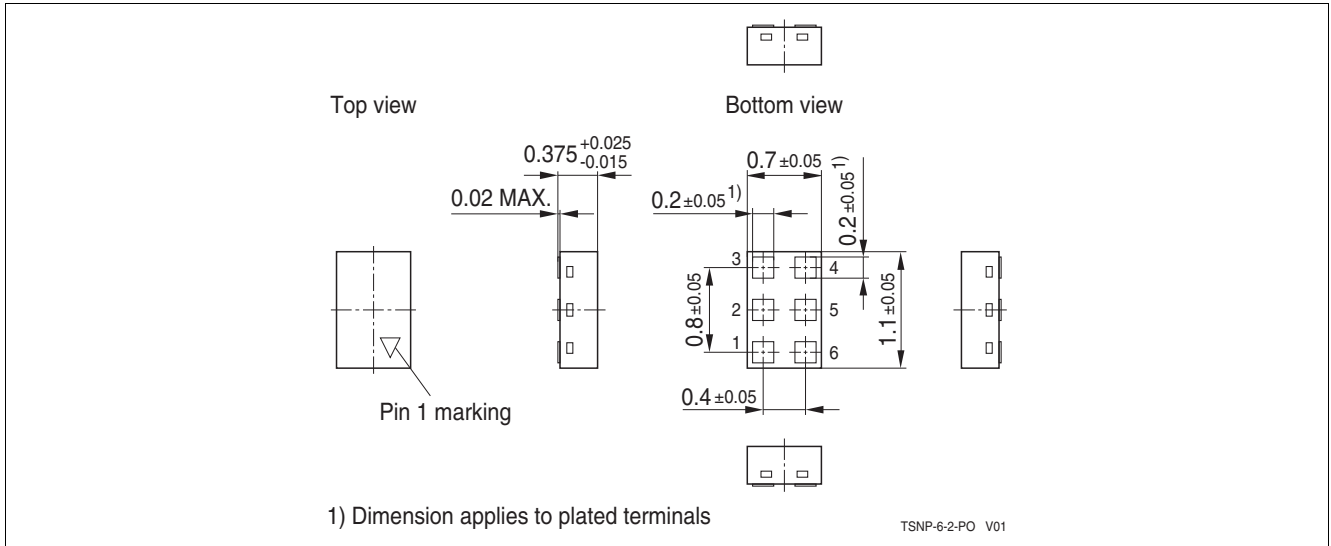


Figure 3 TSNP-6-2 Package Outline (top, side and bottom views)

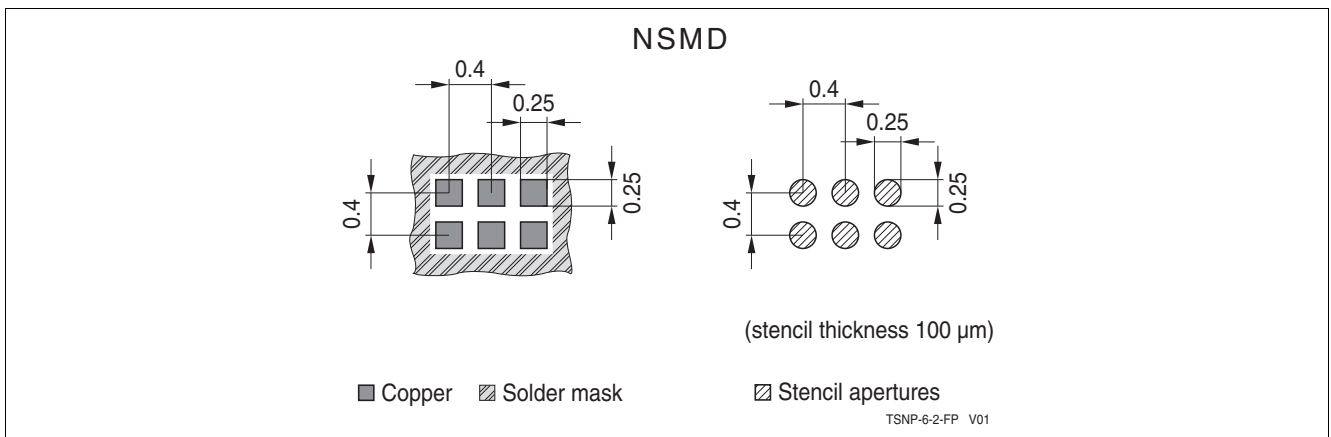


Figure 4 Footprint Recommendation TSNP-6-2

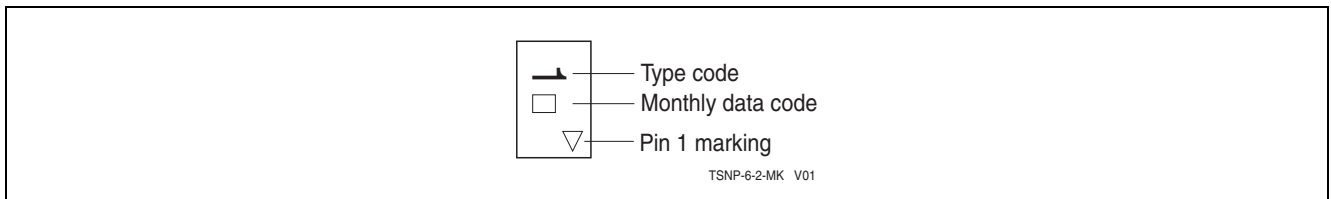


Figure 5 Marking Layout (top view)

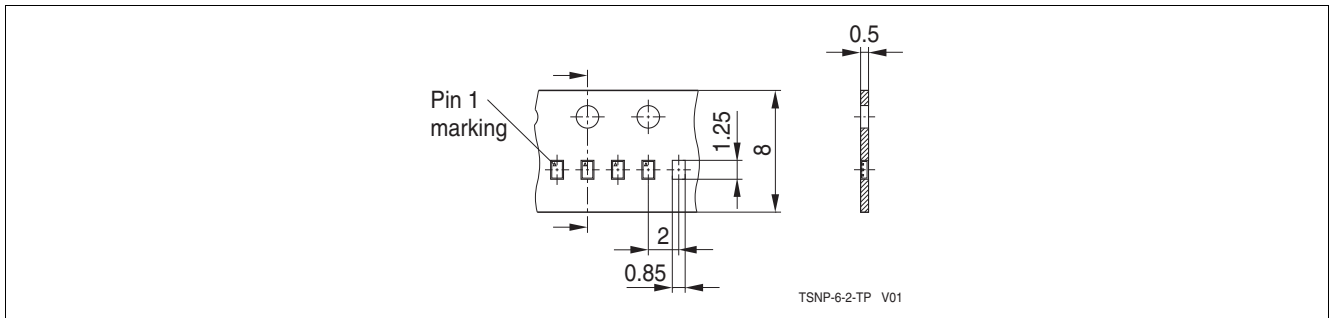




Figure 6 Tape & Reel Dimensions (reel diameter 180 mm, pieces/reel 15000)

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