



**THE DATASHEET OF
ATA8520E-GHPW**



Single-Chip SIGFOX RF Transceiver

DATASHEET COMPLETE

Features

- Fully integrated, single-chip RF transceiver (SIGFOX™ compliant)
- System-on-chip solution including SIGFOX related protocol handling for modem operation
- AVR® microcontroller core with embedded firmware, SIGFOX, protocol stack and ID/PAC
- Supports up- and downlink operation, i.e., transmit and receive of data telegrams with SIGFOX base stations in EU and US
- The device has to be configured before the first usage
- Operating frequencies:
 - EU: uplink 868.0MHz to 868.6MHz, downlink 869.4MHz to 869.65MHz
 - US: uplink and downlink 902MHz to 906MHz
- Low current consumption:
 - 32.7mA (EU) / 16.7mA(US) during transmit and
 - 10.4mA (EU) / 10.5mA (US) during receive operation
- Typical OFF mode current: 5nA (maximum 600nA at $V_S = +3.6V$ and $T = +85^{\circ}C$)
- Data rate:
 - EU: 100bit/s with DBPSK modulation for uplink and 600bit/s with GFSK modulation for downlink
 - US: 600bit/s with DBPSK modulation for uplink and 600bit/s with GFSK modulation for downlink
- SPI interface for data access and transceiver configuration and control
- Event signal indicates the status of the IC to an external microcontroller
- Power-up (typical 10ms (EU), 30ms (US) from OFF mode to idle mode)
- Supply voltage ranges 1.9V to 3.6V and 2.4V to 5.5V (SIGFOX compliant supply range $3V \pm 5\%$ and 3.3V to 5.5V)
- Temperature range $-40^{\circ}C$ to $+85^{\circ}C$
- ESD protection at all pins ($\pm 4kV$ HBM, $\pm 200V$ MM, $\pm 750V$ FCDM)
- Small 5×5mm QFN32 package/pitch 0.5mm

Applications

SIGFOX™ compatible modem for long-range, low-power and low-cost applications using the SIGFOX network

- Home and building automation
- Alarm and security systems
- Smart environment and industrial
- Smart parking
- Tracking
- Metering

Table of Contents

| | |
|---|----|
| Features..... | 1 |
| Applications..... | 2 |
| 1. General Description..... | 4 |
| 1.1. Introduction..... | 4 |
| 1.2. System Overview..... | 4 |
| 1.3. Pinning..... | 5 |
| 1.4. Applications..... | 7 |
| 2. System Functional Description..... | 10 |
| 2.1. SPI Command Interface..... | 10 |
| 2.2. Operating Modes Overview..... | 23 |
| 3. Electrical Characteristics..... | 26 |
| 3.1. ESD Protection Circuits..... | 26 |
| 3.2. Absolute Maximum Ratings..... | 27 |
| 3.3. Thermal Resistance..... | 27 |
| 3.4. Supply Voltages and Current Consumption..... | 28 |
| 3.5. RF Receive Characteristics..... | 29 |
| 3.6. RF Transmit Characteristics..... | 30 |
| 3.7. RF Transmit Characteristics..... | 31 |
| 3.8. I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5..... | 32 |
| 3.9. Hardware Timings..... | 33 |
| 3.10. Hardware SPI Timing Characteristics..... | 33 |
| 4. Ordering and Package Information..... | 35 |
| 5. Disclaimer..... | 36 |
| 6. Revision History..... | 37 |

1. General Description

1.1. Introduction

The Atmel® ATA8520E is a highly integrated, low-power RF transceiver with an integrated AVR® microcontroller for applications using the wide area SIGFOX™ network

The Atmel ATA8520E is partitioned into three sections: an RF front end, a digital baseband and the low-power 8-bit AVR microcontroller. The product is designed for the EU ISM frequency band in the range of 868.0MHz to 868.6MHz and 869.4MHz to 869.65MHz and for the US ISM frequency band in the range of 902.0MHz to 906.0MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The transmit path uses a closed loop fractional-N modulator.

The SPI interface enables external control and device configuration.

1.2. System Overview

Figure 1-1. Circuit Overview

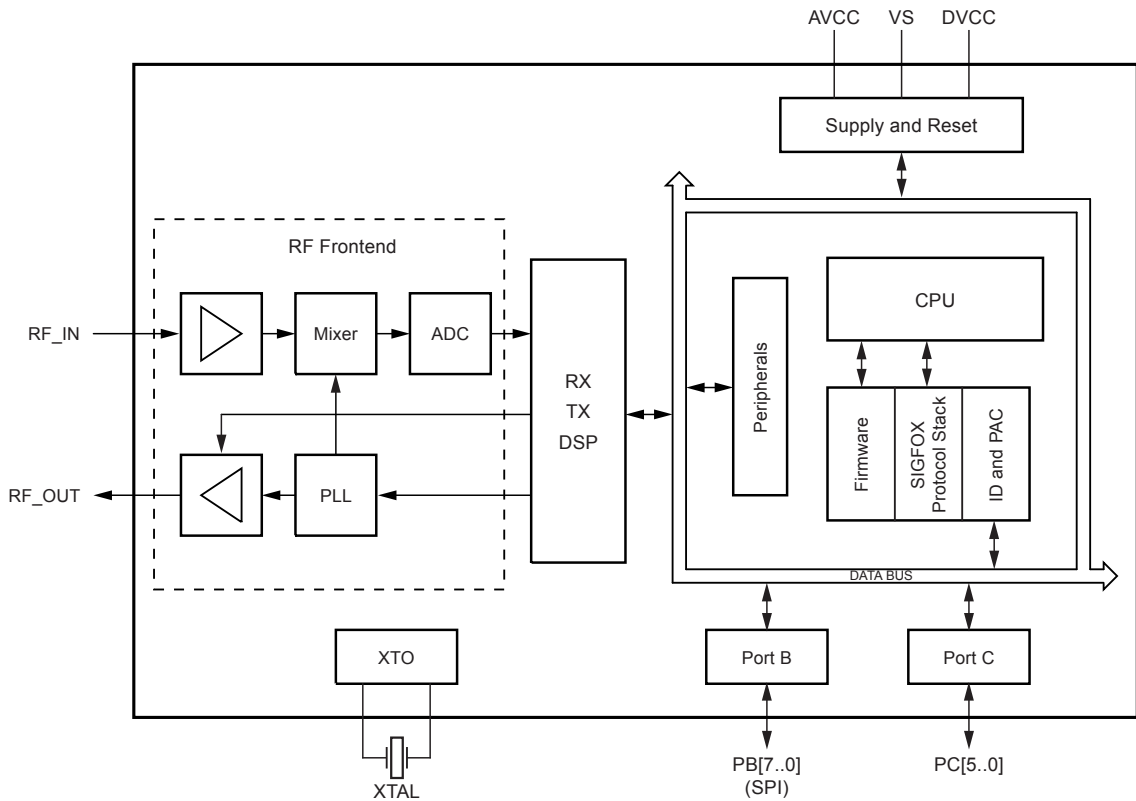


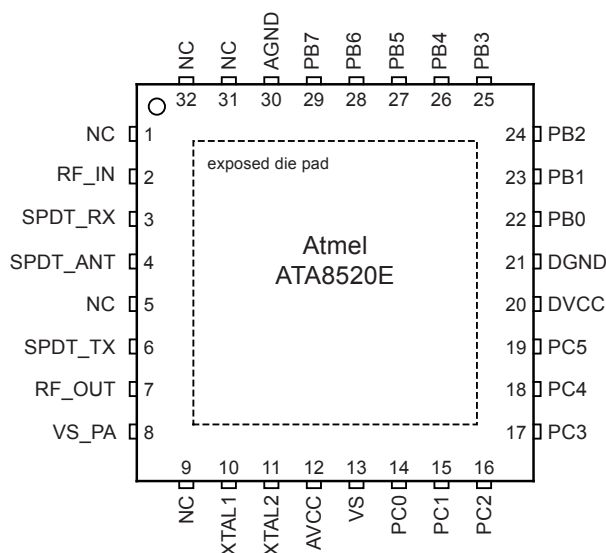
Figure 1-1 shows an overview of the main functional blocks of the Atmel® ATA8520E. External control of the Atmel ATA8520E is performed through the SPI pins SCK, MOSI, MISO, and NSS. The functionality of the device is defined by the internal firmware and processed by the AVR®. SPI commands are used to control the device and to start the data telegram transmission. The end of the telegram transmission is signaled to an external microcontroller on pin 28 (PB6/EVENT).

It is important to note that all PWRON and NPWRON pins (PC1..5, PB4, PB7) are active in OFF mode. This means that even if the Atmel ATA8520E is in OFF mode and the DVCC voltage is switched off, the power management circuitry within the Atmel ATA8520E biases these pins with VS.

The AVR microcontroller ports can be used as button inputs, LED drivers, EVENT pin, general purpose digital inputs, or wake-up inputs, etc. Functionality of these ports is already implemented in the firmware.

1.3. Pinning

Figure 1-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-1. Pin Description

| Pin No. | Pin Name | Type | Description |
|---------|----------|--------|---|
| 1 | NC | – | Connected to GND |
| 2 | RF_IN | Analog | Receiver input |
| 3 | SPDT_RX | Analog | Rx switch output (damped signal output) |
| 4 | SPDT_ANT | Analog | Antenna input (downlink) and output (uplink) of the SPDT switch |
| 5 | NC | | Leave open |
| 6 | SPDT_TX | Analog | TX mode input of the SPDT switch |
| 7 | RF_OUT | Analog | Power amplifier output |
| 8 | VS_PA | Analog | Power amplifier supply. 3V supply: connect to VS. 5V supply: connect to C2. Use SPI command “Write System Configuration” (0x11) to enable 5V supply mode. |
| 9 | NC | – | Connected to GND |
| 10 | XTAL1 | Analog | Crystal oscillator pin 1 (input) |

| Pin No. | Pin Name | Type | Description |
|---------|----------|---------|---|
| 11 | XTAL2 | Analog | Crystal oscillator pin 2 (output) |
| 12 | AVCC | Analog | RF front-end supply regulator output |
| 13 | VS | Analog | Main supply voltage input |
| 14 | PC0 | Digital | Main : NRESET (low active) |
| 15 | PC1 | Digital | Main : AVR Port C1 Alternate : NPWRON1 (low active) |
| 16 | PC2 | Digital | Main : AVR Port C2 Alternate : NPWRON2 (low active) |
| 17 | PC3 | Digital | Main : AVR Port C3 Alternate : NPWRON3 (low active) |
| 18 | PC4 | Digital | Main : AVR Port C4 Alternate : NPWRON4 (low active) |
| 19 | PC5 | Digital | Main : AVR Port C5 Alternate : NPWRON5 (low active) |
| 20 | DVCC | – | Digital supply voltage regulator output |
| 21 | DGND | – | Digital ground |
| 22 | PB0 | Digital | Main : control front-end module; ='1' enable, ='0' disable |
| 23 | PB1 | Digital | Main : SCK |
| 24 | PB2 | Digital | Main : MOSI (SPI master out Slave in) |
| 25 | PB3 | Digital | Main : MISO (SPI master in Slave out) |
| 26 | PB4 | Digital | Main : PWRON |
| 27 | PB5 | Digital | Main : NSS (low active) |
| 28 | PB6 | Digital | Main : EVENT (low active) |
| 29 | PB7 | Digital | Main : ='1' TX active, ='0' RX active Alternate : NPWRON6 (low active) |
| 30 | AGND | – | Analog ground |
| 31 | NC | – | Connected to GND |
| 32 | NC | – | Connected to GND |
| | GND | – | Ground/backplane on exposed die pad |

1.4. Applications

This section provides application examples for the two supply modes for the Atmel® ATA8520E device.

1.4.1. 3V Application Example

Figure 1-3. 3V Application with External Microcontroller

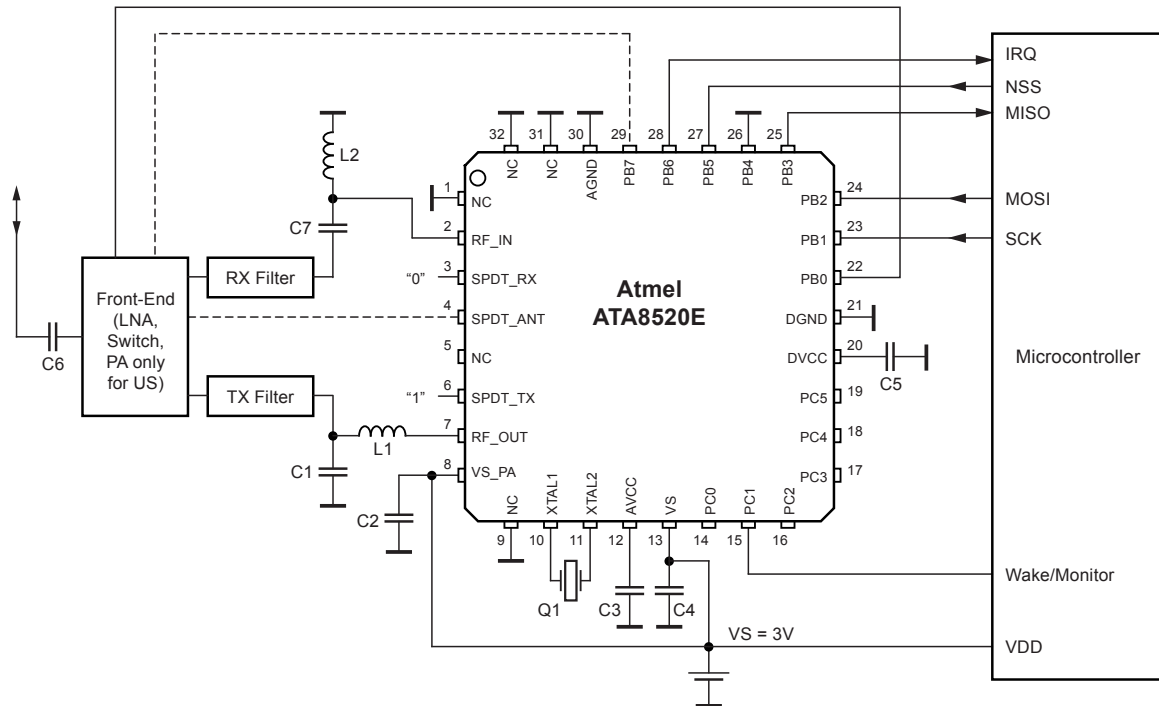


Figure 1-3 shows a typical application circuit with an external host microcontroller operating from a 3V battery. The Atmel® ATA8520E stays in OFFMode until NPWRON1 (PC1) is used to wake it up. In OFFMode the Atmel ATA8520E draws typically less than 5nA at 25°C.

In OFFMode all Atmel ATA8520E AVR® ports PB0..PB7 and PC0..PC5 are switched to input. PC0..PC5 and PB7 have internal pull-up resistors ensuring that the voltage at these ports is VS. PB0..PB6 are tri-state inputs and require additional consideration. PB1, PB2, and PB5 have defined voltages since they are connected to the output of the external microcontroller. PB4 is connected to ground to avoid unwanted power-ups. PB0, PB3 and PB6 do not require external circuitry since the internal circuit avoids transverse currents in OFFMode. The external microcontroller has to tolerate the floating inputs. Otherwise additional pull-down resistors are required on these floating lines.

Typically, the Atmel ATA8520E wake-up is done by pulling NPWRON1 (pin 15) to ground.

RF_OUT is matched with C1/L1 for 50Ω antenna connection and RF_IN with the components C7/L2. The front-end module (FEM) typically includes an antenna switch, an LNA for the receive direction and an optional PA for the transmit connection in one device. The RX and TX filters are additional to increase out-of-band jamming immunity in receive direction and to reduce spurious emissions in transmit direction. For these filters SAW components are typically used. The pins PB0 and PB7 can be used to control the FEM or the unused internal SPDT switch which is controlled by the Atmel ATA8520E for transmit and receive operation.

Together with the fractional-N PLL within the Atmel ATA8520E, an external crystal is used to set the Tx and Rx frequency. Accurate load capacitors for this crystal are integrated to reduce the system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS, and VS_PA of the Atmel ATA8520E. The exposed die pad is the RF and analog ground of the Atmel ATA8520E. It is connected directly to AGND via a fused lead. The Atmel ATA8520E is controlled using specific SPI commands via the SPI interface.

1.4.2. 5V Application Example

Figure 1-4. 5V Application with External Microcontroller

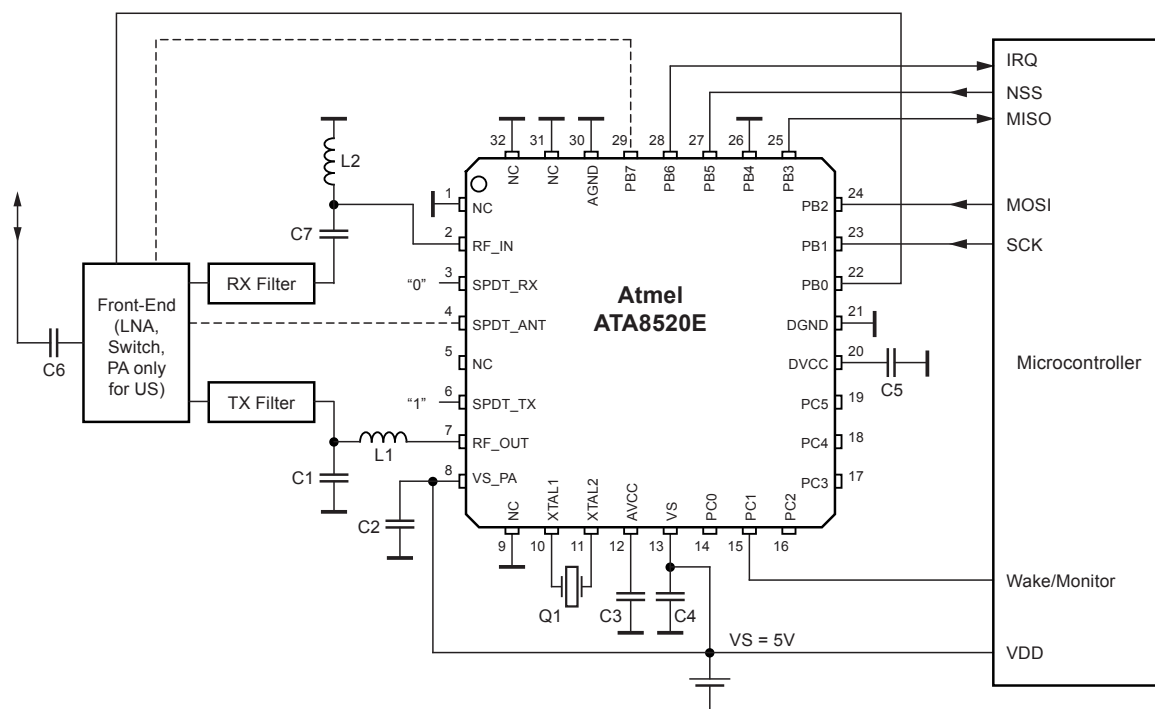


Figure 1-4 shows a typical application circuit with an external host microcontroller operating from a 5V supply. This application differs from the 3V supply mode that VS is not connected to VS_PA. Instead an internal LDO must be activated using the SPI command “Write System Configuration” (0x11) after powering the device and before transmitting a data telegram.

The front-end module (FEM) is controlled by the Atmel[®] ATA8520E device using the port pins PB7 and PB0 as described in section [System and Pin Configuration](#) (Table 2-7): In addition there is an internal switch which can be used to control the direction of the FEM. As shown in [Figure 1-3](#) and [Figure 1-4](#) the pins SPDT_RX, SPDT_TX and SPDT_ANT can be used by applying logical levels “0” and “1” to the pins. Please consider that the voltage levels at these pins are restricted as defined in section [Absolute Maximum Ratings](#) and section [Supply Voltages and Current Consumption](#).

1.4.3. 5V Application for Uplink only
Figure 1-5. 5V Application for Uplink only

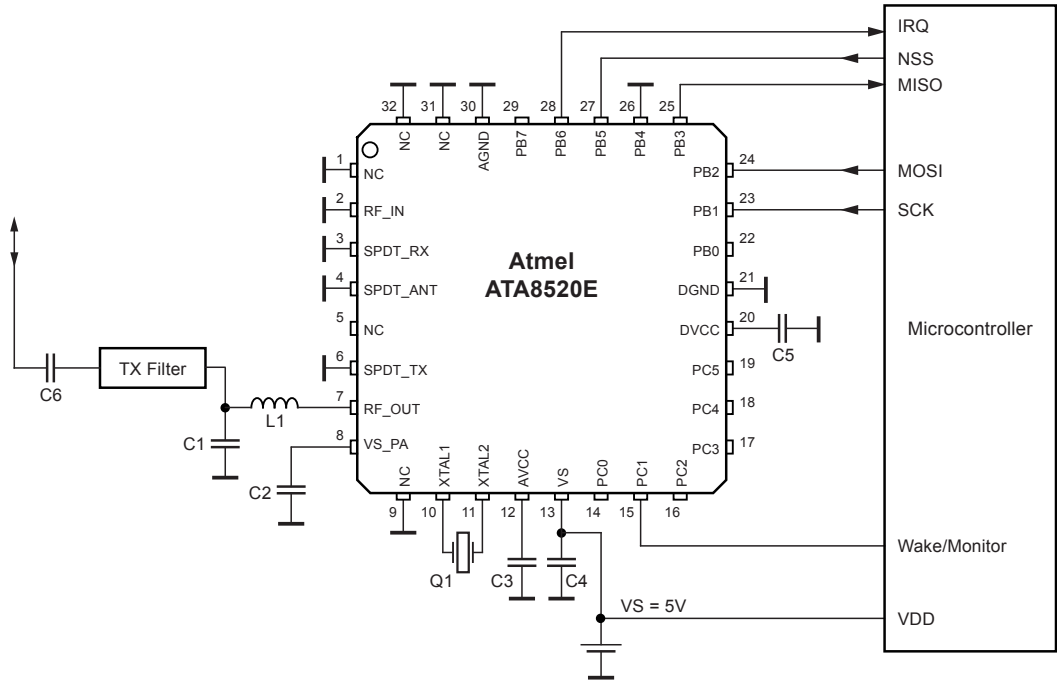


Figure 1-5 shows a 5V application with external microcontroller for uplink only. The downlink (receiving) part is not used together with the front-end module and the RX filter. For the TX filter an SAW filter can be used or a simple LC filter to suppress unwanted spurious and harmonic emissions.

2. System Functional Description

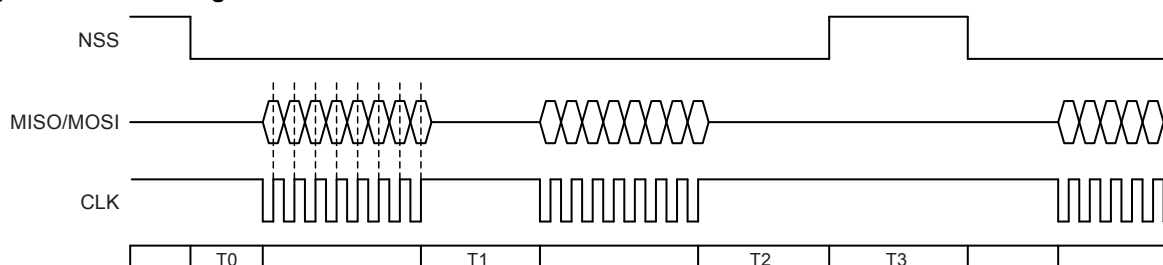
2.1. SPI Command Interface

The SPI command interface requires a timing setup as described in the following section and provides a set of commands to control the operation of the Atmel® ATA8520E device. The SPI transmission occurs with MSB first.

2.1.1. SPI Timing

The SPI communication requires a special timing to prevent data corruption. The SPI peripheral uses a SCK frequency of up to 125kHz for the bit transmission and requires timing delays between the CS signals and the start and stop of the SPI communication as shown in Figure 2-1.

Figure 2-1. SPI Timing Parameters



$T_0 \geq 65\mu\text{s}$, $T_1 \geq 40\mu\text{s}$, $T_2 \geq 100\mu\text{s}$, $T_3 \geq 50\mu\text{s}$, SPI CLK $\leq 125\text{kHz}$ (SPI Mode 0: CPOL = CPHA = 0)

2.1.2. SPI Command Set

The following SPI commands are available to control the Atmel® ATA8520E operation from a host microcontroller.

2.1.2.1. System Reset

This command uses the system internal WDT to do a complete hardware reset of the Atmel® ATA8520E. Resetting the device takes approximately 12ms (EU), 31ms (US). Afterwards the system restarts and generates an event on the EVENT signal after this time. This event will be cleared with the “Get Status” SPI command (0x0A).

| | | |
|----------|--|---------------------|
| Master | | System Reset (0x01) |
| ATA8520E | | Dummy |

2.1.2.2. I/O Init

The I/O lines of port C can be used as additional I/O lines for an application. The port C I/O Init command defines the internal data direction register of output port PORTC (DDRC). Pin PC0 is used as NRESET signal and will always be an input pin, i.e., bit 0 will be written as 0 to be an input pin.

| | | | |
|----------|--|-----------------|--------------|
| Master | | I/O Init (0x02) | DDRC content |
| ATA8520E | | Dummy | Dummy |

2.1.2.3. I/O Write

The I/O write command writes directly to the output port register PORTC to set the I/O pins. Pin PC0 is used as NRESET signal and will always be an input pin with enabled pull-up, i.e., bit 0 will be written as 1 to enable the internal pull-up resistor.

| | | | |
|----------|--|-----------------|---------------|
| Master | | I/O Init (0x03) | PORTC content |
| ATA8520E | | Dummy | Dummy |

2.1.2.4. I/O Read

The I/O read command reads the status of the I/O pins directly from the input port register PINC. Pin PC0 is used as NRESET signal and will always be read as 1.

| | | | | |
|----------|--|-----------------|-------|--------------|
| Master | | I/O Read (0x04) | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | PINC content |

2.1.2.5. OFF Mode

The OFF mode command puts the Atmel® ATA8520E into off mode. To wake up the Atmel ATA8520E device, one of the power on lines has to be activated, i.e., set PWRON line to high or NPWRONx line to low. To switch the device into OFF mode the power on lines have to be de-activated before otherwise the device will remain in the on state.

| | | |
|----------|--|-----------------|
| Master | | OFF Mode (0x05) |
| ATA8520E | | Dummy |

2.1.2.6. Atmel Version

The Atmel® version command reads the version information including a major and a minor version number.

| | | | | | |
|----------|--|----------------------|-------|-----------|-----------|
| Master | | Atmel Version (0x06) | Dummy | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | MajorVers | MinorVers |

2.1.2.7. Write TX Buffer

The write TX buffer command fills the TX buffer to be sent with the next SIGFOX™ ATA8520E data frame with payload data of up to 12 bytes. The buffer can hold any number of bytes ranging from 0 to 12 bytes and are not buffered, i.e., a new SPI command will override the previous data.

| | | | | | | |
|----------|--|------------------------|-----------------|---------------|-------|-------------------|
| Master | | Write TX Buffer (0x07) | RF TX Num bytes | RF TX Bytes 0 | | RF TX Num bytes-1 |
| ATA8520E | | Dummy | Dummy | Dummy | | Dummy |

2.1.2.8. Enable Special Mode

This command will only be used during testing of the system and not during regular operation in a SIGFOX™ network. This commands enables the execution of the following SPI command:

- Firmware tests 0x18

| | | |
|----------|--|--------------------|
| Master | | Enable Mode (0x08) |
| ATA8520E | | Dummy |

2.1.2.9. SIGFOX Version

The SIGFOX™ version reads the SIGFOX library version information as a text string with N = 11 characters.

| | | | | | | |
|----------|--|--------------------------|-------|-------------------|-------|-------------------|
| Master | | SIGFOX Version (0x09) | Dummy | Dummy | | Dummy |
| ATA8520E | | Dummy | Dummy | SFX Verinfo[0] | | SFX Verinfo[N] |

2.1.2.10. Get Status

The get status command reads the internal status of the device. Issuing this command clears the systems event line (PB6) and the status bytes. The event line is set to low when:

- System is ready after power-up or reset
- Finishes the transmit/receive operation
- Finishes a temperature and supply measurement
- Finishes the EEPROM write operation.
- Test mode is finished.

The following status information is read after the event line is activated, i.e., polling using the Get Status command is not necessary:

Hardware SSM status (internal only)

Atmel® status:

- Bit6: System ready to operate (system ready event)
- Bit5: Frame sent (frame ready event)
- Bit4 to Bit1: Error code
 - 0000: no error
 - 0001: command error / not supported
 - 0010: generic error
 - 0011: frequency error
 - 0100: usage error
 - 0101: opening error
 - 0110: closing error
 - 0111: send error
- Bit0: PA on/off indication

SIGFOX™ status:

- 0x00: no error
- 0x30: TX data length > 12 byte
- 0x3E: Time-out for downlink message
- 0x4E: Time-out for bit downlink
- All other codes: Only for internal

SIGFOX status2:

- 0x00: no error
- 0x10: initialization error
- 0x18: error during send
- 0x40: error in RF frequency
- 0x68: error during wait for data frame

The SSM status is used for internal testing only. The SIGFOX status/status2 information may also generate other error codes which are used for internal only. The Atmel status information can be used for detection of issues with the application, i.e., bit6 is set after initialization of the device (reset or power-on) and bit5 is set after a telegram has been sent.

| | | | | | | | |
|----------|--|-------------------|-------|------------|--------------|---------------|----------------|
| Master | | Get Status (0x0A) | Dummy | Dummy | Dummy | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | SSM status | Atmel status | SIGFOX status | SIGFOX status2 |

2.1.2.11. Send Single Bit

This command sends a data bit (0=0x00/1=0x01) within a SIGFOX™ RF frame as specified by SIGFOX. An event on the EVENT signal is generated when finished. This command will only be used during testing of the system and not during regular operation in a SIGFOX network.

| | | | |
|----------|--|-----------------|------------------|
| Master | | Send Bit (0x0B) | Bit Status (0/1) |
| ATA8520E | | Dummy | Dummy |

2.1.2.12. Send Out-Of-Band

This command triggers the out-of-band data transmission (as defined by SIGFOX™). It will generate an event on the EVENT signal when finished. This command will only be used during testing of the system and not during regular operation in a SIGFOX network.

| | | |
|----------|--|-----------------|
| Master | | Send OOB (0x0c) |
| ATA8520E | | Dummy |

2.1.2.13. Send Frame

The send frame command triggers the start of a frame transmit process. The payload data has to be written into the TX buffer before using the write TX buffer command. The transmit operation will take ~7 seconds in EU mode and ~2 seconds in US mode and will generate an event on the EVENT signal when finished.

| | | |
|----------|--|-------------------|
| Master | | Send Frame (0x0D) |
| ATA8520E | | Dummy |

2.1.2.14. Send/Receive Frame

The send/receive frame command triggers the start of a frame transmit process followed by a receive process. The payload data has to be written into the TX buffer before using the write TX buffer command. The transmit and receive operation will take up to 50 seconds and will generate an event on the EVENT signal when finished. The received data bytes can be read with the SPI command (0x10).

| | | |
|----------|--|---------------------------|
| Master | | Send/Receive Frame (0x0E) |
| ATA8520E | | Dummy |

2.1.2.15. Get PAC

The get PAC command will read the 16 byte PAC information which is used for the device registration process at the SIGFOX™ backend. Only the 8 lower bytes (0) .. (7) are used.

| | | | | | | |
|----------|--|----------------|-------|-----------|-------|------------|
| Master | | Get PAC (0x0F) | Dummy | Dummy | | Dummy |
| ATA8520E | | Dummy | Dummy | PAC ID[0] | | PAC ID[15] |

2.1.2.16. Read RX Buffer

This command triggers the read out of the received data packet. The packet length is always 8 bytes.

| | | | | | | |
|----------|--|-----------------------|-------|-----------|-------|-----------|
| Master | | Read RX Buffer (0x10) | Dummy | Dummy | | Dummy |
| ATA8520E | | Dummy | Dummy | RX Byte 0 | | RX Byte 7 |

2.1.2.17. Store System Configuration

The Store System Configuration command writes the configuration data for the port C and the system configuration into the internal EEPROM. This changes will be applied by performing a system reset. An event on the EVENT signal is generated when finished. EDDRC register defines the data direction for the port C pins (0: input, 1: output). EPORTC register defines the output level for an output pin and enables a pull-up resistor for input pins when set. SysConf is used to configure the supply voltage and the up-/downlink operation (see section [System and Pin Configuration](#)). The parameter repeat defines the number of frames to be send for the SPI command Send/Receive Frame (0x0E). Possible values for the parameter repeat are

- 0x00: send 1 frame
- 0x01: send 2 frame
- 0x02: send 3 frame (default)

| | | | | | | |
|----------|--|-----------------------|-------|--------|--------|---------|
| Master | | Store Sys Conf (0x11) | EDDRC | EPORTC | repeat | SysConf |
| ATA8520E | | Dummy | Dummy | Dummy | Dummy | Dummy |

2.1.2.18. Get ID

The get ID command will read the 4 byte ID information which is used for the device registration process at the SIGFOX™ backend.

| | | | | | | |
|----------|--|---------------|-------|--------|-------|--------|
| Master | | Get ID (0x12) | Dummy | Dummy | | Dummy |
| ATA8520E | | Dummy | Dummy | UID[3] | | UID[0] |

2.1.2.19. Read Supply Temperature

This command triggers the read out of the measured supply voltage in idle and active mode and the device temperature. To trigger a measurement the SPI command (0x14) has to be used. The return voltage level is in mV and the temperature value has to be calculated as $T = TM/10$ in °C. The voltage values are of type 16 bit unsigned integer (with high and low byte) while the temperature is a signed value.

| | | | | | | | | | |
|----------|--|--------------------------------|-------|---------|---------|-----------|-----------|-------|-------|
| Master | | Read Supply Temperature (0x13) | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | VL idle | VH idle | VL active | VH active | TML | TMH |

2.1.2.20. Start Measurement

This command triggers the measurement of the supply voltages and the temperature value. An event on the EVENT signal is triggered when finished which is cleared by reading the status with command 0x0A. Using this command will update the crystal calibration before any send command, i.e., it is recommended to adapt to changed ambient temperatures.

| | | |
|----------|--|----------------------------|
| Master | | Trigger Measurement (0x14) |
| ATA8520E | | Dummy |

2.1.2.21. Trigger Test Mode

This command triggers the uplink test procedure defined by SIGFOX™. An event on the EVENT signal is generated when finished. This command will only be used during testing of the system and not during regular operation in a SIGFOX network.

The command parameter are:

- TestMode: Test modes as defined by SIGFOX
- Configuration: configuration data for test modes as defined by SIGFOX

The following test modes are available:

Table 2-1. Trigger Test Modes

| Test Mode | Configuration | Description |
|-----------|---------------|--|
| 0 | repeat: 0-255 | Transmit random data frame without frequency hopping |
| 1 | repeat: 0-255 | Transmit 3 random data frames with frequency hopping |
| 2 | repeat: 0-255 | Test receive operation with SIGFOX tester |
| 3 | repeat: 0-255 | Test receive operation in pure GFSK mode |
| 4 | repeat: 0-255 | Test sensitivity with SIGFOX tester |

| | | | | |
|----------|--|--------------------------|-----------|---------------|
| Master | | Trigger Test Mode (0x15) | Test Mode | Configuration |
| ATA8520E | | Dummy | Dummy | Dummy |

2.1.2.22. Send CW

This command triggers the transmission of a continuous carrier on the programmed RF frequency as defined by SIGFOX™. This command will only be used during testing of the system and not during regular operation in a SIGFOX network.

| | | | |
|----------|--|----------------|------------------|
| Master | | Send CW (0x17) | On=0x11/Off=0x00 |
| ATA8520E | | Dummy | Dummy |

2.1.2.23. Firmware Test

This command selects the firmware internal RX test mode. An event on the EVENT signal is generated when finished. This command will only be used during testing of the system and not during regular operation in a SIGFOX™ network.

This test mode will check for a data packet on the RX frequency with 600bps data rate and 0.8kHz FSK modulation with the following pattern (in hex):

| | | |
|----------|----------|----------------------|
| Preamble | Frame ID | Data payload |
| AA AA | B2 27 | 31 32 33 34 35 36 37 |

It can be used to check the RX functionality and the sensitivity level of the hardware.

| | | | | | |
|----------|----------------------|-------|-------|-------|-------|
| Master | Firmware Test (0x18) | 0x06 | 0x09 | 0xFF | 0xFF |
| ATA8520E | Dummy | Dummy | Dummy | Dummy | Dummy |

2.1.2.24. Store Frequencies

This command store the RF frequencies for TX and RX in the internal EEPROM. The frequency values are 32-bit unsigned integer in [Hz]. An event on the EVENT signal is generated when finished. The system has to be reset to make the changes valid.

| | | | | | | | | | |
|----------|--------------------------|---------------|----------------|-----------------|-----------------|---------------|----------------|-----------------|-----------------|
| Master | Store Frequencies (0x1A) | freqTX [7..0] | freqTX [15..8] | freqTX [23..16] | freqTX [31..24] | freqRX [7..0] | freqRX [15..8] | freqRX [23..16] | freqRX [31..24] |
| ATA8520E | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy |

2.1.2.25. Set TX Frequency

Set TX center frequency temporarily for testing purposes. This settings are lost after reset or when switching the device off. The frequency value is an unsigned 32-bit integer within the range [868.000.000Hz to 868.600.000Hz] and default value 868.130.000Hz for EU. The range for US is [902.000.000Hz to 906.000.000Hz] with default 902.200.000Hz. This command will only be used during testing of the system and not during regular operation in a SIGFOX™ network.

| | | | | | |
|----------|---------------------|-----------|-----------|----------|---------|
| Master | TX Frequency (0x1B) | TX[31:24] | TX[23:16] | TX[15:8] | TX[7:0] |
| ATA8520E | Dummy | Dummy | Dummy | Dummy | Dummy |

2.1.2.26. Set RX Frequency

Set RX center frequency temporarily for testing purposes. This settings are lost after reset or when switching the device off. The frequency value is an unsigned 32-bit integer within the range [869.400.000Hz to 869.650.000Hz] and default value 869.525.000Hz for EU. The range for US is [902.000.000Hz to 906.000.000Hz] with default 905.200.000Hz. This command will only be used during testing of the system and not during regular operation in a SIGFOX™ network.

| | | | | | |
|----------|---------------------|-----------|-----------|----------|---------|
| Master | RX Frequency (0x1C) | RX[31:24] | RX[23:16] | RX[15:8] | RX[7:0] |
| ATA8520E | Dummy | Dummy | Dummy | Dummy | Dummy |

2.1.2.27. Store Crystal Coefficients

This command stores a crystal coefficient for temperature compensation at position INDEX (range 0 to 22). The INDEX is related to a specific temperature value, i.e., index position 0 is for -48°C, index 1 for -40°C, index 2 for -32°C and so forth until index 22 for +128°C. The data value has to be in ppm and is interpreted as a signed value. The final table is composed with a step size of 8°C, starting at -48°C and ending at +128°C. The command will issue an event when finished.

| | | | | |
|----------|--|-----------------------------|-------|-------|
| Master | | Store Crystal Coeff. (0x1D) | Index | Data |
| ATA8520E | | Dummy | Dummy | Dummy |

2.1.2.28. Trigger Read of Crystal Coefficient Table

This command triggers the read operation of the crystal coefficient table into a buffer area for the temperature range of -32°C to $+88^{\circ}\text{C}$ in steps of 8°C (16 coefficients) for verification purposes. The buffer read itself is then performed with command 0x20.

| | | |
|----------|--|-----------------------------|
| Master | | Trigger Crystal Read (0x1E) |
| ATA8520E | | Dummy |

2.1.2.29. Trigger Read of System Configuration

This command triggers the read operation of the center frequencies for up- and downlink in Hz and the system configuration setting as used in command 0x11. The buffer read itself is then performed with command 0x20.

| | | |
|----------|--|---------------------------|
| Master | | Trigger Conf. Read (0x1F) |
| ATA8520E | | Dummy |

2.1.2.30. Read Configuration Buffer

This command returns the data read from EEPROM which has been triggered before by the following commands.

Read Crystal Coefficient Table

This command reads the crystal coefficients in ppm after issuing the trigger command 0x1E. The buffer area includes 16 signed data bytes to be read.

| | | | | | | |
|----------|--|----------------------------|-------|----------|-----|-----------|
| Master | | Read Crystal Coeff. (0x20) | Dummy | Dummy | ... | Dummy |
| ATA8520E | | Dummy | Dummy | Coeff[2] | | Coeff[17] |

Read System Configuration

This command reads the center frequencies for up- and downlink in Hz as 32-bit unsigned value and the system configuration setting as used in command 0x11 after issuing the trigger command 0x1F. The buffer area includes 10 data bytes to be read.

| | | | | | | | | |
|----------|--|----------------------------|-------|---------------|----------------|----------------|----------------|--------------|
| Master | | Read Crystal Coeff. (0x20) | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | freqTX[7..0] | freqTX[15..8] | freqTX[23..16] | freqTX[31..24] | freqRX[7..0] |
| | | | Dummy | Dummy | Dummy | Dummy | Dummy | Dummy |
| | | | | freqRX[15..8] | freqRX[23..16] | freqRX[31..24] | repeat | Sys Config |

Read Current FCC Channel Setting

This command reads the current FCC channel configuration stored in the EEPROM after issuing the trigger command 0x25. The buffer includes 1 FCC data byte with

- Bit 7...4: = 1 if the current FCC Macro Channel is not the default SIGFOX channel
 0 otherwise
- Bit 3...0: # of free Micro Channel inside the current FCC Macro Channel

| | | | | |
|----------|--|-------------------------|-------|----------|
| Master | | Read Current FCC (0x20) | Dummy | Dummy |
| ATA8520E | | Dummy | Dummy | FCC data |

2.1.2.31. Enable Frequency Fixed Mode

This command will toggle between frequency hopping and fixed frequency for testing purposes. After applying a reset the frequency hopping mode is enabled per default. This command will only be used during testing of the system and not during regular operation in a SIGFOX™ network.

| | | |
|----------|--|--------------------------|
| Master | | Enable Fixed Frq. (0x21) |
| ATA8520E | | Dummy |

2.1.2.32. Store Channel Configuration

This command stores the channel configuration for the US mode operation in EEPROM. The following values have to be used for FCC compliance:

- MC1[0..3]: 0xFF, 0x01, 0x00, 0x00
- MC2[0..3]: 0x00, 0x00, 0x00, 0x00
- MC3[0..3]: 0x00, 0x00, 0x00, 0x00
- DC[0..1]: 0x01, 0x00

| | | | | | | | | |
|----------|--|---------------------------|--------|--------|--------|--------|-------|--------|
| Master | | Store Micro-chann. (0x22) | MC1[0] | MC1[1] | MC1[2] | MC1[3] | ... | MC3[0] |
| ATA8520E | | Dummy | Dummy | Dummy | Dummy | Dummy | | Dummy |
| | | | MC3[1] | MC3[2] | MC3[3] | DC[0] | DC[1] | |
| | | | Dummy | Dummy | Dummy | Dummy | Dummy | |

2.1.2.33. Reset Channel Usage

This command will reset the channel configuration of the US mode. It has to be applied before using any send or send/receive command (in US mode only). In addition it has to be ensured in the application software to use this command with a minimum delay of 20 seconds between consecutive calls to comply with FCC regulations.

| | | |
|----------|--|----------------------------|
| Master | | Reset Channel Usage (0x23) |
| ATA8520E | | Dummy |

2.1.2.34. Adjust RSSI - Value

This command will store a value which is automatically added to the measured RSSI level. This value is derived from the gain or loss of the external circuitry including the antenna. This corrected RSSI value will be used during frame sending to the SIGFOX™ network and is calculated as (value is of type signed 8-bit data):

$$RSSI_{system} = RSSI_{measured} + Value$$

| | | | |
|----------|--|-------------------|-------|
| Master | | Adjust RSSI(0x24) | Value |
| ATA8520E | | Dummy | Dummy |

2.1.2.35. Trigger Read of FCC Channel Configuration

This command triggers the read operation of the current FCC channel configuration setting for verification purposes. The buffer read itself is then performed with command 0x20.

| | | |
|----------|--|-------------------------|
| Master | | Trigger FCC Read (0x25) |
| ATA8520E | | Dummy |

2.1.3. Command Table Overview

This section gives an overview about the SPI commands and the separation into the

- application SPI commands used in application software
- configuration SPI commands used during end-of-line configuration
- test and maintenance SPI commands used for testing purposes

Table 2-2. Application SPI Commands

| CMD | Index | Write Data | Read Data | Event |
|-----------------------------------|-------|---------------------------|-----------------------------------|-------|
| System reset | 0x01 | None | None | Yes |
| I/O Init | 0x02 | DDRC register setting | None | - |
| I/O Write | 0x03 | PORTC register setting | None | - |
| I/O Read | 0x04 | None | PINC register setting | - |
| OFF mode | 0x05 | None | None | - |
| Write TX buffer | 0x07 | Data written to TX buffer | None | - |
| Get status | 0x0A | None | SSM / Atmel® FW / SIGFOX™ library | - |
| Send frame ⁽¹⁾ | 0x0D | None | None | Yes |
| Send/receive frame ⁽¹⁾ | 0x0E | None | None | Yes |
| Read RX buffer | 0x10 | None | RX buffer data | - |
| Read supply temperature | 0x13 | None | Vidle, Vactive, temperature | - |
| Trigger measurement | 0x14 | None | None | Yes |
| Reset channel usage | 0x23 | None | None | - |

Note 1: These commands will be available after the initial configuration has been performed (see section [Configuring US- and EU-Mode](#)).

Table 2-3. Configuration SPI Commands

| CMD | Index | Write Data | Read Data | Event |
|-----------------------------|-------|-------------------------|--------------------------------|-------|
| Get PAC | 0x0F | None | PAC[0], PAC[1] PAC[15] | - |
| Store Sys Conf | 0x11 | DDRC, PORTC, SysConf | None | Yes |
| Get ID | 0x12 | None | ID[3] ... ID[0] | - |
| Store frequencies | 0x1A | TX and RX frequency | None | Yes |
| Store crystal coefficients | 0x1D | Index/Data | None | Yes |
| Store channel configuration | 0x22 | Data | None | Yes |
| Adjust RSSI-value | 0x24 | Data | None | Yes |

Table 2-4. Test and Maintenance SPI Commands

| CMD | Index | Write Data | Read Data | Event |
|--|-------|--------------------------------|---------------|-------|
| Atmel version | 0x06 | None | Major / minor | - |
| Enable special mode | 0x08 | None | None | - |
| SIGFOX version | 0x09 | None | Version L-H | - |
| Send bit ⁽¹⁾ | 0x0B | Bit status | None | Yes |
| Send out-of-band ⁽¹⁾ | 0x0C | None | None | Yes |
| Trigger test mode ⁽¹⁾ | 0x15 | Test mode and configuration | None | Yes |
| Send CW ⁽¹⁾ | 0x17 | On/off | None | - |
| Firmware test | 0x18 | Parameter | None | - |
| Set TX frequency | 0x1B | TX frequency | None | - |
| Set RX frequency | 0x1C | RX frequency | None | - |
| Trigger read of crystal coefficient table | 0x1E | None | None | - |
| Trigger read of system configuration | 0x1F | None | None | - |
| Read configuration buffer | 0x20 | None | Data | - |
| Enable frequency fixed mode | 0x21 | None | None | - |
| Trigger read of FCC channel configuration | 0x25 | None | None | - |

Note 1: These commands will be available after the initial configuration has been performed (see section [Configuring US- and EU-Mode](#)).

Table 2-5. Parameter Memory Usage

| Parameter | Size [Bit] | Description | SPI Command |
|----------------------------|------------|--|------------------|
| Volatile Parameters | | | |
| DDRC | 8 | Set the data direction for the Port C pins [1..5]: :0 pin is an input :1 pin is an output | 0x02 |
| PORTC | 8 | Set the output level for the Port C pins [1..5]: :0 pin is low :1 pin is high | 0x03 |
| PINC | 8 | Read the signal level for the Port C pins [1..5] | 0x04 |
| TX buffer | 12 × 8 | Data payload for transmission | 0x07 |
| RX buffer | 8 × 8 | Data payload for reception | 0x10 |
| TX | 32 | Set TX frequency [Hz] | 0x1B |
| RX | 32 | Set RX frequency [Hz] | 0x1C |
| EEPROM Parameters | | | |
| PAC | 16 × 8 | Read the device registration key | 0x0F |
| ID | 32 | Read the device ID | 0x12 |
| EDDRC | 8 | Set the data direction for the Port C pins [1..5]: :0 pin is an input :1 pin is an output | 0x11 |
| EPORTC | 8 | Set the output level for the Port C pins [1..5]: :0 pin is low :1 pin is high | 0x11 |
| Repeat | 8 | Set and read # of repetitions for the send/receive command 0x0E | 0x11, 0x1F, 0x20 |
| SysConf | 8 | Set and read system configuration as defined in section System and Pin Configuration | 0x11, 0x1F, 0x20 |
| freqTX | 32 | Set and read TX frequency [Hz] | 0x1A, 0x1F, 0x20 |
| freqRX | 32 | Set and read RX frequency [Hz] | 0x1A, 0x1F, 0x20 |
| Crystal Data | 23 × 8 | Set and read crystal coefficients for temperature compensation [ppm] | 0x1D, 0x1E, 0x20 |
| MC1, MC2, MC3, DC | 14 × 8 | Set channel configuration for US mode | 0x22 |
| RSSI Value | 8 | Set RSSI value to adjust RSSI level | 0x24 |

2.1.4. System and Pin Configuration

This section specifies the system configuration settings used in the SPI command (0x11). This system configuration has to be set after the system issues a system ready event and before using any other SPI command. The settings are stored in the internal EEPROM and will be applied after a system reset. This settings are typically applied at the EOL testing in the factory. [Table 2-6](#) summarizes the configuration settings.

Table 2-6. System Configuration

| Function | Bit No. | Settings |
|----------------|---------|---|
| None | 7 to 6 | :00 (default) |
| None | 5 to 4 | :11 (default) |
| Supply voltage | 3 | :0, 5V supply :1, 3V supply (default) |
| RX/TX select | 2 | :0, up-/downlink enabled :1, uplink only enabled (default) |
| EU/US select | 1 | :0 US mode |
| | | :1 EU mode |
| None | 0 | :1 (default) |

For an additional front-end module, which includes an antenna switch, a low-noise amplifier for downlink operation and a power amplifier for uplink operation, two control signals are available at the port pins PB0 and PB7. These pins are controlled by the Atmel® ATA8520E device during transmission and reception of a RF data telegram. [Table 2-7](#) summarizes the function of these pins.

Table 2-7. FEM Control Pins

| Function/Pin | PB0 | PB7 |
|-----------------|-----|-----|
| FEM disabled | 0 | X |
| Uplink active | 1 | 1 |
| Downlink active | 1 | 0 |

In case the internal SPDT switch is not used for RF control this switch can be used in addition to control an external FEM. During uplink operation the path between pins SPDT_ANT and SPDT_TX is closed and for downlink operation the path between pins SPDT_ANT and SPDT_RX is closed.

2.1.5. Configuring US- and EU-Mode

The Atmel® device ATA8520E can be configured to operate in US- or in EU-mode and can be switched between these modes. To select the operating mode the settings shown in [Table 2-8](#) have to be set.

Table 2-8. US- and EU-Mode Settings

| Mode | TX Frequency | RX Frequency | Configuration (Bit 1 in Table 2-6) |
|------|--------------|--------------|---|
| EU | 868130000Hz | 869525000Hz | 1 |
| US | 902200000Hz | 905200000Hz | 0 |

To select the frequency use the SPI command sequence:

1. SPI cmd: (0x1A) (TX-freq.) (RX-freq.)
2. wait for EVENT signal and read status with SPI cmd: (0x0A)

To select the mode bit use the SPI cmd sequence:

1. SPI cmd: (0x11) (DDRC) (PORTC) (0x02) (systemConfig)
2. wait for EVENT signal and read status with SPI cmd: (0x0A)

Finally a System Reset with SPI command (0x01) will reset the device and apply the settings.



Caution: The device is delivered without mode configuration per default. Before the first usage a configuration is required with the SPI commands described before. In addition to the frequency and region settings the supply mode should be set with SPI command (0x11). When using the device with 5V supply it has to be ensured that before using the RF transmit operation the 5V supply mode is configured!

For the US mode the channel usage has to be initialized before the first RF command, i.e., the channel configuration has to be stored in EEPROM:

1. SPI cmd: (0x22) (default data)
2. wait for EVENT signal and read status with SPI cmd: (0x0A)
3. System Reset with SPI command (0x01) will reset the device and apply the settings
4. SPI cmd: (0x23)

The SPI cmd (0x23) shall be applied after each wake-up/reset of the device but must keep a 20s wait period before consecutive calls (due to FCC regulations).

When receiving a downstream data packet with 8 bytes the RSSI value is reported with byte no. 8. This RSSI value is determined at device pin level and need adjustment for the system level when using an external LNA. This offset value can be set with SPI cmd (0x24).

2.2. Operating Modes Overview

This section gives an overview of the operating modes supported by the Atmel® ATA8520E.

After connecting the supply voltage to the VS pin, the Atmel ATA8520E always starts in OFF mode. All internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. The Atmel ATA8520E can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence which will set the event line PB6 to low. After the system initialization the Atmel ATA8520E reaches the IDLE Mode.

The idle mode is the basic system mode supporting SPI communication and transitions to the other operating modes.

The transmit mode (TX Mode) starts the data transmission using the payload data which has to be previously written into the TX buffer with the SPI command “Write TX Buffer”. The data transmission is started with the SPI command “Send Frame”. After transmitting the data frame, the end of the transmission is indicated when the event pin PB6 switches to low and the device enters the idle mode again.

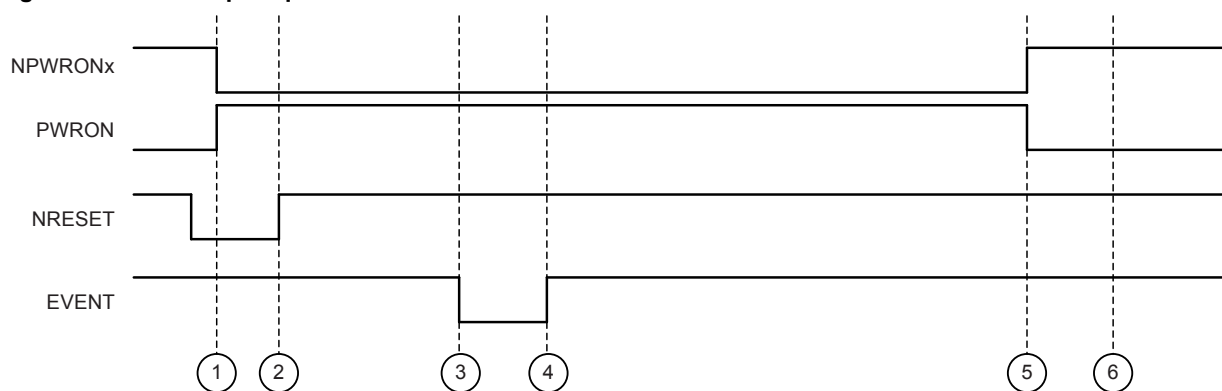
Reading the device status with the “Get Status” SPI command clears the PB6 event line, setting it to high level again.

The transmit/receive mode (TX/RX Mode) will send at first a data telegram in uplink direction and then enter receive mode for downlink direction. The downlink request is captured by the SIGFOX™ backend and processed. After transmission of the uplink frame the device will wait for 20 seconds before entering the receive mode. This receive mode will take up to 30 seconds and will end with an event on pin PB6. This event is cleared when reading the device status with the SPI command “Get Status”. If no error occurs during the downlink operation (Atmel status error code = 0000), the received data telegram of 8 bytes can be read with the SPI command “Read RX Buffer”.

2.2.1. Power-up Sequence

This section describes the power-up sequence for the device as described in Figure 2-2. The device is usually in OFF mode where the signals NPWRONx, PWRON and NRESET are inactive but VS is supplied with power. Switching the NRESET signal active or sending the SPI command System Reset (0x01) will have no effect in OFF mode. Switching one of the power-on pins active will wake-up the device and an internal power-on reset is performed. In addition the external NRESET line can be used to keep the device in reset state when waking-up the device. The minimum activation time for the NPWRONx, PWRON and NRESET signals is 10µs.

Figure 2-2. Power-up Sequence



After applying the reset signal NRESET one of the power-up signals NPWRON1...6 or PWRON is applied at timing point T1. At timing point T2 (~10µs after T1) the external reset signal is removed and the device starts its internal power-up sequence. This internal sequence is finished at timing point T3 (~10ms after T2 in EU mode and ~30ms after T2 in US mode) and is signaled with the event line. Reading the device status with the SPI command (0x0A) “Get status” will clear the event line at timing point T4. The device is now in idle mode and operational even if the NPWRONx and PWRON signals are deactivated (the start-up time between T2 and T3 for the first power-up and the first send or send/receive command after the configuration will take longer as the typical time due to internal initialization steps).

To shutdown the device into OFF mode the power-up signals NPWRON1...6 or PWRON have to be deactivated at first (shown in timing point T5). The shutdown into OFF mode is then performed by sending the SPI command (0x05) “OFF mode” to the device.

2.2.2. Power-down Sequence

The device can be switched into an OFF mode with very low power consumption (5nA at 25°C) using the SPI command 0x05. Before using this command a potential pending event has to be cleared by reading the status information with SPI command 0x0A. This ensures the correct updating of internal status information before power-down. In addition the PWRON and NPWRONx pins have to be released to prevent the wake-up of the device. If one of the power-on pins is active the device will not switch into OFF mode.

2.2.3. Application Example

The software to control the device and to transmit only a data frame (without reception) has to perform the following steps:

1. Initialize device as shown in [Figure 2-2](#) for the power-up sequence
2. Check for the startup event and read the device status with SPI command (0x0A) "Get status" to clear this event
3. Load the transmit buffer with up to 12 bytes using the SPI command (0x07) "Write TX Buffer"
4. Start the data transmit with SPI command (0x0D) "Send Frame"
5. Wait until the event signal appears (this takes about 7-8 seconds in EU mode and 2-3 seconds in US mode)
6. Read the device status with SPI command (0x0A) "Get status" to clear this event
7. Switch off the power-on signals as shown in [Figure 2-2](#)
8. Send the SPI command (0x05) "OFF mode" to the shutdown the device

The software to control the device and to transmit and receive a data frame has to perform the following steps:

1. Initialize device as shown in [Figure 2-2](#) for the power-up sequence
2. Check for the startup event and read the device status with SPI command (0x0A) "Get status" to clear this event
3. Load the transmit buffer with up to 12 bytes using the SPI command (0x07) "Write TX Buffer"
4. Start the data transmit with SPI command (0x0E) "Send/Receive Frame"
5. Wait until the event signal appears (this takes about 20-50 seconds)
6. Read the device status with SPI command (0x0A) "Get status" to clear this event
7. Read the receive buffer with SPI command (0x10) "Read RX Buffer" for the 8 data bytes
8. Process received data, etc.
9. Switch off the power-on signals as shown in [Figure 2-2](#)
10. Send the SPI command (0x05) "OFF mode" to the shutdown the device

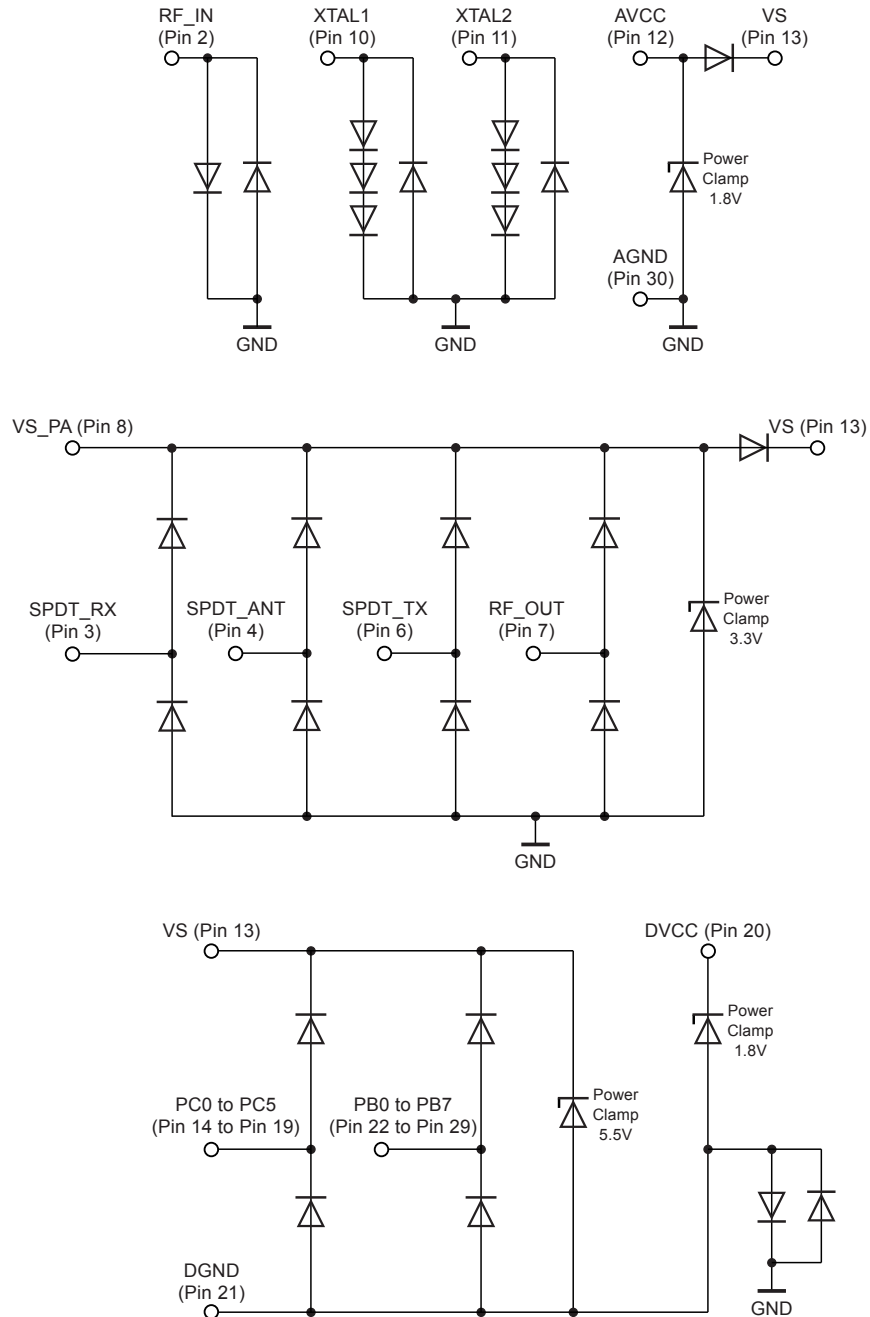
For the SPI communication it is important to keep the timing as shown in [Figure 2-1](#). With the SPI commands (0x0F) „Get PAC" and (0x12) „Get ID" the SIGFOX™ registration information can be read to register the device in the SIGFOX cloud.

3. Electrical Characteristics

3.1. ESD Protection Circuits

GND is the exposed die pad of the Atmel® which is internally connected to AGND (pin 30). All Zener diodes shown in Figure 3-1 (marked as power clamps) are realized with dynamic clamping circuits and not physical Zener diodes. Therefore, DC currents are not clamped to the shown voltages.

Figure 3-1. Atmel ESD Protection Circuit



3.2. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Max. | Unit |
|--|--------------------|------|--|------|
| Junction temperature | T _j | | +150 | °C |
| Storage temperature | T _{stg} | -55 | +125 | °C |
| Ambient temperature | T _{amb} | -40 | +85 | °C |
| Supply voltage | V _{VS} | -0.3 | +6.0 | V |
| Supply voltage PA (1.9 to 3.6V application) | V _{VS_PA} | -0.3 | +4.0 | V |
| ESD (human body model) all pins | HBM | -4 | +4 | kV |
| ESD (machine model) all pins | MM | -200 | +200 | V |
| ESD (field induced charged device model) all pins | FCDM | -750 | +750 | V |
| Maximum peak voltage at pin 4 (SPDT_ANT) ⁽¹⁾ | SPDTANT | -0.3 | V _{S_PA} ⁽²⁾ + 0.3 | V |
| Maximum peak voltage at pin 6 (SPDT_TX) ⁽¹⁾ | SPDTTX | -0.3 | V _{S_PA} ⁽²⁾ + 0.3 | V |
| Note: | | | | |
| 1. The customer application needs to be properly designed. | | | | |
| 2. V _{S_PA} is the voltage applied to pin 8. | | | | |

3.3. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|--------------------|-------|------|
| Thermal resistance, junction ambient, soldered in compliance with JEDEC | R _{th_JA} | 35 | K/W |

3.4. Supply Voltages and Current Consumption

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V across all process tolerances unless otherwise specified. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|------|---------------------------------------|---|---------------|-------------------|------|--------------|--------------|------------------|--------|
| 1.00 | Supply voltage range VS | 3V application | 13 | V_{VS} | 1.9 | 3.0 | 3.6 | V | A |
| | | 5V application | 13 | V_{VS} | 2.4 | 5.0 | 5.5 | V | A |
| 1.01 | Supply voltage for SIGFOX™ compliance | 3V application | 13 | V_{VS} | 2.9 | 3.0 | 3.1 | V | |
| | | 5V application | 13 | V_{VS} | 3.3 | 5.0 | 5.5 | V | |
| 1.05 | Supply voltage rise time | | 13 | V_{VS_rise} | | | 1 | V/ μs | D |
| 1.10 | Supply voltage range VS_PA | 3V application | 8 | V_{VS_PA} | 1.9 | 3 | 3.6 | V | A |
| | | 5V application | 8 | V_{VS_PA} | | 3 | | V | A |
| | | SIGFOX compliant | 8 | V_{VS_PA} | | 3 | | V | |
| 1.20 | OFF mode current consumption | $T_{amb} = 25^{\circ}\text{C}$ $T_{amb} = 85^{\circ}\text{C}$ | 8, 13 | $I_{OFFMode_3V}$ | | 5 | 150 600 | nA nA | B B |
| 1.30 | Idle mode current consumption | Temperature range -40°C to $+65^{\circ}\text{C}$ | 13 | $I_{IdleMode}$ | | 50 | 90 | μA | B |
| 1.80 | RX mode current consumption | $f_{RF} = 869.5\text{MHz}$ $f_{RF} = 905.2\text{MHz}$ | 13 | I_{RXMode} | | 10.4 10.5 | 14.6 14.7 | mA | A |
| 2.00 | TX mode current consumption | $P_{out} = +14\text{dBm}$ $f_{RF} = 868.3\text{MHz}$ $f_{RF} = 902.2\text{MHz}$ | (7), 8, 13 | I_{TXMode} | | 32.7 33.5 | 45 46 | mA | B |
| 2.05 | SIGFOX TX mode current consumption | $T_{amb} = 25^{\circ}\text{C}$, 3V application EU US | (7), 8, 13 | $I_{SIGFOX Mode}$ | | 31.8 16.7 | 40.1 21.0 | mA mA | B B |
| | | | | | | 32.7 | 41.1 | mA | B |
| 2.06 | SIGFOX TX mode current consumption | $T_{amb} = 85^{\circ}\text{C}$, 3V application | (7), 8, 13 | $I_{SIGFOX Mode}$ | | 32.7 | 41.1 | mA | B |

Pin numbers in brackets mean they are measured matched to 50 Ω on the application board.

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.5. RF Receive Characteristics

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V across all process tolerances unless otherwise specified. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|------|--------------------------------|--|--------|--|-----------------|--|-----------------|----------------|---------------------------------|
| 4.50 | Frequency range EU US | Defined by SIGFOX™ protocol | (2) | fRX | 869.40 902.0 | | 869.65 906.0 | MHz | |
| 4.90 | Sensitivity level | FSK at 25kHz IF bandwidth $T_{amb} = 25^{\circ}\text{C}$ 0.75Kbit/s \pm 0.75kHz | 17, 19 | SFSK | -1.5dB | -121.5 | +1.5dB | dBm | B |
| 7.30 | Blocking | FSK at 25kHz IF bandwidth, $T_{amb} = 25^{\circ}\text{C}$ 2.4Kbit/s \pm 2.4kHz | (2) | fdist. \geq 50kHz fdist. \geq 100kHz fdist. \geq 225kHz fdist. \geq 450kHz fdist. \geq 1MHz fdist. \geq 4MHz fdist. >10MHz | | 34 40 52 58 67 75 75 | | dBc | C C C C C C C |
| 7.70 | Image rejection | Large disturber applied before useful signal | (2) | IMRED | 38 | 47 | | dB | A |
| 7.80 | Blocking $3f_{LO}$, $5f_{LO}$ | $3 \times f_{LO} - f_{IF}$ $5 \times f_{LO} + f_{IF}$ | (2) | BLNfLO | | 39 45 | | dB | C C |
| 8.50 | Input impedance | Measured on application board, RC parallel equivalent circuit | 2 | Zin | -20% | 340 1.4 | +20% | Ω pF | C |
| 8.70 | SPDT switch RX insertion loss | Sensitivity matching RF_IN with SPDT to 50Ω compared to matching RF_IN directly to 50Ω | (3, 4) | ILSwitch_RX | | 1.0 | 1.4 | dB | C |
| 9.00 | RSSI accuracy | PRFIN = -70dBm | (2), 4 | RSSIABS_ACCU | -5.5 | | +5.5 | dB | B |
| 9.20 | RSSI resolution | DSP property | (2), 4 | RSSIRES | | 0.5 | | dB/ value | D |

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.6. RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V across all process tolerances unless otherwise specified. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|---|--|--------|-----------------------|----------------|-------------------|-------------------|------------|-------------|
| 10.00 | Output power range | $T_{amb} = 25^{\circ}\text{C}$ EU US | (7) | PRange | | | +14.5 +9.5 | dBm dBm | B C |
| 10.01 | Output power for SIGFOX™ compliance | $T_{amb} = 25^{\circ}\text{C}$, $V_{VS} = 2.9\text{V}$ to 3.1V , 3V application (for 5V applications see no. 11.50) EU US | (7) | PSIGFOX | 13.5 9.2 | 13.8 9.5 | 14.0 9.7 | dBm dBm | C C |
| 10.02 | Output power for SIGFOX compliance | $T_{amb} = -45^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 3.0\text{V}$, 3V application (for 5V applications see no. 11.50) EU US | (7) | PSIGFOX | 13.1 8.9 | 13.8 9.5 | 14.7 10.1 | dBm dBm | C C |
| 10.05 | Frequency range EU US | Defined by SIGFOX protocol | (7) | f_{TX} | 868.0 902.0 | | 868.6 906.0 | MHz | |
| 11.00 | Output power at 14dBm | $T_{amb} = 25^{\circ}\text{C}$ using 14dBm matching | (7) | P_{out_14dBm} | -1.5dB | 14 | +1.5dB | dBm | B |
| 11.10 | Output 2 nd harmonic at 14dBm | $T_{amb} = 25^{\circ}\text{C}$ using 14dBm matching | (7) | HM214dBm | | -24 | | dBc | C |
| 11.20 | Output 3 rd harmonic at 14dBm | $T_{amb} = 25^{\circ}\text{C}$ using 14dBm matching | (7) | HM314dBm | | -50 | | dBc | C |
| 11.50 | Output power change full temperature and supply voltage range | For 13.8dBm $V_{VS_PA} = 3.0\text{V} \pm 0.3\text{V}$ $P = P_{out} + \Delta P$ | (7) | $\Delta P_{TambVs2}$ | -3.5 | | +2 | dB | C C |
| 11.60 | Spurious emission | at $\pm f_{XTO}$ at $\pm f_{AVR}$ ($f_{XTO} / 4$) at $\pm f_{CLK_OUT}$ ($f_{XTO}/6$) | (7) | SPTX | | -72 -85 -78 | -60 -60 -60 | dBc | B C C |
| 12.40 | SPDT insertion loss TX | Transmitted power using matching RF_OUT with SPDT to 50Ω compared to matching RF_OUT directly to 50Ω | (4, 6) | ILSwitch_TX | | 0.7 | 1.2 | dB | C |
| 12.45 | Maximum peak voltage on SPDT_ANT (pin 4) | | 4 | $V_{PEAK_SPDT_ANT}$ | -0.3 | | $V_{S_PA} + 0.3$ | V | D |

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|---|-----------------|-----|---------------|------|------|-------------|------|-------|
| 12.50 | Maximum peak voltage on SPDT_TX (pin 6) | | 6 | VPEAK_SPDT_TX | -0.3 | | VS_PA + 0.3 | V | D |

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.7. RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V over all process tolerances, quartz parameters $C_m = 4\text{fF}$ and $C_0 = 1\text{pF}$ unless otherwise specified. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|---|--|--------|---------------------|------|--------|------|------|-------|
| 13.30 | XTO frequency range | | 10, 11 | f_{xto} | | 24.305 | | MHz | C |
| 13.35 | XTO frequency for SIGFOX™ compliance | KDS: 1C324305AB0B NDK: NX3225SA EXS00A-CS08559 | 10, 11 | f_{SIGFOX_XTO} | | 24.305 | | MHz | |
| 13.40 | XTO pulling due to internal capacitance and XTO tolerance | $C_m = 4\text{fF}$, $T_{amb} = 25^{\circ}\text{C}$ | 10, 11 | ΔF_{XTO1} | -10 | | +10 | ppm | B |
| 13.50 | XTO pulling due to temperature and supply voltage | $C_m = 4\text{fF}$ $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | 10, 11 | ΔF_{XTO2} | -4 | | +4 | ppm | B |
| 13.60 | Maximum C_0 of XTAL | XTAL parameter | 10, 11 | C_{0_max} | | 1 | 2 | pF | D |
| 13.70 | XTAL, C_m motional capacitance | XTAL parameter | 10, 11 | C_m | | 4 | 10 | fF | D |
| 13.90 | XTAL, real part of XTO impedance at start-up | $C_m = 4\text{fF}$, $C_0 = 1\text{pF}$ | 10, 11 | R_{e_start} | 1100 | | | Ω | B |
| 14.00 | XTAL, maximum R_m after start-up | XTAL parameter | 10, 11 | R_{m_max} | 110 | | | Ω | D |
| 14.10 | Internal load capacitors | Including ESD and package capacitance. XTAL has to be specified for 7.5pF load capacitance (incl. 1pF PCB capacitance per pin) | 10, 11 | C_{L1} , C_{L2} | 13.3 | 14 | 14.7 | pF | B |

Pin numbers in brackets mean they are measured matched to 50Ω on the application board.

*) Type means: A = 100% tested, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.8. I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V over all process tolerances unless otherwise specified. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|--|------------------------------------|----------------|---------------------|---------------------|-------|---------------------|------------------|-------|
| 15.00 | Input low voltage | PC0 to PC5 PB0 to PB7 | 14-19 22-29 | V_{IL} | -0.3 | | $0.2 \times V_{VS}$ | V | A |
| 15.05 | Input low leakage current I/O pin | PC0 to PC5 PB0 to PB7 | 14-19 22-29 | I_{IL} | | | -1 | μA | A |
| 15.10 | Input high voltage | PC0 to PC5 PB0 to PB7 | 14-19 22-29 | V_{IH} | $0.8 \times V_{VS}$ | | $V_{VS} + 0.3$ | V | A |
| 15.15 | Input high leakage current I/O pin | PC0 to PC5 PB0 to PB7 | 14-19 22-29 | I_{IH} | | | 1 | μA | A |
| 15.20 | Output low voltage | $I_{OL} = 0.2\text{mA}$ | 14-19 22-29 | V_{OL_3V} | | | $0.1 \times V_{VS}$ | V | A |
| 15.30 | Output high voltage | $I_{OH} = -0.2\text{mA}$ | 14-19 22-29 | V_{OH_3V} | $0.9 \times V_{VS}$ | | | V | A |
| 15.40 | I/O pin pull-up resistor | OFF mode: see port B and port C | 14-19 22-29 | R_{PU} | 30 | 50 | 70 | $\text{k}\Omega$ | A |
| 16.10 | I/O pin output delay time (rising edge) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | $T_{del_rise_3V}$ | 13.6 | 17.5 | 22.4 | ns | D |
| 16.20 | I/O pin rise time ($0.1 \times V_{VS}$ to $0.9 \times V_{VS}$) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | T_{rise_3V} | 20.7 | 23.9 | 28.4 | ns | D |
| 16.30 | I/O pin slew rate (rising edge) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | $T_{sr_rise_3V}$ | 0.115 | 0.100 | 0.084 | V/ns | D |
| 16.40 | I/O pin output delay time (falling edge) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | $T_{del_fall_3V}$ | 13.7 | 17.4 | 22.7 | ns | D |
| 16.50 | I/O pin fall time ($0.9 \times V_{VS}$ to $0.1 \times V_{VS}$) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | T_{fall_3V} | 16.2 | 19.2 | 22.5 | ns | D |
| 16.60 | I/O pin slew rate (falling edge) | $C_{Load} = 10\text{pF}$ | 14-19 22-29 | $T_{sr_fall_3V}$ | 0.148 | 0.125 | 0.106 | V/ns | D |

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

3.9. Hardware Timings

All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V over all process tolerances. Typical values are given at $V_{VS} = 3\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|--------------------------------|---|--------|-------------|------|------|------|------|-------|
| 17.50 | Startup time EU ⁽¹⁾ | PWRON = '1' or NPWRON = '0' to EVENT generation | 13, 20 | TSTARTUP_EU | | 10 | | ms | C |
| | Startup time US ⁽¹⁾ | PWRON = '1' or NPWRON = '0' to EVENT generation | 13, 20 | TSTARTUP_US | | 30 | | ms | C |

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

Note: The start-up time after the configuration and before the first send or send/receive command is typically longer (in the range of some 100ms) due to internal system initialization steps.

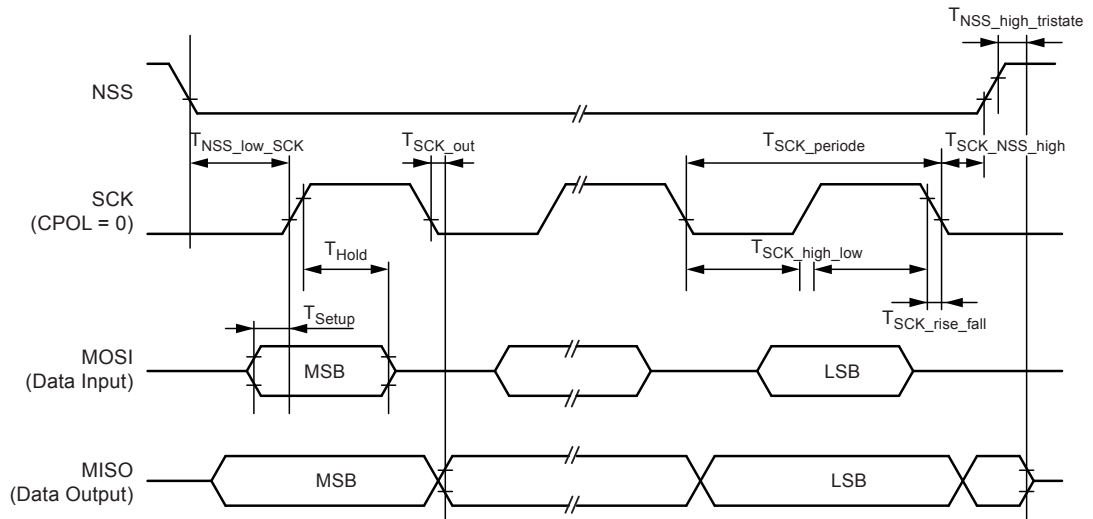
3.10. Hardware SPI Timing Characteristics

Timing shown for CPHA=0 and CPOL=0 in [Figure 3-2](#), timing is valid for all CPHA and CPOL configurations. See also section [SPI Command Interface](#) for functional SPI description and for firmware limitations on SPI data transfer. All parameters refer to GND (backplane) and are valid for $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{VS} = 1.9\text{V}$ to 3.6V (3V application) and 4.5V to 5.5V (5V application) over all process tolerances. Typical values are given at $V_{VS} = 5\text{V}$, $T_{amb} = 25^{\circ}\text{C}$, and for a typical process unless otherwise specified. Crystal oscillator frequency $f_{XTO} = 24.305\text{MHz}$.

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-------|--|-------------------|--------|--------------------|------|------|------|---------------|-------|
| 49.10 | SCK cycle time | | 23 | TSCK_period | 8 | | | μs | D |
| 49.20 | SCK high or low time | | 23 | TSCK_high_low | 330 | | | ns | D |
| 49.30 | SCK rise or fall time | | 23 | TSCK_rise_fall | | | 100 | ns | D |
| 49.40 | MOSI setup time to active edge of SCK | | 23, 24 | TSetup | 80 | | | ns | D |
| 49.50 | MOSI hold time to active edge of SCK | | 23, 24 | THold | 245 | | | ns | D |
| 49.60 | Time period active edge of SCK to data out at MISO | CLOAD_MISO = 10pF | 23, 25 | TSCK_out | | | 250 | ns | D |
| 49.70 | Time period SCK inactive to NSS high | | 23, 27 | TSCK_NSS_high | 100 | | | μs | D |
| 49.80 | Time period NSS high to MISO tristate | CLOAD_MISO = 10pF | 25, 27 | TNSS_high_tristate | | | 250 | ns | D |
| 49.90 | Time period NSS low to active edge SCK | | 23, 27 | TNSS_low_SCK | 65 | | | μs | D |

*) Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = characterized on samples, D = design parameter

Figure 3-2. SPI Interface Timing Requirements

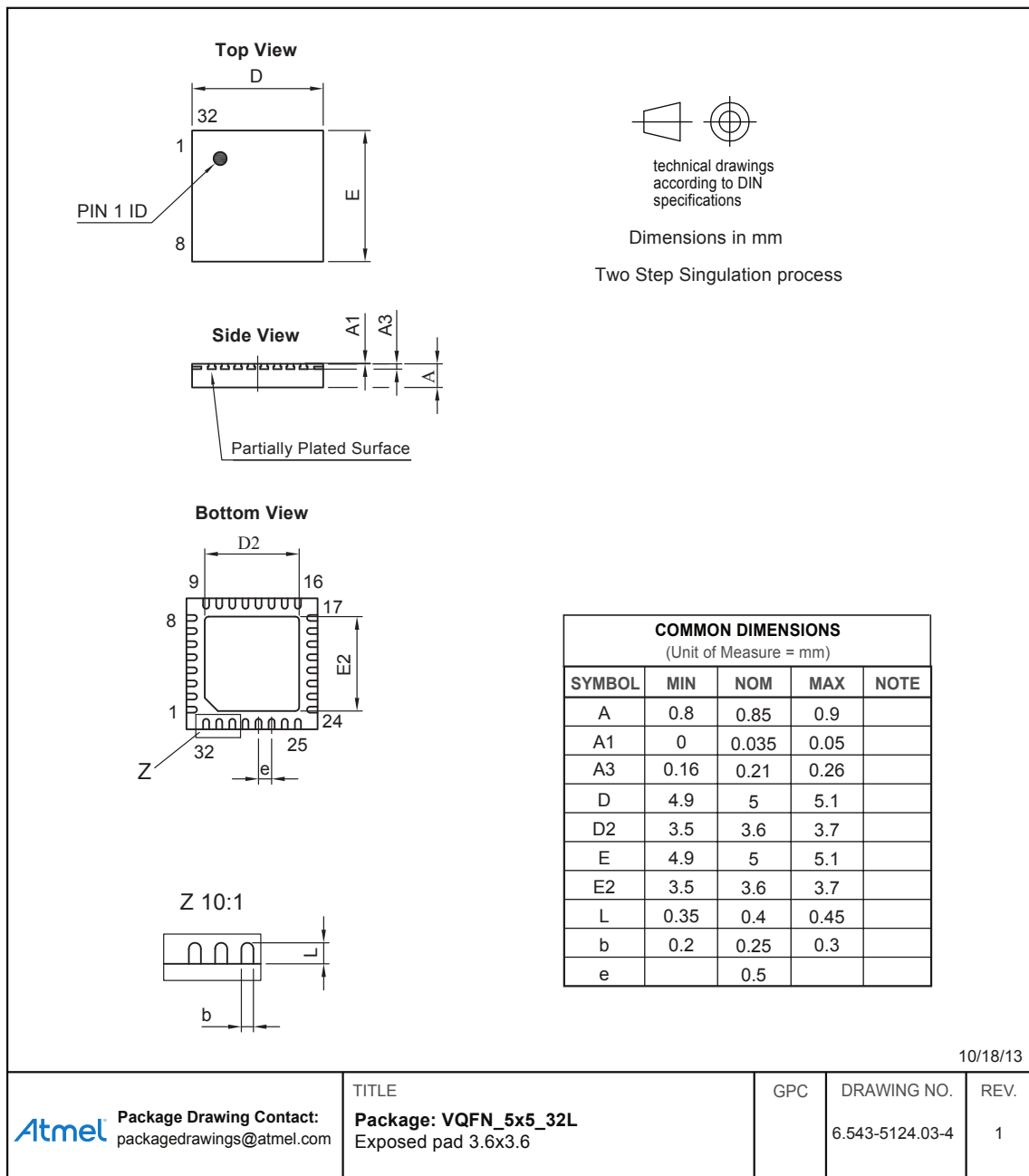


4. Ordering and Package Information

Table 4-1. Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|---------|--|
| ATA8520E-GHQW | QFN32 | 5mm × 5mm, Pb-free, 6k, taped and reeled |
| ATA8520E-GHPW | QFN32 | 5mm × 5mm, Pb-free, 1.5k, taped and reeled |

Figure 4-1. Package Information



5. Disclaimer

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6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|-------------------|---|
| 9409C-09/16 | <ul style="list-style-type: none">• Put datasheet in new template• Sections changed or added:<ul style="list-style-type: none">2.1.2.30. Read Configuration Buffer2.1.2.35. Trigger Read of FCC Channel Configuration3.7. RF Transmit Characteristics• Table changed: Table 2-4. Test and Maintenance SPI Commands• Ordering and Package Information changed |
| 9409B-INDCO-08/16 | <ul style="list-style-type: none">• Section 2.1.5 “Configuring US- and EU-Mode” on page 20 updated |

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