THE DATASHEET OF

ADT7463ARQZ-REEL7

ADT7463

Remote Thermal Controller and Voltage Monitor

The ADT7463 controller is a complete systems monitor and multiple PWM fan controller for noise−sensitive applications requiring active system cooling. It can monitor 12 V, 5 V, and 2.5 V CPU supply voltages, plus its own supply voltage. It can monitor the temperature of up to two remote sensor diodes, plus its own internal temperature. It can measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise. The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7463 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Monitors Up to 5 Supply Voltages
- Controls and Monitors up to 4 Fan Speeds
- 1 On−Chip and 2 Remote Temperature Sensors
- Monitors Up to 6 Processor VID Bits
- Dynamic T_{MIN} Control Mode Optimizes System Acoustics Intelligently
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 2−wire and 3−wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- This is a Pb−Free Device

Applications

- Low Acoustic Noise PCs
- Networking and Telecommunications Equipment

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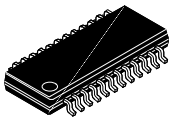
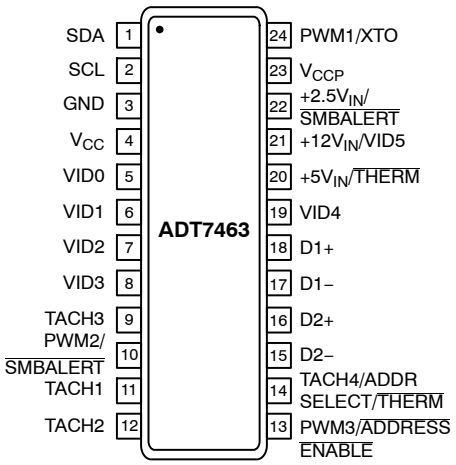


QSOP24 NB
CASE 492B

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM

ADT7463ARQZ	= Specific Device Code
#	= Pb−Free Package
YY	= Date Code
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 49 of this data sheet.

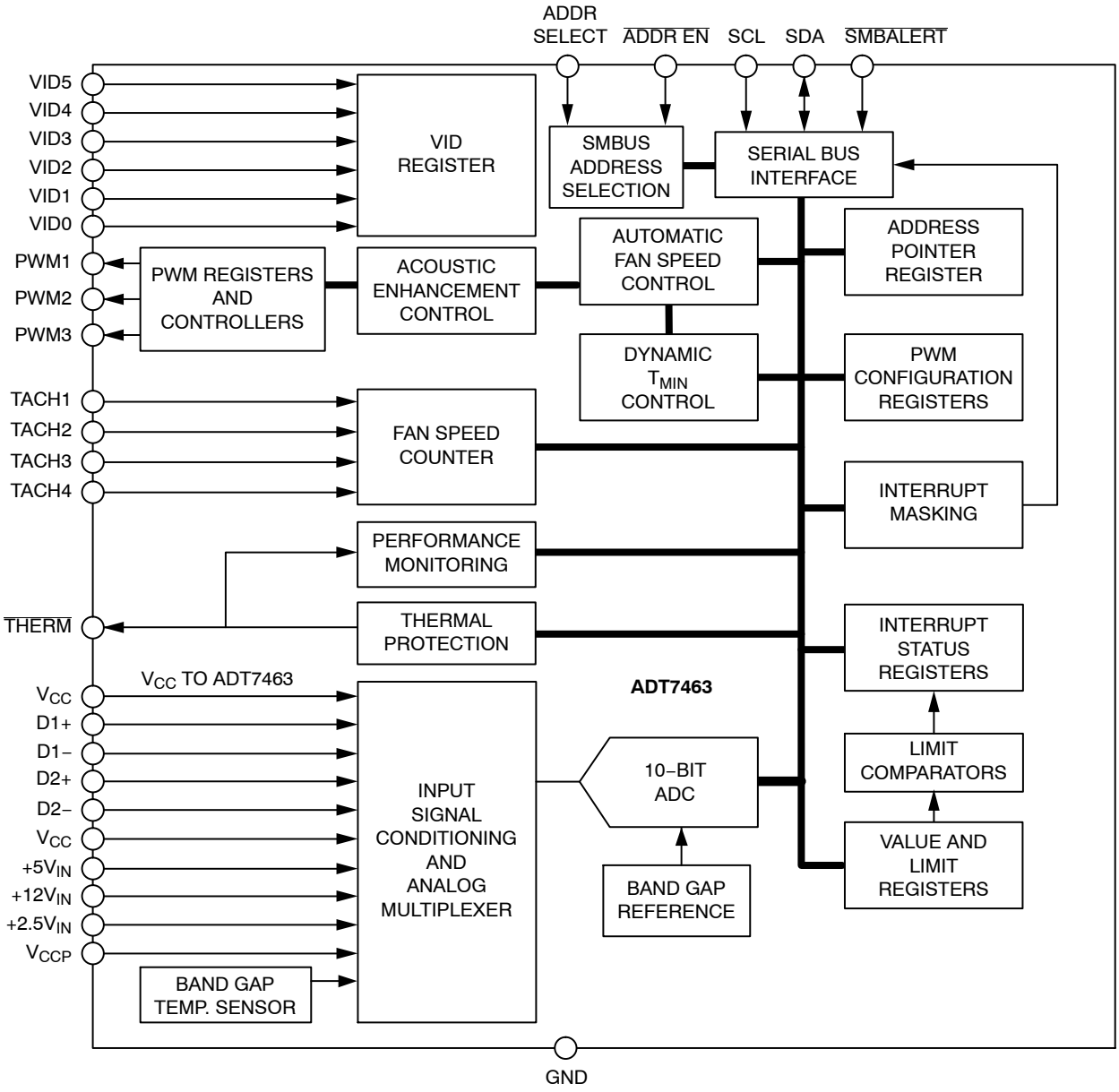


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	6.5	V
Voltage on $+12V_{IN}$ Pin	20	V
Voltage on Any Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature IR Reflow Peak Temperature for Pb−Free Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
24−lead QSOP	105	39	°C/W

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull−up.
3	GND	Ground Pin for the ADT7463.
4	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7463 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (Reg. 0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
5	VID0	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
6	VID1	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
7	VID2	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
8	VID3	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2−wire fans.
10	PWM2 $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pull−up. Pulse−width modulated output to control FAN 2 speed. Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
11	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2−wire fans.
12	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2−wire fans.
13	PWM3 $\overline{\text{ADDRESS ENABLE}}$	Digital I/O (Open Drain). Pulse−width modulated output to control Fan 3/Fan 4 speed. Requires 10 kΩ typical pull−up. If pulled low on power−up, this places the ADT7463 into address select mode, and the state of Pin 14 will determine the ADT7463's slave address.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
14	TACH4 ADDRESS SELECT $\overline{\text{THERM}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2−wire fans. If in address select mode, this pin determines the SMBus device address. Alternatively, the pin may be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
15	D2−	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1−	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4	Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
20	$+5V_{IN}$ $\overline{\text{THERM}}$	Analog Input. Monitors 5 V power supply. Alternatively, this pin may be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium® 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
21	$+12V_{IN}$ VID5	Analog Input. Monitors 12 V power supply. Digital Input (Open Drain). Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43). Supports VRM10 solutions.
22	$+2.5V_{IN}$ $\overline{\text{SMBALERT}}$	Analog Input. Monitors 2.5 V supply, typically a chipset voltage. Digital Output (Open Drain). This pin may be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
24	PWM1 XTO	Digital Output (Open Drain). Pulse−width modulated output to control Fan 1 speed. Requires 10 kΩ typical pull−up. Also functions as the output from the XOR tree in XOR test mode.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		3.0	5.0	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	− −	− −	3.0 20	mA μA
TEMPERATURE−TO−DIGITAL CONVERTER					
Local Sensor Accuracy	$0°C \le T_A \le 70°C$ $-40°C \le T_A \le +120°C$	− −	±0.5 −	±1.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Diode Sensor Accuracy	$0°C \le T_A \le 70°C$; $0°C \le T_D \le 120°C$ $0°C \le T_A \le 105°C$; $0°C \le T_D \le 120°C$ $0°C \le T_A \le 120°C$; $0°C \le T_D \le 120°C$	− − −	±0.5 − −	±1.5 ±2.5 ±3.0	°C
Resolution		−	0.25	−	°C
Remote Sensor Source Current	High Level Low Level	− −	180 11	− −	μA
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE		−	−	±1.5	%
Differential Non−linearity, DNL		−	−	±1.0	LSB
Power Supply Sensitivity		−	±0.1	−	%/V
Conversion Time (Voltage Input)	Averaging Enabled	−	11.38	13	ms
Conversion Time (Local Temperature)	Averaging Enabled	−	12.09	13.50	ms
Conversion Time (Remote Temperature)	Averaging Enabled	−	25.59	28	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	− −	120.17 13.51	134.50 15	ms

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Input Resistance		100	140	200	kΩ
FAN RPM−TO−DIGITAL CONVERTER					
Accuracy	0°C ≤ T_A ≤ 70°C 0°C ≤ T_A ≤ 105°C −40°C ≤ T_A ≤ +120°C	− − −	− − −	±7 ±11 ±13	%
Full−scale Count		−	−	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	− − − −	109 329 5,000 10,000	− − − −	RPM
Internal Clock Frequency		82.8	90.0	97.2	kHz
OPEN−DRAIN DIGITAL OUTPUTS, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}		−	−	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA, V_{CC} = 3.3 V	−	−	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	1.0	μA
OPEN−DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA, V_{CC} = 3.3 V	−	−	0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$	−	0.1	1.0	μA
SMBUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	−	−	V
Input Low Voltage, V_{IL}		−	−	0.4	V
Hysteresis		−	500	−	mV
DIGITAL INPUT LOGIC LEVELS (VID0 TO VID5)					
Input High Voltage, V_{IH}	Bit 6 (THLD) Reg. 0x43 = 0 (VID Threshold = 1 V)	1.7	−	−	V
Input Low Voltage, V_{IL}	Bit 6 (THLD) Reg. 0x43 = 0 (VID Threshold = 1 V)	−	−	0.8	V
Input High Voltage, V_{IH}	Bit 6 (THLD) Reg. 0x43 = 1 (VID Threshold = 0.6 V)	0.8	−	−	V
Input Low Voltage, V_{IL}	Bit 6 (THLD) Reg. 0x43 = 1 (VID Threshold = 0.6 V)	−	−	0.4	V
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	 Maximum Input Voltage	2.0 −	− −	− 5.5	V
Input Low Voltage, V_{IL}	 Minimum Input Voltage	− −0.3	− −	+0.8 −	V
Hysteresis		−	0.5	−	V p−p
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{THERM}}$) AGTL+					
Input High Voltage, V_{IH}		−	0.75 × V_{CCP}	−	V
Input Low Voltage, V_{IL}		−	−	0.4	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	−1.0	−	−	μA
Input Low Current, I_{IL}	V_{IN} = 0	−	−	+1.0	μA
Input Capacitance, C_{IN}		−	5.0	−	pF

Table 4. ELECTRICAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted.) (Notes 1, 2, 3, 4)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING (Note 5)					
Clock Frequency, f_{SCLK}	See Figure 2	–	–	400	kHz
Glitch Immunity, t_{SW}	See Figure 2	–	–	50	ns
Bus Free Time, t_{BUF}	See Figure 2	1.3	–	–	μs
Start Setup Time, $t_{SU;STA}$	See Figure 2	0.6	–	–	μs
Start Hold Time, $t_{HD;STA}$	See Figure 2	0.6	–	–	μs
SCL Low Time, t_{LOW}	See Figure 2	1.3	–	–	μs
SCL High Time, t_{HIGH}	See Figure 2	0.6	–	50	μs
SCL, SDA Rise Time, t_R	See Figure 2	–	–	1,000	ns
SCL, SDA Fall Time, t_F	See Figure 2	–	–	300	μs
Data Setup Time, $t_{SU;DAT}$	See Figure 2	100	–	–	ns
Data Hold Time, $t_{HD;DAT}$	See Figure 2	300	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise specified.
2. Typicals are at T_A = 25°C and represent the most likely parametric norm.
3. Logic inputs accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}.
4. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.0 V for a rising edge.
5. Guaranteed by design; not production tested

NOTE: Specifications subject to change without notice.

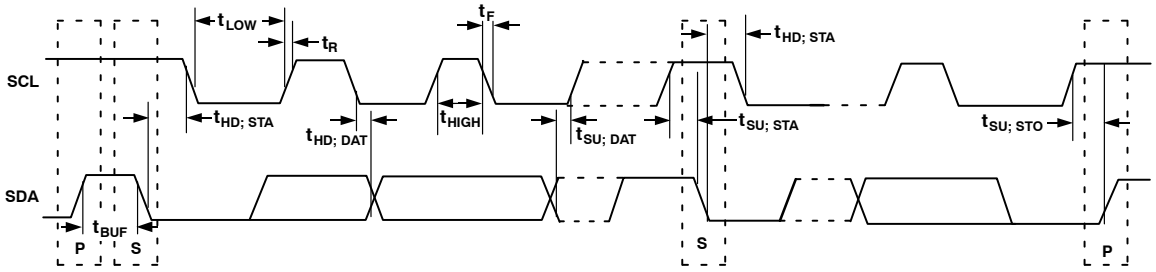


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

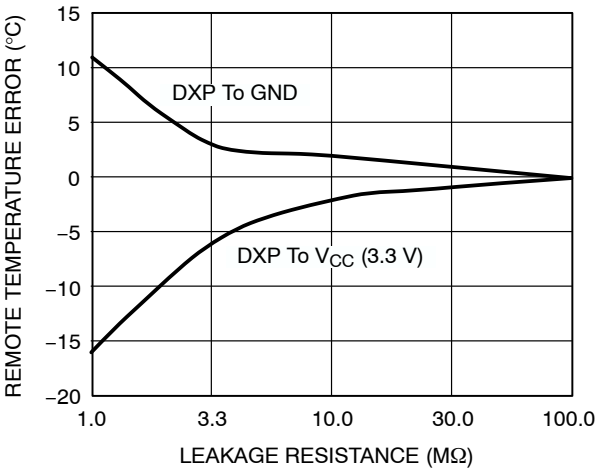


Figure 3. Remote Temperature Error vs. Leakage Resistance

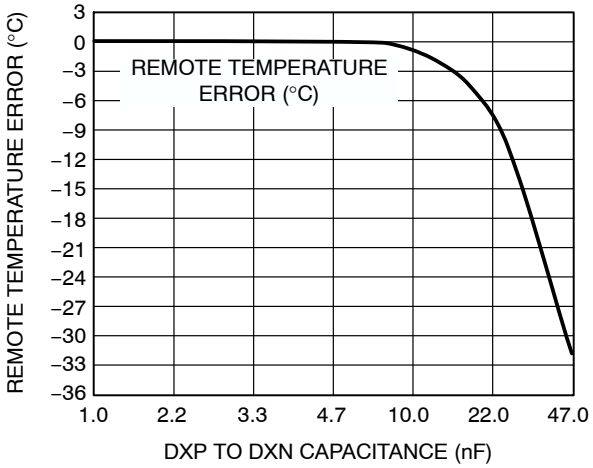


Figure 4. Remote Temperature Error vs. Capacitance between D+ and D−

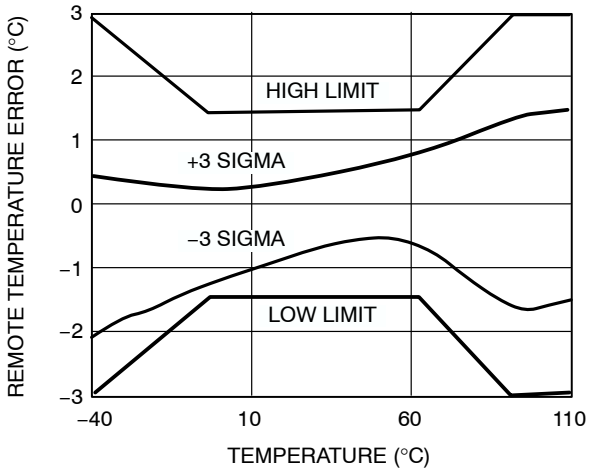


Figure 5. Remote Temperature Error vs. Actual Temperature

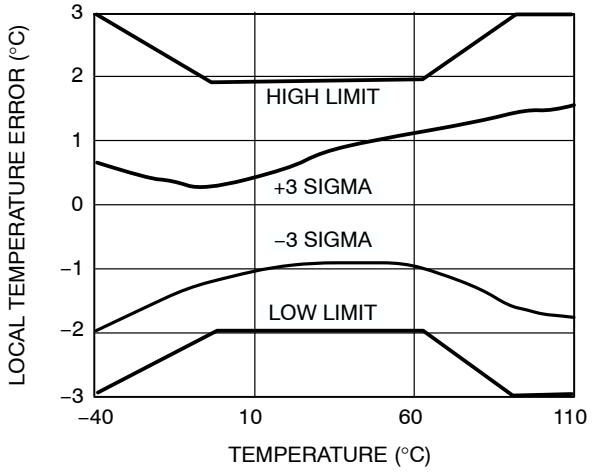


Figure 6. Local Temperature Error vs. Actual Temperature

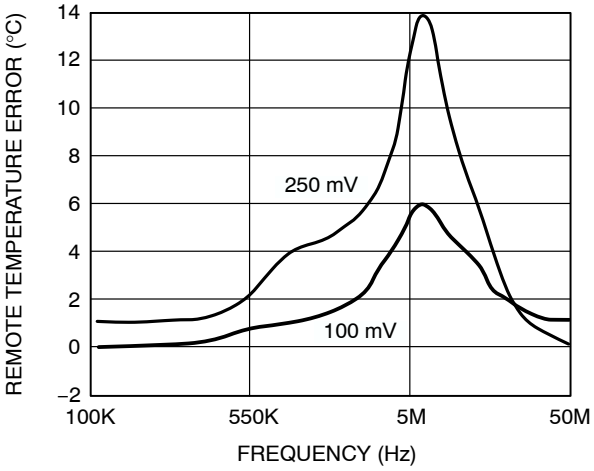


Figure 7. Remote Temperature Error vs. Power Supply Noise Frequency

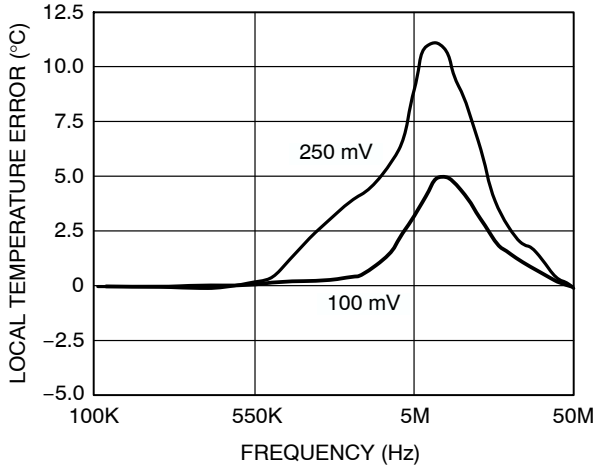


Figure 8. Local Temperature Error vs. Power Supply Noise Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

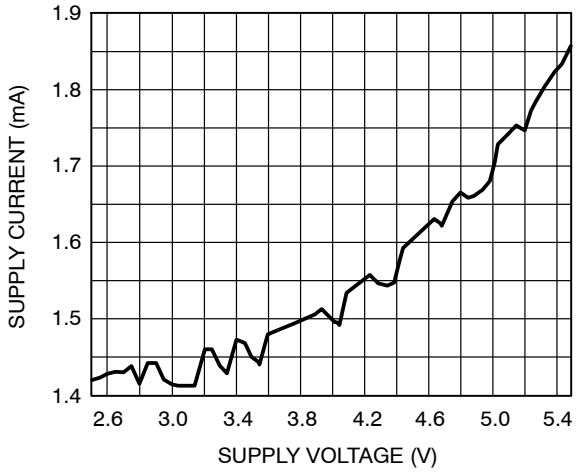


Figure 9. Supply Current vs. Supply Voltage

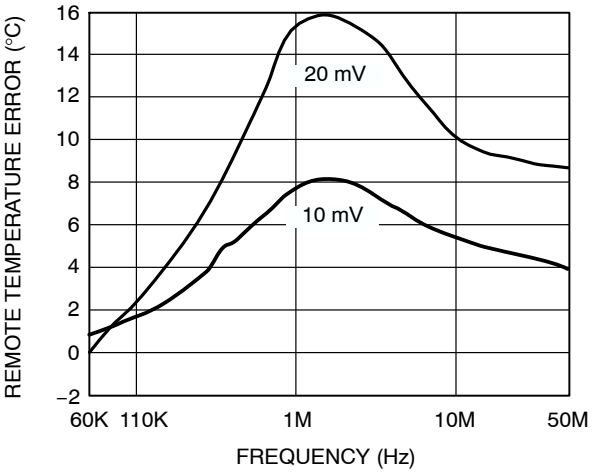


Figure 10. Remote Temperature Error vs. Differential−Mode Noise Frequency

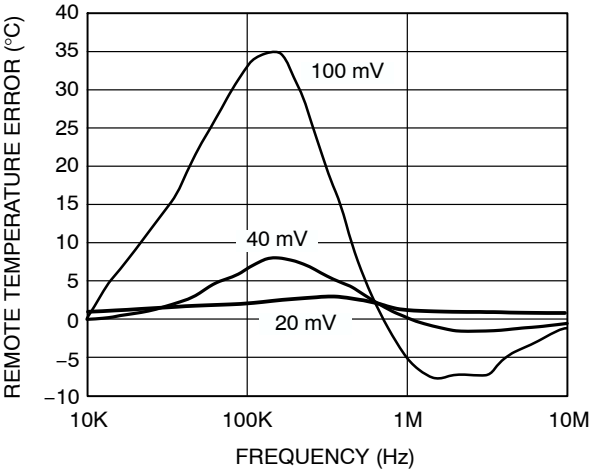


Figure 11. Remote Temperature Error vs. Common−Mode Noise Frequency

Functional Description

General Description

The ADT7463 is a complete systems monitor and multiple fan controller for any system requiring monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has an optional address line for device selection (Pin 14), a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions of the ADT7463 are performed over the serial bus. In addition, two of the pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to indicate out−of−limit conditions.

Measurement Inputs

The device has six measurement inputs, four for voltage and two for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on−chip temperature sensor.

Pins 20 through 23 are analog inputs with on−chip attenuators, configured to monitor 5 V, 12 V, 2.5 V, and the processor core voltage (2.25 V input), respectively.

Power is supplied to the chip via Pin 4, and the system also monitors V_{CC} through this pin. In PCs, this pin is normally connected to a 3.3 V standby supply. This pin can, however, be connected to a 5 V supply and monitor it without overranging.

Remote temperature sensing is provided by the D1± and D2± inputs, to which diode−connected, external temperature−sensing transistors, such as a 2N3904 or CPU thermal diode, may be connected.

The ADC also accepts input from an on−chip band gap temperature sensor that monitors system ambient temperature.

Sequential Measurement

When the ADT7463 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensors. Measured values from these inputs are stored in value registers. These can be read out over the serial bus or can be compared with programmed limits stored in the limit registers. The results of out−of−limit comparisons are stored in the status registers, which can be read over the serial bus to flag out−of−limit conditions.

Processor Voltage ID

Five digital inputs (VID0 to VID5 − Pins 5 to 8, 19, and 21) read the processor voltage ID code and store it in the VID register, from which it can be read out by the management system over the serial bus. The VID code monitoring function is compatible with both VRM9.x and future VRM10 solutions. Additionally, an $\overline{\text{SMBALERT}}$ can be generated to flag a change in VID code.

ADT7463 Address Selection

Pin 13 is the dual−function PWM3/$\overline{\text{ADDRESS ENABLE}}$ pin. If Pin 13 is pulled low on power−up, the ADT7463 reads the state of Pin 14 (TACH4/ADDRESS SELECT/ $\overline{\text{THERM}}$ pin) to determine the ADT7463's slave address. If Pin 13 is high on power−up, then the ADT7463 defaults to the SMBus slave Address 0x2E. This function is described in more detail later.

Internal Registers of the ADT7463

A brief description of the ADT7463's principal internal registers is given below. More detailed information on the function of each register is given in Tables X4 to X42.

Configuration Registers

The configuration registers provide control and configuration of the ADT7463, including alternate pinout functionality.

Address Pointer Register

This register contains the address that selects one of the other internal registers. When writing to the ADT7463, the first byte of data is always a register address, which is written to the address pointer register.

Status Registers

These registers provide the status of each limit comparison and are used to signal out−of−limit conditions on the temperature, voltage, or fan speed channels. If Pin 10 or Pin 22 is configured as $\overline{\text{SMBALERT}}$, then this pin asserts low whenever a status bit gets set.

Interrupt Mask Registers

These registers allow each interrupt status event to be masked when Pin 10 or Pin 22 is configured as an $\overline{\text{SMBALERT}}$ output.

VID Register

The status of the VID0 to VID5 pins of the processor can read from this register. VID code changes can also generate $\overline{\text{SMBALERT}}$ interrupts.

Value and Limit Registers

The results of analog voltage inputs, temperature, and fan speed measurements are stored in these registers, along with their limit values.

Offset Registers

These registers allow each temperature channel reading to be offset by a twos complement value written to these registers.

T_{MIN} Registers

These registers program the starting temperature for each fan under automatic fan speed control.

T_{RANGE} Registers

These registers program the temperature−to−fan speed control slope in automatic fan speed control mode for each PWM output.

Operating Point Registers

These registers define the target operating temperatures for each thermal zone when running under dynamic T_{MIN} control. This function allows the cooling solution to adjust dynamically in response to measured temperature and system performance.

Enhance Acoustics Registers

These registers allow each PWM output controlling fan to be tweaked to enhance the system's acoustics.

Recommended Implementation

Configuring the ADT7463 as in Figure 12 allows the systems designer the following features:

- Six VID Inputs (VID0 to VID5) for VRM10 Support
- Two PWM Outputs for Fan Control of Up to Three Fans (The Front and Rear Chassis Fans Are Connected in Parallel)
- Three TACH Fan Speed Measurement Inputs
- V_{CC} Measured Internally Through Pin 4
- CPU Core Voltage Measurement (V_{CORE})
- 2.5 V Measurement Input Used to Monitor CPU Current (Connected to V_{COMP} Output of ADP316x VRM Controller) This Is Used to Determine CPU Power Consumption
- 5 V Measurement Input
- VRM Temperature Uses Local Temperature Sensor
- CPU Temperature Measured Using Remote 1 Temperature Channel
- Ambient Temperature Measured Through Remote 2 Temperature Channel
- If Not Using VID5, This Pin Can Be Reconfigured as the 12 V Monitoring Input
- Bidirectional $\overline{\text{THERM}}$ Pin. Allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ Monitoring and Can Function as an Overtemperature $\overline{\text{THERM}}$ *O*utput
- $\overline{\text{SMBALERT}}$ System Interrupt Output

NOTE: See the AN−612 ADT7463 Configuration Application Note for more information and register settings for all possible configurations.

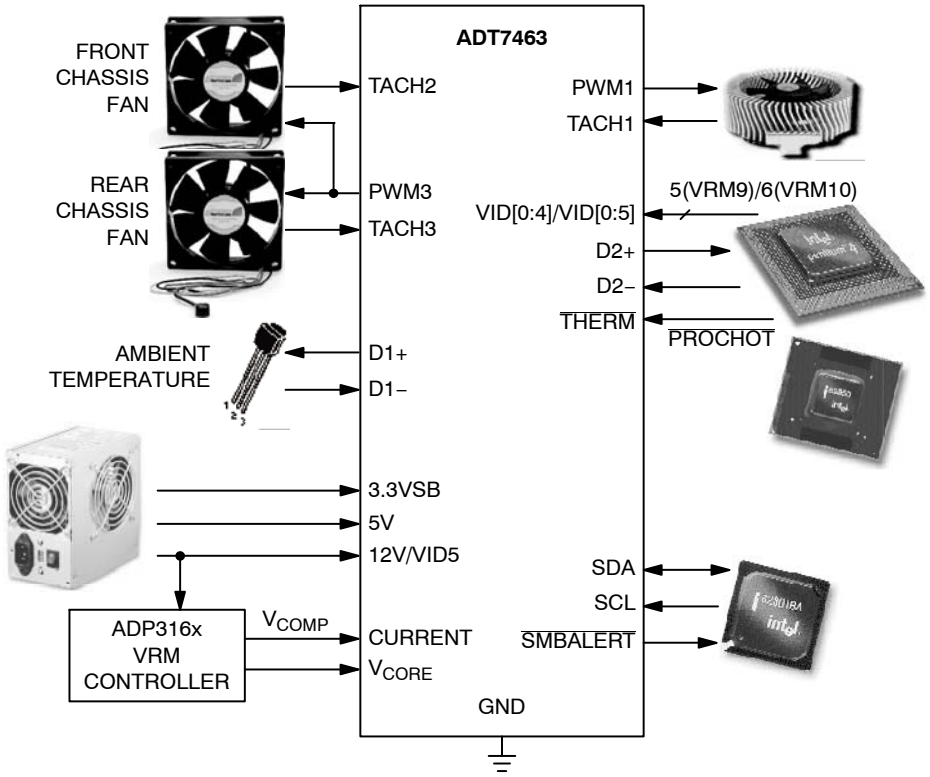


Figure 12. Recommended Implementation

Serial Bus Interface

Control of the ADT7463 is carried out using the serial system management bus (SMBus). The ADT7463 is connected to this bus as a slave device, under the control of a master controller.

The ADT7463 has a 7−bit serial bus address. When the device is powered up with Pin 13 (PWM3/ $\overline{\text{ADDRESS ENABLE}}$) high, the ADT7463 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8−bit address. If more than one ADT7463 is used in a system, then each ADT7463 should be placed in address select mode by strapping Pin 13 low on power−up. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled upon power−up.

The device address is sampled and latched on the first valid SMBus transaction, more precisely on the low−to−high transition at the beginning of the 8th SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the address enable/address select pins. Any attempted changes in the address will have no effect after this.

Table 5. ADDRESS SELECT MODE

Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull−up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)

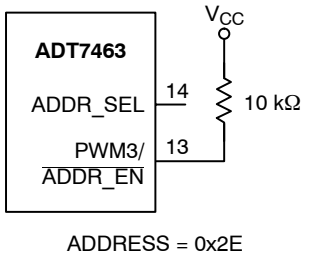


Figure 13. Default SMBus Address = 0x2E

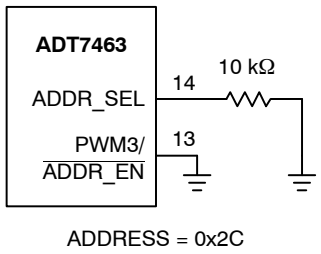


Figure 14. SMBus Address = 0x2C (Pin 14 = 0)

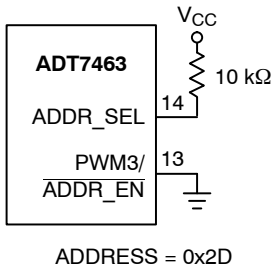
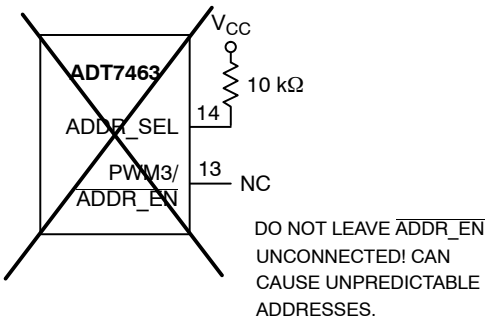


Figure 15. SMBus Address = 0x2D (Pin 14 = 1)



CARE SHOULD BE TAKEN TO ENSURE THAT PIN 13 (PWM3/$\overline{\text{ADDR\_EN}}$) IS EITHER TIED HIGH OR LOW. LEAVING PIN 13 FLOATING COULD CAUSE THE ADT7463 TO POWERUP WITH AN UNEXPECTED ADDRESS.

NOTE THAT IF THE ADT7463 IS PLACED INTO ADDRESS SELECT MODE, PINS 13 AND 14 CAN BE USED AS THE ALTERNATE FUNCTIONS (PWM3, TACH4/$\overline{\text{THERM}}$) ONLY IF THE CORRECT CIRCUIT IS MUXED IN AT THE CORRECT TIME.

Figure 16. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7463 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high−to−low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus a R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.
   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth

clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, then the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low−to−high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master pulls the data line high during the tenth clock pulse to assert a STOP condition. In READ mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADT7463, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 17. The device address is sent over the bus followed by R/$\overline{W}$ being set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

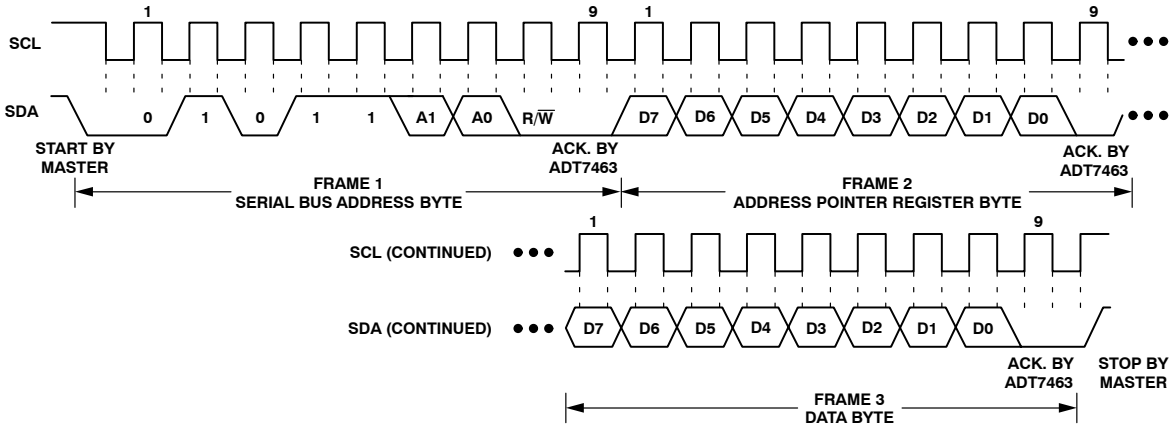


Figure 17. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

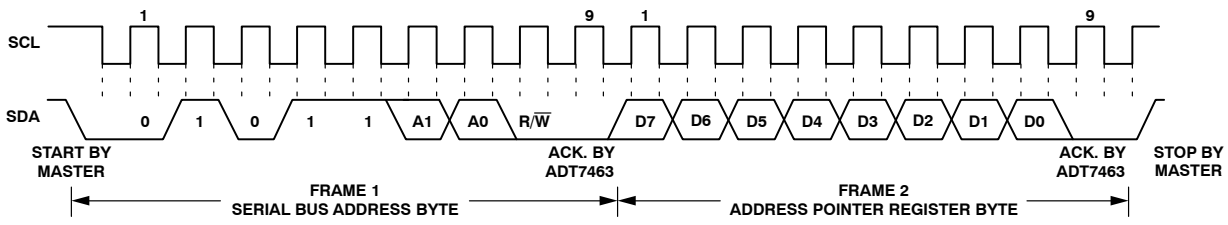


Figure 18. Writing to the Address Pointer Register Only

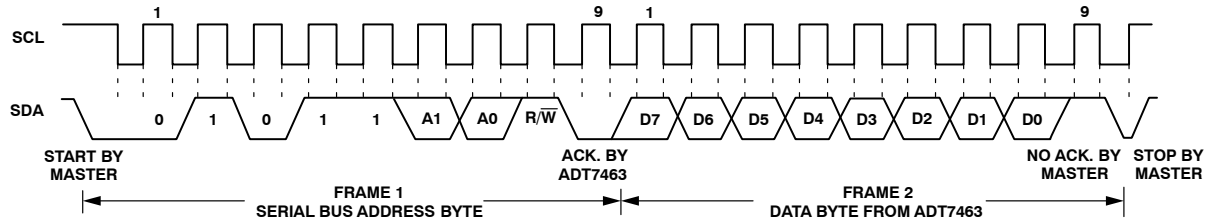


Figure 19. Reading Data from a Previously Selected Register

When reading data from a register, there are two possibilities:

1. If the ADT7463's address pointer register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7463 as before, however, only the data byte is sent and this contains the register address. This is shown in Figure 18.
   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 19.
2. If the address pointer register is already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, so Figure 18 can be omitted.

NOTES:

1. It is possible to *read* a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to *write* data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.
2. In Figures 17 to 19, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the address select mode function previously defined.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADT7463 also supports the Read Byte protocol (see System Management Bus specifications Rev. 2.0 for more information).
4. If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

ADT7463 Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7463 are discussed below. The following abbreviations are used in the diagrams:

S – START
P – STOP
R – READ
W – WRITE
A – ACKNOWLEDGE
$\overline{A}$ – NO ACKNOWLEDGE

The ADT7463 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the write bit (low)
3. The addressed slave device asserts ACK on SDA
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master asserts a stop condition on SDA and the transaction ends

For the ADT7463, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This is illustrated in Figure 20.

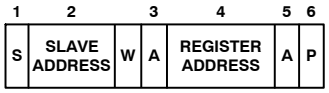


Figure 20. Setting a Register Address for Subsequent Read

If it is required to read data from the register immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the write bit (low)
3. The addressed slave device asserts ACK on SDA
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master sends a data byte
7. The slave asserts ACK on SDA
8. The master asserts a stop condition on SDA to end the transaction

This is illustrated in Figure 21.

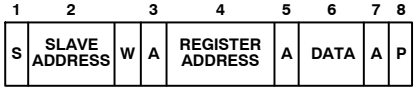


Figure 21. Single Byte Write to a Register

ADT7463 Read Operations

The ADT7463 uses the following SMBus read protocols.

Receive Byte

This is useful when repeatedly reading a single register. The register address needs to have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA
2. The master sends the 7−bit slave address followed by the read bit (high)
3. The addressed slave device asserts ACK on SDA
4. The master receives a data byte
5. The master asserts NO ACK on SDA
6. The master asserts a stop condition on SDA and the transaction ends

In the ADT7463, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation.

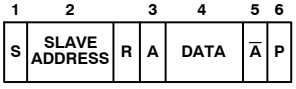


Figure 22. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as an interrupt output or can be used as an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address will have priority in accordance with normal SMBus arbitration
5. Once the ADT7463 has responded to the alert response address, the master must read the status registers and the $\overline{\text{SMBALERT}}$ will only be cleared if the error condition has gone away

SMBus Timeout

The ADT7463 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7463 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description
<6> TODIS	0: SMBus Timeout Enabled (Default)
<6> TODIS	1: SMBus Timeout Disabled

Voltage Measurement Inputs

The ADT7463 has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pins 20 to 23 are dedicated to measuring 5 V, 12 V, and 2.5 V supplies and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). Setting Bit 7 of Configuration Register 1 (Reg. 0x40) allows a 5 V supply to power the ADT7463 and be measured without overranging the V_{CC} measurement channel. The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

Analog−to−Digital Converter (ADC)

All analog inputs are multiplexed into the on−chip, successive approximation, ADC. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built−in attenuators to allow measurement of 2.5 V, 3.3 V, 5 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow for the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 23. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first−order, low−pass filter that gives the input immunity to high frequency noise.

Table 7. VOLTAGE MEASUREMENT REGISTERS

Register	Description	Default
0x20	2.5 V Reading	0x00
0x21	V_{CCP} Reading	0x00
0x22	V_{CC} Reading	0x00
0x23	5 V Reading	0x00
0x24	12 V Reading	0x00

Associated with each voltage measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 8. VOLTAGE MEASUREMENT LIMITS REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

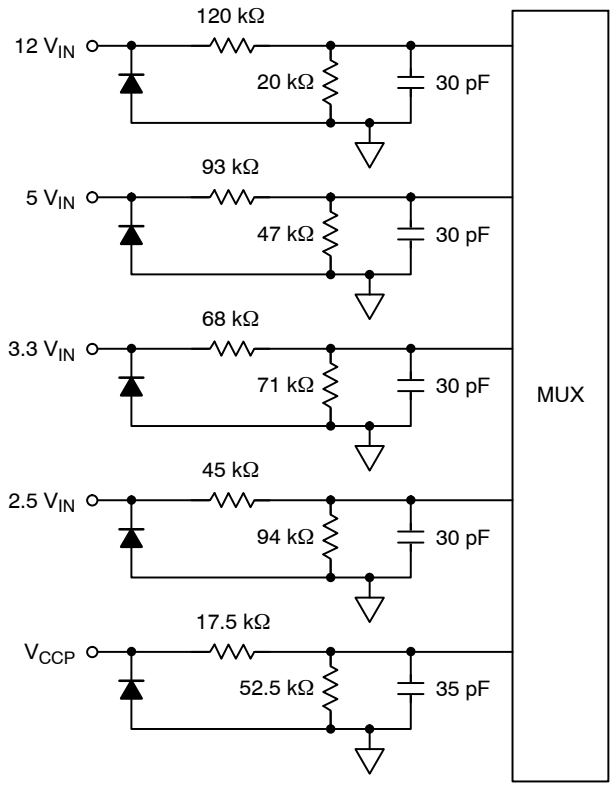


Figure 23. Structure of Analog Inputs

Table 12 shows the input ranges of the analog inputs and output codes of the 10−bit ADC.

When the ADC is running, it samples and converts a voltage input in 711 μs and averages 16 conversions to reduce noise; a measurement on each input takes nominally 11.38 ms.

VID Code Monitoring

The ADT7463 has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID register (Reg. 0x43) to determine the processor voltage required/being used in the system. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

Table 9. VID CODE REGISTER (REG. 0X43)

Bit	Description
<0> VID0	Reflects Logic State of Pin 5
<1> VID1	Reflects Logic State of Pin 6
<2> VID2	Reflects Logic State of Pin 7
<3> VID3	Reflects Logic State of Pin 8
<4> VID4	Reflects Logic State of Pin 19
<5> VID5	Reconfigurable 12 V Input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID Code Input Threshold Voltage

The switching threshold for the VID code inputs is approximately 1 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of VID register (Reg. 0x43) controls the VID input threshold voltage.

Table 10. VID CODE REGISTER (REG. 0X43)

Bit	Description
<6> THLD	0: VID Switching Threshold = 1 V, V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V 1: VID Switching Threshold = 0.6 V, V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V

Reconfiguring Pin 21 (+12V/VID5) as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10−compatible systems. Since the pin is configured as VID5, it is no longer possible to monitor a 12 V supply.

Bit 7 of the VID register (Reg. 0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or is monitoring a sixth VID input.

Table 11. VID CODE REGISTER (REG. 0X43)

Bit	Description
<7> VIDSEL	0: Pin 21 functions as a 12 V measurement input. Software can read this bit to determine that there are five VID inputs being monitored. Bit 5 of Register 0x43 (VID5) always reads back 0. Bit 0 of Status Register 2 (Reg. 0x42) reflects 12 V out−of−limit measurements. 1: Pin 21 functions as the sixth VID code input (VID5). Software can read this bit to determine that there are six VID inputs being monitored. Bit 5 of Register 0x43 reflects the logic state of Pin 21. Bit 0 of Status Register 2 (Reg. 0x42) reflects VID code changes.

Table 12. 10−BIT A/D OUTPUT CODE VS. V_{IN}

Input Voltage					A/D Output	
$+12V_{IN}$	$+5V_{IN}$	V_{CC} ($3.3V_{IN}$) (Note 1)	$+2.5V_{IN}$	$+V_{CCP}$	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156–0.0312	0.0065–0.0130	0.0042–0.0085	0.0032–0.0065	0.0293–0.0058	1	00000000 01
0.0312–0.0469	0.0130–0.0195	0.0085–0.0128	0.0065–0.0097	0.0058–0.0087	2	00000000 10
0.0469–0.0625	0.0195–0.0260	0.0128–0.0171	0.0097–0.0130	0.0087–0.0117	3	00000000 11
0.0625–0.0781	0.0260–0.0325	0.0171–0.0214	0.0130–0.0162	0.0117–0.0146	4	00000001 00
0.0781–0.0937	0.0325–0.0390	0.0214–0.0257	0.0162–0.0195	0.0146–0.0175	5	00000001 01
0.0937–0.1093	0.0390–0.0455	0.0257–0.0300	0.0195–0.0227	0.0175–0.0205	6	00000001 10
0.1093–0.1250	0.0455–0.0521	0.0300–0.0343	0.0227–0.0260	0.0205–0.0234	7	00000001 11
0.1250–0.14060	0.0521–0.0586	0.0343–0.0386	0.0260–0.0292 • • •	0.0234–0.0263	8	00000010 00
4.0000–4.0156	1.6675–1.6740	1.1000–1.1042	0.8325–0.8357 • • •	0.7500–0.7529	256 (1/4 Scale)	01000000 00
8.0000–8.0156	3.3300–3.3415	2.2000–2.2042	1.6650–1.6682 • • •	1.5000–1.5029	512 (1/2 Scale)	10000000 00
12.0000–12.0156	5.0025–5.0090	3.3000–3.3042	2.4975–2.5007 • • •	2.2500–2.2529	768 (3/4 Scale)	11000000 00
15.8281–15.8437	6.5983–6.6048	4.3527–4.3570	3.2942–3.2974	2.9677–2.9707	1013	11111101 01
15.8437–15.8593	6.6048–6.6113	4.3570–4.3613	3.2974–3.3007	2.9707–2.9736	1014	11111101 10
15.8593–15.8750	6.6113–6.6178	4.3613–4.3656	3.3007–3.3039	2.9736–2.9765	1015	11111101 11
15.8750–15.8906	6.6178–6.6244	4.3656–4.3699	3.3039–3.3072	2.9765–2.9794	1016	11111110 00
15.8906–15.9062	6.6244–6.6309	4.3699–4.3742	3.3072–3.3104	2.9794–2.9824	1017	11111110 01
15.9062–15.9218	6.6309–6.6374	4.3742–4.3785	3.3104–3.3137	2.9824–2.9853	1018	11111110 10
15.9218–15.9375	6.6374–6.4390	4.3785–4.3828	3.3137–3.3169	2.9853–2.9882	1019	11111110 11
15.9375–15.9531	6.6439–6.6504	4.3828–4.3871	3.3169–3.3202	2.9882–2.9912	1020	11111111 00
15.9531–15.9687	6.6504–6.6569	4.3871–4.3914	3.3202–3.3234	2.9912–2.9941	1021	11111111 01
15.9687–15.9843	6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	2.9941–2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

1. The V_{CC} output codes listed assume that V_{CC} is 3.3 V. If V_{CC} input is reconfigured for 5 V operation (by setting Bit 7 of Configuration Register 1), then the V_{CC} output codes are the same as for the $+5V_{IN}$ column.

VID Code Change Detect Function

The ADT7463 has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes can be detected and reported back by the ADT7463. Bit 0 of Status Register 2 (Reg. 0x42) is the 12V/VC bit and denotes a VID change when set. The VID code change bit gets set when the logic states on the VID inputs are different than they were 11 μs previously. The change of VID code can be used to generate an $\overline{\text{SMBALERT}}$ interrupt. If an $\overline{\text{SMBALERT}}$ interrupt is not required, Bit 0 of Interrupt Mask Register 2 (Reg. 0x75), when set, prevents $\overline{\text{SMBALERT}}$s from occurring on VID code changes.

Table 13. STATUS REGISTER (REG. 0X42)

Bit	Description
<0> 12V/VC	0: If Pin 21 is configured as VID5, then a Logic 0 denotes no change in VID code within last 11 μs. 1: If Pin 21 is configured as VID5, then a Logic 1 means that a change has occurred on the VID code inputs within the last 11 μs. An $\overline{\text{SMBALERT}}$ generates if this function is enabled.

Additional ADC Functions for Voltage Measurement

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility, including:

Turn−off Averaging

For each voltage measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. There may be an instance where you would like to speed up conversions. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (Reg 0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single−channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7463 into single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read a single voltage channel only. If the internal ADT7463 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 Minimum High Byte Register (0x55).

Table 14. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<5>	1: Bypass Input Attenuators
<6>	1: Single−channel Convert Mode

Table 15. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description	
<7:5>	Selects ADC Channel for Single−channel Convert Mode	
	Value	**Channel Selected**
	000	2.5 V
	001	V_{CCP}
	010	V_{CC}
	011	5 V
	100	12 V

Temperature Measurement System

Local Temperature Measurement

The ADT7463 contains an on−chip band gap temperature sensor whose output is digitized by the on−chip 10−bit ADC. The 8−bit MSB temperature data is stored in the local temperature register (Address 26h). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 16. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside this range are not possible.

Remote Temperature Measurement

The ADT7463 can measure the temperature of two remote diode sensors or diode−connected transistors connected to Pins 15 and 16, or 17 and 18.

The forward voltage of a diode or diode−connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7463 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by

$$\Delta V_{BE} = KT/q \times \ln(N) \qquad \text{(eq. 1)}$$

where:

K is Boltzmann's constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvins.

N is the ratio of the two currents.

Figure 24 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could equally well be a discrete transistor, such as a 2N3904.

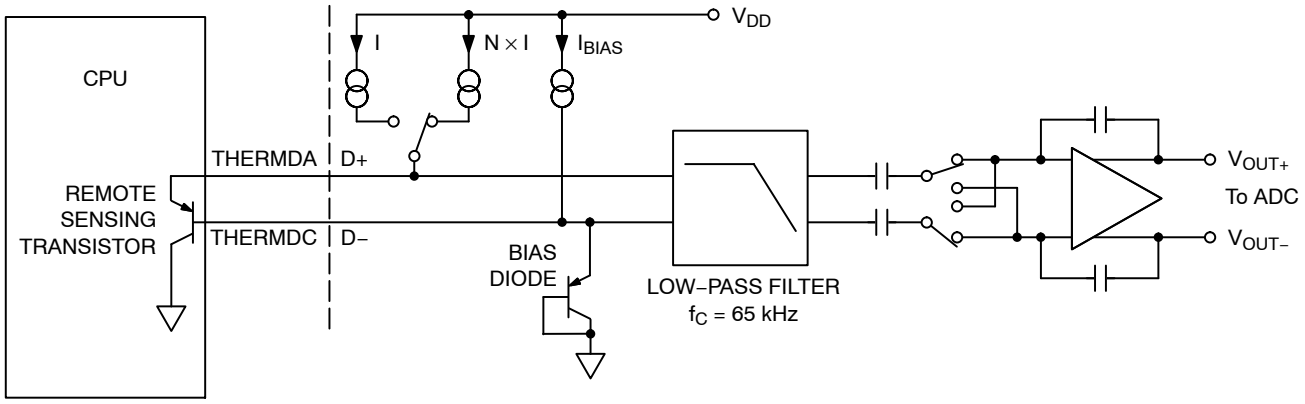


Figure 24. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector will not be grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figures 25 and 26 show how to connect the ADT7463 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D– input.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low−pass filter to remove noise and to a chopper−stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10−bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 25.5 ms. The results of remote temperature measurements are stored in 10−bit, twos complement format, as illustrated in Table 16. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

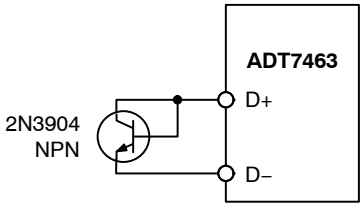


Figure 25. Measuring Temperature by Using an NPN Transistor

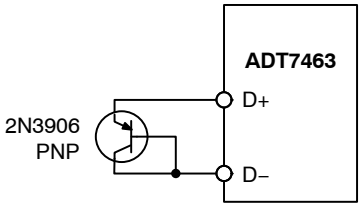


Figure 26. Measuring Temperature by Using a PNP Transistor

Table 16. TEMPERATURE DATA FORMAT

Temperature	Digital Output (10−bit) (Note 1)
−128°C	1000 0000 **00**
−125°C	1000 0011 **00**
−100°C	1001 1100 **00**
−75°C	1011 0101 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 17. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	0x80
0x26	Local Temperature	0x80
0x27	Remote 2 Temperature	0x80
0x77	Extended Resolution 2	0x00

Table 18. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS (REG. 0X77)

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Reading Temperature from the ADT7463

It is important to note that temperature can be read from the ADT7463 as an 8−bit value (with 1°C resolution) or as a 10−bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10−bit measurement is required, this involves a 2−register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its 2 LSBs are being read and vice versa.

Nulling Out Temperature Errors

As CPUs run faster, it is getting more difficult to avoid high frequency clocks when routing the D+, D− traces around a system board. Even when recommended layout guidelines are followed, there may still be temperature errors attributed to noise being coupled onto the D+/D− lines. High frequency noise generally has the effect of giving temperature measurements that are too high by a constant amount. The ADT7463 has temperature offset registers at Addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one−time calibration of the system, one can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8−bit reading to every temperature measurement. The LSBs add 0.25°C offset to the temperature reading so the 8−bit register effectively allows temperature offsets of up to ±32°C with a resolution of 0.25°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Table 19. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 20. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Registers 0x6A to 0x6C are the $\overline{\text{THERM}}$ limits. When a temperature exceeds its $\overline{\text{THERM}}$ limit, all fans run at 100% duty cycle. The fans stay running at 100% until the temperature drops below $\overline{\text{THERM}}$ – Hysteresis (this can be disabled by setting the boost bit in Configuration Register 3, Bit 2, Register 0x78). The hysteresis value for that $\overline{\text{THERM}}$ limit is the value programmed into Registers 0x6D, 0x6E (hysteresis registers). The default hysteresis value is 4°C.

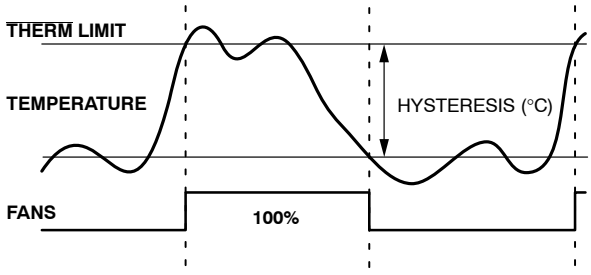


Figure 27. $\overline{\text{THERM}}$ Limit Operation

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7463 to offer the systems designer increased flexibility.

Turn−off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged before being placed into the value register. Sometimes it may be necessary to take a very fast measurement, e.g., of CPU temperature. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This takes a reading every 13 ms. The measurement itself takes 4 ms.

Single−channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7463 into single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read a single temperature channel only. If the internal ADT7463 clock is used, the selected input is read every 1.4 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 Minimum High Byte Register (0x55).

Table 21. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description
<4>	1: Averaging Off
<6>	1: Single−channel Convert Mode

Table 22. TACH1 MINIMUM HIGH BYTE (REG. 0X55)

Bit	Description	
<7:5>	Selects ADC Channel for Single−channel Convert Mode	
	Value	Channel Selected
	101	Remote 1 Temp
	110	Local Temp
	111	Remote 2 Temp

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the ADT7463 are high and low limits. These can form the basis of system status monitoring: a status bit can be set for any out−of−limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out−of−limit conditions.

8−bit Limits

The following is a list of 8−bit limits on the ADT7463.

Table 23. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x44	2.5 V Low Limit	0x00
0x45	2.5 V High Limit	0xFF
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF
0x4A	5 V Low Limit	0x00
0x4B	5 V High Limit	0xFF
0x4C	12 V Low Limit	0x00
0x4D	12 V High Limit	0xFF

Table 24. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64

Table 25. $\overline{\text{THERM}}$ LIMIT REGISTERS

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Limit	0x00

16−bit Limits

The fan TACH measurements are 16−bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Since fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Since fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 26. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out−of−Limit Comparisons

Once all limits are programmed, the ADT7463 can be enabled for monitoring. The ADT7463 measures all parameters in round−robin format and sets the appropriate status bit for out−of−limit conditions. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed

Low Limit: < or = Comparison Performed

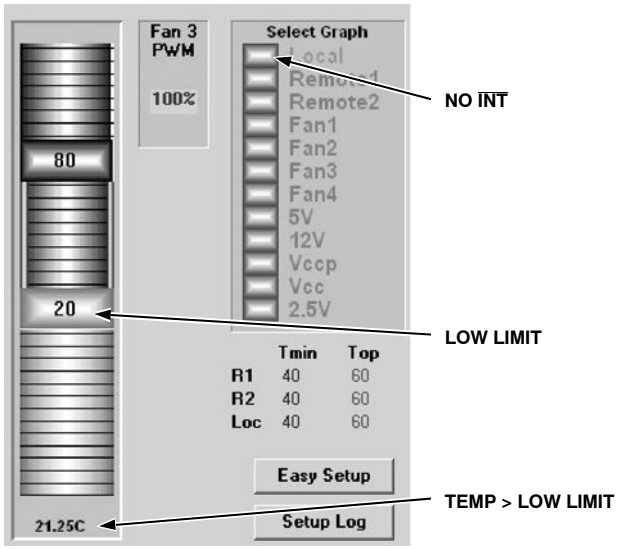


Figure 28. Temperature > Low Limit: No $\overline{INT}$

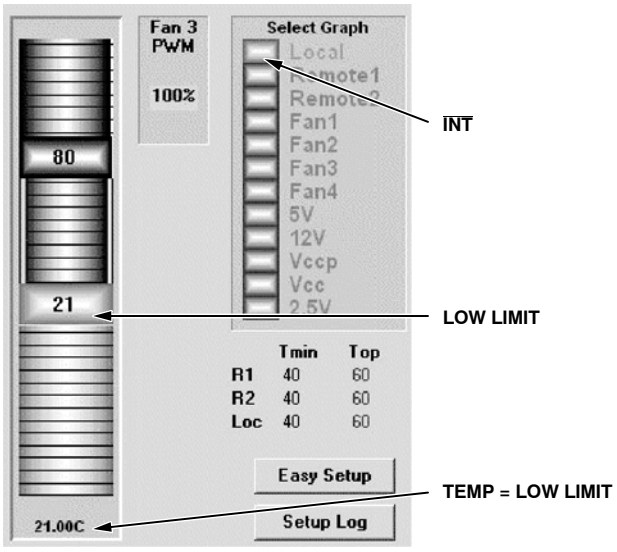


Figure 29. Temperature = Low Limit: $\overline{INT}$ Occurs

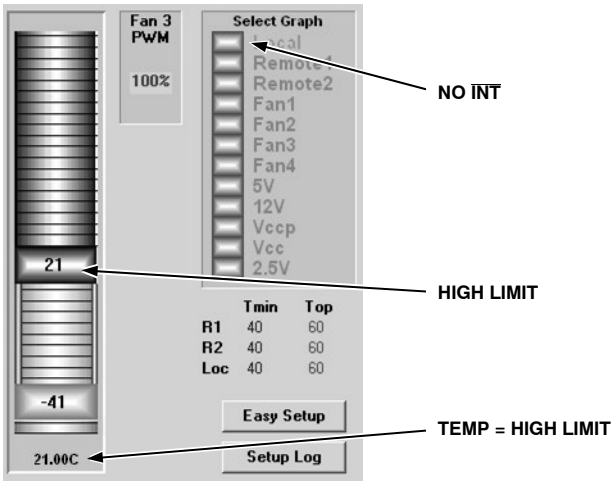


Figure 30. Temperature = High Limit: No $\overline{INT}$

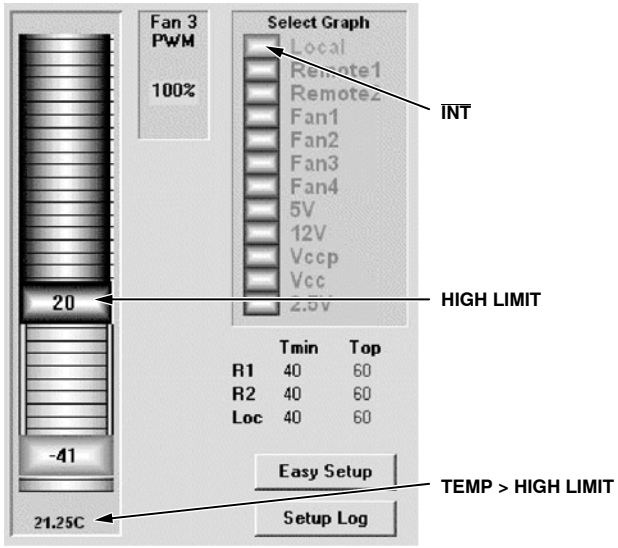


Figure 31. Temperature > High Limit: $\overline{INT}$ Occurs

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn and as each measurement is completed, the result is automatically stored in the appropriate value register. This round−robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

Because the ADC is normally left to free−run in this manner, the time taken to monitor all the analog inputs is normally not of interest, since the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it is easily calculated.

The total number of channels measured is:

- Four Dedicated Supply Voltage Inputs
- 3.3 V_{STBY} or 5 V Supply (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round−robin conversions and takes 11.38 ms for each voltage measurement, 12 ms for a local temperature reading, and 25.5 ms for each remote temperature reading.

The total monitoring cycle time for averaged voltage and temperature monitoring is therefore nominally

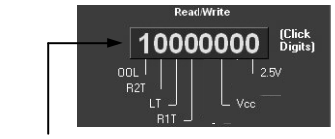
$$(5 \times 11.38) + 12\ (2 \times 25.5) = 120\ \text{ms} \quad \text{(eq. 2)}$$

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Status Registers 1 and 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out−of−limits, the corresponding status register bit is set to 1.

The state of the various measurement channels may be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Status Register 1 (Reg. 0x41), 1 means that an out−of−limit event has been flagged in Status Register 2. This means that a user need only read Status Register 2 when this bit is set. Alternatively, Pin 10 or Pin 22 can be configured as an $\overline{\text{SMBALERT}}$ output. This automatically notifies the system supervisor of an out−of−limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are “sticky.” Whenever a status bit gets set, indicating an out−of−limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out−of−limit, its associated status bit gets set in the interrupt status registers.

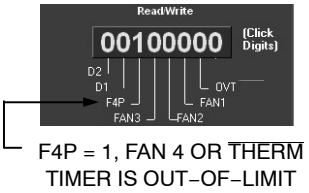


OOL = 1 DENOTES A PARAMETER MONITORED THROUGH STATUS REG 2 IS OUT−OF−LIMIT

Figure 32. Status Register 1

Table 27. STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1: denotes a bit in Status Register 2 is set and Status Register 2 should be read.
6	R2T	1: Remote 2 Temperature High or Low Limit has been exceeded.
5	LT	1: Local Temperature High or Low Limit has been exceeded.
4	R1T	1: Remote 1 Temperature High or Low Limit has been exceeded.
3	5V	1: 5 V High or Low Limit has been exceeded.
2	V_{CC}	1: V_{CC} High or Low Limit has been exceeded.
1	V_{CCP}	1: V_{CCP} High or Low Limit has been exceeded.
0	2.5V	1: 2.5 V High or Low Limit has been exceeded.



F4P = 1, FAN 4 OR $\overline{\text{THERM}}$ TIMER IS OUT−OF−LIMIT

Figure 33. Status Register 2

Table 28. STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D2+/D2− inputs.
5	F4P	1 indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ limit has been exceeded if the $\overline{\text{THERM}}$ function is used.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.
0	12V/VC	1 indicates that 12 V High or Low Limit has been exceeded. If the VID code change function is used, this bit indicates a change in VID code on the VID0 to VID5 inputs.

SMBALERT Interrupt Behavior

The ADT7463 can be polled for status, or an SMBALERT interrupt can be generated for out−of−limit conditions. It is important to note how the SMBALERT output and status bits behave when writing Interrupt Handler software.

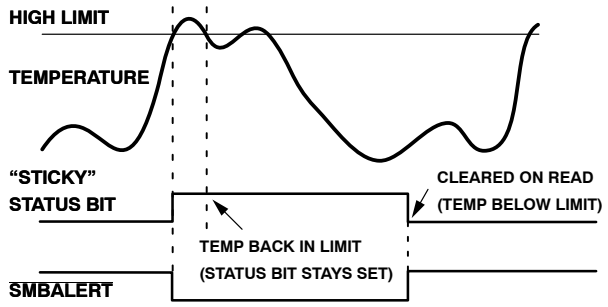


Figure 34. SMBALERT and Status Bit Behavior

Figure 34 shows how the SMBALERT output and "sticky" status bits behave. Once a limit is exceeded, the corresponding status bit gets set to 1. The status bit remains set until the error condition subsides and the status register gets read. The status bits are referred to as sticky since they remain set until read by software. This ensures that an out−of−limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low for the entire duration that a reading is out−of−limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74, 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the Interrupt Handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 35.

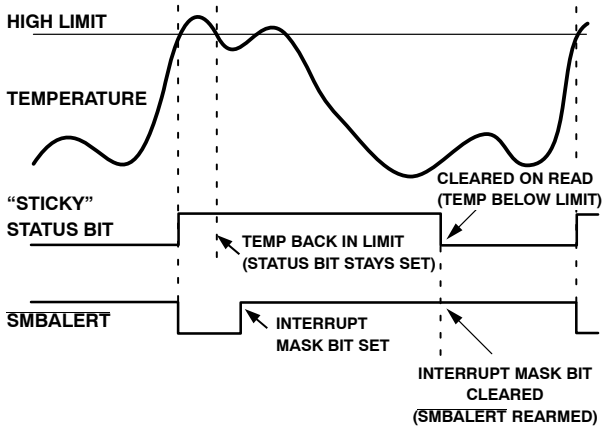


Figure 35. How Masking the Interrupt Source Affects SMBALERT Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent SMBALERT interrupts. Note that masking an interrupt source only prevents the SMBALERT output from being asserted; the appropriate status bit gets set as normal.

Table 29. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature.
5	LT	1 masks SMBALERT for Local Temperature.
4	R1T	1 masks SMBALERT for Remote 1 Temperature.
3	5V	1 masks SMBALERT for 5 V channel.
2	V_{CC}	1 masks SMBALERT for V_{CC} channel.
1	V_{CCP}	1 masks SMBALERT for V_{CCP} channel.
0	2.5V	1 masks SMBALERT for 2.5 V channel.

Table 30. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).
0	12V/VC	1 masks SMBALERT for 12 V channel or for a VID code change, depending on the function used.

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 10 or Pin 22 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out−of−limit conditions.

Table 31. CONFIGURATION PIN 22 AS $\overline{\text{SMBALERT}}$ OUTPUT (REG. 0X78)

Register	Bit Setting
Config Reg 3	<0> ALERT = 1

Table 32. CONFIGURATION PIN 22 AS $\overline{\text{SMBALERT}}$ OUTPUT (REG. 0X7D)

Register	Bit Setting
Config Reg 4	<0> AL2.5V = 1

To Assign $\overline{\text{THERM}}$ Functionality to a Pin

Pin 14 or Pin 20 can be configured as the $\overline{\text{THERM}}$ pin on the ADT7463.

To enable the $\overline{\text{THERM}}$ functionality, users must first set the $\overline{\text{THERM}}$ enable bit. The TH5V bit then determines which pin the $\overline{\text{THERM}}$ functionality is enabled on (i.e., users cannot enable $\overline{\text{THERM}}$ on two pins at once).

To configure Pin 20 as the $\overline{\text{THERM}}$ pin:

1. Set the TH5V bit (Bit 1) in the Configuration Register 4 (Address = 0x7D) = 1.
2. Set the $\overline{\text{THERM}}$ Enable Bit (Bit 1) in the Configuration Register 3 (Address = 0x78) = 1.

To configure Pin 14 as the $\overline{\text{THERM}}$ pin:

1. Set the TH5V bit (Bit 1) in the Configuration Register 4 (Address = 0x7D) = 0.
2. Set the $\overline{\text{THERM}}$ Enable Bit (Bit 1) in the Configuration Register 3 (Address = 0x78) = 1.

$\overline{\text{THERM}}$ as an Input

When configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance. See this data sheet for more information on timing $\overline{\text{THERM}}$ assertions and generating $\overline{\text{ALERT}}$s based on $\overline{\text{THERM}}$.

The user can also setup the ADT7463 so when the THERM pin is driven low externally the fans run at 100%. The fans run at 100% for the duration of the $\overline{\text{THERM}}$ pin being pulled low.

This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address = 0x78) to 1. This only works if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00 or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, then pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 36 for more information.

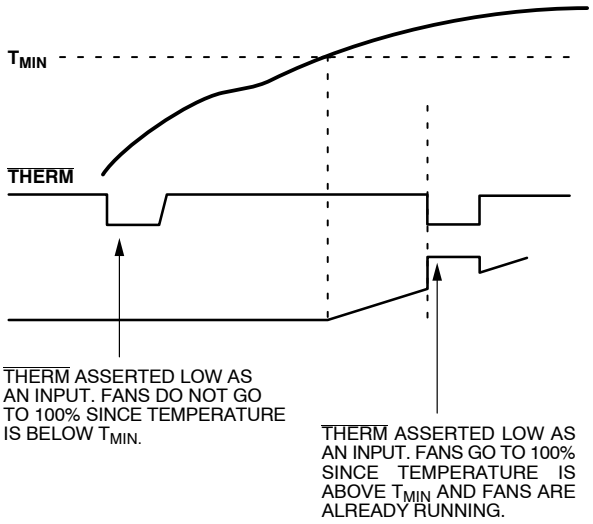


Figure 36. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7463 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input may be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium® 4 CPU and measure system performance. The $\overline{\text{THERM}}$ input may also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7463's $\overline{\text{THERM}}$ input and stopped on the negation of the pin. The timer counts $\overline{\text{THERM}}$ times cumulatively, i.e., the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8−bit $\overline{\text{THERM}}$ timer register (Reg. 0x79) is designed such that Bit 0 gets set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer gets set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms.

Figure 37 illustrates how the $\overline{\text{THERM}}$ timer behaves as the $\overline{\text{THERM}}$ input is asserted and negated. Bit 0 gets set on the first $\overline{\text{THERM}}$ assertion detected. This bit remains set until such time as the cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms. At this time, Bit 1 of the $\overline{\text{THERM}}$ timer gets set, and Bit 0 is cleared. Bit 0 now reflects timer readings with a resolution of 22.76 ms.

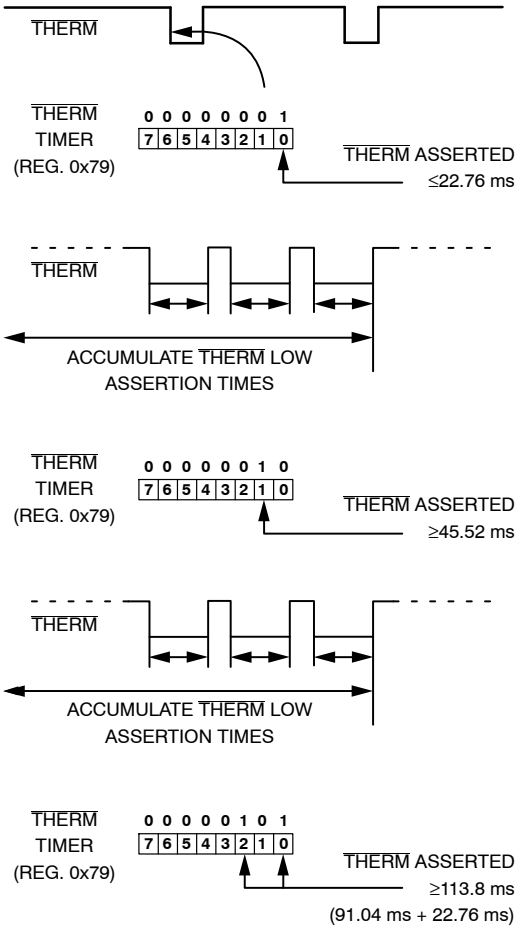


Figure 37. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

- After a THERM timer read (Reg. 0x79):
  1. The contents of the timer get cleared on read.
  2. The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming the THERM limit has been exceeded).
- If the THERM timer is read during a THERM assertion, then the following will happen:
  1. The contents of the timer are cleared.
  2. Bit 0 of the THERM timer is set to 1 (since a THERM assertion is occurring).
  3. The THERM timer increments from zero.
  4. If the THERM limit (Reg. 0x7A) = 0x00, then the F4P bit gets set.

Generating SMBALERT Interrupts from THERM Events

The ADT7463 can generate SMBALERTs when a programmable THERM limit has been exceeded. This allows the systems designer to ignore brief, infrequent THERM assertions, while capturing longer THERM events. Register 0x7A is the THERM Limit Register. This 8−bit register allows a limit from 0 seconds (first THERM assertion) to 5.825 seconds to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM limit register. If the THERM timer value exceeds the THERM limit value, then the F4P bit (Bit 5) of Status Register 2 gets set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 still gets set if the THERM limit is exceeded.

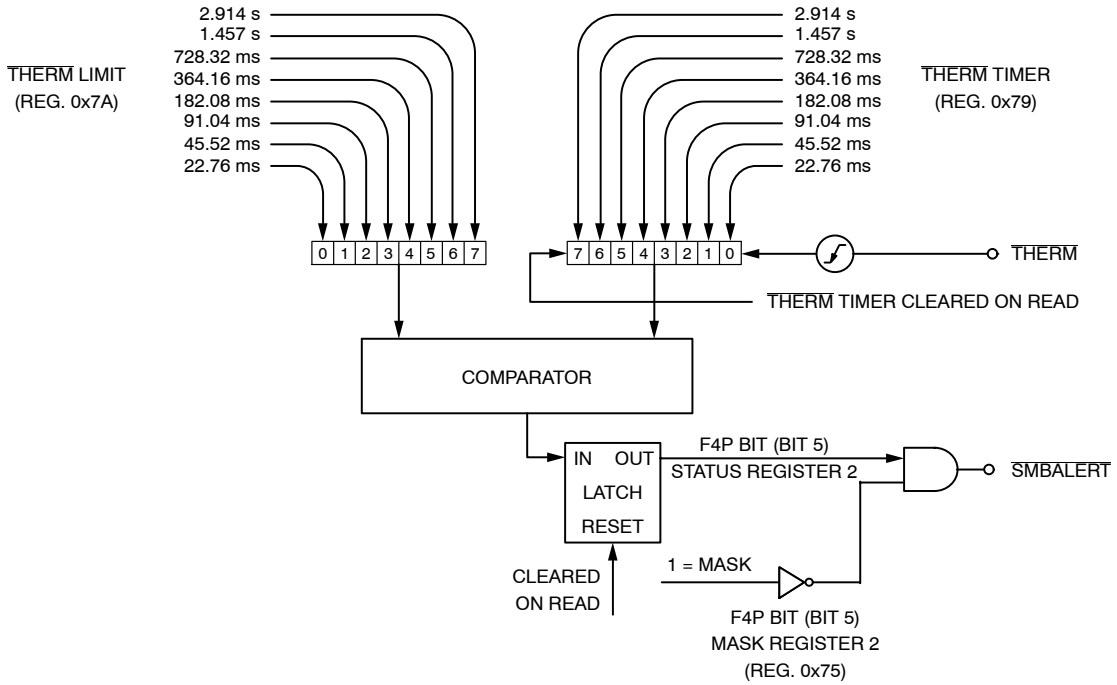


Figure 38. Functional Diagram of the ADT7463 THERM Monitoring Circuitry

Figure 38 is a Functional Block Diagram of the $\overline{\text{THERM}}$ timer, limit, and associated circuitry. Writing a value of 0x00 to the $\overline{\text{THERM}}$ limit register (Reg. 0x7A) causes $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion. A $\overline{\text{THERM}}$ limit value of 0x01 generates an $\overline{\text{SMBALERT}}$ once cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms.

Configuring the Desired $\overline{\text{THERM}}$ Behavior

1. Configure the desired pin as the $\overline{\text{THERM}}$ input:
   Setting Bit 1 ($\overline{\text{THERM}}$ Enable) of Configuration Register 3 (Reg. 0x78) enables the $\overline{\text{THERM}}$ monitoring functionality. This is enabled on Pin 14 by default.
   Setting Bit 1 (TH5V) of Configuration Register 4 (Reg. 0x7D) enables $\overline{\text{THERM}}$ monitoring on Pin 20 (Bit 1 of Configuration Register 3 must also be set). Pin 14 can be used as TACH4.
2. Select the desired fan behavior for $\overline{\text{THERM}}$ events:
   Setting Bit 2 (BOOST bit) of Configuration Register 3 (Reg. 0x78) causes all fans to run at 100% duty cycle whenever $\overline{\text{THERM}}$ gets asserted. This allows fail−safe system cooling. If this bit = 0, the fans run at their current settings and are not affected by $\overline{\text{THERM}}$ events.
3. Select whether $\overline{\text{THERM}}$ events should generate $\overline{\text{SMBALERT}}$ interrupts:
   Bit 5 (F4P) of Mask Register 2 (Reg. 0x75), when set, masks out $\overline{\text{SMBALERT}}$s when the $\overline{\text{THERM}}$ limit value gets exceeded. This bit should be cleared if $\overline{\text{SMBALERT}}$s based on $\overline{\text{THERM}}$ events are required.
4. Select a suitable $\overline{\text{THERM}}$ limit value:
   This value determines whether an $\overline{\text{SMBALERT}}$ is generated on the first $\overline{\text{THERM}}$ assertion, or only if a cumulative $\overline{\text{THERM}}$ assertion time limit is exceeded. A value of 0x00 causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion.
5. Select a $\overline{\text{THERM}}$ monitoring time:
   This is how often OS or BIOS level software checks the $\overline{\text{THERM}}$ timer. For example, BIOS could read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >5.825 s in Hour 3, this can indicate that system performance is degrading significantly since $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.
   Alternatively, OS or BIOS level software can time−stamp when the system is powered on. If an $\overline{\text{SMBALERT}}$ is generated due to the $\overline{\text{THERM}}$ limit being exceeded, another time−stamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ limit time. For example, if it takes one week for a $\overline{\text{THERM}}$ limit of 2.914 s to be exceeded and the next time it takes only 1 hour, then this is an indication of a serious degradation in system performance.

Configuring the ADT7463 $\overline{\text{THERM}}$ Pin as an Output

In addition to the ADT7463 being able to monitor $\overline{\text{THERM}}$ as an input, the ADT7463 can optionally drive $\overline{\text{THERM}}$ low as an output. The user can preprogram system critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Since the temperature for that channel is measured only every monitoring cycle, once $\overline{\text{THERM}}$ asserts it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low if the Remote 1, Local, or Remote 2 Temperature $\overline{\text{THERM}}$ limits get exceeded by 0.25°C. The $\overline{\text{THERM}}$ limit registers are at locations 0x6A, 0x6B, and 0x6C, respectively. Setting Bit 3 of Registers 0x5F, 0x60, and 0x61 enables the $\overline{\text{THERM}}$ output feature for the Remote 1, Local, and Remote 2 Temperature channels, respectively. Figure 39 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

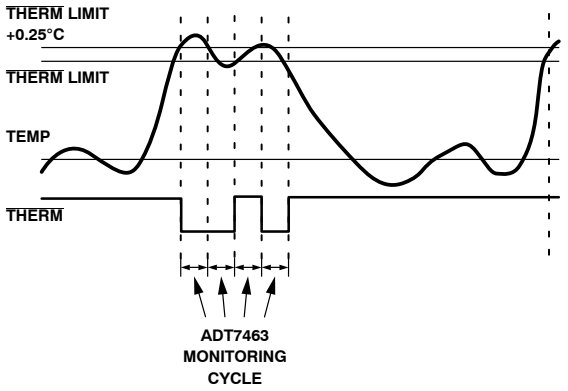


Figure 39. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

Fan Drive Using PWM Control

The ADT7463 uses pulse−width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. A single NMOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA, and so SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET needs to handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V for direct interfacing to the PWM_OUT pin. V_{GS} can be greater than 3.3 V as long as the

pull−up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET. This reduces the voltage applied across the fan and therefore the maximum operating speed of the fan.

Figure 40 shows how a 3−wire fan may be driven using PWM control.

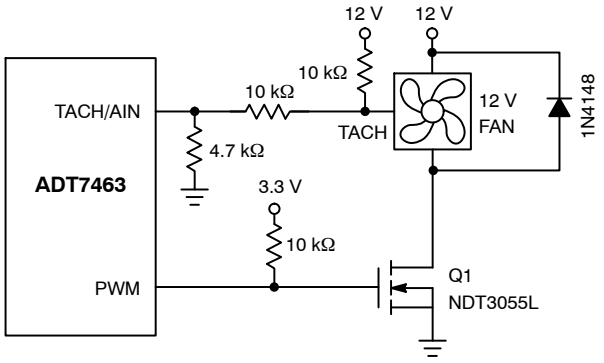


Figure 40. Driving a 3−wire Fan Using an N−channel MOSFET

Figure 40 uses a 10 kΩ pull−up resistor for the TACH signal. This assumes that the TACH signal is open−collector from the fan. In all cases, the TACH signal from the fan *must* be kept below 5 V maximum to prevent damaging the ADT7463. If in doubt as to whether the fan used has an open−collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section of the data sheet.

Figure 41 shows a fan drive circuit using an NPN transistor such as a general−purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

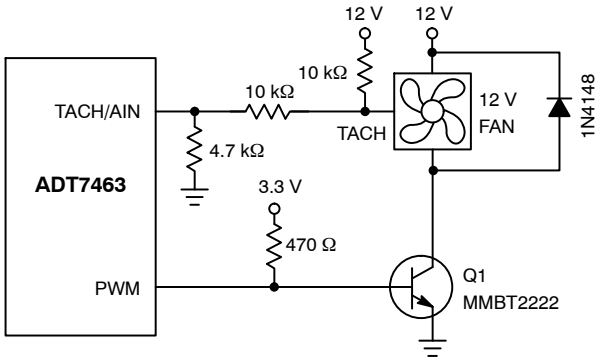


Figure 41. Driving a 3−wire Fan Using an NPN Transistor

Driving Two Fans from PWM3

Note that the ADT7463 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 42 shows how to drive two fans in parallel using low cost NPN transistors. Figure 43 is the equivalent circuit using the NDT3055L MOSFET. Note that since the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first.

Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current and that they sink less than the 8 mA maximum current specified on the data sheet.

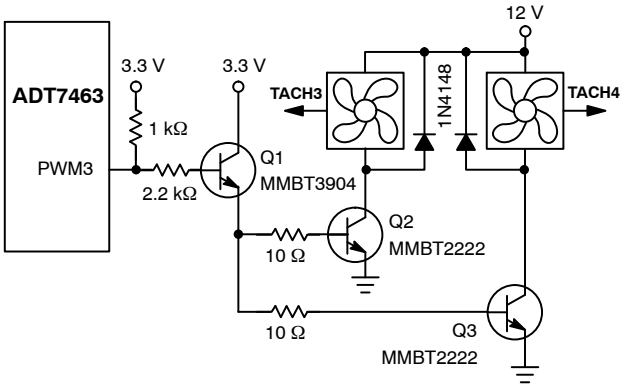


Figure 42. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

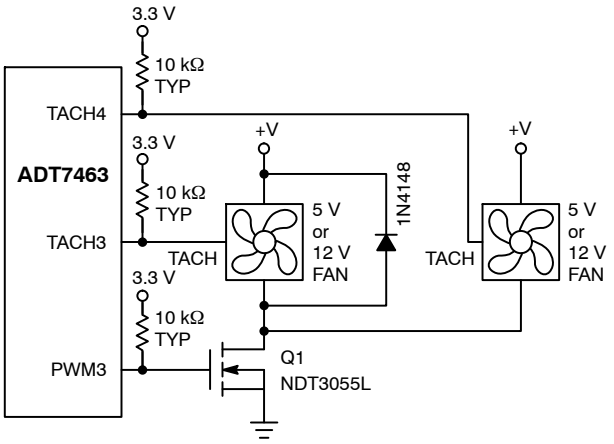


Figure 43. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N−channel MOSFET

Driving Up to Three Fans from PWM2

TACH measurements for fans are synchronized to particular PWM channels, e.g., TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to

PWM3 so PWM3 can drive 2 fans. Alternatively, PWM2 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM2 output. This allows PWM2 to drive two or three fans. In this case, the drive circuitry looks the same as shown in Figures 42 and 43. The SYNC bit in Register 0x62 enables this function.

Table 33. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM2.

Driving 2−wire Fans

Figure 44 shows how a 2−wire fan may be connected to the ADT7463. This circuit allows the speed of a 2−wire fan to be measured, even though the fan has no dedicated TACH signal. A series resistor, R_{SENSE}, in the fan circuit converts the fan commutation pulses into a voltage. This is ac−coupled into the ADT7463 through the 0.01 μF capacitor. On−chip signal conditioning allows accurate monitoring of fan speed. The value of R_{SENSE} chosen depends upon the programmed input threshold and the current drawn by the fan. For fans drawing approximately 200 mA, a 2 Ω R_{SENSE} value is suitable when the threshold is programmed as 40 mV. For fans that draw more current, such as larger desktop or server fans, R_{SENSE} may be reduced for the same programmed threshold. The smaller the threshold programmed the better, since more voltage is developed across the fan and the fan spins faster. Figure 45 shows a typical plot of the sensing waveform at the TACH/AIN pin. The most important thing is that the voltage spikes (either negative going or positive going) are more than 40 mV in amplitude. This allows fan speed to be reliably determined.

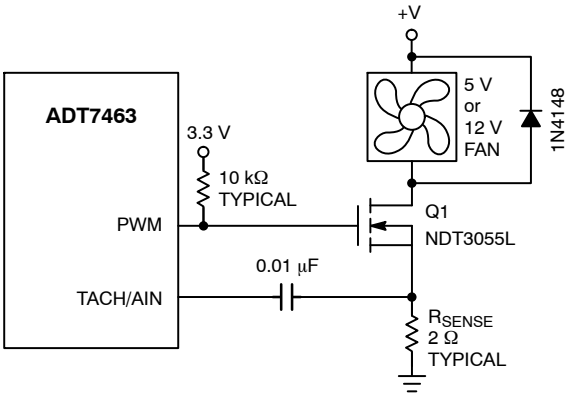


Figure 44. Driving a 2−wire Fan

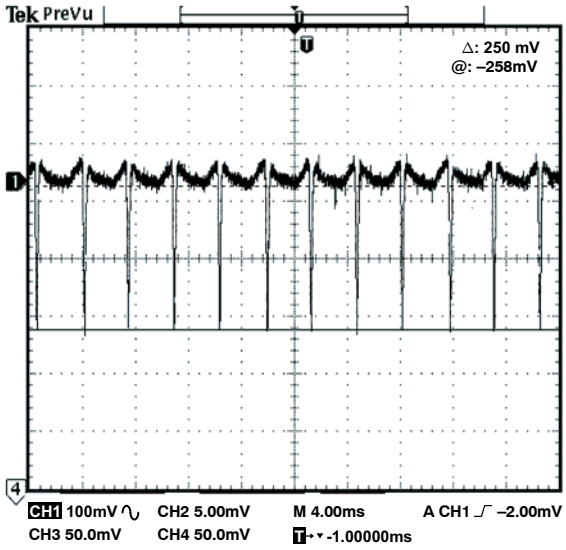


Figure 45. Fan Speed Sensing Waveform at TACH/AIN Pin

Laying Out 2−wire and 3−wire Fans

Figure 46 shows how to lay out a common circuit arrangement for 2−wire and 3−wire fans. Some components are not populated, depending on whether a 2−wire or 3−wire fan is being used.

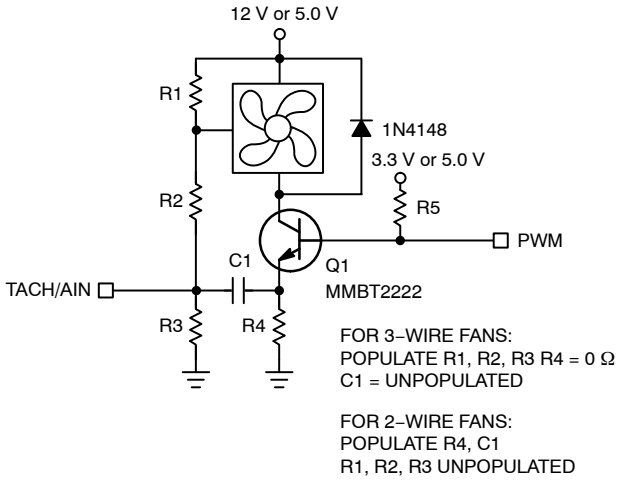


Figure 46. Planning for 2−wire or 3−wire Fans on a PCB

TACH Inputs

Pins 9, 11, 12, and 14 are open−drain TACH inputs intended for fan speed measurement.

Signal conditioning in the ADT7463 accommodates the slow rise and fall times typical of fan tachometer outputs.

The maximum input signal range is 0 V to 5 V, even where V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 47 to 50 show circuits for most common fan TACH outputs.

If the fan TACH output has a resistive pull−up to V_{CC}, it can be connected directly to the fan input, as shown in Figure 47.

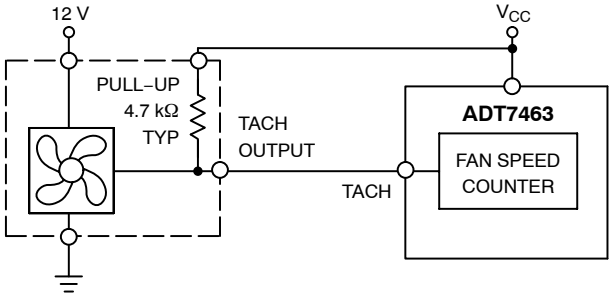


Figure 47. Fan with TACH Pull−up to V_{CC}

If the fan output has a resistive pull−up to 12 V (or other voltage greater than 5 V) then the fan output can be clamped with a Zener diode, as shown in Figure 48. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

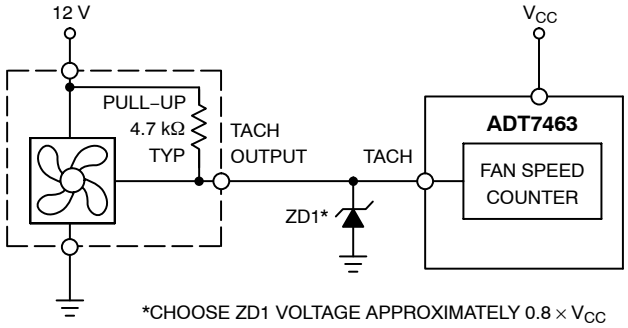


Figure 48. Fan with TACH Pull−up to Voltage > 5.0 V, e.g., 12 V, Clamped with Zener Diode

If the fan has a strong pull−up (less than 1 kΩ) to 12 V or a totempole output, then a series resistor can be added to limit the Zener current, as shown in Figure 49. Alternatively, a resistive attenuator may be used, as shown in Figure 50. R1 and R2 should be chosen such that:

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5\ V \quad \text{(eq. 3)}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values.

With a pull−up voltage of 12 V and pull−up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This gives a high input voltage of 3.83 V.

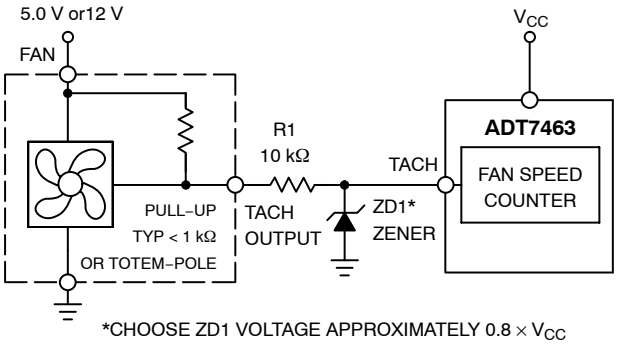


Figure 49. Fan with Strong TACH. Pull−up to > V_{CC} or Totem−Pole Output, Clamped with Zener and Resistor

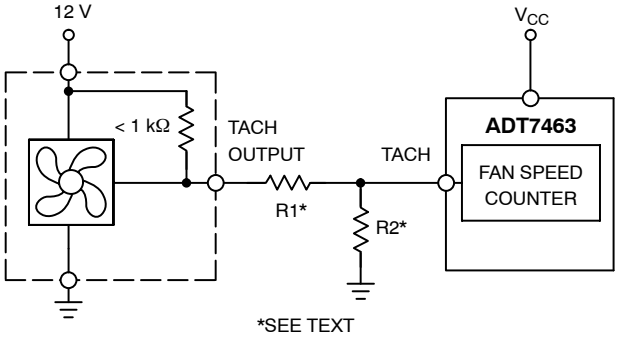


Figure 50. Fan with Strong TACH. Pullup to > V_{CC} or Totem−Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly because the fan speed may be less than 1,000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on−chip 90 kHz oscillator into the input of a 16−bit counter for N periods of the fan TACH output (Figure 51), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

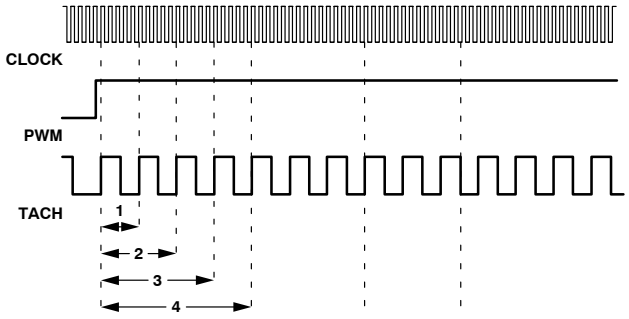


Figure 51. Fan Speed Measurement

N, the number of pulses counted, is determined by the settings of Register 0x7B (fan pulses per revolution register). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

The fan tachometer readings are 16−bit values consisting of a 2−byte read from the ADT7463.

Table 34. FAN SPEED MEASUREMENT REGISTERS

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7463

If fan speeds are being measured, this involves a 2−register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read from. This prevents erroneous TACH readings.

The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Since the device is essentially measuring the fan TACH period, the higher the count value the slower the fan is actually running. A 16−bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (< 100 RPM).

$$\text{HighLimit} :> \text{ComparisonPerformed}$$

Since the actual fan TACH period is being measured, exceeding a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

The fan TACH limit registers are 16−bit values consisting of two bytes.

Table 35. FAN TACH LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

The FAST bit (Bit 3) of Configuration Register 3 (Reg. 0x78), when set, updates the fan TACH readings every 250 ms.

If any of the fans are not being driven by a PWM channel but are powered directly from 5 V or 12 V, its associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source.

Calculating Fan Speed

Assuming a fan with a two pulses/revolution (and two pulses/revolution being measured), fan speed is calculated by:

$$\text{Fan Speed (RPM)} = (90,000 \times 60)/\text{Fan TACH Reading}$$

where:

Fan TACH Reading = 16−bit Fan Tachometer Reading

Example:

TACH1 HIGH Byte (Reg. 0x29) = 0x17

TACH1 LOW Byte (Reg. 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 Decimal

$$\text{RPM} = (f \times 60)/\text{Fan 1 TACH Reading}$$

$$\text{RPM} = (90,000 \times 60)/6143$$

Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either 1, 2, 3, or 4 Tach pulses per revolution. Once the number of fan Tach pulses has been determined, it is programmed into the fan pulses per revolution register (Reg. 0x7B) for each fan. Alternatively, this register can be used to determine the number or pulses/revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses/revolution setting, the smoothest graph with the lowest ripple determines the correct pulses/revolution value.

Table 36. FAN PULSES PER REVOLUTION REGISTER (REG. 0X7B)

Bit	Mnemonic	Description
<1:0>	FAN1 Default	2 Pulses per Revolution
<3:2>	FAN2 Default	2 Pulses per Revolution
<5:4>	FAN3 Default	2 Pulses per Revolution
<7:6>	FAN4 Default	2 Pulses per Revolution

Table 37. FAN PULSES PER REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

2−wire Fan Speed Measurements

The ADT7463 is capable of measuring the speed of 2−wire fans, i.e., fans without TACH outputs. To do this, the fan must be interfaced as shown in the Fan Drive Circuitry section of the data sheet. In this case, the TACH inputs need to be reprogrammed as analog inputs, AIN.

Table 38. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Mnemonic	Description
3	AIN4	1 indicates that Pin 14 is reconfigured to measure the speed of a 2−wire fan using an external sensing resistor and coupling capacitor.
2	AIN3	1 indicates that Pin 9 is reconfigured to measure the speed of a 2−wire fan using an external sensing resistor and coupling capacitor.
1	AIN2	1 indicates that Pin 12 is reconfigured to measure the speed of a 2−wire fan using an external sensing resistor and coupling capacitor.
0	AIN1	1 indicates that Pin 11 is reconfigured to measure the speed of a 2−wire fan using an external sensing resistor and coupling capacitor.

AIN Switching Threshold

Having configured the TACH inputs as AIN inputs for 2−wire measurements, users can select the sensing threshold for the AIN signal.

Table 39. CONFIGURATION REGISTER 4 (REG. 0X7D)

Bit	Mnemonic	Description
<3:2>	AINL	These two bits define the input threshold for 2−wire fan speed measurements. 00 = ±20 mV 01 = ±40 mV 10 = ±80 mV 11 = ±130 mV

Fan Spin−up

The ADT7463 has a unique fan spin−up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two pulses are detected, the PWM duty cycle goes to the expected running value, e.g., 33%. The advantage of this is that fans have different spin−up characteristics and takes different times to overcome inertia. The ADT7463 just runs the fans fast enough to overcome inertia and are quieter on spin−up than fans programmed to spin−up for a given spin−up time.

Fan Start−up Timeout

To prevent false interrupts being generated as a fan spins up (since it is below running speed), the ADT7463 includes a fan start−up timeout function. This is the time limit allowed for two TACH pulses to be detected on spin−up. For example, if 2−second fan start−up timeout is chosen and no TACH pulses occur within 2 seconds of the start of spin−up, a fan fault is detected and flagged in the interrupt status registers.

Table 40. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E)

Bit	Mnemonic	Description
<2:0>	SPIN	These bits control the start−up timeout for PWM1, PWM2, PWM3: 000 = No Start−up Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s

Disabling Fan Start−up Timeout

Although fan start−up makes fan spin−ups much quieter than fixed−time spin−ups, the option exists to use fixed spin−up times. Bit 5 (FSPDIS) = 1 in Configuration Register 1 (Reg. 0x40) disables the spin−up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Registers 0x5C to 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non inverted) or low for 100% duty cycle (inverted).

Table 41. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E)

Bit	Mnemonic	Description
<4>	INV	0 = Logic High for 100% PWM Duty Cycle 1 = Logic Low for 100% PWM Duty Cycle

PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Registers 0x5F to 0x61 configure the PWM frequency for PWM1 to PWM3, respectively.

Table 42. PWM1 TO PWM3 FREQUENCY REGISTERS (REG. 0X5F TO 0X61)

Bit	Mnemonic	Description
<2:0>	FREQ	000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

Fan Speed Control

The ADT7463 can control fan speed using two different modes. The first is automatic fan speed control mode. In this mode, fan speed is automatically varied with temperature and without CPU intervention, once initial parameters are set up. The advantage of this is in the case of the system hanging, the user is guaranteed that the system is protected from overheating. The automatic fan speed control

incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For more information and how to program the automatic fan speed control loop and dynamic T_{MIN} calibration, see the AN−613 Programming the Automatic Fan Speed Control Loop Application Note. The second fan speed control method is manual fan speed control which is described in the next paragraph.

Manual Fan Speed Control

The ADT7463 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if users wish to change fan speed in software or want to adjust PWM duty cycle output for test purposes. Bits <7:5> of Registers 0x5C to 0x5E (PWM Configuration) control the behavior of each PWM output.

Table 43. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E)

Bit	Mnemonic	Description
<7:5>	BHVR	111 = Manual Mode

Once under manual control, each PWM output may be manually updated by writing to Registers 0x30 to 0x32 (PWMx current duty cycle registers).

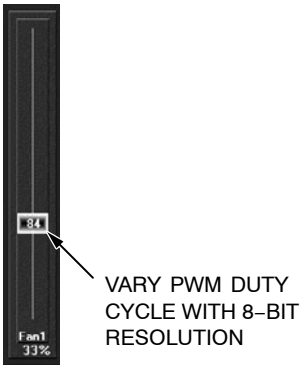


Figure 52. Control PWM Duty Cycle Manually with a Resolution of 0.39%

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8−bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

$$Value(Decimal) = PWM_{MIN}/0.39$$

Example 1: For a PWM duty cycle of 50%,

$$Value(Decimal) = 50/0.39 = 128\ Decimal$$

$$Value = 128\ Decimal\ or\ 0x80$$

Example 2: For a PWM duty cycle of 33%,

$$Value(Decimal) = 33/0.39 = 85\ Decimal$$

$$Value = 85\ Decimal\ or\ 0x54$$

Table 44. PWM DUTY CYCLE REGISTERS

Register	Description	Default
0x30	PWM1 Duty Cycle	0xFF (100%)
0x31	PWM2 Duty Cycle	0xFF (100%)
0x32	PWM3 Duty Cycle	0xFF (100%)

By reading the PWMx current duty cycle registers, users can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

Operating from 3.3 V Standby

The ADT7463 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. If using the dynamic T_{MIN} mode, lowering the core voltage of the processor would change the CPU temperature and change the dynamics of the system under dynamic T_{MIN} control. Likewise, when monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

Dynamic T_{MIN} Control Register (Reg. 0x36) <1> V_{CCP}LO = 1

When the power is supplied from 3.3 V STBY and the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

- Status Bit 1 (V_{CCP}) in Status Register 1 Gets Set
- $\overline{\text{SMBALERT}}$ Gets Generated If Enabled
- $\overline{\text{THERM}}$ Monitoring Is Disabled. The $\overline{\text{THERM}}$ Timer Should Hold Its Value Prior To the S3 or S5 State
- Dynamic T_{MIN} Control Is Disabled. This Prevents T_{MIN} from Being Adjusted Due To an S3 or S5 State
- The ADT7463 Is Prevented from Entering the Shutdown State

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything gets re−enabled and the system resumes normal operation. Note that since other voltages can drop or be turned off during a low power state, these voltage channels set status bits or generate $\overline{\text{SMBALERT}}$s. It is still necessary to mask out these channels prior to entering a low power state using the interrupt mask registers. When exiting the low power state, the mask bits can be cleared. This prevents the device from generating unwanted $\overline{\text{SMBALERT}}$s during the low power state.

XOR Tree Test Mode

The ADT7463 includes an XOR Tree Test Mode. This mode is useful for in−circuit test equipment at board−level testing. By applying stimulus to the pins included in the XOR Tree, it is possible to detect opens or shorts on the system board. Figure 53 shows the signals that are exercised in the XOR Tree Test Mode.

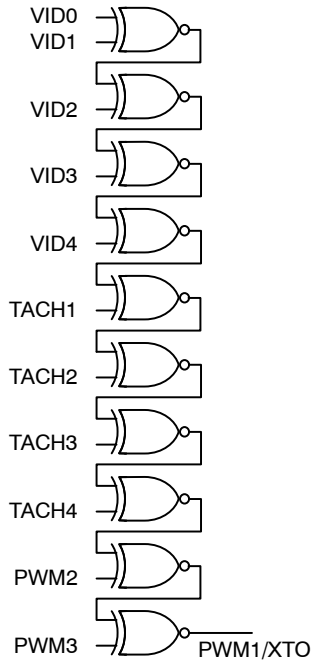


Figure 53. XOR Tree Test

The XOR Tree Test is invoked by setting Bit 0 (XEN) of the XOR Tree Test Enable Register (Reg. 0x6F).

Power−on Default

The ADT7463 does not monitor temperature and fan speed by default on power−up. Monitoring of temperature and fan speed is enabled by setting the Start Bit in Configuration Register 1 (Bit 0, Address 0x40) to 1. The fans run at full speed on power−up. This is because the BHVR bits (Bits <7:5>) in the PWMx configuration registers are set to 100 (fans run full speed) by default.

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x20	R	2.5 V Reading	9	8	7	6	5	4	3	2	0x00	
0x21	R	V_{CCP} Reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} Reading	9	8	7	6	5	4	3	2	0x00	
0x23	R	5 V Reading	9	8	7	6	5	4	3	2	0x00	
0x24	R	12 V Reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x80	
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x80	
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x80	
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x33	R/W	Remote 1 Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x34	R/W	Local Temp Operating Point	7	6	5	4	3	2	1	0	0x64	YES
0x35	R/W	Remote 2 Operating Point	7	6	5	4	3	2	1	0	0x64	YES

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x36	R/W	Dynamic T_{MIN} Control Reg 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V_{CCP}LO	CYR2	0x00	YES
0x37	R/W	Dynamic T_{MIN} Control Reg 2	CYR2	CYR2	CYL	CYL	CYL	CYR1	CYR1	CYR1	0x00	YES
0x3	R	Device ID Register	7	6	5	4	3	2	1	0	0x27	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision Number	VER	VER	VER	VER	STP	STP	STP	STP	0x62 or 0x6A	
0x40	R/W	Configuration Register 1	V_{CC}	TODIS	FSPDIS	V × I	FSPD	RDY	LOCK	STRT	0x00	YES
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	5V	V_{CC}	V_{CCP}	2.5V	0x00	
0x42	R	Interrupt Status Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12V/VC	0x00	
0x43	R/W	VID Register	VIDSEL	THLD	VID5	VID4	VID3	VID2	VID1	VID0	0xFF	
0x44	R/W	2.5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x45	R/W	2.5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4A	R/W	5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4B	R/W	5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4C	R/W	12 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4D	R/W	12 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x62	YES
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x62	YES
0x5E	R/W	PWM3 Configuration Register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x62	YES

Table 45. ADT7463 REGISTERS

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 Freq.	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	YES
0x60	R/W	Local Temp T_{RANGE}/PWM2 Freq.	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	YES
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Freq.	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	YES
0x62	R/W	Enhance Acoustics Register 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0x00	YES
0x63	R/W	Enhance Acoustics Register 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	YES
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	YES
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	YES
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6B	R/W	Local $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Limit	7	6	5	4	3	2	1	0	0x64	YES
0x6D	R/W	Remote 1 Local Temp Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	YES
0x6E	R/W	Remote 2 Temp Hysteresis	HYSR2	HYSR2	HYSR2	HYSR2	RES	RES	RES	RES	0x40	YES
0x6F	R/W	XOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	YES
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0	0x00	YES
0x73	R/W	Configuration Register 2	SHDN	CONV	ATTN	AVG	AIN4	AIN3	AIN2	AIN1	0x00	YES
0x74	R/W	Interrupt Mask 1 Reg.	OOL	R2T	LT	R1T	5V	V_{CC}	V_{CCP}	2.5V	0x00	
0x75	R/W	Interrupt Mask 2 Reg.	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12V/VC	0x00	
0x76	R/W	Extended Resolution Register 1	5V	5V	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	2.5V	2.5V	0x00	
0x77	R/W	Extended Resolution Register 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12V	12V	0x00	
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}$ ENABLE	ALERT	0x00	YES
0x79	R	$\overline{\text{THERM}}$ Status Reg.	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/ TMR0	0x00	
0x7A	R/W	$\overline{\text{THERM}}$ Limit Reg.	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	
0x7B	R/W	Fan Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	
0x7D	R/W	Configuration Register 4	RES	RES	RES	RES	AINL	AINL	TH5V	AL2.5V	0x00	YES
0x7E	R	Test Register 1	DO NOT WRITE TO THESE REGISTERS								0x00	YES
0x7F	R	Test Register 2	DO NOT WRITE TO THESE REGISTERS								0x00	YES

Table 46. VOLTAGE READING REGISTERS (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x20	Read−only	2.5 V Reading (8 MSBs of Reading)
0x21	Read−only	V_{CCP} Reading: Holds Processor Core Voltage Measurement (8 MSBs of Reading)
0x22	Read−only	V_{CC} Reading: Measures V_{CC} through the V_{CC} Pin (8 MSBs of Reading)
0x23	Read−only	5 V Reading (8 MSBs of Reading)
0x24	Read−only	12 V Reading (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution registers get read, the associated MSB reading registers get frozen until read. Both the extended resolution registers and the MSB registers get frozen.

Table 47. TEMPERATURE READING REGISTERS (POWER−ON DEFAULT = 0X80) (Note 1)

Register Address	R/W	Description
0x25	Read−only	Remote 1 Temperature Reading (8 MSBs of reading) (Note 2)
0x26	Read−only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read−only	Remote 2 Temperature Reading (8 MSBs of reading) (Note 2)

1. These voltage readings are in twos complement format.
2. Note that a reading of 0x80 in a temperature reading register indicates a diode fault (open or short) on that channel. If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) should be read first. Once the extended resolution registers are read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.

Table 48. FAN TACHOMETER READING REGISTERS (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x28	Read−only	TACH1 Low Byte
0x29	Read−only	TACH1 High Byte
0x2A	Read−only	TACH2 Low Byte
0x2B	Read−only	TACH2 High Byte
0x2C	Read−only	TACH3 Low Byte
0x2D	Read−only	TACH3 High Byte
0x2E	Read−only	TACH4 Low Byte
0x2F	Read−only	TACH4 High Byte

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the fan pulses per revolution register (Reg. 0x7B). This allows the fan speed to be accurately measured. Since a valid fan tachometer reading requires that two bytes are read, the low byte MUST be read first. Both the low and high bytes are then frozen until read. At power−on, these registers contain 0x0000 until such time as the first valid fan TACH measurement is read in to these registers. This prevents false interrupts from occurring while the fans are spinning up.
   A count of 0xFFFF indicates that a fan is:
   - Stalled or blocked (object jamming the fan).
   - Failed (internal circuitry destroyed).
   - Not populated. (The ADT7463 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low byte should be set to 0xFFFF.)
   - Alternate function, for example, TACH4 reconfigured as a $\overline{\text{THERM}}$ pin.
   - 2−wire Instead of 3−wire Fan

Table 49. CURRENT PWM DUTY CYCLE REGISTERS (POWER−ON DEFAULT = 0XFF) (Note 1)

Register Address	R/W	Description
0x30	R/W	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF).

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7463 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 50. OPERATING POINT REGISTERS (POWER−ON DEFAULT = 0X64) (Note 1)

Register Address	R/W	Description
0x33	R/W	Remote 1 Operating Point Register (Default = 100°C)
0x34	R/W	Local Temp Operating Point Register (Default = 100°C)
0x35	R/W	Remote 2 Operating Point Register (Default = 100°C)

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers will fail. These registers set the target operating point for each temperature channel when the dynamic T_{MIN} control feature is enabled. The fans being controlled are adjusted to maintain temperature about an operating point.

Table 51. REGISTER 0X36 − DYNAMIC T_{MIN} CONTROL REGISTER 1 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<0>	CYR2	R/W	MSB of 3−bit Remote 2 Cycle Value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (Reg. 0x37). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.
<1>	V_{CCP}LO	R/W	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Reg. 0x46), the following occurs: • Status Bit 1 in Status Register 1 gets set • $\overline{\text{SMBALERT}}$ gets generated if enabled • $\overline{\text{PROCHOT}}$ monitoring is disabled • Dynamic T_{MIN} control is disabled • The device is prevented from entering shutdown • Everything re−enabled once V_{CCP} increases above V_{CCP} low limit
<2>	PHTR1	R/W	PHTR1 = 1 copies the Remote 1 current temperature to the Remote 1 Operating Point Register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. PHTR1 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 1 Operating Point Tegister reflects its programmed value.
<3>	PHTL	R/W	PHTL = 1 copies the local channel's current temperature to the Local Operating Point Register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. PHTL = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Local Temperature Operating Point Register reflects its programmed value.
<4>	PHTR2	R/W	PHTR2 = 1 copies the Remote 2 current temperature to the Remote 2 Operating Point Register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without system performance being affected. PHTR2 = 0 ignores any $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 2 Operating Point Register reflects its programmed value.
<5>	R1T	R/W	R1T = 1 enables dynamic T_{MIN} control on the Remote 1 Temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R1T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control section.
<6>	LT	R/W	LT = 1 enables dynamic T_{MIN} control on the Local Temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. LT = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control section.
<7>	R2T	R/W	R2T = 1 enables dynamic T_{MIN} control on the Remote 2 Temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. R2T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control section.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 52. REGISTER 0X37 − DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<2:0>	CYR1	R/W	3−bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop. **Bits** **Decrease Cycle** **Increase Cycle** 000 4 Cycles (0.5 s) 8 Cycles (1 s) 001 8 Cycles (1 s) 16 Cycles (2 s) 010 16 Cycles (2 s) 32 Cycles (4 s) 011 32 Cycles (4 s) 64 Cycles (8 s) 100 64 Cycles (8 s) 128 Cycles (16 s) 101 128 Cycles (16 s) 256 Cycles (32 s) 110 256 Cycles (32 s) 512 Cycles (64 s) 111 512 Cycles (64 s) 1024 Cycles (128 s)
<5:3>	CYL	R/W	3−bit Local Temperature Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for local temperature channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop. **Bits** **Decrease Cycle** **Increase Cycle** 000 4 Cycles (0.5 s) 8 Cycles (1 s) 001 8 Cycles (1 s) 16 Cycles (2 s) 010 16 Cycles (2 s) 32 Cycles (4 s) 011 32 Cycles (4 s) 64 Cycles (8 s) 100 64 Cycles (8 s) 128 Cycles (16 s) 101 128 Cycles (16 s) 256 Cycles (32 s) 110 256 Cycles (32 s) 512 Cycles (64 s) 111 512 Cycles (64 s) 1024 Cycles (128 s)
<7:6>	CYR2	R/W	2 LSBs of 3−bit Remote 2 Cycle Value. The MSB of the 3−bit code resides in Dynamic T_{MIN} Control Register 1 (Reg. 0x36). These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 2 channel, in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop. **Bits** **Decrease Cycle** **Increase Cycle** 000 4 Cycles (0.5 s) 8 Cycles (1 s) 001 8 Cycles (1 s) 16 Cycles (2 s) 010 16 Cycles (2 s) 32 Cycles (4 s) 011 32 Cycles (4 s) 64 Cycles (8 s) 100 64 Cycles (8 s) 128 Cycles (16 s) 101 128 Cycles (16 s) 256 Cycles (32 s) 110 256 Cycles (32 s) 512 Cycles (64 s) 111 512 Cycles (64 s) 1024 Cycles (128 s)

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 53. REGISTER 0X40 − CONFIGURATION REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	STRT	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power−up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes read−only and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable.)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the ADT7463 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	Read−only	This bit is set to 1 by the ADT7463 to indicate that the device is fully powered−up and ready to begin systems monitoring.
<3>	FSPD	R/W	When set to 1, all fans run at full speed. Power−on default = 0. (This bit cannot be locked.)
<4>	V × I	R/W	BIOS should set this bit to a 1 when the ADT7463 is configured to measure current from an ADI ADOPT™ VRM controller and measure the CPU's core voltage. This allows monitoring software to display CPU watts usage. (Lockable.)
<5>	FSPDIS	R/W	Logic 1 disables fan spin−up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin−up timeout selected.
<6>	TODIS	R/W	When set to 1, the SMBus timeout feature is disabled. This allows the ADT7463 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
<7>	V_{CC}	R/W	When set to 1, the ADT7463 rescales its V_{CC} pin to measure a 5.0 V supply. When set to 0, the ADT7463 measures V_{CC} as a 3.3 V supply. (Lockable.)

Table 54. REGISTER 0X41 − INTERRUPT STATUS REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	2.5V	Read−only	A 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<1>	V_{CCP}	Read−only	A 1 indicates the V_{CCP} high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<2>	V_{CC}	Read−only	A 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5V	Read−only	A 1 indicates the 5 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided.
<4>	R1T	Read−only	A 1 indicates that the Remote 1 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read−only	A 1 indicates the Local Low or High temperature limit has been exceeded. This bit is cleared on a read of the Status Register only if the error condition has subsided.
<6>	R2T	Read−only	A 1 indicates that the Remote 2 Low or High temperature limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read−only	A 1 indicates that an out−of−limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out−of−limit. This saves the need to read Status Register 2 every interrupt or polling cycle.

Table 55. REGISTER 0X42 − INTERRUPT STATUS REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<0>	12V/VC	Read−only	A one indicates the 12 V high or low limit has been exceeded. This bit gets cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit gets set when the levels on VID0 to VID5 are different than they were 11 μs previously. This can be used to generate an $\overline{\text{SMBALERT}}$ whenever the VID code changes.
<1>	OVT	Read−only	A 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
<2>	FAN1	Read−only	A 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM1 output is off.
<3>	FAN2	Read−only	A 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM2 output is off.
<4>	FAN3	Read−only	A 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM3 output is off.
<5>	F4P	Read−only	A 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is NOT set when the PWM3 output is off. If Pin 14 or Pin 20 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ Limit Register (Reg. 0x7A).
<6>	D1	Read−only	A 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read−only	A 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 56. REGISTER 0X43 − VID REGISTER (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<4:0>	VID[4:0]	Read−only	The VID[4:0] inputs from the CPU to indicate the expected processor core voltage. On power−up, these bits reflect the state of the VID pins even if monitoring is not enabled.
<5>	VID5	Read−only	Reads VID5 from the CPU when Bit 7 = 1. If Bit 7 = 0, then the VID5 bit always reads back 0 (power−on default).
<6>	THLD	R/W	This selects the input switching threshold for the VID inputs. THLD = 0 selects a threshold of 1 V (V_{OL} < 0.8 V, V_{IH} > 1.7 V). THLD = 1 lowers the switching threshold to 0.6 V (V_{OL} < 0.4 V, V_{IH} > 0.8 V).
<7>	VIDSEL	R/W	VIDSEL = 0 configures Pin 21 as the 12 V measurement input (default). VIDSEL = 1 configures Pin 21 as the VID5 input. This also allows VID code changes to be detected.

Table 57. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x44	R/W	2.5 V Low Limit	0x00
0x45	R/W	2.5 V High Limit	0xFF
0x46	R/W	V_{CCP} Low Limit	0x00
0x47	R/W	V_{CCP} High Limit	0xFF
0x48	R/W	V_{CC} Low Limit	0x00
0x49	R/W	V_{CC} High Limit	0xFF
0x4A	R/W	5 V Low Limit	0x00
0x4B	R/W	5 V High Limit	0xFF
0x4C	R/W	12 V Low Limit	0x00
0x4D	R/W	12 V High Limit	0xFF

1. Setting the Configuration Register 1 Lock bit has no effect on these registers.
2. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); Low limits: an interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 58. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the Interrupt Status Register. Setting the Configuration Register 1 Lock bit has no effect on these registers.
2. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); Low limits: an interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 59. FAN TACHOMETER LIMIT REGISTERS (POWER−ON DEFAULT = 0XFF) (Note 1)

Register Address	R/W	Description
0x54	R/W	TACH1 Minimum Low Byte
0x55	R/W	TACH1 Minimum High Byte
0x56	R/W	TACH2 Minimum Low Byte
0x57	R/W	TACH2 Minimum High Byte
0x58	R/W	TACH3 Minimum Low Byte
0x59	R/W	TACH3 Minimum High Byte
0x5A	R/W	TACH4 Minimum Low Byte
0x5B	R/W	TACH4 Minimum High Byte

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 60. PWM CONFIGURATION REGISTERS (POWER−ON DEFAULT = 0X62) (Note 1)

Register Address	R/W	Description
0x5C	R/W	PWM1 Configuration
0x5D	R/W	PWM2 Configuration
0x5E	R/W	PWM3 Configuration

1. These registers become read−only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 61. PWM CONFIGURATION REGISTER BITS

Bit	Name	R/W	Description
<2:0>	SPIN	R/W	These bits control the start−up timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan start−up timeout period, the TACH measurement reads 0xFFFF and Status Register 2 reflects the fan fault. If the TACH Minimum High and Low Byte contains 0xFFFF or 0x0000, the Status Register 2 Bit is not set, even if the fan has not started. 000 = No Start−up Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s
<3>	SLOW	R/W	SLOW = 1 makes the ramp rates for acoustic enhancement four times longer.
<4>	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 Temperature controls PWMx (Automatic Fan Control Mode). 001 = Local Temperature controls PWMx (Automatic Fan Control Mode). 010 = Remote 2 Temperature controls PWMx (Automatic Fan Control Mode). 011 = PWMx runs full speed (Default). 100 = PWMx is disabled. 101 = Fastest speed calculated by Local and Remote 2 Temperature Control PWMx. 110 = Fastest speed calculated by all three Temperature Channels Control PWMx. 111 = Manual Mode. PWM duty cycle registers (Reg. 0x30−0x32) become writable.

Table 62. TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (POWER−ON DEFAULT = 0XC4) (Note 1)

Register Address	R/W	Description
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 Frequency
0x60	R/W	Local Temp T_{RANGE}/PWM2 Frequency
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Frequency

1. These registers become read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to the is register have no effect.

Table 63. TEMP T_{RANGE}/PWM FREQUENCY REGISTER BITS

Bit	Name	R/W	Description
<2:0>	FREQ	R/W	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	THRM	R/W	THRM = 1 causes the $\overline{\text{THERM}}$ pin (Pin 14 or Pin 20) to assert low as an output when this temperature channel's $\overline{\text{THERM}}$ limit is exceeded by 0.25°C. The $\overline{\text{THERM}}$ pin remains asserted until the temperature is equal to or below the $\overline{\text{THERM}}$ limit. The minimum time that $\overline{\text{THERM}}$ asserts for is one monitoring cycle. This allows clock modulation of devices that incorporate this feature. THRM = 0 makes the $\overline{\text{THERM}}$ pin act as an input only, for example, for Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring, when Pin 14 or Pin 20 is configured as $\overline{\text{THERM}}$.
<7:4>	RANGE	R/W	These bits determine the PWM duty cycle vs. temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (Default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

Table 64. REGISTER 0X62 − ENHANCED ACOUSTICS REGISTER 1 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<2:0>	ACOU	R/W	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN1	R/W	When this bit is 1, acoustic enhancement is enabled on PWM1 output.
<4>	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0, only TACH3 and TACH4 are synchronized to PWM3 output.
<5>	MIN1	R/W	When the ADT7463 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM1 Minimum Duty Cycle below T_{MIN} − Hysteresis
<6>	MIN2	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} − Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM2 Minimum Duty Cycle below T_{MIN} − Hysteresis
<7>	MIN3	R/W	When the ADT7463 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN}− Hysteresis value. 0 = 0% Duty Cycle below T_{MIN} − Hysteresis 1 = PWM3 Minimum Duty Cycle below T_{MIN} − Hysteresis

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 65. REGISTER 0X63 − ENHANCED ACOUSTICS REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<2:0>	ACOU3	R/W	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN3	R/W	When this bit is 1, acoustic enhancement is enabled on PWM3 output.
<6:4>	ACOU2	R/W	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 4 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<7>	EN2	R/W	When this bit is 1, acoustic enhancement is enabled on PWM2 output.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 66. PWM MIN DUTY CYCLE REGISTERS (Note 1)

Register Address	R/W	Description	Power−On Default
0x64	R/W	PWM1 Min Duty Cycle	0x80 (50% Duty Cycle)
0x65	R/W	PWM2 Min Duty Cycle	0x80 (50% Duty Cycle)
0x66	R/W	PWM3 Min Duty Cycle	0x80 (50% Duty Cycle)

1. These registers become read−only when the ADT7463 is in automatic fan control mode.

Table 67. PWM MIN DUTY CYCLE REGISTER BITS

Bit	Name	R/W	Description
<7:0>	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

Table 68. T_{MIN} REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x67	R/W	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T_{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T_{MIN}	0x5A (90°C)

1. These registers become read−only when the Configuration Register 1 Lock bit is set. Further attempts to write to these registers have no effect.
2. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increase with temperature according to T_{RANGE}.

Table 69. $\overline{\text{THERM}}$ LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Limit	0x64 (100°C)

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.
2. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail−safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ Limit − Hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.

Table 70. TEMPERATURE HYSTERESIS REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x6D	R/W	Remote 1 Local Temperature Hysteresis	0x44
0x6E	R/W	Remote 2 Temperature Hysteresis	0x40

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.
2. Each 4−bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − Hysteresis. Up to 15°C of hysteresis may be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its $\overline{\text{THERM}}$ limit is exceeded. The PWM output being controlled goes to 100% if the $\overline{\text{THERM}}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ − Hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.

Table 71. XOR TREE TEST ENABLE REGISTER (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description		
0x6F	R/W	XNOR Tree Test Enable		
		Bit	**Name**	**Description**
		<0>	XEN	If the XEN bit is set to 1, the device enters the XOR tree test mode. Clearing the bit removes the device from the XOR test mode.
		<7:1>	RES	Unused. Do not write to these bits.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 72. REMOTE 1 TEMPERATURE OFFSET REGISTER (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x70	R/W	Remote 1 Temperature Offset
<7:0>	R/W	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 Temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.25°C.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 73. LOCAL TEMPERATURE OFFSET REGISTER (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x71	R/W	Local Temperature Offset
<7:0>	R/W	Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.25°C.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 74. REMOTE 2 TEMPERATURE OFFSET REGISTER (POWER−ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x72	R/W	Remote 2 Temperature Offset
<7:0>	R/W	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.25°C.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 75. REGISTER 0X73 − CONFIGURATION REGISTER 2 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
0	AIN1	R/W	AIN1 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 11 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
1	AIN2	R/W	AIN2 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 12 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
2	AIN3	R/W	AIN3 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 9 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
3	AIN4	R/W	AIN4 = 0, Speed of 3−wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 14 is reconfigured to measure the speed of 2−wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (Reg. 0x7D).
4	AVG	R/W	AVG = 1, Averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
5	ATTN	R/W	ATTN = 1, the ADT7463 removes the attenuators from the 2.5 V, V_{CCP}, 5 V, and 12 V inputs. The inputs can be used for other functions such as connecting up external sensors.
6	CONV	R/W	CONV = 1, the ADT7463 is put into a single−channel ADC conversion mode. In this mode, the ADT7463 can be made to read continuously from one input only, for example, Remote 1 temperature. It is also possible to start ADC conversions using an external clock on Pin 11 by setting Bit 2 of Test Register 2 (Reg. 0x7F). This mode could be useful if, for example, users wanted to characterize/profile CPU temperature quickly. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 min high byte register (Reg. 0x55). **Bits <7:5> Reg. 0x55 — Channel Selected** 000 — 2.5V 001 — V_{CCP} 010 — V_{CC} (3.3V) 011 — 5V 100 — 12V 101 — Remote 1 Temp 110 — Local Temp 111 — Remote 2 Temp
7	SHDN	R/W	SHDN = 1, ADT7463 goes into shutdown mode. All PWM outputs assert low (or high depending, on state of INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 76. REGISTER 0X74 − INTERRUPT MASK REGISTER 1 (POWER−ON DEFAULT <7:0> = 0X00)

Bit	Name	R/W	Description
0	2.5V	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the 2.5 V channel.
1	V_{CCP}	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CCP} channel.
2	V_{CC}	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CC} channel.
3	5V	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the 5 V channel.
4	R1T	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the Remote 1 Temperature channel.
5	LT	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the Local Temperature channel.
6	R2T	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the Remote 2 Temperature channel.
7	OOL	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for any out−of−limit condition in Status Register 2.

Table 77. REGISTER 0X75 – INTERRUPT MASK REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
0	12V/VC	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the 12 V channel.
1	OVT	Read−only	A 1 masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
2	FAN1	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	F4P	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ timer event.
6	D1	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 1 channel.
7	D2	R/W	A 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on Remote 2 channel.

Table 78. REGISTER 0X76 – EXTENDED RESOLUTION REGISTER 1

Bit	Name	R/W	Description
<1:0>	12V	Read−only	2.5 V LSBs. Holds the 2 LSBs of the 10−bit 2.5 V measurement.
<3:2>	V_{CCP}	Read−only	V_{CCP} LSBs. Holds the 2 LSBs of the 10−bit V_{CCP} measurement.
<5:4>	V_{CC}	Read−only	V_{CC} LSBs. Holds the 2 LSBs of the 10−bit V_{CC} measurement.
<7:6>	5V	Read−only	5 V LSBs. Holds the 2 LSBs of the 10−bit 5 V measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 79. REGISTER 0X77 – EXTENDED RESOLUTION REGISTER 2 (Note 1)

Bit	Name	R/W	Description
<1:0>	12V	Read−only	12 V LSBs. Holds the 2 LSBs of the 10−bit 12 V measurement.
<3:2>	TDM1	Read−only	Remote 1 Temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 1 temperature measurement.
<5:4>	LTMP	Read−only	Local Temperature LSBs. Holds the 2 LSBs of the 10−bit local temperature measurement.
<7:6>	TDM2	Read−only	Remote 2 Temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 2 temperature measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 80. REGISTER 0X78 – CONFIGURATION REGISTER 3 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<0>	ALERT	R/W	ALERT = 1, Pin 10 (PWM2/ $\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions.
<1>	$\overline{\text{THERM}}$ ENABLE	R/W	$\overline{\text{THERM}}$ ENABLE = 1 enables $\overline{\text{THERM}}$ monitoring functionality on the pin determined by Bit 1 (TH5V) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, fans can be run at full speed (if the BOOST bit is set), or a timer can be triggered to time how long $\overline{\text{THERM}}$ has been asserted for.
<2>	BOOST	R/W	BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at 100% duty cycle for fail−safe cooling.
<3>	FAST	R/W	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second, to once every 250 ms (4×).
<4>	DC1	R/W	DC1 = 1 enables TACH measurements to be continuously made on TACH1.
<5>	DC2	R/W	DC2 = 2 enables TACH measurements to be continuously made on TACH2.
<6>	DC3	R/W	DC3 = 1 enables TACH measurements to be continuously made on TACH3.
<7>	DC4	R/W	DC4 = 1 enables TACH measurements to be continuously made on TACH4.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 81. REGISTER 0X79 – $\overline{\text{THERM}}$ STATUS REGISTER (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:1>	TMR	Read−only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read 0 until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/TMR0	Read−only	Is set high on the assertion of the $\overline{\text{THERM}}$ input. Cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8−bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 s to be reported back with a resolution of 22.76 ms.

Table 82. REGISTER 0X7A – $\overline{\text{THERM}}$ LIMIT REGISTER (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	LIMT	R/W	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8−bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 s to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (Reg. 0x42) is set. If the limit value is 0x00, an interrupt is generated immediately upon the assertion of the $\overline{\text{THERM}}$ input.

Table 83. REGISTER 0X7B – FAN PULSES PER REVOLUTION REGISTER (POWER−ON DEFAULT = 0X55)

Bit	Mnemonic	R/W	Description
<1:0>	FAN1	R/W	Sets number of pulses to be counted when measuring Fan1 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<3:2>	FAN2	R/W	Sets number of pulses to be counted when measuring FAN2 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<5:4>	FAN3	R/W	Sets number of pulses to be counted when measuring FAN3 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<7:6>	FAN4	R/W	Sets number of pulses to be counted when measuring FAN4 speed. Can be used to determine fan's pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

Table 84. REGISTER 0X7D − CONFIGURATION REGISTER 4 (POWER−ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<0>	AL2.5V	R/W	AL2.5V = 1, Pin 14 (2.5 V/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions. AL2.5V = 0, Pin 14 (2.5 V/$\overline{\text{SMBALERT}}$) is configured as a 2.5 V measurement input.
<1>	TH5V	R/W	TH5V = 1, Pin 20 (5V/$\overline{\text{THERM}}$) is configured as $\overline{\text{THERM}}$ pin. For $\overline{\text{THERM}}$ Monitoring, Bit 1 ($\overline{\text{THERM}}$ Timer) of Configuration Register 3 must also be set. TH5V = 0, Pin 20 (5V/$\overline{\text{THERM}}$) is configured as 5 V measurement input.
<3:2>	AINL	R/W	These two bits define the input threshold for 2−wire fan speed measurements: 00 = ±20 mV 01 = ±40 mV 10 = ±80 mV 11 = ±130 mV
<7:4>	RES		Unused.

1. This register becomes read−only when the Configuration Register 1 Lock bit is set to 1. Further attempts to write to this register have no effect.

Table 85. REGISTER 0X7E − MANUFACTURER'S TEST REGISTER 1 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	RES	Read−only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 86. REGISTER 0X7F − MANUFACTURER'S TEST REGISTER 2 (POWER−ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	RES	Read−only	Manufacturer's Test Register. These bits are reserved for manufacturer's test purposes and should NOT be written to under normal operation.

Table 87. ORDERING INFORMATION

Device Number	Temperature Range	Package Type	Package Option	Shipping†
ADT7463ARQZ−REEL	−40°C to +120°C	24−lead QSOP	RQ−24	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb−Free part.

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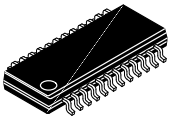
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

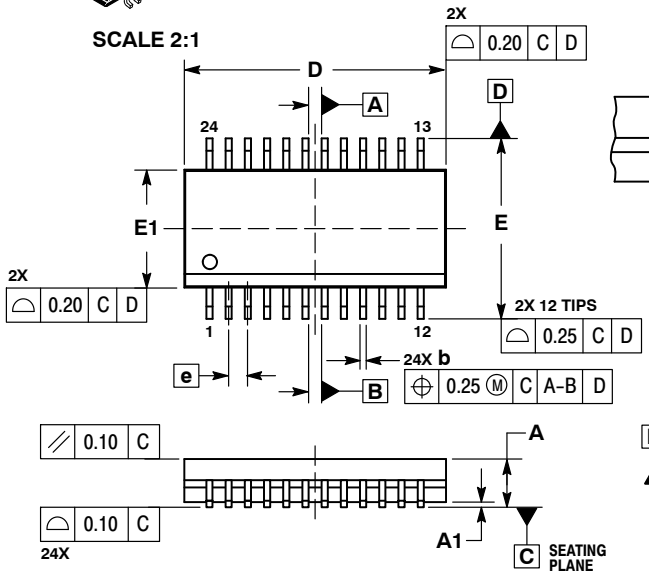
ON Semiconductor®

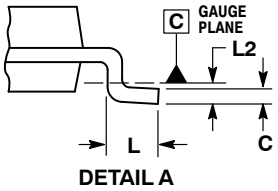
QSOP24 NB
CASE 492B–01
ISSUE A

DATE 06 MAY 2008

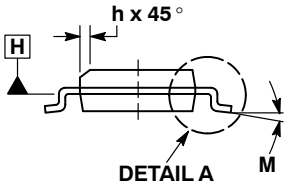


SCALE 2:1





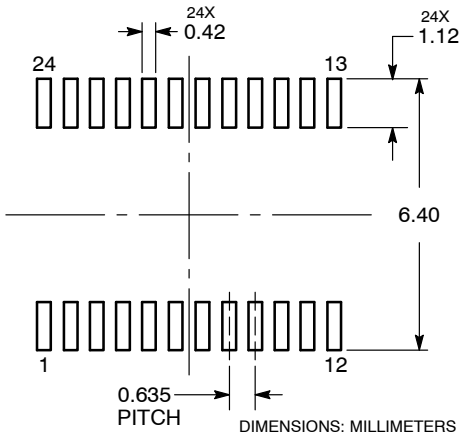
DETAIL A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

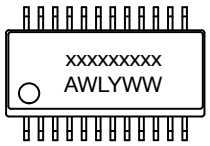
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.20	0.30
C	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G”, may or not be present.

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