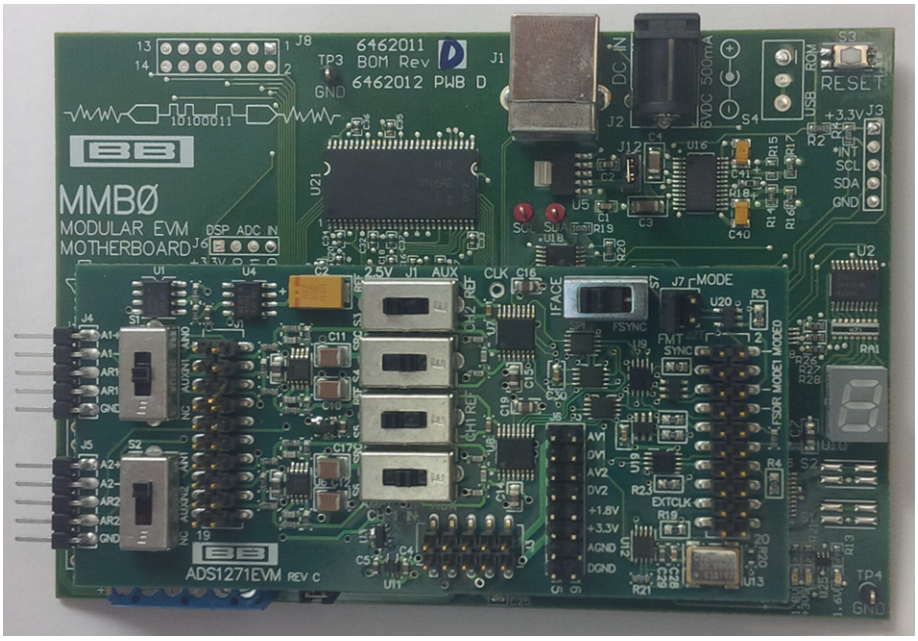
# THE DATASHEET OF

# ADS1271EVM

# ADS1271EVM and ADS1271EVM-PDK User's Guide




**ADS1271EVM-PDK**

This user's guide describes the characteristics, operation, and use of the ADS1271EVM, both by itself and as part of the ADS1271EVM-PDK. This EVM is a 24-bit analog-to-digital converter evaluation module.

This document includes an EVM Quick Start, hardware and software details, bill of materials, and schematic.

The following related documents are available through the Texas Instruments web site at www.ti.com.

**Table 1. EVM-Compatible Device Data Sheets**

| Device | Literature Number |
|---|---|
| ADS1271 | SBAS306 |
| OPA350 | SBOS099B |
| OPA1632 | SBOS286 |
| REF1004 | SBVS002 |
| REF3125 | SBVS046A |
| SN74AVC1T45 | SCES530C |
| SN74AVC2T45 | SCES531D |
| SN74LVC1G125 | SCES223L |
| SN74LVC2G66 | SCES325G |
| SN74LVC2G157 | SCES207I |
| TPS71550 | SLVS338H |

# 1 EVM Overview

## 1.1 Features

**ADS1271EVM Features:**

- Contains all support circuitry needed for the ADS1271
- Two ADS1271 converters on board illustrate use of daisy-chain mode
- Onboard reference and oscillator circuits
- Compatible with the TI Modular EVM System

**ADS1271EVM-PDK** includes the ADS1271EVM board with the DSP-based MMB0 motherboard, that can be used with provided software to quickly evaluate the device.

This manual covers the operation of the ADS1271EVM-PDK. Throughout this document, the abbreviation EVM and the term evaluation module are synonymous with the ADS1271EVM.

# 2 Quick Start

This section provides a Quick Start guide to quickly begin evaluating the ADS1271EVM.

## 2.1 Default Jumper/Switch Configuration

Figure 1 shows the jumpers found on the EVM and locations of ***left***, ***middle*** and ***right*** for switch settings in the following discussion.

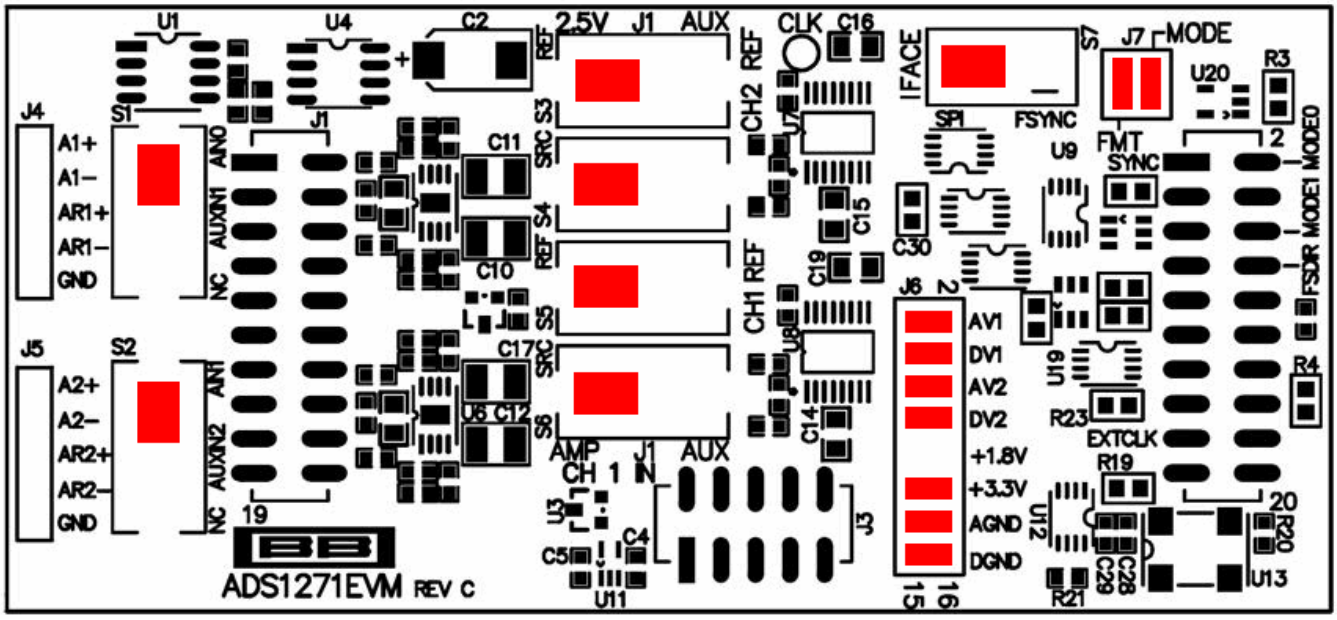



**Figure 1. ADS1271EVM Default Configuration**

Table 2 lists the jumpers and switches and the factory default conditions

**Table 2. Default Jumper/Switch Configuration**

| Switch | Default Position | | Switch Description |
|---|---|---|---|
| S1 | Up | | Analog input from aux header (J4) connected to buffer |
| S2 | Up | | Analog input from aux header (J5) connected to buffer |
| S3 | Left | | 2.5V reference connection to CH2 reference |
| S4 | Left | | Buffer connected to CH2 input |
| S5 | Left | | 2.5V reference connection to CH1 reference |
| S6 | Left | | Buffer connected to CH1 input |
| S7 | Left | | Hardware control of Format is floating |
| J6 | AV1 | Installed | AVDD connection for ADC1 |
| | DV1 | Installed | DVDD connection for ADC1 |
| | AV2 | Installed | AVDD connection for ADC2 |
| | DV2 | Installed | DVDD connection for ADC2 |
| | +1.8V | Uninstalled | Do not connect 1.8V to DVDD (misc ICs and switches) |
| | +3.3V | Installed | Connect 3.3V to DVDD (misc ICs and switches) |
| | AGND | Uninstalled | Do not connect AGND to EVM ground |
| | DGND | Installed | Connect DGND to EVM ground |
| J7 | Installed 1-2 (FMT) | | SPI Format controlled by software or hardware (S7) |
| | Installed 3-4 (MODE) | | ADS1271 MODE pin controlled via software |

## 2.2 ADS1271EVM-PDK Operation

Follow these steps to evaluate the ADS1271 with the ADS1271EVM-PDK:

1. Verify that the jumpers on the ADS1271EVM are as shown in Figure 1 (note that these settings are the factory-configured settings for the EVM).
2. Verify that the MMB0 jumpers are in the default position.
   - MMB0 J13A → Open
   - MMB0 J13B → Short
3. Plug the ADS1271EVM onto the MMB0 (if not already connected). Connectors J1B, J2B, and J3B (female connectors on the bottom side) on the EVM align with male connectors J7, J4, and J5 respectively on the MMB0.

> **CAUTION**
>
> Do not misalign the pins when plugging the ADS1271EVM into the MMB0. Check the pin alignment of the connectors carefully before applying power to the PDK.

4. Complete the following steps to install the evaluation software onto your PC.

> **NOTE:** This software is designed to run on Microsoft® Windows® XP. Other operating systems are not supported.

(a) Download the software from the ADS1271EVM-PDK product folder. Unzip the file and locate the Setup program on the disk and execute it. The Setup program installs the ADS1271 evaluation software on your PC. Follow the instructions and prompts given.

(b) After the main program is installed, a dialog box appears with instructions for installing NI-VISA 3.1 Runtime.

(i) Click *OK* to proceed.

(ii) Click *Unzip* and the archive extracts itself and automatically runs the NI-VISA 3.1 Runtime installer.

(c) Follow the instructions in the NI-VISA 3.1 Runtime Installer. When prompted for which features to install, do the following:

(i) Click on the disk icon next to NI-VISA 3.1

(ii) Select, ***Do not install this feature***.

(iii) Click on the disk icon next to *USB*.

(iv) Select the option which installs this feature.

(v) Click *Next*.

(vi) Accept the license agreement, and continue the installation.

(vii) When the installation completes, click *Finish* on the ADS1271EVM installer window. You may be prompted to restart your computer.

5. When installation is complete, attach a USB cable from your PC to the MMB0.
6. Connect the included AC adapter to the MMB0.
7. If you intend to utilize the analog signal buffers on the EVM, connect ±15V and ground via J14 terminal connections +VA, -VA, and GND on the MMB0. Otherwise, skip this step.
8. Start the software on your PC. The software should automatically find the ADS1271EVM, and a screen similar to the one in Figure 2 should appear.

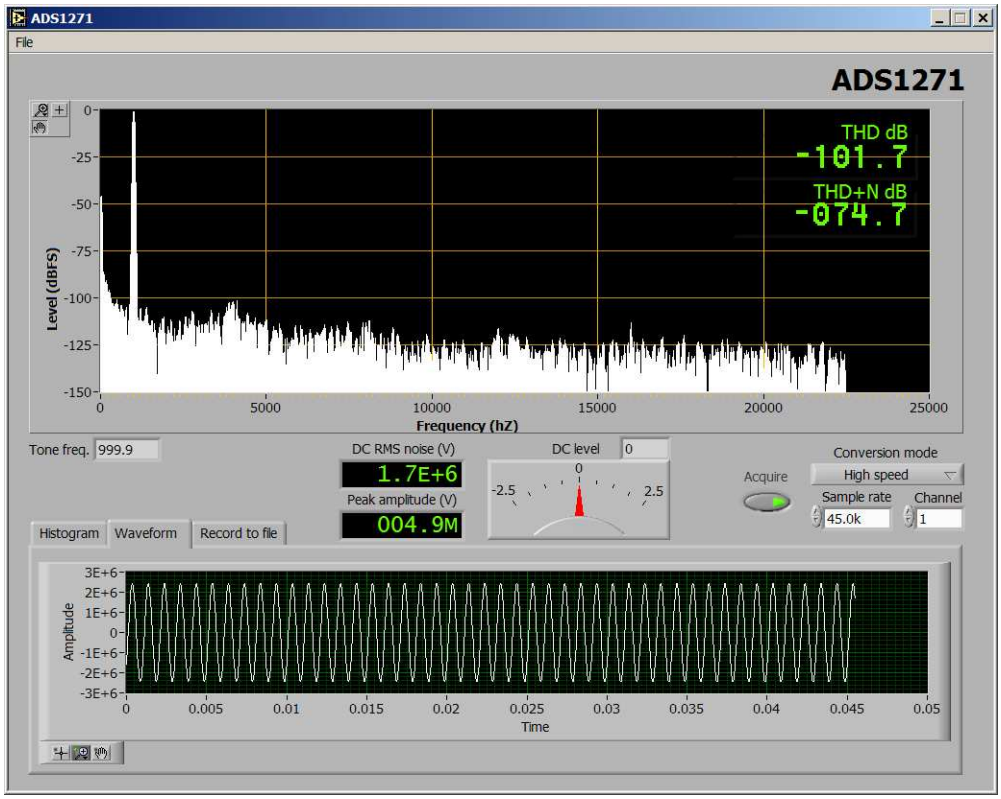



**Figure 2. Default Software Screen**

## 3 Quick Reference

Table 3 provides a quick summary of the connections required for operation of the EVM as a stand-alone board.

**Table 3. Critical Connections**

| Function | | Header/Pin | Pin Name | Description |
|---|---|---|---|---|
| SPI | SCLK | J2.5 | CLKR | SPI Serial Clock |
| | DIN | J2.13 (Top) | DR | SPI Data Input to ADC (MOSI) |
| | DOUT | J2.13 (Bottom) | DR | SPI Data Output from ADC (MISO) |
| | $\overline{\text{DRDY}}$/FSYNC | J2.9 Top | FSOUT | SPI new conversion indication (see Section 5.6.2) |
| | | J2.9 Bottom | FSR | |
| Power | 1.8V | J3.7 | +1.8VD | 1.8V supply for ADC DVDD (option) |
| | 3.3V | J3.9 | +3.3VD | 3.3V supply for ADC DVDD (option) |
| | 5.0V | J3.3 | +5VA | 5.0V supply for ADC AVDD |
| | AVDD (EVM supply) | J3.1 | +VA | Positive supply for buffers (+15V) (only required when using analog buffers) |
| | AVSS (EVM supply) | J3.2 | -VA | Negative supply for buffers (-15V) (only required when using analog buffers) |
| | DGND | J3.5 | DGND | Digital ground from MMB0 |
| | AGND | J3.6 | AGND | Analog ground from MMB0 |
| Analog Inputs | Analog inputs and external reference | J4/5 | Various | Analog inputs and external reference to ADC |

# 4 Software

Once the ADS1271EVM-PDK software (described in Step 4) is installed, evaluation and development with the ADS1271 can begin.

## 4.1 Basic Usage

Once the evaluation software is started, it checks to see whether an MMB0 is connected. If hardware is connected and recognized, the program downloads the firmware to it, and continues to operate. If no hardware is detected, a dialog box is displayed telling you that it cannot find an MMB0. If you see this, make sure the MMB0 is connected and powered on and click *Retry*. If the software cannot find the hardware, you can click *Cancel* to quit the application.

After the program loads the MMB0 successfully, you will see a screen similar to that shown in Figure 2. The top portion of the display shows an FFT of the ADC data and certain AC analysis numbers. Immediately below the FFT graph (middle portion of the display) are a number of controls and meters. At the bottom of the display is a set of tabs, which show either a histogram, a picture of the incoming waveform, or the data recording controls.

To exit the program, select ***File*** → ***Exit*** from the menu bar.

When the program starts, it will be in idle mode. You can put it in either Acquire Mode or Record Mode.

### 4.1.1 Acquire Mode

In Acquire mode, the ADS1271EVM software collects data from the board in 2,048-sample blocks and performs the appropriate analysis. Both AC and DC analyses are performed.

To put the program into Acquire mode, click the **Acquire** button.

In Acquire mode, you can only view the data from one channel at a time. To choose channels, use the **Channel** box.

#### *4.1.1.1 AC Analysis*

The basic AC analysis consists of the FFT graph and THD calculations. The THD analyzer uses an automatic tone-detection algorithm, which searches for the highest harmonic to use for the THD analysis. The detected frequency is shown in the indicator marked *Tone Freq*.

**NOTE:** For the THD analysis to work, the input must be a sine wave below half the Nyquist frequency, since the THD analyzer needs at least one harmonic for correct operation.

#### *4.1.1.2 Time Domain Analysis*

The ADC data is plotted as a waveform in the time domain on the **Waveform** tab located at the bottom of the screen.

#### *4.1.1.3 DC Analysis*

For DC analysis, the middle section of the application provides DC RMS noise (standard deviation), peak amplitude, and a DC level meter.

A histogram of the ADC data is plotted on the **Histogram** tab located at the bottom of the screen. Basic DC measurements work best when the ADC is driven by an amplifier, stable voltage source, or by shorting the inputs.

### 4.1.2 Record Mode

To record/save ADC data, go to the **Record To File** tab and do the following:

1. If **Acquire** is on, turn it off. You must stop acquisition before the record feature can be enabled.
2. Enter acquisition settings using the **Conversion Mode** drop-down control and **Sample Rate** field. The **Channel** selector can be ignored since it has no effect during data recording.

3. Enter a path in the **Destination File** field. You can use the folder icon to browse for the file with a standard file dialog. If the file you enter cannot be opened or created, the record button will be disabled. If the path points to an existing file, the file will be overwritten when you activate recording.
4. Enter the number of ADC samples to record to the file. You can enter this in time duration or number of samples; the controls will update automatically to match. The number of samples is limited by available memory on the MMB0 to a minimum of 2048 samples and a maximum of approximately 2,700,00 points.
5. Click the **Record** button. You will see the **Samples Retrieved** bar graph increase. When it reaches the number of samples you selected, recording will stop and the record button will be turned off.

The data file is a comma-separated values (CSV) file containing comma-delimited decimal ADC values. The first data column is Channel 1 followed by Channel 2. The data file can be imported into a spreadsheet for future inspection and analysis.

## 4.2 Configuration

Sample rate and conversion mode are set to the same for both ADS1271 devices on the EVM.

The three ADS1271 conversion modes are selectable from the drop-down control, **Conversion Mode**.

The ADS1271 clock is generated by a PLL synthesizer on the MMB0. The synthesizer will generate a clock/data rate that is as close as possible to the requested frequency, but the data rate may be slightly different.

The data rate is limited for each of the possible device modes. For high-speed mode, the maximum data rate is approximately 105kSPS. For other modes, it is approximately 52.5kSPS. The application will automatically reduce the data rate to the maximum allowed for that mode that is selected.

# 5 ADS1271EVM Hardware Details

The ADS1271EVM is designed to easily interface with multiple control platforms. Dual-row, header/socket combinations of J1 and J2 allow connection to external circuitry for evaluation and debug.

## 5.1 Jumpers and Switches

The jumpers and switches functions are shown below in Table 4

**Table 4. Jumper and Switch Descriptions**

| Jumper/Switch | Functions | Descriptions |
|---|---|---|
| J1 | Analog inputs/external reference (primary) | Primary analog input/external reference connectors (from MMB0) |
| J2 | Digital Interface signals | Serial Interface and GPIO signals (from MMB0) |
| J3 | Power | Power supply connections (from MMB0) |
| J4 | Analog inputs/external reference (aux) | Auxiliary analog input/eternal reference connector for U7 |
| J5 | Analog inputs/external reference (aux) | Auxiliary analog input/eternal reference connector for U7 |
| J6 | Power | Power selection and supply monitoring |
| J7 | Format/Mode Selection | Connection of Format and Mode controls to ADCs |
| S1 | Analog input to buffer | Selection of which analog signal header to connect to buffer, U5 |
| S2 | Analog input to buffer | Selection of which analog signal header to connect to buffer, U6 |
| S3 | U7 Reference selector | Select source of reference for U7 |
| S4 | U7 Analog Input selector | Select source of analog input for U7 |
| S5 | U8 Reference selector | Select source of reference for U8 |
| S6 | U8 Analog Input selector | Select source of analog input for U8 |
| S7 | Interface selector | Select interface type (FORMAT) |

## 5.2 Analog Connections

### 5.2.1 Analog Interface, J1, J4, and J5

The ADS1271EVM features several analog input options. Signals can be routed directly to the converters or can pass through the onboard buffer amplifiers (U5, U6). Signals can be applied to the board through the standard modular EVM analog connector (J1) or brought in through the auxiliary input connectors (J4, J5). A set of switches selects which analog connector source is used and whether the buffer amplifiers are in the signal path. These switches enable several configurations for evaluation. Switch operation and analog path configuration are described in Section 5.2.2, Table 6 , and Table 7.

For maximum flexibility, the ADS1271EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J1. This header/socket provides access to the analog input pins of the ADS1271.

**Table 5. Analog Interface Pinout (J1)**

| Pin Number | Signal | Description |
|---|---|---|
| J1.1 | AIN0N | ADS1271 (U7) AINN |
| J1.2 | AIN0P | ADS1271 (U7) AINP |
| J1.3 | AIN1N | ADS1271 (U8) AINN |
| J1.4 | AIN1P | ADS1271 (U8) AINP |
| J1.5 | Unused | |
| J1.6 | Unused | |
| J1.7 | Unused | |

**Table 5. Analog Interface Pinout (J1) (continued)**

| Pin Number | Signal | Description |
|---|---|---|
| J1.8 | Unused | |
| J1.15 | Unused | |
| J1.18 | REF(-) | External reference source low side |
| J1.20 | REF(+) | External reference source input (2.5V NOM) |
| J1.9-J1.19 (odd) | GND | Analog ground connections (except J1.15) |
| J1.10-J1.16 (even) | Unused | |

**Table 6. Auxiliary Analog Input 1 Pinout (J4)**

| Pin Number | Signal | Description |
|---|---|---|
| J4.1 | AUX1P | Auxiliary Signal Input 1 - Positive terminal |
| J4.2 | AUX1N | Auxiliary Signal Input 1 - Negative terminal |
| J4.3 | AUXREF1P | Auxiliary Reference Input 1 - Positive terminal |
| J4.4 | AUXREF1N | Auxiliary Reference Input 1 - Negative terminal |
| J4.5 | GND | Ground |

**Table 7. Auxiliary Analog Input 2 Pinout (J5)**

| Pin Number | Signal | Description |
|---|---|---|
| J5.1 | AUX2P | Auxiliary Signal Input 2 - Positive terminal |
| J5.2 | AUX2N | Auxiliary Signal Input 2 - Negative terminal |
| J5.3 | AUXREF2P | Auxiliary Reference Input 2 - Positive terminal |
| J5.4 | AUXREF2N | Auxiliary Reference Input 2 - Negative terminal |
| J5.5 | GND | Ground |

### 5.2.2 Analog Input Selection

The analog input signals can be routed directly to the two ADS1271s on the EVM or they can be routed through an optional buffer amplifier stage built around U5 or U6. Consult the ADS1271 data sheet to determine the maximum analog input range. Table 8 summarizes the position of switches S1 and S2. S4 and S6 can be used to select the routing of the ADS1271 analog inputs as shown in Table 9.

**Table 8. Buffer Amplifier Options - S1 and S2**

| S1/S2 Position | Analog Inputs |
|---|---|
| Top | Input from J1 |
| Middle | Input from J4/J5 auxiliary inputs |
| Bottom | No connection |

**Table 9. ADC Analog Input Options - S4 and S6**

| S4/S6 Position | Analog Inputs |
|---|---|
| Left | Input from Buffer Amplifier |
| Middle | Input from J1 |
| Right | Input from J4/J5 auxiliary inputs |

#### 5.2.2.1 Buffer Amplifiers

The buffer amplifiers on this EVM are OPA1632s (U5, U6). These amplifiers are optimized for ac performance and are configured as fully-differential unity gain buffers. They require ±15V supplies, which are provided from J3 pins 1 and 2.

The OPA1632 requires a common-mode voltage, which is provided on this EVM by U2 and U3. Some users may not wish to use the buffer amplifier section and provide the ±15V supplies. If the ±15V supplies are not connected, then having a voltage on the $V_{OCM}$ pins of the amplifiers would exceed their maximum ratings. Thus, U2 and U3 provide a separate 2.5V reference for the buffer amplifier section rather than using the same reference as the ADS1271, which would always be powered. For this reason, U2 and U3 power is provided through a separate regulator, U11.

## 5.3 Digital Interface, J2

The ADS1271EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the ADS1271.

Because the ADS1271 devices are capable of daisy-chaining, this EVM has been designed to permit stacking; up to four EVMs can be stacked, allowing for eight devices to be placed in a signal chain. To accommodate stacking of EVMs, J2 has some different connections on the top and the bottom side of the board. Differences between top and bottom connectors are highlighted in Table 10.

**Table 10. Digital Interface Pinout (J2)**

| Pin Number | Signal | Description |
|---|---|---|
| J2.1 | $\overline{\text{SYNC}}$ | Synchronization Control |
| J2.2 | MODE0 | 0 = High-Speed Mode<br>1 = Low-Power Mode<br>(In either case, only if Mode1=0) |
| J2.3 | CLKX | CLKXMODE = 1: master clock output<br>CLKXMODE = 0: no connection |
| J2.4 | DGND | Digital ground |
| J2.5 | SCLK | Serial Clock |
| J2.6 | MODE1 | 0 = Mode determined by MODE0<br>1 = High-Resolution Mode |
| J2.7 | Unused. | |
| J2.8 | FSDIR | Indicates FSR direction:<br>0 = Output (DRDY in SPI™ mode)<br>1 = Input (FSYNC mode) |
| J2.9 | Top: FSOUT<br>Bottom: FSR | FSOUT: in FSYNC mode, copy of FSR; in SPI mode, not connected<br>FSR: in FSYNC mode, frame-sync input; in SPI mode, DRDY output from U8 |
| J2.10 | DGND | Digital ground |
| J2.11 | Unused | |
| J2.12 | CLKRMODE | 0 = Use CLKR for SPI Clock<br>1 = Use ADC Clock for SPI clock |
| J2.13 | Top: DIN<br>Bottom: DOUT | Top: Serial data input<br>Bottom: Serial data output |
| J2.14 | CLKXMODE | 0 = CLKX is High Z<br>1 = CLKX outputs ADC master clock |
| J2.15 | Unused | |
| J2.16 | SCL | $I^2C$™ bus serial clock |
| J2.17 | EXTCLK | External ADC clock input |
| J2.18 | DGND | Digital ground |
| J2.19 | OBCLKSEL | Onboard Clock Select:<br>High to select onboard clock instead of external clock. |

**Table 10. Digital Interface Pinout (J2) (continued)**

| Pin Number | Signal | Description |
|---|---|---|
| J2.20 | SDA | $I^2C$ bus data line |

## 5.4 Power Supplies, J3

J3 provides connection to the common power bus for the ADS1271EVM. Power is supplied on the pins listed in Table 11.

**Table 11. Power Supply Pinout**

| Signal | Pin Number | | Signal |
|---|---|---|---|
| +VA (+15V to power buffer amplifier section) | 1 | 2 | –VA (–15V to power buffer amplifier section) |
| +5VA | 3 | 4 | Unused |
| DGND | 5 | 6 | AGND |
| +1.8VD | 7 | 8 | Unused |
| +3.3VD | 9 | 10 | +5VD |

When power is supplied to J3, J6 allows for either 3.3V or 1.8V to be applied to the digital sections of the ADS1271. J6 also provides for a method of measuring AVDD and DVDD supply currents if the shunts on J6.1-2, J6.3-4, J6.5-6, and J6.7-8 are removed and a current meter is connected between the appropriate pins. See the schematic and printed circuit board silkscreen for details.

### 5.4.1 ADC Power

Power for the ADS1271 analog supply voltage (AVDD) comes from +5VA, which is supplied through J3.3. The shunt from J6 pins 1 to 2 applies this supply to the U7 ADS1271 device, while the shunt from J6 pins 5 to 6 applies this supply to the U8 ADS1271.

The ADS1271 digital supply voltage (DVDD) is selected using J6. When a shunt is applied from J6 pins 9 to 10, +1.8VD is selected, and this power comes from J3.7. If a shunt is placed from J6 pins 11 to 12 (the default factory setting), +3.3VD is selected, which is provided from J3.9. J6 pins 13 and 15 provide a means of connecting analog and digital grounds to the EVM; these grounds come from J3.6 and J3.5, respectively. These grounds are always connected together at the EVM.

**CAUTION**

Verify that all power supplies are within the safe operating limits shown on the ADS1271 data sheet before applying power to the EVM.

**CAUTION**

Note that a shunt should only be connected between J6 pins 9 and 10 *OR* pins 11 and 12, but never both; doing so would short the +3.3V supply to the +1.8V digital supply.

### 5.4.2 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied to J6.2 and J6.6, referenced to J6.13. DVDD can be applied to J6.4 and J6.8, referenced to J6.15.

## 5.5 Reference Voltage

The ADS1271 requires an external voltage reference. Two switches, S3 and S5, select the source of the reference for the two ADS1271s on the EVM. An external reference may be supplied through J1 pin 20 on the ADS1271EVM, or through J4 and J5, the auxiliary analog input connectors. A 2.5V reference is provided on the EVM for convenience. These different reference sources can be selected using S3 and S5, as shown in Table 12.

**CAUTION**

Verify that the external reference voltage is within the safe operating limits shown on the ADS1271 data sheet before applying power to the EVM.

**Table 12. Reference Selection Options - S3 and S5**

| S3/S5 Position | Reference Inputs |
|---|---|
| Left | Onboard 2.5V reference |
| Middle | External Reference from J1.20 (REFP) referenced to J1.18 (REFN) |
| Right | S3: AUXREF1 from J4.3 referenced to J4.4<br>S5: AUXREF2 from J5.3 referenced to J5.4 |

## 5.6 Communication Modes

The ADS1271EVM has a digital routing network which can help simulate several possible system connections. The routing network also provides level-shifting, which allows the ADS1271 to be operated at any supported logic level regardless of the logic level used on J2. Note that you are not required to include this circuitry in your own designs; typically no glue logic is required to connect one or more ADS1271s to a processor.

### 5.6.1 Digital Signal Routing Control

Routing is controlled by pins CLKRMODE, CLKXMODE, and OBCLKSEL on J2.

#### 5.6.1.1 CLKR Routing

CLKRMODE controls the direction and connection of CLKR. When CLKRMODE is low, CLKR is an input connected only to SCLK. When CLKRMODE is high, CLKR becomes an output connected to SCLK, and SCLK is tied to CLK. This connection can be useful in both FSYNC and SPI modes.

A pull-down resistor is installed on CLKRMODE, making FSYNC mode the default setting.

**Table 13. CLKR Routing**

| CLKRMODE | CLKR Direction | CLKR Connection to: |
|---|---|---|
| 0 (Low) | Input | SCLK |
| 1 (High) | Output | SCLK (SCLK tied to CLK) |

#### 5.6.1.2 CLKX Routing

When CLKXMODE is high, CLKX is an output connected to CLK. This setting is primarily useful for certain configurations using the McBSP interface of various processors, where CLKX can be used as a reference clock input for the serial port. When CLKXMODE is low, CLKX on J2 is unconnected.

A pull-down resistor is installed on CLKXMODE, making low the default setting.

**Table 14. CLKX Routing**

| CLKXMODE | CLKX Direction | CLX Connected to: |
|---|---|---|
| 0 (Low) | Input | not connected |
| 1 (High) | Output | CLK |

#### *5.6.1.3 OBCLKSEL Routing*

OBCLKSEL selects between one of two master clock sources. When OBCLKSEL is high, the onboard clock is active and used for the master clock. When OBCLKSEL is low, the master clock is taken from EXTCLK on J2, and the onboard oscillator is disabled.

A pull-down resistor is installed on OBCLKSEL, making connection to an external clock the default setting.

**Table 15. OBCLKSEL**

| OBCLKSEL | Master Clock is connected to: |
|---|---|
| 0 (Low) | EXTCLK (J2.17) |
| 1 (High) | On-board clock (U13) |

### 5.6.2 ADS1271 Communication Modes

The ADS1271EVM supports both interface modes for the ADS1271. The interface mode is chosen using switch S7, located near the top-right corner of the EVM.

Depending of the communication mode, J2 pin 9 (FSR on the bottom connector and FSOUT on the top connector) connect to different signals (see Table 16).

In SPI mode, FSR is connected to DRDY output signal from the first ADC (U8), while the second ADC (U7) DRDY line is not connected. FSOUT is not connected.

In FSYNC mode, the FSYNC pins of both ADCs are tied together, and the signal on FSR is copied to the top connector on pin FSOUT.

**Table 16. J2 Pin 9 Routing**

| J2 Pin 9 | Communications Mode | ADC1 (U8) | ADC2 (U7) |
|---|---|---|---|
| FSOUT (Top side) | SPI Mode | Not connected | Not connected |
| | FSYNC Mode | FSYNC | FSYNC |
| FSR (Bottom side) | SPI Mode | DRDY | Not connected |
| | FSYNC Mode | FSYNC | FSYNC |

These configurations provide th capability of stacking ADS1271EVMs in either mode. To stack EVMs, each EVM is required to operating in the same mode.

The MMB0 has the ability to determine the configuration of S7 by monitoring the FSDIR pin on J2. This pin is high when FSOUT is active and FSR is an input, and low when FSOUT is disconnected and FSR is an output.

## *5.7 Clock Source*

The ADS1271 requires a clock signal for proper operation. Several options are available to source this clock signal to the ADC.

### 5.7.1 Onboard Oscillator

A 27MHz clock oscillator is included on the EVM and is selected as the clock source for the device when OBCLKSEL (J2.19) is high.

### 5.7.2 External Oscillator

When OBCLKSEL (J2.19) is low, an external clock source should be connected to J2.17. In this setting, the onboard clock oscillator is shut down.

# 6 EVM Bill of Materials and Schematic

Table 17 contains a complete bill of materials for the modular ADS1271EVM.

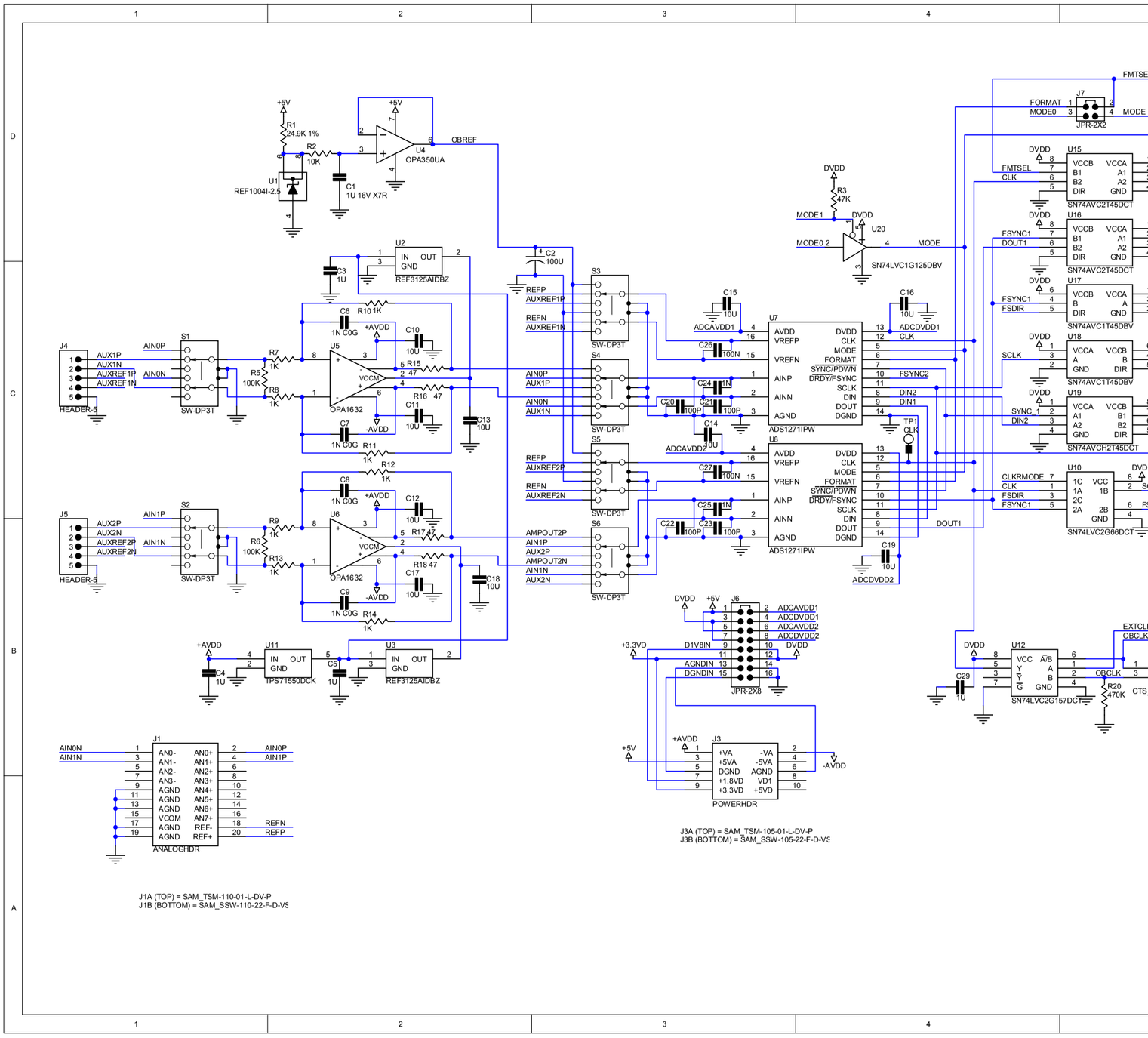
**Table 17. ADS1271EVM Bill of Materials**

| Item | Qty | Value | Ref Des | Description | MFR | Part number |
|---|---|---|---|---|---|---|
| 1 | 1 | | N/A | ADS1271 EVM PWB | Texas Instruments | 6466897 |
| 2 | 5 | 1uF | C1, C3-C5, C29 | CAP CER 1UF 16V 10% X7R 0603 | TDK | C1608X7R1C105K080AC |
| 3 | 1 | 100uF | C2 | CAP TANT 100UF 10V 20% 2917 | Kemet | T520D107M010ATE055 |
| 4 | 6 | 1000pF | C6-C9, C24, C25 | CAP CER 1000PF 50V 5% NP0 0603 | TDK | C1608C0G1H102J080AA |
| 8 | 4 | 10uF | C10-C12, C17 | CAP CER 10UF 25V 20% X7R 1210 | TDK | C3225X7R1E106M250AC |
| 6 | 6 | 10uF | C13-C16, C18, C19 | CAP CER 10UF 6.3V 20% X5R 0805 | TDK | C2012X5R0J106M125AB |
| 7 | 4 | 100pF | C20-C23 | CAP CER 100PF 50V 5% NP0 0603 | TDK | C1608C0G1H101J080AA |
| 8 | 4 | 0.1uF | C26, C27, C30, C31 | CAP CER 0.1UF 50V 10% X7R 0603 | TDK | C1608X7R1H104K080AA |
| 9 | 1 | 0.01uF | C28 | CAP CER 10000PF 50V 10% X7R 0603 | TDK | C1608X7R1H103K080AA |
| 10 | 2 | | J1A, J2T | 20 Pin SMT Plug | Samtec | TSM-110-01-L-DV-P |
| 11 | 2 | | J1B, J2B | 20 pin SMT Socket | Samtec | SSW-110-22-F-D-VS-K |
| 12 | 1 | | J3A | 10 Pin SMT Plug | Samtec | TSM-105-01-L-DV-P |
| 13 | 1 | | J3B | 10 pin SMT Socket | Samtec | SSW-105-22-F-D-VS-K |
| 14 | 2 | | J4, J5 | Terminal Strip, 5 pin (5x1), Right Angle | Samtec | TSW-105-08-L-S-RA |
| 15 | 1 | | J6 | Terminal Strip, 16-pin (8x2) | Samtec | TSW-108-07-L-D |
| 16 | 1 | | J7 | Terminal Strip, 4-pin (2x2) | Samtec | TSW-102-07-L-D |
| 17 | 1 | 24.9K | R1 | RES 24.9K OHM 1/10W 1% 0603 SMD | Panasonic | ERJ-3EKF2492V |
| 18 | 1 | 10K | R2 | RES 10K OHM 1/10W 5% 0603 SMD | Panasonic | ERJ-3GEYJ103V |
| 19 | 4 | 47K | R3, R4, R21, R22 | RES 47K OHM 1/10W 5% 0603 SMD | Panasonic | ERJ-3GEYJ473V |
| 20 | 2 | 100K | R5, R6 | RES 100K OHM 1/10W 5% 0603 SMD | Panasonic | ERJ-3GEYJ104V |
| 21 | 8 | 1K | R7-R14 | RES 1K OHM 1/10W 1% 0603 SMD | Panasonic | ERJ-3EKF1001V |
| 22 | 8 | 47 | R15-R18, R23-R26 | RES 47 OHM 1/10W 5% 0603 SMD | Panasonic | ERJ-3GEYJ470V |
| 23 | 2 | 470K | R19, R20 | RES 470K OHM 1/10W 5% 0603 SMD | Panasonic | ERJ-3GEYJ474V |
| 24 | 6 | | S1-S6 | SWITCH SLIDE DP3T L=2MM 30V | E-Switch | EG2305A |
| 25 | 1 | | S7 | SWITCH SLIDE 2POS VERT BLK 125V | TE Connectivity | 1825115-1 |
| 26 | 0 | | TP1 | | | |
| 27 | 1 | | U1 | IC VREF SHUNT 2.5V 8SOIC | Texas Instruments | REF1004I-2.5 |
| 28 | 2 | | U2, U3 | IC VREF SERIES 2.5V SOT23-3 | Texas Instruments | REF3125AIDBZT |
| 29 | 1 | | U4 | IC OPAMP GP 38MHZ RRO 8SOIC | Texas Instruments | OPA350UA |
| 30 | 2 | | U5, U6 | IC OPAMP AUDIO 180MHZ 8MSOP | Texas Instruments | OPA1632DGN |
| 31 | 2 | | U7, U8 | IC ADC 24BIT 52.73K/105K 16TSSOP | Texas Instruments | ADS1271IPW |
| 32 | 2 | | U9, U10 | IC SWITCH DUAL 1X1 SM8 | Texas Instruments | SN74LVC2G66DCT |
| 33 | 1 | | U11 | IC REG LDO 5V 50MA SC70-5 | Texas Instruments | TPS71550DCKR |
| 34 | 1 | | U12 | IC 2-1LINE DATA SELECT/MUX SM8 | Texas Instruments | SN74LVC2G157DCTR |
| 35 (1) | 1 | 27MHz | U13 | OSC XO 27.000MHZ HCMOS TTL SMD | CTS | CB3LV-5I-27M0000 |
| | | | | OSC XO 27.000MHZ CMOS TTL SMD | CITIZEN | CSX750FBC27.000MT |
| | | | | OSCILLATOR CMOS PROG 3.3V OE SMD | EPSON | SG-8002CA-PCB |
| 36 | 2 | | U15, U16 | IC BUS TXRX TRI-ST 2BIT SM8 | Texas Instruments | SN74AVC2T45DCTR |
| 37 | 2 | | U17, U18 | IC BUS TRANSCVR TRI-ST SOT23-6 | Texas Instruments | SN74AVC1T45DBVR |
| 38 | 1 | | U19 | IC BUS TRANSCVR TRI-ST 2B SM8 | Texas Instruments | SN74AVCH2T45DCTR |
| 39 | 1 | | U20 | IC BUS BUFF TRI-ST N-INV SOT23-5 | Texas Instruments | SN74LVC1G125DBVR |
| 40 | 9 | | N/A | SHUNT JUMPER .1" BLACK GOLD | 3M | 969102-0000-DA |

(1) **NOTE:** Any of these part numbers is acceptable for Item # 35

## 6.1 ADS1271EVM Schematic

The schematic diagram is provided as a reference.


+5V
R1
24.9K 1%
R2
10K
U1
REF1004I-2.5
C1
1U 16V X7R
U4
OPA350UA
OBREF
U2
REF3125AIDBZ
C3
1U
C2
100U
REFP
AUXREF1P
REFN
AUXREF1N
J4
HEADER-5
AUX1P
AUX1N
AUXREF1P
AUXREF1N
AIN0P
AIN0N
S1
SW-DP3T
R7
1K
R5
100K
R8
1K
U5
OPA1632
VOCM
C6
1N C0G
C10
10U
R10 1K
R15
47
R16
47
C11
10U
C7
1N C0G
C13
10U
-AVDD
+AVDD
R11
1K
R12
1K
J5
HEADER-5
AUX2P
AUX2N
AUXREF2P
AUXREF2N
AIN1P
AIN1N
S2
SW-DP3T
R9
1K
R6
100K
R13
1K
U6
OPA1632
C8
1N C0G
C12
10U
R17 47
R18 47
C17
10U
C9
1N C0G
C18
10U
R14
1K
U11
TPS71550DCK
C4
1U
C5
1U
U3
REF3125AIDBZ
J1
ANALOGHDR
AN0-
AN1-
AN2-
AN3-
AGND
VCOM
REF-
REF+
AN0+
AN1+
AN2+
AN3+
AN4+
AN5+
AN6+
AN7+
REFN
REFP
J1A (TOP) = SAM_TSM-110-01-L-DV-P
J1B (BOTTOM) = SAM_SSW-110-22-F-D-VS
S3
S4
S5
S6
SW-DP3T
AMPOUT2P
AMPOUT2N
AUX1P
AUX2P
AUX1N
AUX2N
U7
U8
ADS1271IPW
AVDD
VREFP
VREFN
AINP
AINN
AGND
DVDD
CLK
MODE
FORMAT
SYNC/PDWN
DRDY/FSYNC
SCLK
DIN
DOUT
C15
10U
C16
10U
C26
100N
C24
1N
C21
100P
C20
100P
C14
10U
C27
100N
C25
1N
C22
100P
C23
100P
C19
10U
ADCAVDD1
ADCAVDD2
ADCDVDD1
ADCDVDD2
TP1
CLK
DOUT1
FSYNC2
DIN2
DIN1
R3
47K
U20
SN74LVC1G125DBV
MODE1
MODE0
MODE
J6
D1V8IN
AGNDIN
DGNDIN
JPR-2X8
J3
POWERHDR
+VA
+5VA
DGND
+1.8VD
+3.3VD
-VA
-5VA
AGND
VD1
+5VD
-AVDD
+3.3VD
J3A (TOP) = SAM_TSM-105-01-L-DV-P
J3B (BOTTOM) = SAM_SSW-105-22-F-D-VS
J7
JPR-2X2
FORMAT
MODE0
MODE
FMTSEL
U15
U16
U17
U18
U19
SN74AVC2T45DCT
SN74AVC1T45DBV
SN74AVCH2T45DCT
FSYNC1
DOUT1
SCLK
DIN2
DIN1
SYNC_1
CLKRMODE
FSDIR
U10
SN74LVC2G66DCT
U12
SN74LVC2G157DCT
C29
1U
R20
470K
EXTCLK
OBCLK
CTS_

# Revision History

| Changes from B Revision (February 2008) to C Revision | Page |
|---|---|
| • Added front page picture. | 1 |
| • Added Quick Start section. | 3 |
| • Changed setup steps for clarification. | 4 |
| • Added note to explain operating system limitations. | 4 |
| • Added Critical Connections table to consolidate connection information. | 5 |
| • Changed Sections 4 and 5 organization for clarity. | 6 |
| • Changed text to indicated minimum and maximum number of points for collection | 7 |
| • Changed BOM to reflect latest hardware values. | 15 |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      **CAUTION**

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      **FCC Interference Statement for Class A EVM devices**

      *NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

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4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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