THE DATASHEET OF

ADRF6720-27ACPZ-R7

www.win-source.net 0086-755-83957316

Wideband Quadrature Modulator with Integrated Fractional-N PLL and VCOs

Data Sheet

ADRF6720-27

FEATURES

I/Q modulator with integrated fractional-N PLL
RF output frequency range: 400 MHz to 3000 MHz
Internal LO frequency range: 356.25 MHz to 2855 MHz
Output P1dB: 10.8 dBm at 2140 MHz
Output IP3: 31.1 dBm at 2140 MHz
Carrier feedthrough: −44.3 dBm at 2140 MHz
Sideband suppression: −40.8 dBc at 2140 MHz
Noise floor: −159.5 dBm/Hz at 2140 MHz
Baseband 1 dB modulation bandwidth: >1000 MHz
Baseband input bias level: 2.68 V
Power supply: 3.3 V/425 mA
Integrated RF tunable balun allowing single-ended RF output
Multicore integrated VCOs
HD3/IP3 optimization
Sideband suppression and carrier feedthrough optimization
High-side/low-side LO injection
Programmable via 3-wire serial port interface (SPI)
40-lead 6 mm × 6 mm LFCSP

APPLICATIONS

2G/3G/4G/LTE broadband communication systems
Microwave point-to-point radios
Satellite modems
Military/aerospace
Instrumentation

GENERAL DESCRIPTION

The ADRF6720-27 is a wideband quadrature modulator with an integrated synthesizer ideally suited for 3G and 4G communication systems. The ADRF6720-27 consists of a high linearity broadband modulator, an integrated fractional-N phase-locked loop (PLL), and four low phase noise multicore voltage controlled oscillators (VCOs).

The ADRF6720-27 local oscillator (LO) signal can be generated internally via the on-chip integer-N and fractional-N synthesizers, or externally via a high frequency, low phase noise LO signal. The internal integrated synthesizer enables LO coverage from 356.25 MHz to 2855 MHz using the multicore VCOs. In the case of internal LO generation or external LO input, quadrature signals are generated with a divide by 2 phase splitter. When the ADRF6720-27 is operated with an external 1 × LO input, a polyphase filter generates the quadrature inputs to the mixer.

The ADRF6720-27 offers digital programmability for carrier feedthrough optimization, sideband suppression, HD3/IP3 optimization, and high-side or low-side LO injection.

The ADRF6720-27 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, RoHS-compliant, 6 mm × 6 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

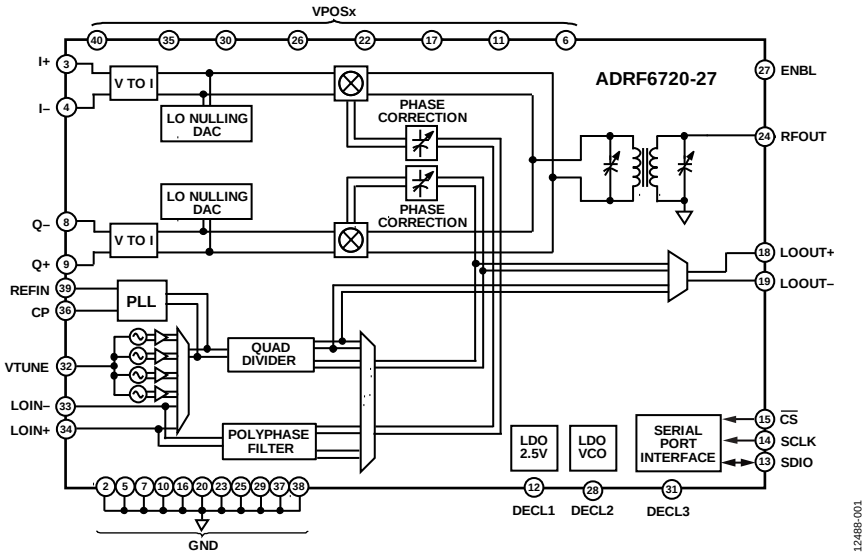

Figure 1.

Rev. B **Document Feedback**

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REVISION HISTORY

9/15—Rev. A to Rev. B

Changed RF_{OUT} = 4 dBm to RF_{OUT} ≈ 4 dBm, and USB to Sideband Suppression ... Throughout
Changes to Spurious Performance Section and Figure 59 ... 28
Changes to Figure 60 ... 29

3/15—Rev. 0 to Rev. A

Added Spurious Performance Section and Figure 57 to Figure 59; Renumbered Sequentially ... 28
Added Figure 60 ... 29

10/14—Revision 0: Initial Version

SPECIFICATIONS

VPOSx = 3.3 V, T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 2.68 V dc bias, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE	RF output range	400		3000	MHz
	Internal LO range	356.25		2855	MHz
	External LO range	400		3000	MHz
RF OUTPUT = 460 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		−0.7		dBm
Modulator Voltage Gain			−4.68		dB
Output P1dB			6.1		dBm
Carrier Feedthrough			−53.0		dBm
Sideband Suppression			−50.2		dBc
Quadrature Error			0.18		Degrees
I/Q Amplitude Balance			0.023		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−77.1		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−61.5		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		58.1		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		27.2		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−161.2		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−160.1		dBm/Hz
RF OUTPUT = 940 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		5.0		dBm
Modulator Voltage Gain			1.02		dB
Output P1dB			11.75		dBm
Carrier Feedthrough			−45.5		dBm
Sideband Suppression			−47.3		dBc
Quadrature Error			−0.05		Degrees
I/Q Amplitude Balance			0.022		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−69.5		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−60.6		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		65.8		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		34.8		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−158.2		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.3		dBm/Hz
RF OUTPUT = 1900 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		4.5		dBm
Modulator Voltage Gain			0.52		dB
Output P1dB			11.4		dBm
Carrier Feedthrough			−37.5		dBm
Sideband Suppression			−40.4		dBc
Quadrature Error			1.21		Degrees
I/Q Amplitude Balance			0.006		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−65.0		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−61.4		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		59.8		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		32.7		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−157.5		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−156.6		dBm/Hz
RF OUTPUT = 2140 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		4.0		dBm
Modulator Voltage Gain			0.02		dB
Output P1dB			10.8		dBm
Carrier Feedthrough			−44.3		dBm
Sideband Suppression			−40.8		dBc
Quadrature Error			−0.78		Degrees
I/Q Amplitude Balance			−0.015		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−58.4		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−67.3		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		58.7		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		31.1		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−159.5		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−158.6		dBm/Hz
RF OUTPUT = 2300 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		3.5		dBm
Modulator Voltage Gain			−0.48		dB
Output P1dB			10.3		dBm
Carrier Feedthrough			−40.8		dBm
Sideband Suppression			−37.4		dBc
Quadrature Error			−1.38		Degrees
I/Q Amplitude Balance			−0.015		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−58.8		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−65.8		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		57.5		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		28.1		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−158.6		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.5		dBm/Hz
RF OUTPUT = 2600 MHz					
Output Power, P_{OUT}	Baseband V_{IQ} = 1 V p-p differential		2.9		dBm
Modulator Voltage Gain			−1.08		dB
Output P1dB			9.9		dBm
Carrier Feedthrough			−37.1		dBm
Sideband Suppression			−40.7		dBc
Quadrature Error			−0.80		Degrees
I/Q Amplitude Balance			0.003		dB
Second Harmonic	$P_{OUT} - P(f_{LO} \pm (2 \times f_{BB}))$		−61.2		dBc
Third Harmonic	$P_{OUT} - P(f_{LO} \pm (3 \times f_{BB}))$		−59.1		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		53.5		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, baseband I/Q amplitude per tone = 0.3 V p-p differential		27.9		dBm
Noise Floor	I/Q input with 2.68 V dc bias and no RF output, 20 MHz carrier offset		−158.6		dBm/Hz
	I/Q input with 2.68 V dc bias and −10 dBm RF output, 20 MHz carrier offset		−157.3		dBm/Hz
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to the modulator output				
Figure of Merit (FOM)[1]			−218.5		dBc/Hz/Hz
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
REFIN Input Frequency		5.7		320	MHz
REFIN Input Amplitude			4		dBm
Phase Detector Frequency		11.4		40	MHz
MUXOUT Output Level	Low (lock detect output selected)		0.25		V
	High (lock detect output selected)		2.7		V
MUXOUT Duty Cycle			50		%
CHARGE PUMP					
Charge Pump Current	Programmable to 250 µA, 500 µA, 750 µA, or 1000 µA		1000		µA
Output Compliance Range		1		2.8	V
PHASE NOISE, FREQUENCY = 460 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−102.1		dBc/Hz
	100 kHz offset		−125.2		dBc/Hz
	1 MHz offset		−144.4		dBc/Hz
	5 MHz offset		−149.6		dBc/Hz
	10 MHz offset		−150.8		dBc/Hz
	20 MHz offset		−150.6		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.09		°rms
Reference Spurs	f_{PFD}		−97.7		dBc
	$f_{PFD} \times 2$		−93.3		dBc
	$f_{PFD} \times 3$		−91.5		dBc
	$f_{PFD} \times 4$		−96.2		dBc
PHASE NOISE, FREQUENCY = 940 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−97.9		dBc/Hz
	100 kHz offset		−121.3		dBc/Hz
	1 MHz offset		−144.3		dBc/Hz
	5 MHz offset		−153.7		dBc/Hz
	10 MHz offset		−154.3		dBc/Hz
	20 MHz offset		−154.7		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.15		°rms
Reference Spurs	f_{PFD}		−99.2		dBc
	$f_{PFD} \times 2$		−92.3		dBc
	$f_{PFD} \times 3$		−95.2		dBc
	$f_{PFD} \times 4$		−101.3		dBc
PHASE NOISE, FREQUENCY = 1900 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−92.2		dBc/Hz
	100 kHz offset		−114.8		dBc/Hz
	1 MHz offset		−139.8		dBc/Hz
	5 MHz offset		−151.4		dBc/Hz
	10 MHz offset		−152.8		dBc/Hz
	20 MHz offset		−153.4		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.31		°rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Reference Spurs	f_{PFD}		−93.2		dBc
	$f_{PFD} \times 2$		−86.8		dBc
	$f_{PFD} \times 3$		−89.8		dBc
	$f_{PFD} \times 4$		−101.7		dBc
PHASE NOISE, FREQUENCY = 2140 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−92.9		dBc/Hz
	100 kHz offset		−116.2		dBc/Hz
	1 MHz offset		−140.3		dBc/Hz
	5 MHz offset		−150.7		dBc/Hz
	10 MHz offset		−151.8		dBc/Hz
	20 MHz offset		−152.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.29		°rms
Reference Spurs	f_{PFD}		−91.3		dBc
	$f_{PFD} \times 2$		−90.3		dBc
	$f_{PFD} \times 3$		−85.6		dBc
	$f_{PFD} \times 4$		−91.0		dBc
PHASE NOISE, FREQUENCY = 2300 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−94.6		dBc/Hz
	100 kHz offset		−114.8		dBc/Hz
	1 MHz offset		−139.0		dBc/Hz
	5 MHz offset		−149.4		dBc/Hz
	10 MHz offset		−151.1		dBc/Hz
	20 MHz offset		−151.5		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.26		°rms
Reference Spurs	f_{PFD}		−96.1		dBc
	$f_{PFD} \times 2$		−91.9		dBc
	$f_{PFD} \times 3$		−88.2		dBc
	$f_{PFD} \times 4$		−94.8		dBc
PHASE NOISE, FREQUENCY = 2600 MHz, f_{PFD} = 38.4 MHz	Closed-loop operation (20 kHz loop filter, see Figure 44 for loop filter design)				
	10 kHz offset		−92.4		dBc/Hz
	100 kHz offset		−111.4		dBc/Hz
	1 MHz offset		−137.2		dBc/Hz
	5 MHz offset		−147.7		dBc/Hz
	10 MHz offset		−148.9		dBc/Hz
	20 MHz offset		−149.9		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth, with spurs		0.36		°rms
Reference Spurs	f_{PFD}		−95.5		dBc
	$f_{PFD} \times 2$		−85.4		dBc
	$f_{PFD} \times 3$		−93.4		dBc
	$f_{PFD} \times 4$		−91.0		dBc
LO INPUT/OUTPUT					
LO Output Frequency Range	1 × LO mode	356.25		2855	MHz
	2 × LO mode	712.5		5710	MHz
LO Output Level	2 × LO or 1 × LO mode, into a 50 Ω load, LO buffer enabled at 2140 MHz				
	LO_DRV_LVL = 0		−5.8		dBm
	LO_DRV_LVL = 1		−1.0		dBm
	LO_DRV_LVL = 2		2.2		dBm
LO Input Level	Externally applied LO, PLL disabled	−6	0	+6	dBm
LO Input Impedance	Externally applied LO, PLL disabled		50		Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BASEBAND INPUTS	I± and Q± pins				
I and Q Input DC Bias Level			2.68		V
Bandwidth	1 dB		>1000		MHz
Differential Input Impedance	Frequency = 100 MHz[2]		55		KΩ
Differential Input Capacitance	Frequency = 100 MHz[2]		0.97		pF
OUT ENABLE	ENBL pin				
Turn-On Settling Time	ENBL low to high (90% of envelope), when Register 0x01[10] = 1, Register 0x10[10] = 1		170		ns
Turn-Off Settling Time	ENBL high to low (10% of envelope), when Register 0x01[10] = 1, Register 0x10[10] = 1		10		ns
DIGITAL LOGIC	SCLK, SDIO, $\overline{CS}$, and ENBL				
Input Voltage High (V_{IH})		1.4			V
Input Voltage Low (V_{IL})				0.7	V
Input Current (I_{IH}/I_{IL})		−1		+1	µA
Input Capacitance (C_{IN})			5		pF
Output Voltage High (V_{OH})	I_{OH} = −100 µA	2.3			V
Output Voltage Low (V_{OL})	I_{OL} = +100 µA			0.2	V
POWER SUPPLIES					
Voltage Range	VPOSx		3.3		V
Supply Current	Tx mode at internal LO mode (PLL, internal VCO , and modulator enabled, LO output driver disabled)		425		mA
	Tx mode at external 1× LO mode (PLL, internal VCO disabled, modulator enabled, LO output driver disabled)		218		mA
	LO output driver; LO_DRV_LVL bits (Register 0x22[7:6]) = 10		42		mA
	Power-down mode		14.5		mA

[1] The figure of merit (FOM) is computed as phase noise (dBc/Hz) − 10log10(f_{PFD}) − 20log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm with a 38.4 MHz f_{PFD}. The FOM was computed at a 50 kHz offset.
[2] Refer to Figure 47 for a plot of input impedance over frequency.

TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCLK}	Serial clock period	38			ns
t_{DS}	Setup time between data and rising edge of SCLK	8			ns
t_{DH}	Hold time between data and rising edge of SCLK	8			ns
t_S	Setup time between falling edge of $\overline{CS}$ and SCLK	10			ns
t_H	Hold time between rising edge of $\overline{CS}$ and SCLK	10			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		13		ns
t_z	Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance			5	ns

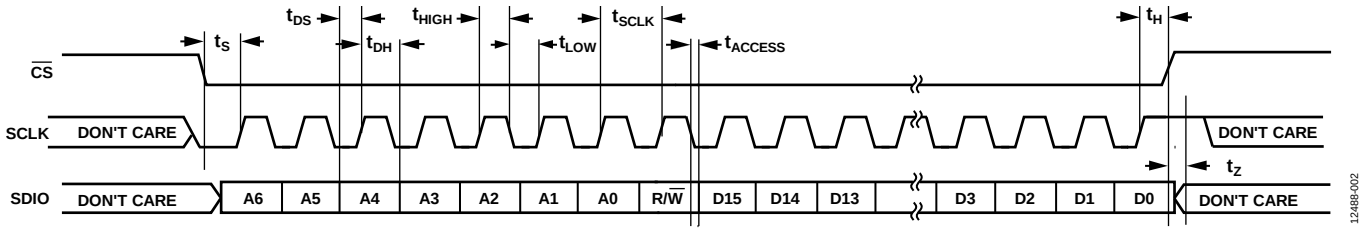


Figure 2. Serial Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
I+, I−, Q+, Q−	−0.5 V to +3.6 V
LOIN+, LOIN−	16 dBm differential
REFIN	−0.3 V to +3.6 V
ENBL	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
$\overline{CS}$, SCLK, SDIO	−0.3 V to +3.6 V
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
40-Lead LFCSP	30.23	0.44	°C/W

[1] See JEDEC standard JESD51-2 for information on optimizing thermal impedance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

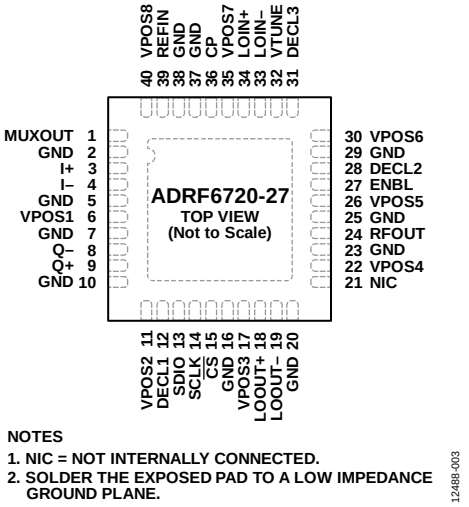


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MUXOUT	Multiplexer Output. This output allows a digital lock detect signal, a voltage proportional to absolute temperature (VPTAT), or a buffered, frequency-scaled reference signal to be accessed externally. The output is selected by programming Bits[6:4] in Register 0x21.
2, 10	GND	Baseband Ground.
3, 4	I+, I–	Differential In-Phase Baseband Inputs.
5, 7	GND	Mixer Core (I and Q) Ground.
6	VPOS1	3.3 V Supply Voltage for Baseband. Decouple VPOS1 with 100 pF and 0.1 µF capacitors located close to the pin.
8, 9	Q–, Q+	Differential Quadrature Baseband Inputs.
11	VPOS2	3.3 V Supply Voltage for 2.5 V LDO. Decouple VPOS2 with 100 pF and 0.1 µF capacitors located close to the pin.
12	DECL1	Decoupling Pin for 2.5 V LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
13	SDIO	Serial Data Input/Output for SPI.
14	SCLK	Serial Clock Input/Output for SPI.
15	$\overline{CS}$	Chip Select Input/Output for SPI.
16	GND	Digital Ground.
17	VPOS3	3.3 V Supply Voltage for LO. Decouple VPOS3 with 100 pF and 0.1 µF capacitors located close to the pin.
18, 19	LOOUT+, LOOUT–	Differential LO Outputs. Either the internally generated LO or external 1 × LO/2 × LO is available at 1 × LO or 2 × LO on these pins.
20	GND	LO Ground.
21	NIC	Not Internally Connected. This pin can be left open or tied to RF ground.
22	VPOS4	3.3 V Supply Voltage for RF. Decouple VPOS4 with 100 pF and 0.1 µF capacitors located close to the pin.
23, 25	GND	RF Ground.
24	RFOUT	Single-Ended 0 V DC RF Output.
26	VPOS5	3.3 V Supply Voltage for RF. Decouple VPOS5 with 100 pF and 0.1 µF capacitors located close to the pin.
27	ENBL	Enables/Disables the Circuit Blocks. References the settings at Register 0x01 and Register 0x10. Refer to the ENBL section for more information.
28	DECL2	Decoupling Pin for VCO LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
29	GND	VCO Ground.
30	VPOS6	3.3 V Supply Voltage for VCO LDO. Decouple VPOS6 with 100 pF and 0.1 µF capacitors located close to the pin.
31	DECL3	Decoupling Pin for VCO LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
32	VTUNE	VCO Tuning Voltage.
33, 34	LOIN–, LOIN+	Differential External LO Inputs.
35	VPOS7	3.3 V Supply Voltage for Charge Pump. Decouple VPOS7 with 100 pF and 0.1 µF capacitors located close to the pin.

Pin No.	Mnemonic	Description
36	CP	Charge Pump Output.
37	GND	Charge Pump Ground.
38	GND	PLL Reference Ground.
39	REFIN	PLL Reference Input.
40	VPOS8	3.3 V Supply Voltage for PLL Reference. Decouple VPOS8 with 100 pF and 0.1 µF capacitors located close to the pin.
	EP	Exposed Pad. Solder the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VPOSx = 3.3 V; T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 2.68 V dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz; f_{PFD} = 38.4 MHz; f_{REF} = 153.6 MHz at 4 dBm referred to 50 Ω (1 V p-p); 20 kHz loop filter, unless otherwise noted.

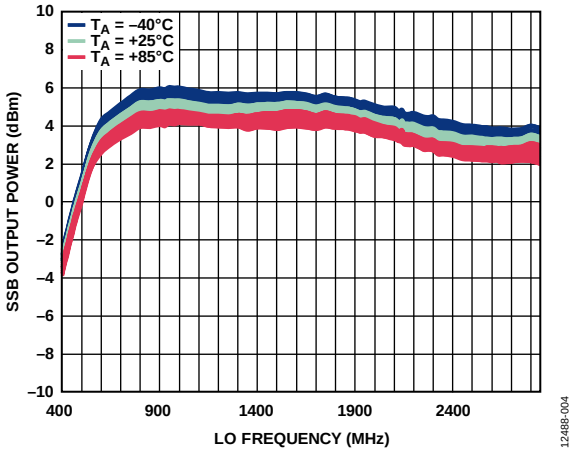


Figure 4. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

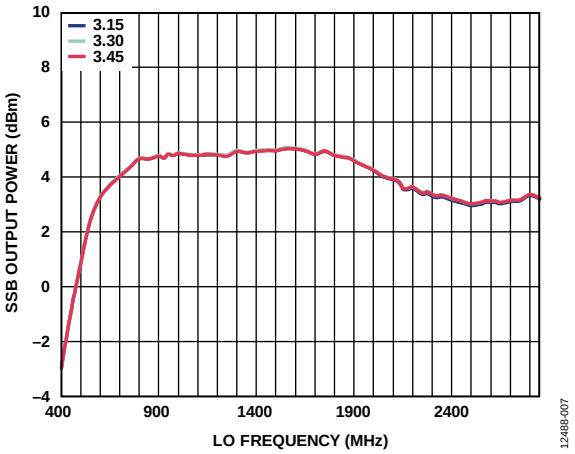


Figure 7. SSB Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Supply

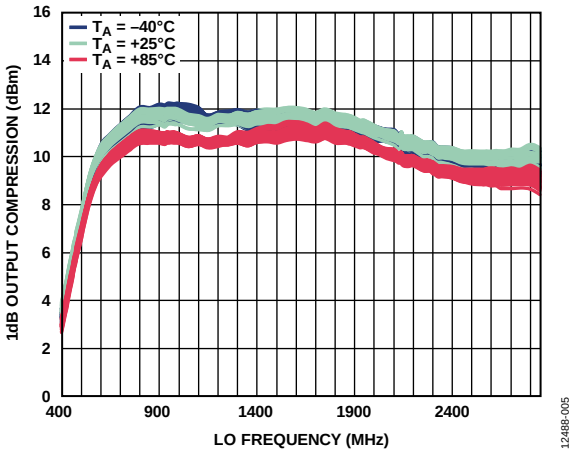


Figure 5. SSB 1 dB Output Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

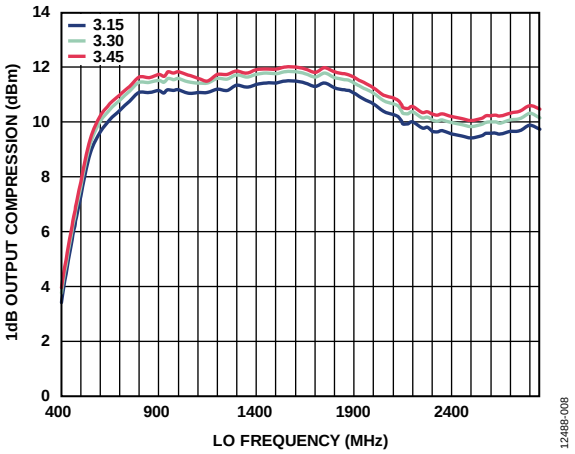


Figure 8. SSB 1 dB Output Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Supply

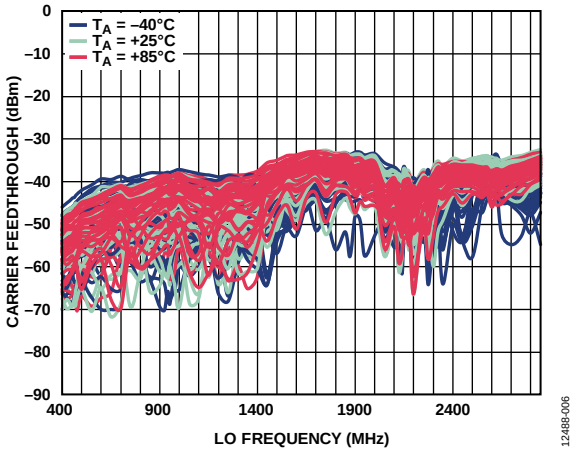


Figure 6. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature Before Nulling; Multiple Devices Shown

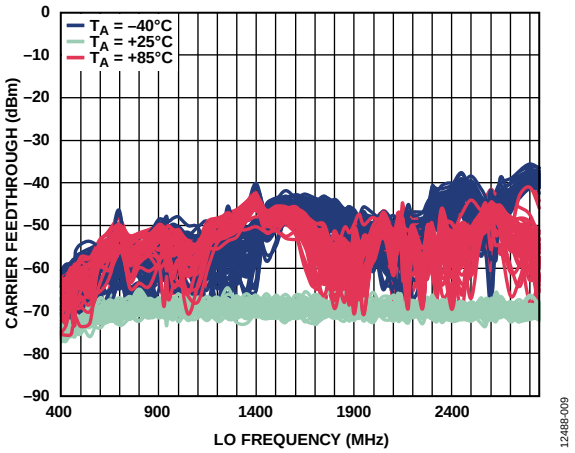


Figure 9. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature After Nulling Using DCOFF_I and DCOFF_Q at 25°C; Multiple Devices Shown

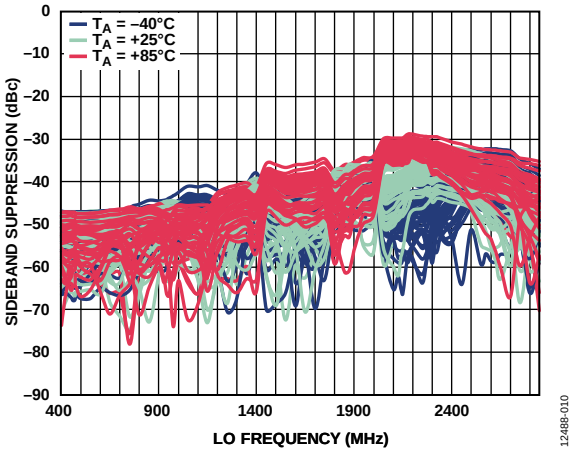


Figure 10. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature Before Nulling; Multiple Devices Shown

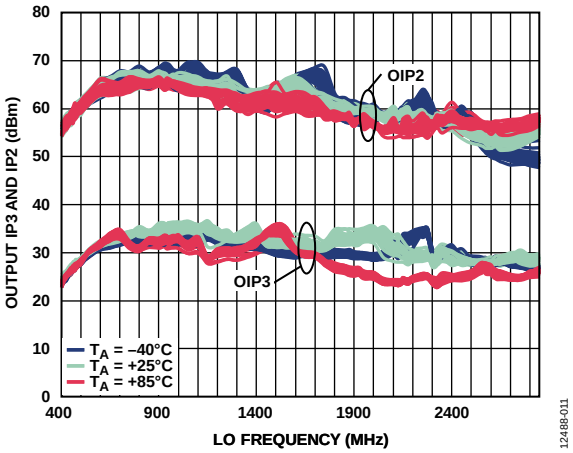


Figure 11. OIP3 and OIP2 vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ –5 dBm per Tone); Multiple Devices Shown

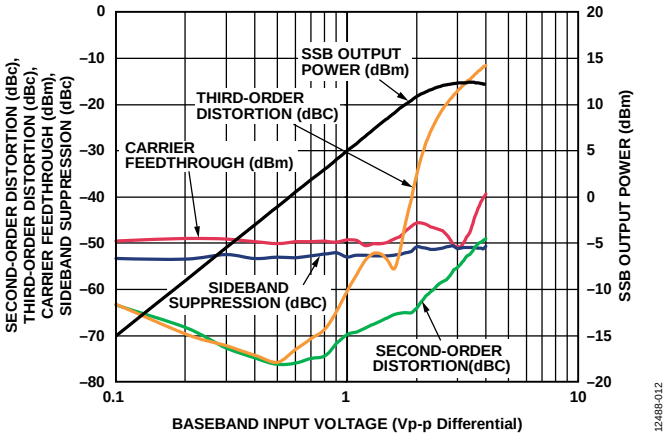


Figure 12. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 940 MHz)

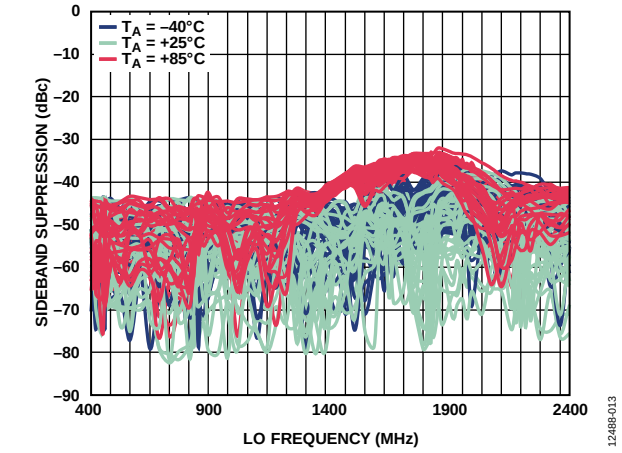


Figure 13. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature After Nulling Using I_LO and Q_LO at 25°C; Multiple Devices Shown

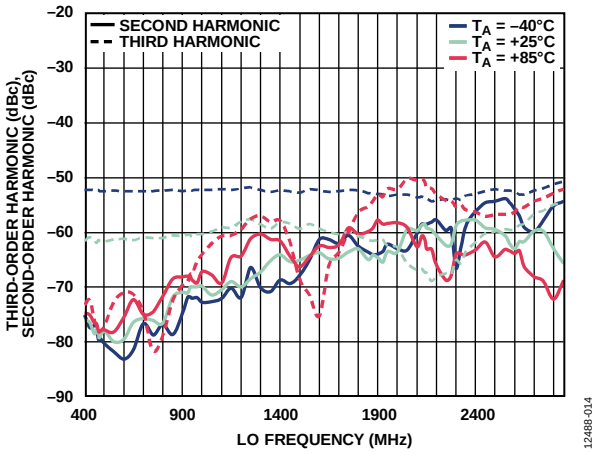


Figure 14. Second- and Third-Order Harmonics vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ 5 dBm)

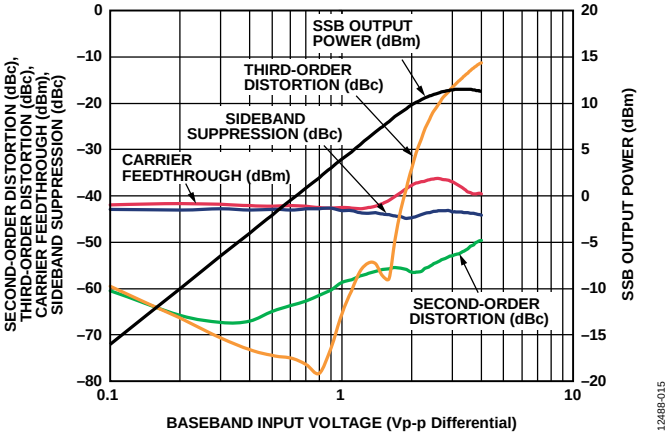


Figure 15. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2140 MHz)

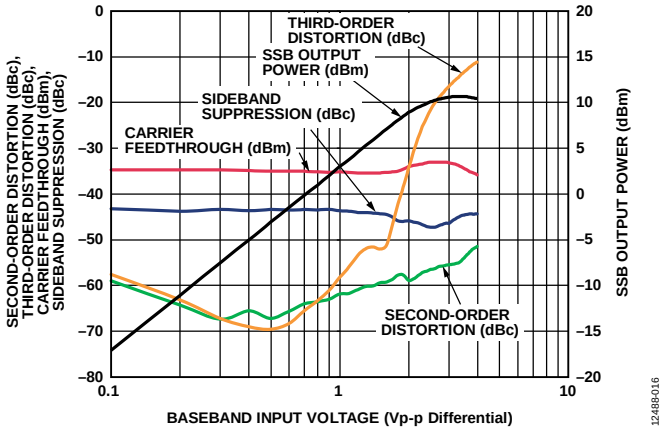


Figure 16. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2600 MHz)

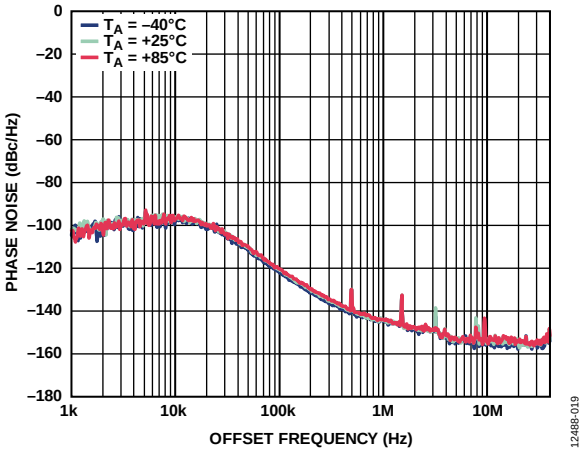


Figure 19. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 940 MHz; 20 kHz Loop Filter

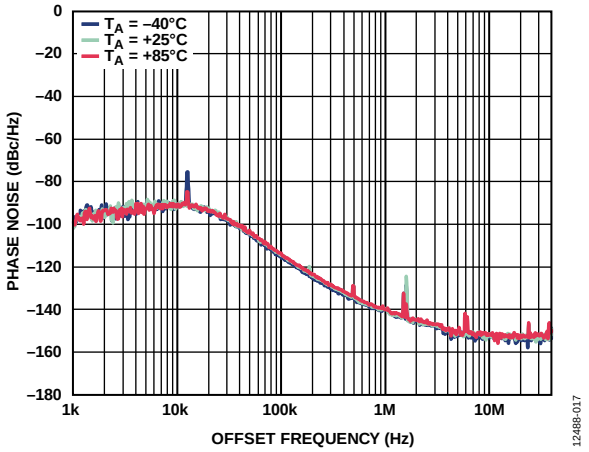


Figure 17. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 1900 MHz; 20 kHz Loop Filter

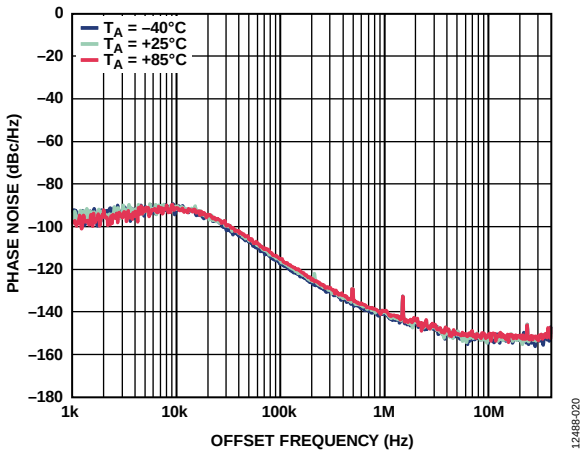


Figure 20. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2140 MHz; 20 kHz Loop Filter

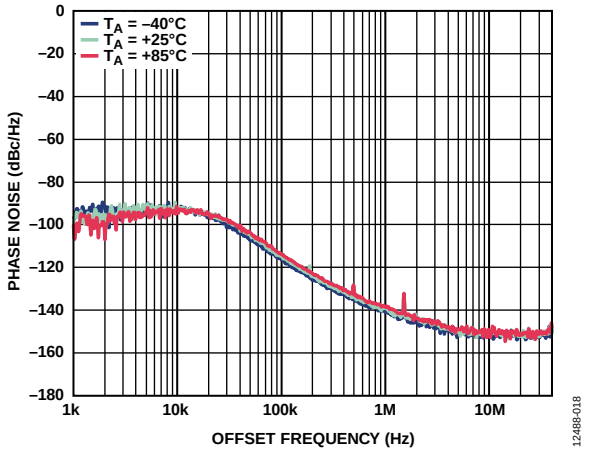


Figure 18. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2300 MHz; 20 kHz Loop Filter

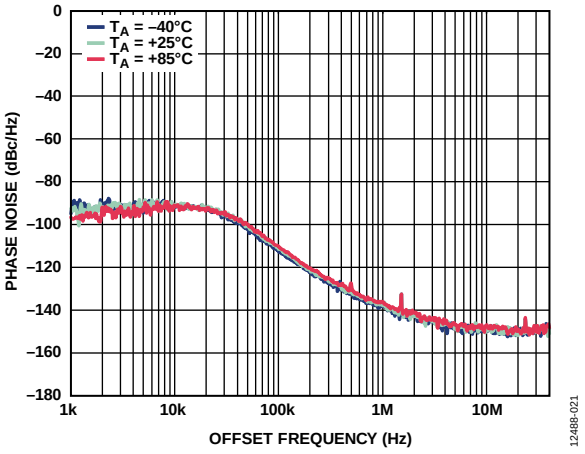


Figure 21. Closed-Loop Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2600 MHz; 20 kHz Loop Filter

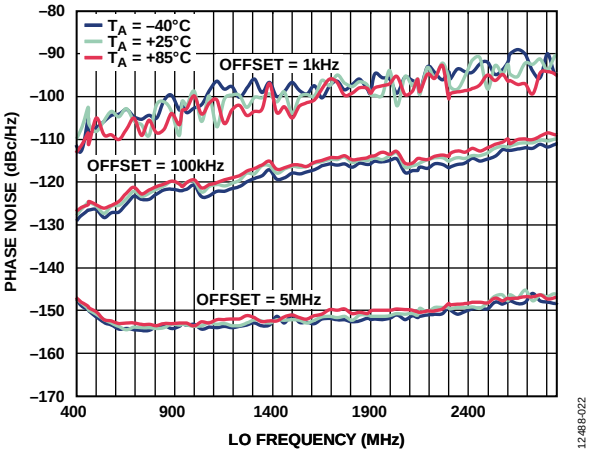


Figure 22. Closed-Loop Phase Noise vs. LO Frequency at 1 kHz, 100 kHz, and 5 MHz Offsets

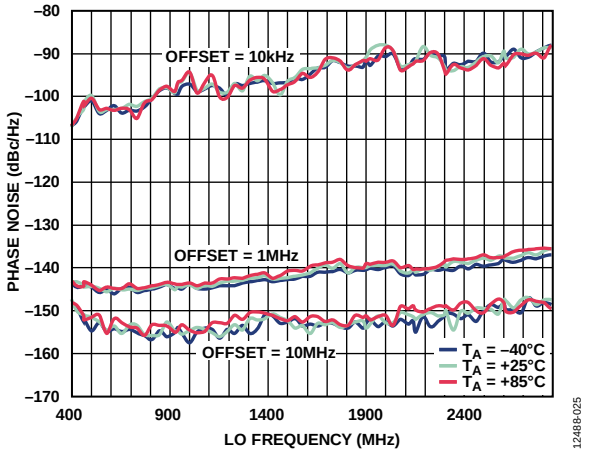


Figure 25. Closed-Loop Phase Noise vs. LO Frequency at 10 kHz, 1 MHz, and 10 MHz Offsets

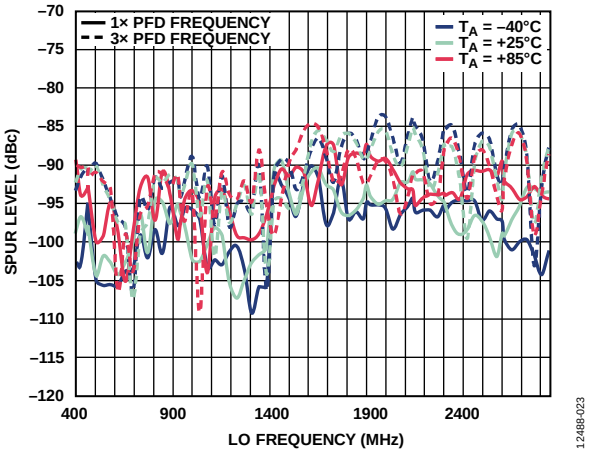


Figure 23. PLL Reference Spurs vs. LO Frequency (1 × PFD and 3 × PFD) at Modulator Output

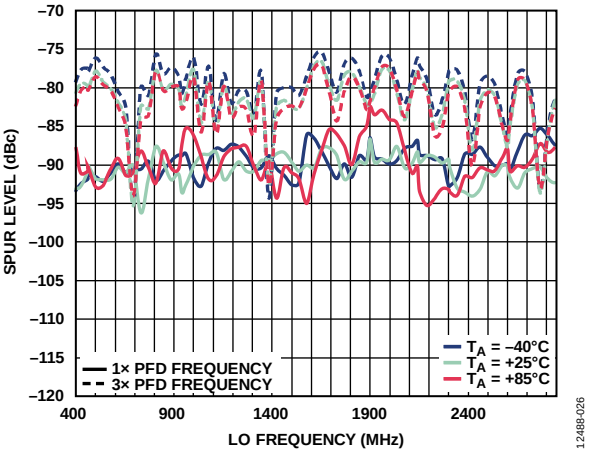


Figure 26. PLL Reference Spurs vs. LO Frequency (1 × PFD and 3 × PFD) at LO Output

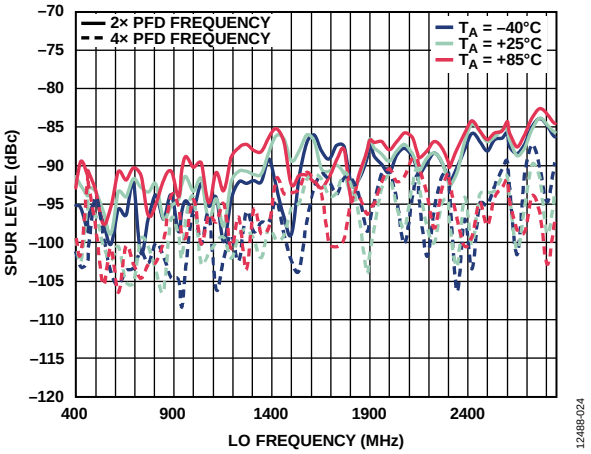


Figure 24. PLL Reference Spurs vs. LO Frequency (2 × PFD and 4 × PFD) at Modulator Output

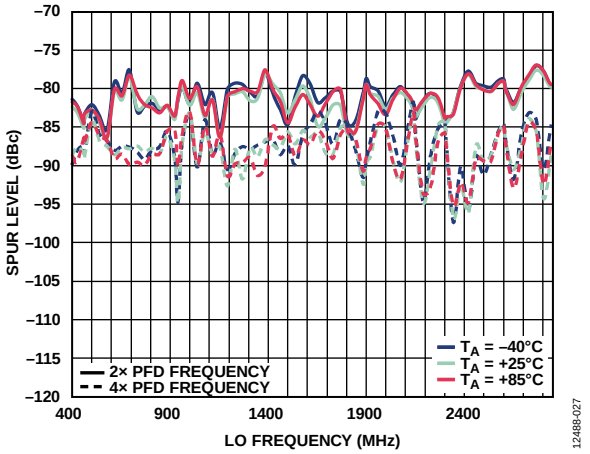


Figure 27. PLL Reference Spurs vs. LO Frequency (2 × PFD and 4 × PFD) at LO Output

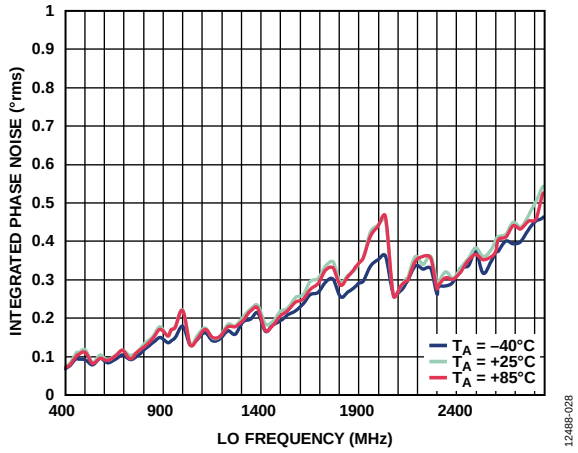


Figure 28. Integrated Phase Noise with Spurs vs. LO Frequency and Temperature

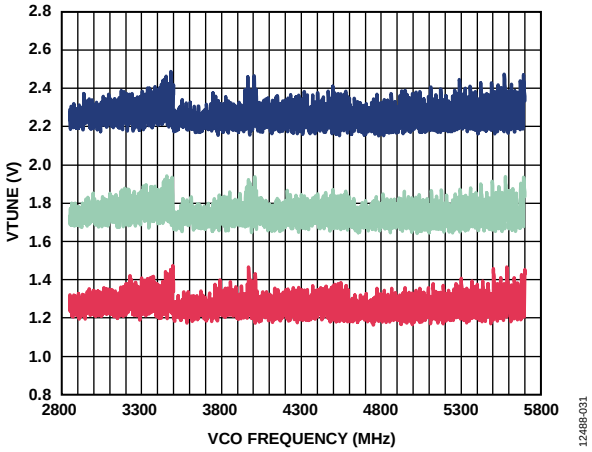


Figure 31. VTUNE vs. VCO Frequency and Temperature

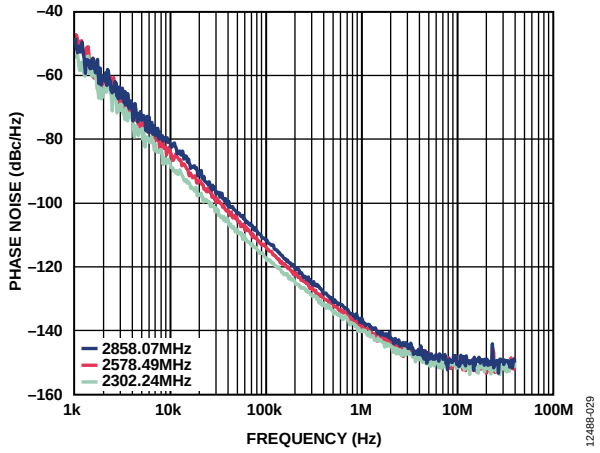


Figure 29. Open-Loop VCO Phase Noise for VCO 0 Measured at 2302.24 MHz, 2578.49 MHz, and 2858.07 MHz (VCO ÷ 2)

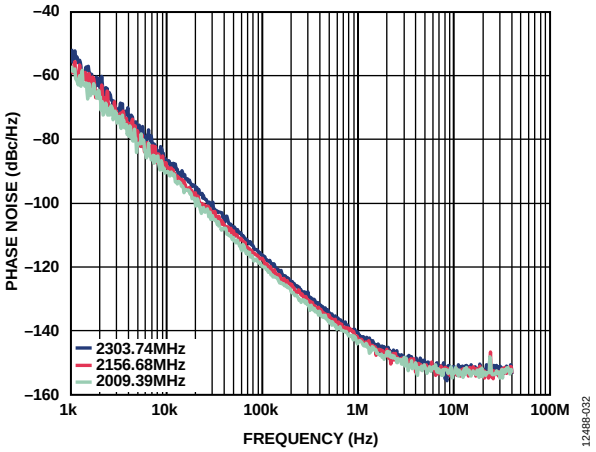


Figure 32. Open-Loop VCO Phase Noise for VCO 1 Measured at 2009.39 MHz, 2156.68 MHz, and 2303.74 MHz (VCO ÷ 2)

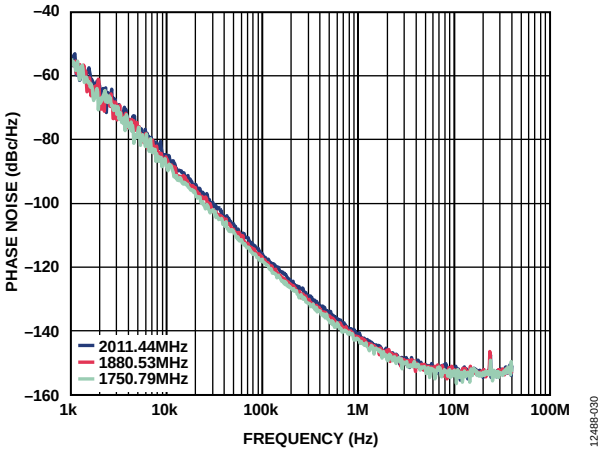


Figure 30. Open-Loop VCO Phase Noise for VCO 2 Measured at 1750.79 MHz, 1880.53 MHz, and 2011.44 MHz (VCO ÷ 2)

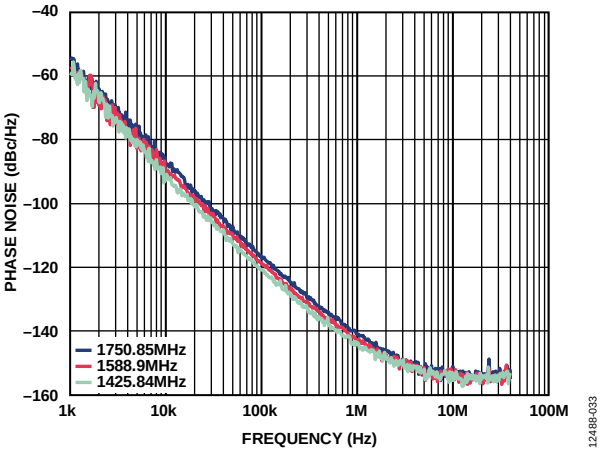


Figure 33. Open-Loop VCO Phase Noise for VCO 3 Measured at 1425.84 MHz, 1588.9 MHz, and 1750.85 MHz (VCO ÷ 2)

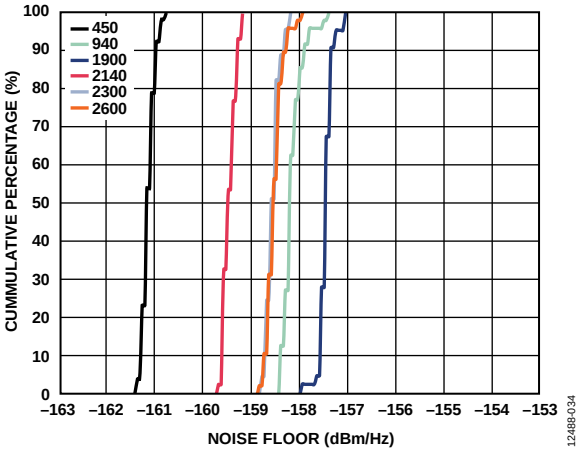


Figure 34. Noise Floor Cumulative Distribution at Various LO Frequencies Using Internal LO; I/Q Input with 2.68 V DC Bias and No RF Output

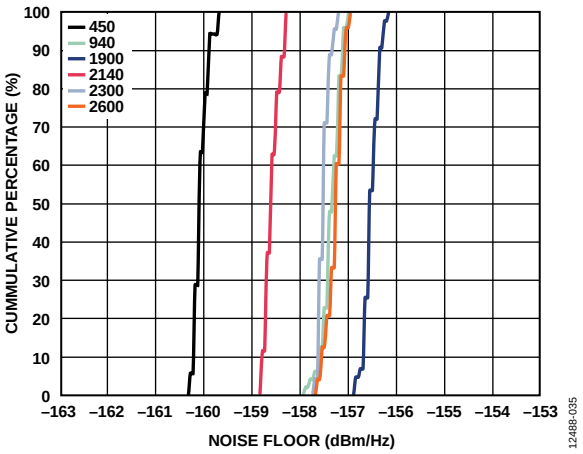


Figure 35. Noise Floor Cumulative Distribution at Various LO Frequencies Using Internal LO; I/Q Input with 2.68 V DC Bias and RF Output = −10 dBm

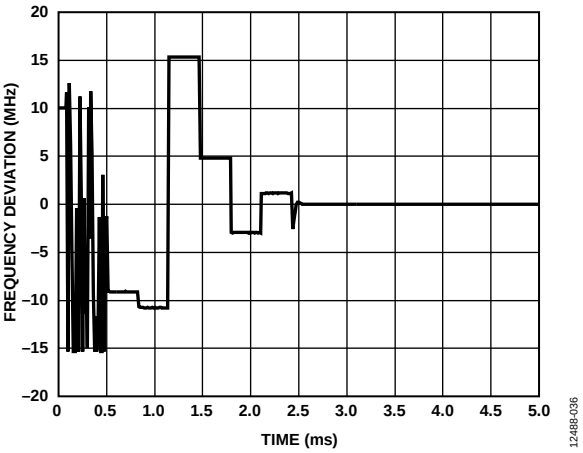


Figure 36. Frequency Deviation from LO Frequency at LO = 1.91 GHz to 1.9 GHz vs. Lock Time

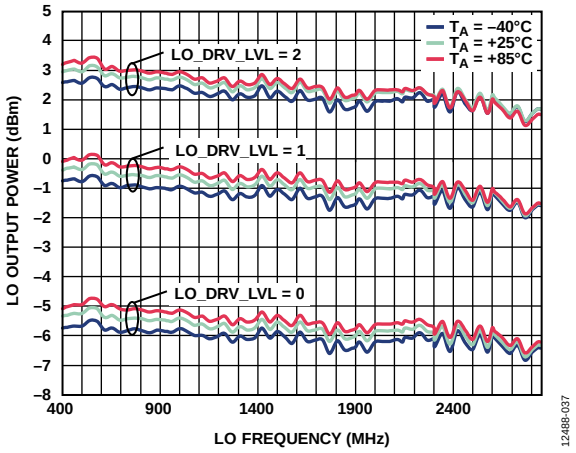


Figure 37. LO Output Power vs. LO Frequency at Various LO_DRV_LVL Settings

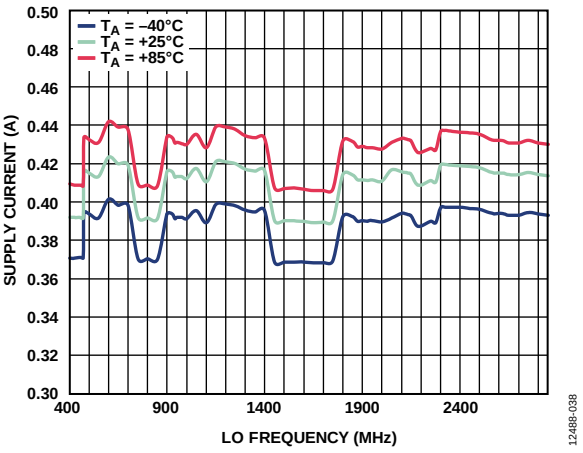


Figure 38. Supply Current vs. LO Frequency and Temperature (PLL and I/Q Modulator Enabled, LO Buffer Disabled)

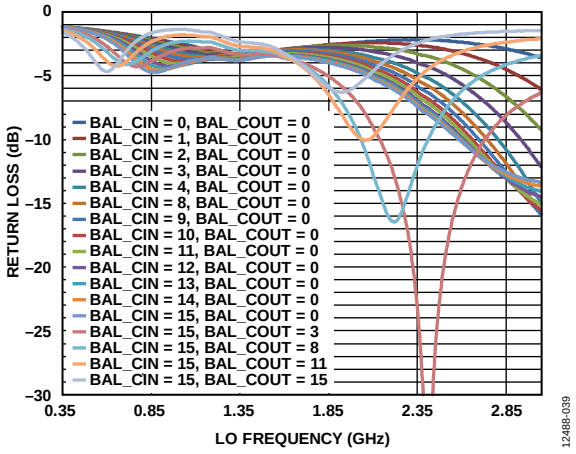


Figure 39. RF Output Return Loss vs. LO Frequency (f_{LO}) for Multiple BAL_CIN and BAL_COUT Combinations

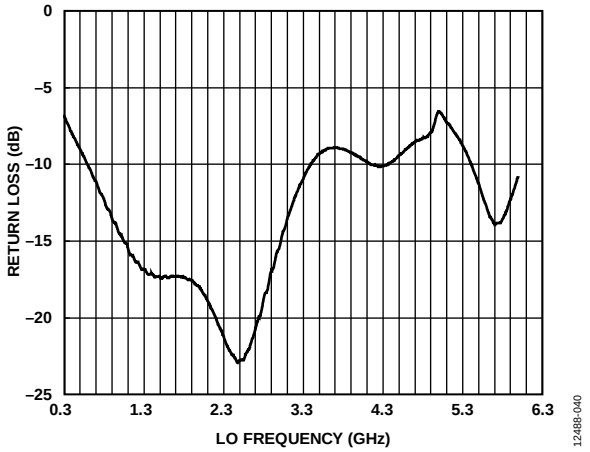


Figure 40. LO Input Return Loss vs. LO Frequency (f_{LO})

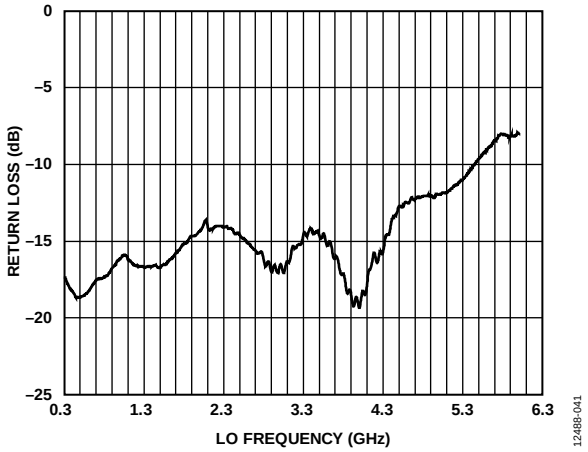


Figure 41. LO Output Return Loss vs. LO Frequency (f_{LO})

THEORY OF OPERATION

The ADRF6720-27 integrates a high performance broadband I/Q modulator with a fractional-N PLL and low noise multicore VCOs. The baseband inputs mix with the LO generated internally or provided externally, and convert it to a single-ended RF using an integrated RF balun. A block diagram of the device is shown in Figure 1. The ADRF6720-27 is programmed via an SPI.

LO GENERATION BLOCK

The ADRF6720-27 supports the use of both internal and external LO signals for the mixers. The internal LO is generated by an on-chip VCO, which is tunable over an octave frequency range of 2850 MHz to 5710 MHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce in-phase and quadrature phase LO signals over the 356.25 MHz to 2855 MHz frequency range to drive the mixers, steer the VCO outputs through a combination of frequency dividers, as shown in Figure 42.

Alternatively, an external signal can be used with the dividers or a polyphase phase splitter to generate the LO signals in quadrature to the mixers. In demanding applications that require the lowest possible phase noise performance, it may be necessary to source the LO signal externally. The different methods of quadrature LO generation and the control register programming needed are listed in Table 6.

Internal LO Mode

For internal LO mode, the ADRF6720-27 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 42, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and divides it down by a factor of 2, 4, or 8, or multiplies it by a factor of 1 or 2, and then passes it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends either an up or down signal to the charge pump if the VCO signal is either slow or fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (V_{TUNE}).

The ADRF6720-27 integrates four VCO cores, covering an octave range of 2850 MHz to 5710 MHz.

Table 6 lists the frequency range covered by each VCO. The desired VCO can be selected by addressing the VCO_SEL bits at Register 0x22[2:0].

The LO source and quadrature generation path can be selected by setting the QUAD_DIV_EN bit (Register 0x01[9]) and the LO_1XVCO_EN bit (Register 0x01[11]).

The mode of the VCO signal through a polyphase filter is intended to extend the operating frequency with an internal VCO and is only useful for baseband input frequencies high enough to prevent the RF output from pulling the VCO.

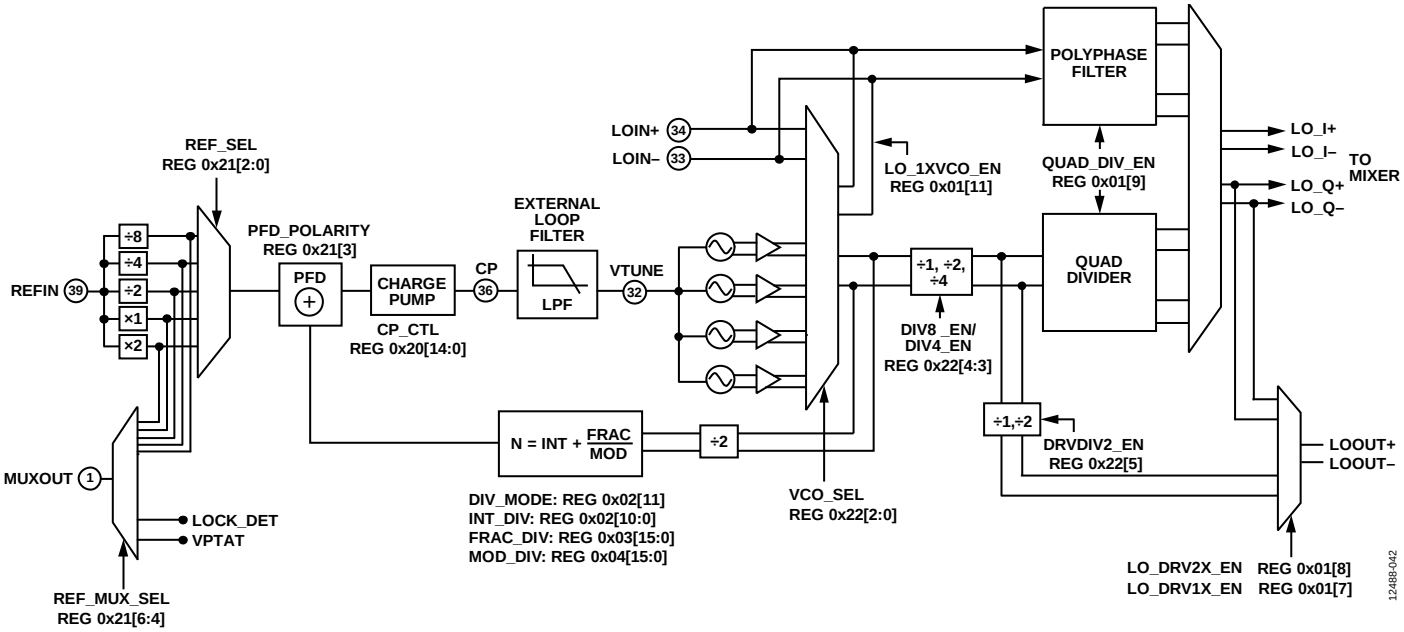


Figure 42. LO Block Diagram

Table 6. LO Mode Selection

LO Selection	f_{VCO} or f_{EXT} (MHz)	Quadrature Generation	QUAD_DIV_EN (Register 0x01[9])	LO_1XVCO_EN (Register 0x1[11])	Enables (Register 0x01[6:0])	VCO_SEL (Register 0x22[2:0])
Internal (VCO)	2850 to 3500	Divide by 2	1	0	111 111X[1]	011
	3500 to 4020	Divide by 2	1	0	111 111X[1]	010
	4020 to 4600	Divide by 2	1	0	111 111X[1]	001
	4600 to 5710	Divide by 2	1	0	111 111X[1]	000
	2855 to 3000	Polyphase	0	1	111 111X[1]	011
External	700 to 6000	Divide by 2	1	0	101 000X[1]	1XX[1]
	700 to 3000	Polyphase	0	0	000 000X[1]	XXX[1]

[1] X = don't care.

LO Frequency and Dividers

The signal coming from the VCO or the external LO inputs goes through a series of dividers before it is buffered to drive the active mixers. Two programmable divide by 2 stages divide the frequency of the incoming signal by 1, 2, or 4 before reaching the quadrature divider that further divides the signal frequency by 2 to generate the in-phase and quadrature phase LO signals for the mixers. The control bits (Register 0x22[4:3]) needed to select the different LO frequency ranges are listed in Table 7.

Table 7. LO Frequency and Dividers

LO Frequency Range (MHz)	f_{VCO}/f_{LO} or $f_{EXT\,LO}/f_{LO}$	DIV8_EN (Register 0x22[4])	DIV4_EN (Register 0x22[3])
1425 to 2855	2	0	0
712.5 to 1425	4	0	1
356.25 to 712.5	8	1	1

PLL Frequency Programming

The N divider with divide by 2 divides down the VCO signal to the PFD frequency. The N divider can be configured for fractional or integer mode by addressing the DIV_MODE bit (Register 0x02[11]). The default configuration is set for fractional mode. Use the following equations to determine the N value and PLL frequency:

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{fvco}{LO_DIVIDER} = \frac{f_{PFD} \times 2 \times N}{LO_DIVIDER}$$

where:
f_{PFD} is the phase frequency detector frequency.
f_{VCO} is the VCO frequency.
N is the fractional divide ratio ($INT + FRAC/MOD$).
INT is the integer divide ratio programmed in Register 0x02.
$FRAC$ is the fractional divider programmed in Register 0x03.
MOD is the modulus divide ratio programmed in Register 0x04.
f_{LO} is the LO frequency going to the mixer core when the loop is locked.

LO_DIVIDER is the final frequency divider ratio that divides the frequency of the VCO or the external LO signal down by 2, 4, or 8 before it reaches the mixer, as shown in Table 7.

Loop Filter

The loop filter is connected between the CP and VTUNE pins. The recommended components for 20 kHz filter designs are shown in Table 8 and referenced in Figure 44.

The ADRF6720-27 closed-loop phase noise is characterized using a 20 kHz loop filter. Operation with an external VCO is possible. In this case, the output of the loop filter is connected to the tuning pin of the external VCO. The output of the VCO is brought back into the device on the LOIN+ and LOIN− pins. For assistance in designing loop filters with other characteristics, download the most recent revision of ADIsimPLL™ from www.analog.com/adisimpll.

Table 8. Recommended Loop Filter Components

Component	20 kHz Loop Filter
C57	2700 pF
R12	300 Ω
C58	100 nF
R23	5.6 Ω
C59	2700 pF
R26	820 Ω
C60	1500 pF

PLL Lock Time

It takes time to lock the PLL after the last register is written. VCO band calibration time and loop settling time are used to determine the PLL lock time.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration takes approximately 94,208 PFD cycles. For a 40 MHz f_{PFD}, this corresponds to 2.36 ms. After a band calibration completes, the feedback action of the PLL results in the VCO locking to the correct frequency. The speed to be locked depends on the nonlinear cycle slipping behavior, as well as the small signal settling of the loop. For an accurate estimation of the lock time, download the ADIsimPLL tool to capture these effects correctly. In general, higher bandwidth loops tend to lock more quickly than lower bandwidth loops.

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with a logic high signifying that the loop is locked. The control bits for the MUXOUT pin are the REF_MUX_SEL bits (Register 0x21[6:4]), and the default configuration is for PLL lock detect.

Required PLL/VCO Settings and Register Write Sequence

In addition to writing to the necessary registers to configure the PLL and VCO for the desired LO frequency and phase noise performance, the registers listed in Table 9 are the required registers to write.

To ensure that the PLL locks to the desired frequency, follow the proper write sequence of the PLL registers. Configure the PLL registers accordingly to achieve the desired frequency, and the last writes must be to Register 0x02 (INT_DIV), Register 0x03 (FRAC_DIV), or Register 0x04 (MOD_DIV). When Register 0x02, Register 0x03, and Register 0x04 are programmed, an internal VCO calibration initiates, which is the last step to locking the PLL.

Table 9. Required PLL/VCO Register Writes

Address	Bit Name	Setting	Description
0x21[3]	PFD_POLARITY	0x01	Negative polarity
0x49[13:0]	SET_1[13:9], SET_0[8:0]	0x14B4	Internal settings

External LO Mode

Use the VCO_SEL bits (Register 0x22[2:0]) to select external or internal LO mode. To configure for external LO mode, set Register 0x22[2:0] to 4 decimal and apply the differential LO signals to Pin 33 (LOIN−) and Pin 34 (LOIN+). The external LO frequency range is 700 MHz to 3 GHz. When the polyphase phase splitter is selected, a 1 × LO signal is required for the active mixer, or a 2 × LO can be used with the internal quadrature divider, as shown in Table 6.

There is also the option of using an external VCO with the internal PLL. In this case, the PLL is enabled, but the VCO blocks are turned off.

The LOIN+ and LOIN− input pins must be ac-coupled. When not in use, leave the LOIN+ and LOIN− pins unconnected.

LO Polarity

The ADRF6720-27 offers the flexibility of specifying the quadrature polarity on LO to the I channel or Q channel mixers. This specification determines whether the LO is injected above or below the RF frequency. RF frequency can place either above or below the LO depending on the Register 0x32[11:8] setting as well as the phase relationship between the baseband I and Q. For normal operation and characterization, the Register 0x32 settings are 2 decimal for POL_I (Register 0x32[9:8]) and 1 decimal for POL_Q (Register 0x32, Bits[11:10]). Setting Register 0x32 as such places the RF frequency below the LO ($f_{RF} < f_{LO}$) when Q leads I and places the RF frequency above the LO ($f_{RF} > f_{LO}$) when I leads Q.

Table 10. LO Polarity Setting

Address	Bit Name	Settings	Description
0x32[11:10]	POL_Q		Quadrature polarity switch, Q channel
		01	Inverted Q channel polarity
		10	Normal polarity
0x32[9:8]	POL_I		Quadrature polarity switch, I channel.
		01	Normal polarity
		10	Inverted I channel polarity

LO Outputs

The ADRF6720-27 can provide either a differential 1 × or 2 × LO output signal at the LOOUT+ and LOOUT− pins (Pin 18 and Pin 19, respectively). The availability of the LO signal makes it possible to daisy-chain many devices. One ADRF6720-27 device can serve as the master where the LO signal is sourced, and the subsequent slave devices can share the same LO output signal from the master.

When the quadrature LO signals are generated using the quadrature divider, the output signal is available at either 2× or 1× the frequency of the LO signal at the mixer by setting LO_DRV2X_EN bit (Register 0x1[8]) and DRVDIV2_EN bit (Register 0x22[5]). However, 1× the frequency of the LO signal in this case has a phase ambiguity of 180° relative to the LO signal that drives the mixer core. Because of this phase ambiguity, the utility of this 1 × LO output signal as a system daisy-chained LO signal is compromised. To avoid this ambiguity, a second 1× the frequency of the LO signal output is made available after the quadrature divider. This second 1 × LO output path is enabled by setting the LO_DRV1X_EN bit (Register 0x01[7]) high.

When the quadrature LO signals are generated using the polyphase phase splitter, the output signal is also available at 1× the frequency of the LO signal by setting LO_DRV1X_EN bit (Register 0x10[7]) high.

Set the output to different drive levels by accessing the LO_DRV_LVL bits (Register 0x22[7:6]), as shown in Table 11.

Table 11. LO Output Level at 2140 MHz

LO_DRV_LVL (Register 0x22[7:6])	Amplitude (dBm)
00	−5.8
01	−1.0
10	2.2

BASEBAND

The baseband inputs are designed to work with a 2.68 V common-mode voltage. To match the 100 Ω impedance of the DAC, place a shunt 100 Ω external resistor across the I and Q inputs.

The voltages applied to the differential baseband inputs (I+, I–, Q+, and Q–) drive the V-to-I stage that converts baseband voltages into currents. The converted modulated signal current feeds the modulator mixer core.

A programmable dc current can be added to both the I and Q channels to null any carrier feedthrough at the RF output. Refer to the Carrier Feedthrough Nulling section for more information

The linearity can be optimized by adding the amplitude and phase correction signals to the current output via the MOD_RSEL (Register 0x31[12:6]) and MOD_CSEL (Register 0x31[5:0]) adjustment. Refer to the Linearity section for more information.

ACTIVE MIXERS

The ADRF6720-27 has two double balanced mixers: one for the in-phase channel (I channel) and the other for the quadrature channel (Q channel). They upconvert the modulated baseband signal currents by the LO signals to the RF.

Tunable RF_{OUT} Balun

The ADRF6720-27 integrates a programmable balun operating over a frequency range from 700 MHz to 3000 MHz. It offers single-ended-to-differential conversion and provides additional common-mode noise rejection.

The capacitors at the input and output of the balun in parallel with the inductive windings of the balun change the resonant frequency of the inductor capacitor (LC) tank. Therefore, selecting the proper combination of BAL_CIN (Register 0x30[3:0]) and BAL_COUT (Register 0x30[7:4]) sets the desired frequency and optimizes gain. Under most circumstances, it is suggested to set BAL_CIN and BAL_COUT over the frequency profile given in Table 12. However, for matching reasons, it is advantageous to tune the registers independently.

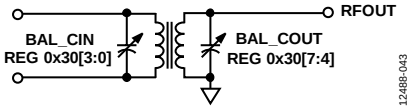


Figure 43. Integrated Tunable Balun

Table 12. Optimum Balun Setting For Desired Frequency Range

BAL_CIN	BAL_COUT	Frequency Range (MHz)
0	0	f_{RF} > 1730
1	0	1550 < f_{RF} < 1730
2	0	1380 < f_{RF} < 1550
3	0	1250 < f_{RF} < 1380
4	0	1170 < f_{RF} < 1250
8	0	1100 < f_{RF} < 1170
9	0	1020 < f_{RF} < 1100
10	0	970 < f_{RF} < 1020
11	0	930 < f_{RF} < 970
12	0	890 < f_{RF} < 930
13	0	840 < f_{RF} < 890
14	0	820 < f_{RF} < 840
15	0	780 < f_{RF} < 820
15	3	730 < f_{RF} < 780
15	8	680 < f_{RF} < 730
15	11	630 < f_{RF} < 680
15	15	f_{RF} < 630

ENBL

The ENBL pin quickly enables/disables the RF output. The circuit blocks that are enabled/disabled with the ENBL pin can be programmed by setting the appropriate bits in the enables register (Register 0x01) and the ENBL_MASK register (Register 0x10). When the bits in the enables and the ENBL_MASK register are 1, pulling the ENBL pin low disables and pulling high enables the internal blocks more quickly than possible with an SPI write operation.

Table 13. Enable/Disable Settings

Register 0x01 Enables Bit[1]	Register 0x10 ENBL_MASK Bit[1]	ENBL Pin Voltage	State
0	X[2]	X[2]	Block controlled by Register 0x01 enables bit [A] disabled. No effect by ENBL.
1	0	X[2]	Block controlled by Register 0x01 enables bit [A] enabled. No effect by ENBL.
1	1	>1.8 V	Block controlled by Register 0x01 enables bit [A] enabled.
1	1	<0.5 V	Block controlled by Register 0x01 enables bit [A] disabled

[1] This bit refers to any of the 11 bits in the register.
[2] X = don't care.

SERIAL PORT INTERFACE

The SPI of the ADRF6720-27 allows the user to configure the device for specific functions or operations via a 3-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of three control lines: SCLK, SDIO, and $\overline{CS}$. The timing requirements for the SPI port are shown in Table 2.

The ADRF6720-27 protocol consists of seven register address bits, followed by a read/write and 16 data bits. Both the address and data fields are organized with the most significant bit (MSB) first, and end with the least significant bit (LSB).

On a write cycle, up to 16 bits of serial write data are shifted in, MSB to LSB. If the rising edge of $\overline{CS}$ occurs before the LSB of the serial data is latched, only the bits that were latched are written to the device. If more than 16 data bits are shifted in, the 16 most recent bits are written to the device. The ADRF6720-27 input logic level for the write cycle supports an interface as low as 1.4 V.

On a read cycle, up to 16 bits of serial read data are shifted out, MSB first. Data shifted out beyond 16 bits is undefined. Readback content at a given register address does not necessarily correspond with the write data of the same address. The output logic level for a read cycle is 2.3 V.

BASIC CONNECTIONS FOR OPERATION

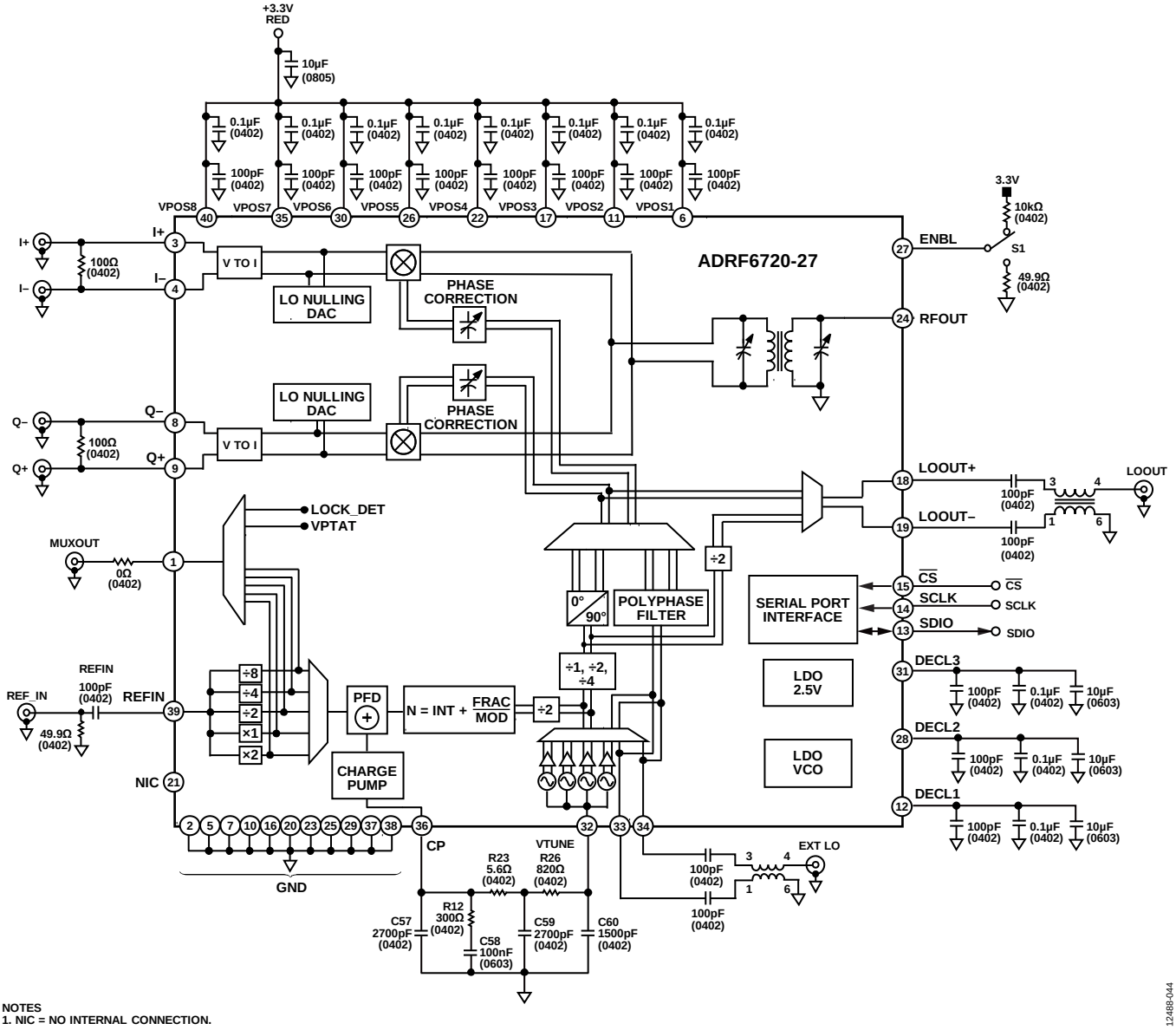


Figure 44. Basic Connections for Operation (Loop Filter Set to 20 kHz)

Figure 44 shows the basic connections for operating the ADRF6720-27 as they are implemented on the evaluation board of the device.

POWER SUPPLY AND GROUNDING

Connect the power supply pins to a 3.3 V source; the pins can range between 3.15 V and 3.45 V. Individually decouple the pins using 100 pF and 0.1 µF capacitors located as close as possible to the pins. Individually decouple the three internal decoupling nodes (labeled DECL3, DECL2, and DECL1) with capacitors as shown in Figure 44.

Tie the 11 GND pins to the same ground plane through low impedance paths.

Solder the exposed pad on the underside of the package to a ground plane with low thermal and electrical impedance. If the ground plane spans multiple layers on the circuit board, stitch them together under the exposed pad. The AN-772 Application Note discusses the thermal and electrical grounding of the LFCSP package in detail.

BASEBAND INPUTS

Drive the four I and Q inputs with an external bias level of 2.68 V. These inputs are generally dc-coupled to the outputs of a dual DAC. The nominal drive level used in the characterization of the ADRF6720-27 is 1 V p-p differential (or 500 mV p-p on each pin).

LO INPUT

The external LO input is designed to be driven differentially. AC couple both sides of the differential LO source through a pair of series capacitors to the LOIN+ and LOIN− pins.

The typical LO drive level, used for the characterization of the ADRF6720-27, is 0 dBm.

Apply the reference frequency for the PLL (between 5.7 MHz and 320 MHz) to the REFIN pin, which is ac-coupled. If the REFIN pin is being driven from a 50 Ω source, terminate the pin with 50 Ω as shown in Figure 44. Apply a drive level of about 4 dBm to 14 dBm; 4 dBm is used at characterization.

LOOP FILTER

The loop filter in Figure 44 is connected between the CP and VTUNE pins. The recommended components for 20 kHz filter designs are shown in Table 8.

RF OUTPUT

The RF output is available at the RFOUT pin (Pin 24), which can drive a 50 Ω load.

APPLICATIONS INFORMATION

DAC TO I/Q MODULATOR INTERFACING

The ADRF6720-27 is designed to interface with minimal components to members of the Analog Devices, Inc., family of TxDAC® converters. These dual- or quad-channel differential current sinking DACs provide a current swing from 0 mA to 20 mA. The interface described in this section can be used with any DAC that has a similar output.

An example of interfacing the dual-channel differential current sinking TxDAC is shown in Figure 45. The baseband inputs of the ADRF6720-27 require a dc bias of 2.68 V and the TxDAC outputs interface seamlessly with ADRF6720-27. Place a shunt 100 Ω external resistor across the I and Q inputs to match the 100 Ω impedance of the DAC. With the 50 Ω termination resistors to the power supply in the DAC outputs , the 100 Ω shunt resistors across the I and Q inputs with a 20 mA full-scale current and bleed current , the resulting drive signal from each differential pair is 1 V p-p differential (with the DAC running at 0 dBFS), with a 2.68 V dc bias.

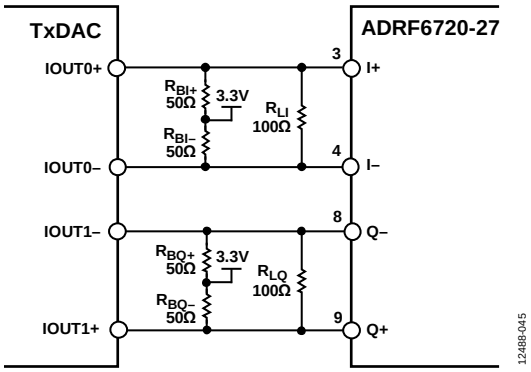


Figure 45. Interface Between the TxDAC and ADRF6720-27 with 50 Ω Resistors to Ground to Establish the 2.68 V DC Bias for the ADRF6720-27 Baseband Inputs

Adjust the voltage swing for a given DAC output current by placing a different resistance value on R_{LI} and R_{LQ} to the interface (see Figure 45). This adjustment has the effect of varying the ac swing without changing the dc bias already established by the 50 Ω resistors. A higher resistance value increases the output power of the ADRF6720-27 and signal-to-noise ratio (SNR) at the cost of higher intermodulation distortion.

Figure 46 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used. The differential peak-to-peak swing at the modulator input is

$$V_{SIGNAL} = I_{FS} \times \frac{\left[2 \times R_B \times R_L\right]}{\left[2 \times R_B + R_L\right]}$$

Figure 47 shows the differential input resistance and capacitance over baseband input frequencies.

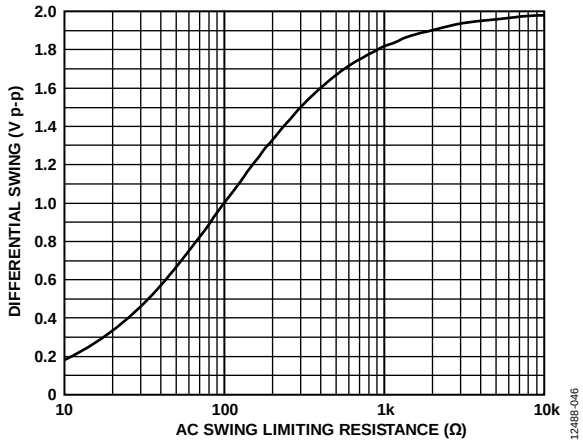


Figure 46. Relationship Between the AC Swing Limiting Resistance and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

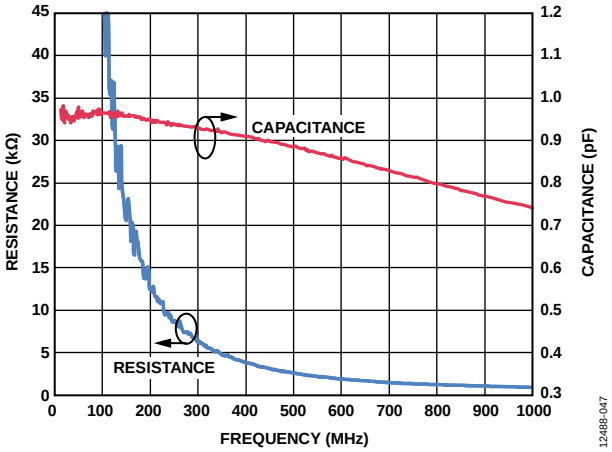


Figure 47. Differential Baseband Input Resistance and Input Capacitance Equivalents (Shunt R, Shunt C)

I/Q Filtering

An antialiasing filter between the DAC and modulator is necessary to filter out Nyquist images, common-mode noise, and broadband DAC noise. The interface for setting up the biasing and ac swing described in the DAC to I/Q Modulator Interfacing section lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing limiting resistor. With this configuration, the dc bias setting resistors set the source impedance, and the ac swing limiting resistor sets the load impedance with a high differential I and Q input impedance in parallel for the filter.

BASEBAND BANDWIDTH

The ADRF6720-27 can be used with a DAC generating a complex IF (CIF), as well as a zero IF signal (ZIF). The 1 dB bandwidth of the ADRF6720-27 is more than 1000 MHz. Figure 48 shows the baseband frequency response of ADRF6720-27, facilitating high CIF and providing sufficient flat bandwidth for digital predistortion (DPD) algorithms. Any flatness variations across frequency at the ADRF6720-27 RF output have been calibrated out of this measurement.

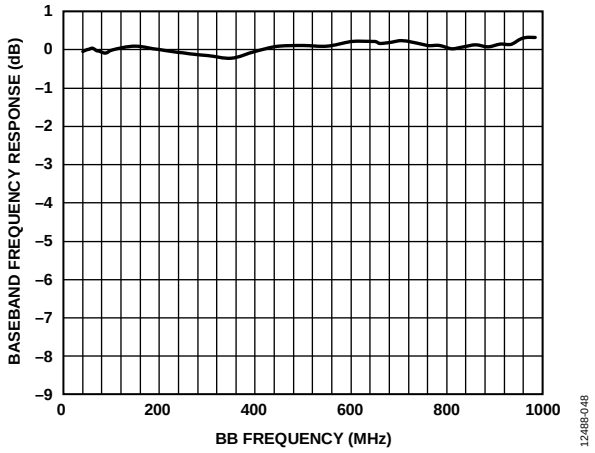


Figure 48. ADRF6720-27 Baseband Frequency Response

CARRIER FEEDTHROUGH NULLING

Carrier feedthrough results from minute dc offsets that occur on the differential baseband inputs. In an I/Q modulator, nonzero differential offsets mix with the LO and result in carrier feedthrough to the RF output. In addition to this effect, some of the signal power at the LO input couples directly to the RF output (this may be as a result of bond wire to bond wire coupling or coupling through the silicon substrate). The net carrier feedthrough at the RF output is the vector combination of the signals that appear at the output as a result of these two effects.

The ADRF6720-27 has a feature to add dc current, positive or negative, to both the I and Q channels for carrier feedthrough nulling. Figure 49 shows carrier feedthrough vs. DCOFF_I (Register 0x33[15:8]) and DCOFF_Q (Register 0x33[7:0]).

The carrier feedthrough nulling can also be accomplished externally by a TxDAC.

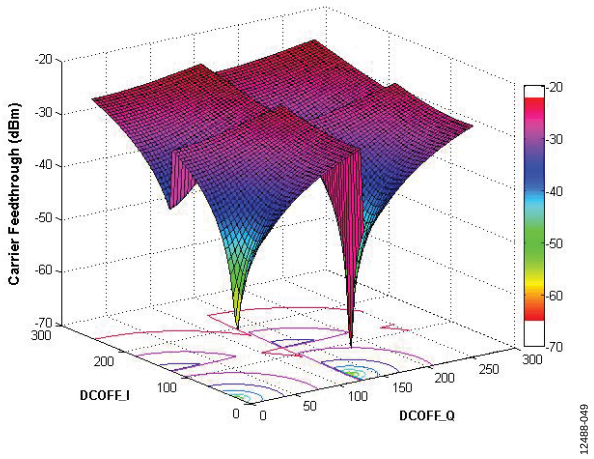


Figure 49. Carrier Feedthrough Optimization Through DCOFF_I and DCOFF_Q Adjustment

SIDEBAND SUPPRESSION OPTIMIZATION

Sideband suppression results from gain and phase imperfection between the I and Q channels. Sideband suppression also results from the quadrature error in generating quadrature LO signals. The net unwanted sideband signal at the RF output is the vector combination of the signals as a result of these effects.

The ADRF6720-27 offers quadrature phase adjustment through the I_LO (Register 0x32[3:0]) and Q_LO (Register 0x32[7:4]) parameters to reject unwanted sideband signal.

Figure 50 shows the level of unwanted sideband signal achievable from the ADRF6720-27 across the I_LO and Q_LO parameters

If further optimization is required, the amplitude and phase adjustments can be made externally by a TxDAC. The result of this type of adjustment is shown in Figure 51.

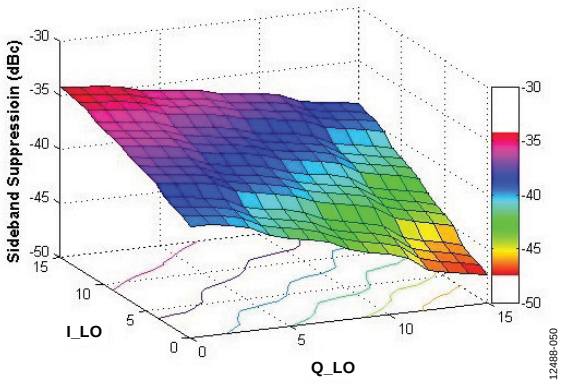


Figure 50. Sideband Suppression Optimization Through I_LO and Q_LO Adjustment; LO = 2140 MHz

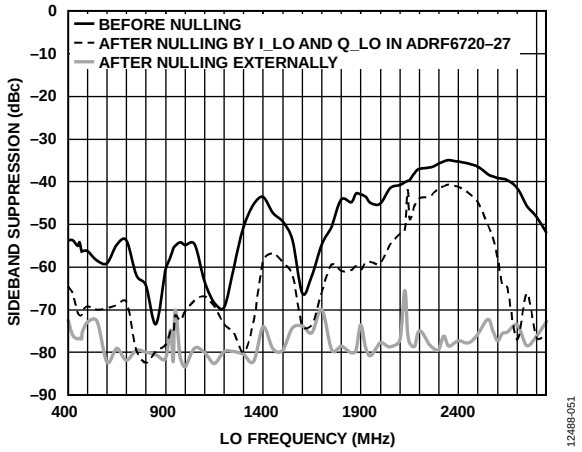


Figure 51. Sideband Suppression Before and After Nulling Using I_LO and Q_LO Through External Adjustment; LO = 2140 MHz

LINEARITY

The linearity in ADRF6720-27 can be optimized through the MOD_RSEL (Register 0x31[12:6]) and MOD_CSEL (Register 0x31[5:0]) settings. The resistance and capacitance curves as a function of the MOD_RSEL and MOD_CSEL settings. These settings control the amount of antiphase distortion to the baseband input stages to correct for distortion.

The top two bits (Register 0x31[12:11]) of MOD_RSEL and the MSB (Register 0x31[5]) of MOD_CSEL are used as a range setting. Figure 52 and Figure 53 show the output IP3 and output IP2 that are achievable across the MOD_RSEL and MOD_CSEL settings.

Figure 52 and Figure 53 show both a surface and a contour plot in one figure. The contour plot is located directly underneath the surface plot. The peaks on the surface plot indicate the maximum output IP3 and maximum output IP2, and the same color pattern on the contour plot determines the optimized MOD_RSEL and MOD_CSEL values. The overall shape of the output IP3 plot varies with the MOD_RSEL setting more than the MOD_CSEL setting.

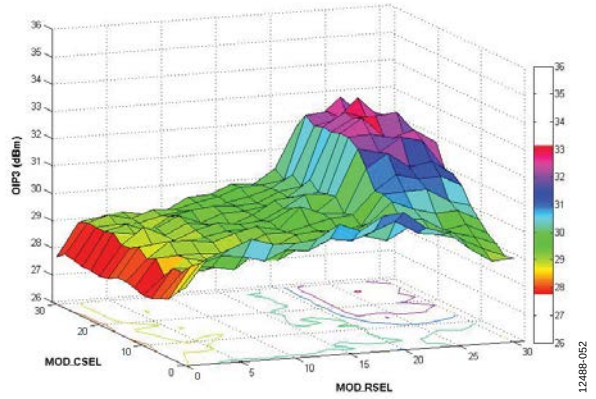


Figure 52. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, I/Q Amplitude Per Tone = 0.3 V p-p Differential

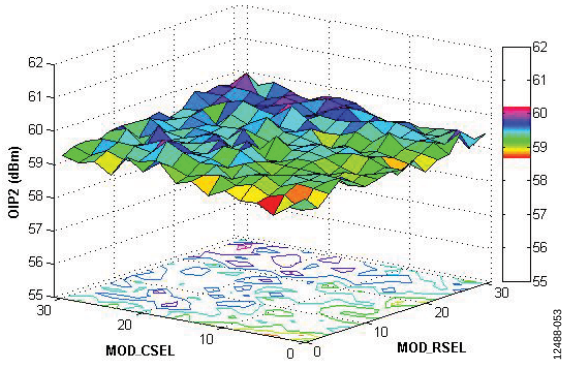


Figure 53. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, I/Q Amplitude per Tone = 0.3 V p-p Differential

LO AMPLITUDE AND COMMON-MODE VOLTAGE

The typical External LO driving level of the ADRF6720-27 is 0 dBm differential. All the baseband inputs must be externally dc biased to 2.68 V. Figure 54 and Figure 55 show the performance variation vs. the external LO amplitude and baseband common-mode voltage, respectively.

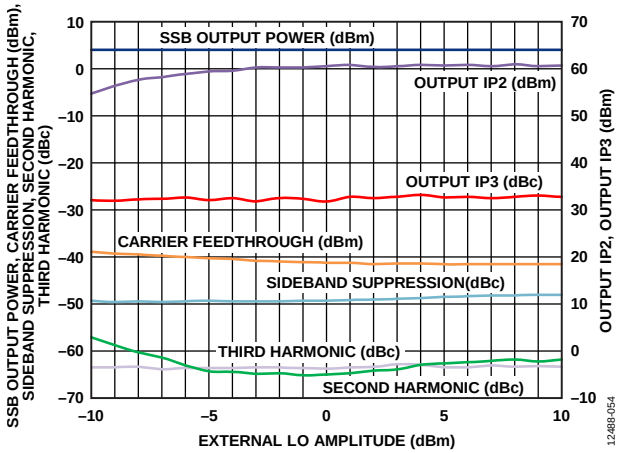


Figure 54. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, Sideband Suppression, OIP2, and OIP3 vs. External LO Amplitude; Baseband I/Q Amplitude = 0.6 V p-p Differential for OIP2, and OIP3, 1 V p-p Differential for P_{OUT}, Sideband Suppression, HD2, HD3, Carrier Feedthrough, f_{OUT} = 2140 MHz, 25°C

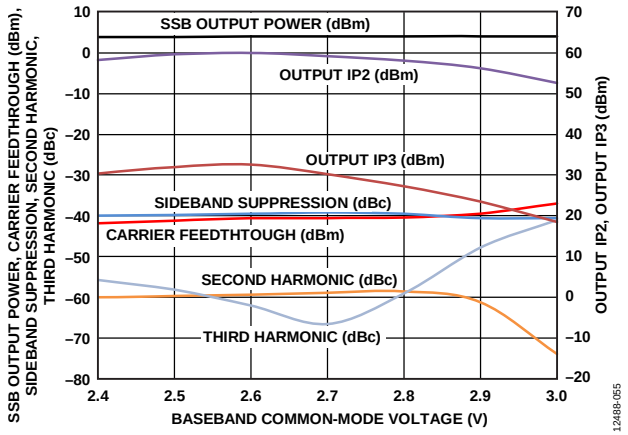


Figure 55. SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, Sideband Suppression, OIP2, and OIP3 vs. Baseband I/Q Amplitude = 0.6 V p-p Differential for OIP2, and OIP3, 1 V p-p Differential for P_{OUT}, Sideband Suppression, HD2, HD3, Carrier Feedthrough, f_{OUT} = 2140 MHz, 25°C

OPERATING OUT OF FREQUENCY RANGE

The operating frequency range of the ADRF6720-27 can be extended above 3000 MHz using the external 1x LO through the polyphase filter. Above the specified RF frequency range of 3000 MHz, loss from internal balun results in output power drop and output IP2 and IP3 degradation, accordingly. See Figure 56 for a plot of typical SSB output power, second- and third-order harmonics, carrier feedthrough, sideband suppression, OIP2, and OIP3 performance from 3000 MHz to 4000 MHz above operating frequency.

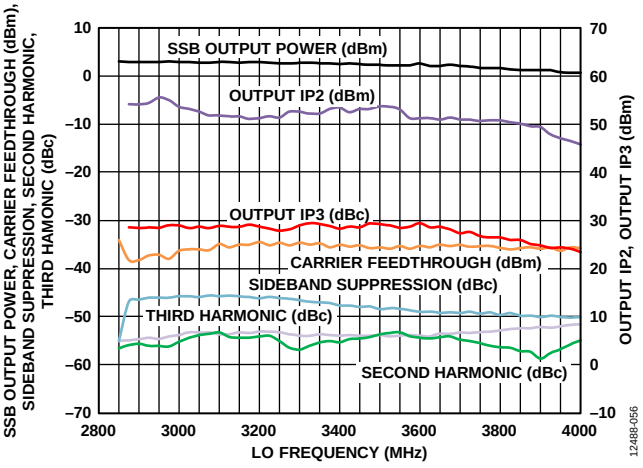


Figure 56. Typical SSB Output Power, Second- and Third-Order Harmonics, Carrier Feedthrough, Sideband Suppression, OIP2, and OIP3 Performance Above Operating Frequency; Baseband I/Q Amplitude = 0.6 V p-p Differential for OIP2, and OIP3, 1 V p-p Differential for P_{OUT}, Sideband Suppression, HD2, HD3, Carrier Feedthrough, 25°C

SPURIOUS PERFORMANCE

Figure 57 to Figure 60 show typical spurious emission of the PFD harmonics at the RF output ($f_{LO} \pm N \times f_{PFD}$). As shown in Figure 57 to Figure 60, the ADRF6720-27 typically achieves better than −90 dBc/Hz PFD harmonic spurious emissions at most offsets. If required, the spurious emission profile shown in Figure 57 to Figure 60 can be tailored to each individual application by selecting a combination of PLL reference frequency, PFD frequency, and LO frequency in order to ensure that the higher spurious emissions fall out of the band of interest. For more information, contact application support.

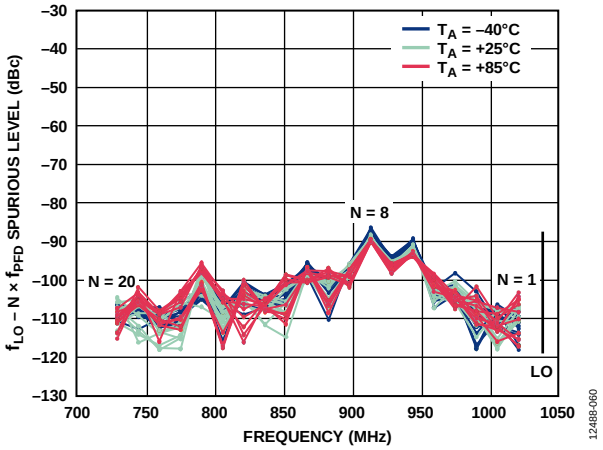


Figure 57. PFD Spurious Emissions on Modulator Output, $f_{LO} - N \times f_{PFD}$; f_{LO} = 1036.8 MHz, $RF_{OUT} \approx$ 4 dBm at 25°C, f_{REF} = 61.44 MHz at 4 dBm, f_{PFD} = 15.36 MHz, Integer PLL Mode

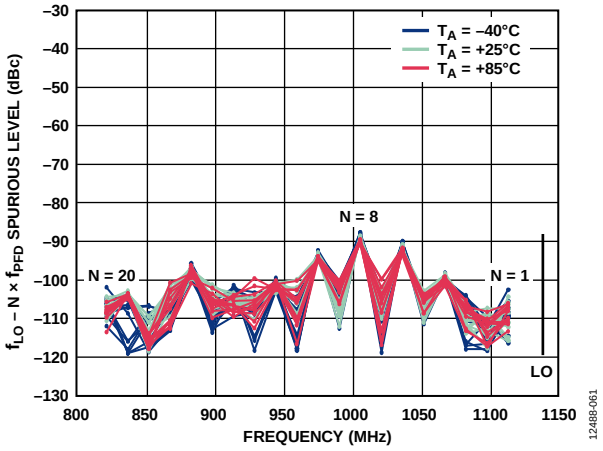


Figure 58. PFD Spurious Emissions on Modulator Output, $f_{LO} - N \times f_{PFD}$; f_{LO} = 1128.96 MHz, $RF_{OUT} \approx$ 4 dBm at 25°C, f_{REF} = 61.44 MHz at 4 dBm, f_{PFD} = 15.36 MHz, Integer PLL Mode

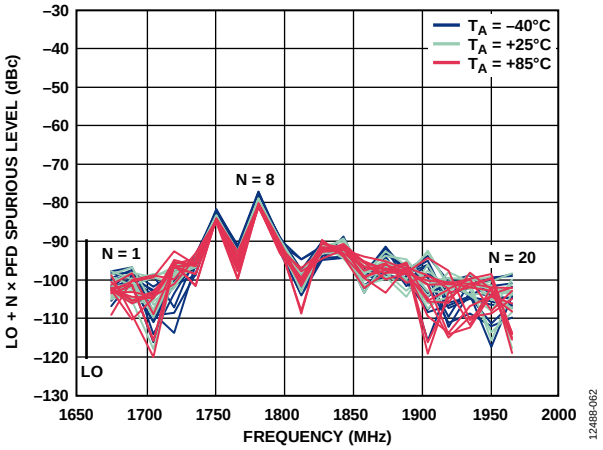


Figure 59. PFD Spurious Emissions on Modulator Output, $f_{LO} + N \times f_{PFD}$; f_{LO} = 1658.88 MHz, $RF_{OUT} \approx$ 4 dBm at 25°C, f_{REF} = 61.44 MHz at 4 dBm, f_{PFD} = 15.36 MHz, Integer PLL Mode

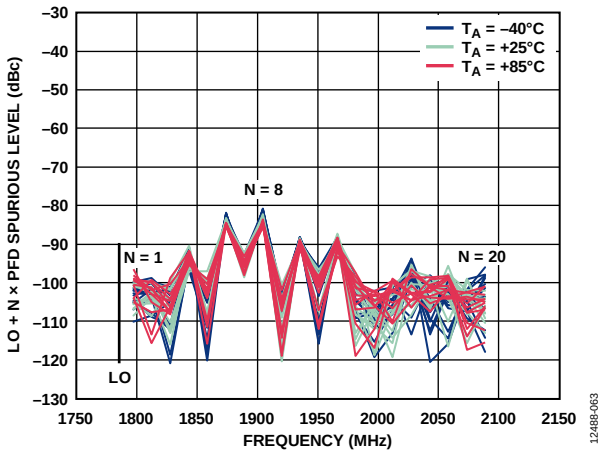


Figure 60. PFD Spurious Emissions on Modulator Output, $f_{LO} + N \times f_{PFD}$; f_{LO} = 1781.76 MHz, $RF_{OUT} \approx$ 4 dBm at 25°C, f_{REF} = 61.44 MHz at 4 dBm, f_{PFD} = 15.36 MHz, Integer PLL Mode

LAYOUT

Solder the exposed pad on the underside of the ADRF6720-27 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Notice the use of 25 via holes on the exposed pad of the ADRF6720-27 evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package.

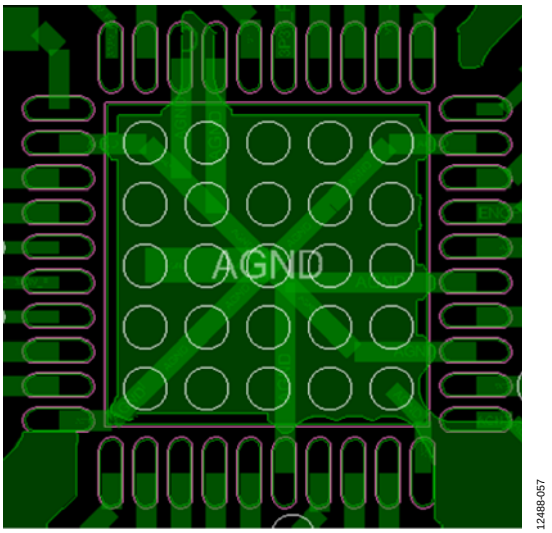


Figure 61. Evaluation Board Layout for the ADRF6720-27 Package

CHARACTERIZATION SETUPS

The primary setup used to characterize the ADRF6720-27 is shown in Figure 62. This setup was used to evaluate the product as a single-sideband modulator. An automated software program (VEE) was used to control equipment over the IEEE bus. The setup was used to measure SSB, OIP2, OIP3, output P1 dB (OP1dB), LO, and sideband suppression null.

For phase noise and reference spur measurements, see the phase noise setup shown in Figure 63. Phase noise was measured on an LO and modulator output.

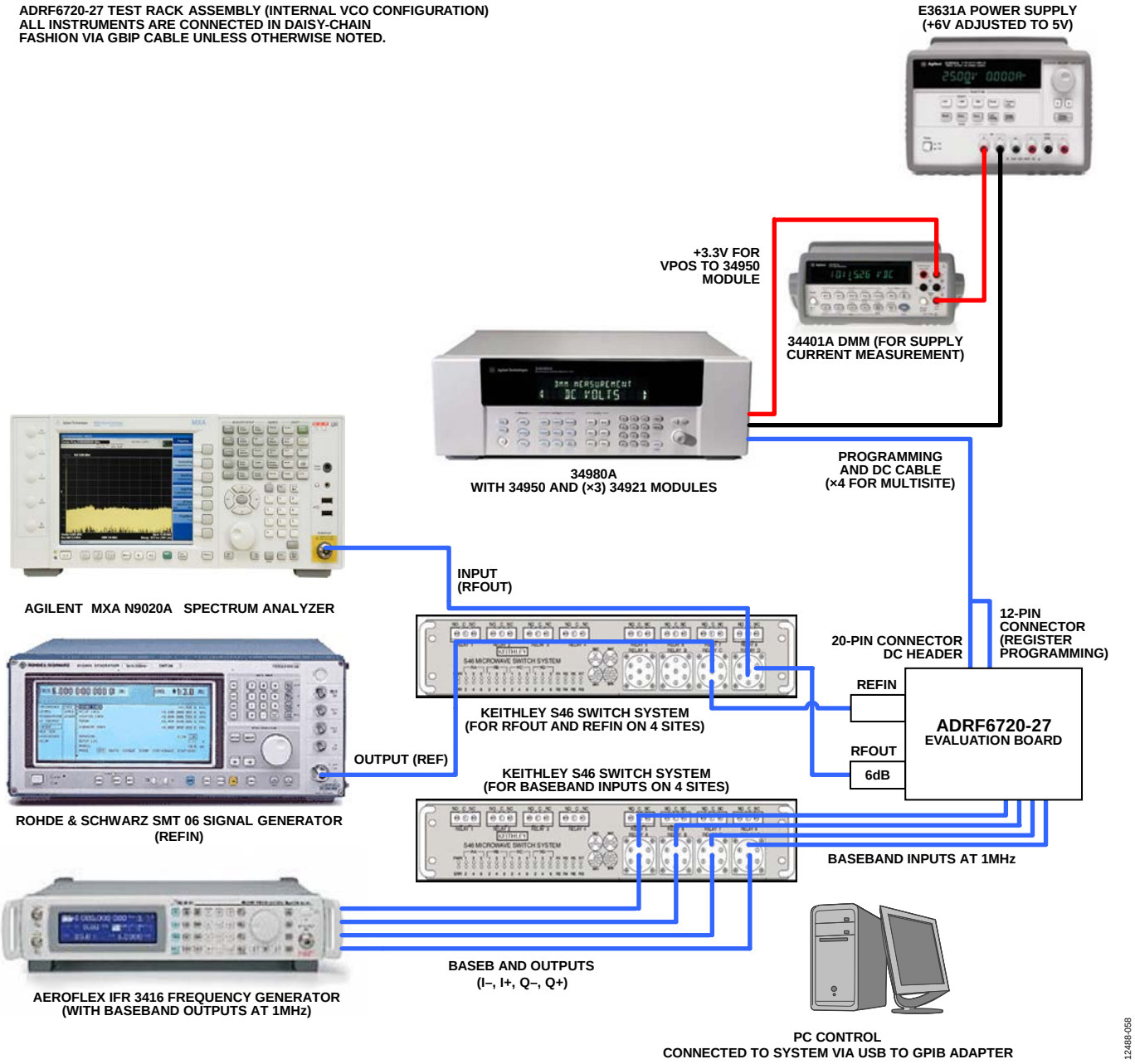


Figure 62. General Characterization Setup

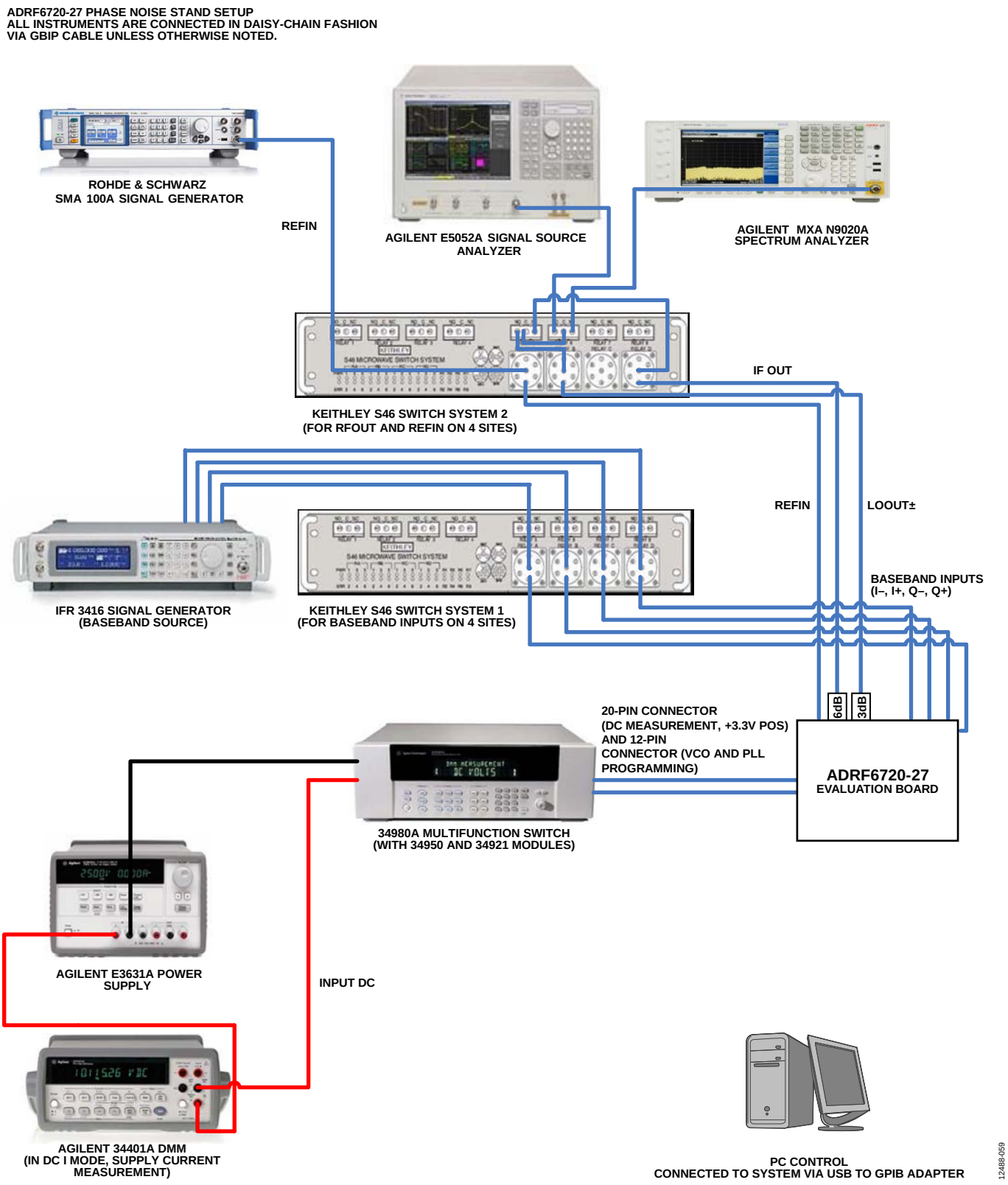


Figure 63. Characterization Setup for Phase Noise and Reference Spur Measurements

REGISTER MAP

Table 14. ADRF6720-27 Register Map

Reg	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x00	SOFT_RESET	[15:8]	RESERVED								0x0000	W
		[7:0]	RESERVED							SOFT_RESET		
0x01	ENABLES	[15:8]	RESERVED				LO_1XVCO_EN	MOD_EN	QUAD_DIV_EN	LO_DRV2X_EN	0xF67F	RW
		[7:0]	LO_DRV1X_EN	VCO_MUX_EN	REF_BUF_EN	VCO_EN	DIV_EN	CP_EN	VCO_LDO_EN	RESERVED		
0x02	INT_DIV	[15:8]	RESERVED				DIV_MODE	INT_DIV[10:8]			0x002C	RW
		[7:0]	INT_DIV[7:0]									
0x03	FRAC_DIV	[15:8]	FRAC_DIV[15:8]								0x0128	RW
		[7:0]	FRAC_DIV[7:0]									
0x04	MOD_DIV	[15:8]	MOD_DIV[15:8]								0x0600	RW
		[7:0]	MOD_DIV[7:0]									
0x10	ENBL_MASK	[15:8]	RESERVED				LO_1XVCO_MASK	MOD_MASK	QUAD_DIV_MASK	LO_DRV2X_MASK	0xF67F	RW
		[7:0]	LO_DRV1X_MASK	VCO_MUX_MASK	REF_BUF_MASK	VCO_MASK	DIV_MASK	CP_MASK	VCO_LDO_MASK	RESERVED		
0x20	CP_CTL	[15:8]	RESERVED	CP_SEL	CP_CSCALE				RESERVED		0x0C26	RW
		[7:0]	RESERVED		CP_BLEED							
0x21	PFD_CTL	[15:8]	RESERVED								0x000B	RW
		[7:0]	RESERVED	REF_MUX_SEL			PFD_POLARITY	REF_SEL				
0x22	VCO_CTL	[15:8]	VCO_LDO_R4SEL				VCO_LDO_R2SEL				0x2A03	RW
		[7:0]	LO_DRV_LVL		DRVDIV2_EN	DIV8_EN	DIV4_EN	VCO_SEL				
0x30	BALUN_CTL	[15:8]	RESERVED								0x0000	RW
		[7:0]	BAL_COUT				BAL_CIN					
0x31	MOD_LIN_CTL	[15:8]	RESERVED			MOD_RSEL[6:2]					0x1101	RW
		[7:0]	MOD_RSEL[1:0]		MOD_CSEL							
0x32	MOD_CTL0	[15:8]	RESERVED	MOD_BLEED			POL_Q	POL_I			0x0900	RW
		[7:0]	Q_LO				I_LO					
0x33	MOD_CTL1	[15:8]	DCOFF_I								0x0000	RW
		[7:0]	DCOFF_Q									
0x40	PFD_CP_CTL	[15:8]	RESERVED								0x0010	RW
		[7:0]	RESERVED	ABLDLY		CP_CTRL		PFD_CLK_EDGE				
0x42	DITH_CTL1	[15:8]	RESERVED								0x000E	RW
		[7:0]	RESERVED				DITH_EN	DITH_MAG		DITH_VAL		
0x43	DITH_CTL2	[15:8]	DITH_VAL[15:8]								0x0000	RW
		[7:0]	DITH_VAL[7:0]									
0x45	VCO_CTL2	[15:8]	RESERVED						VTUNE_CTRL		0x0000	RW
		[7:0]	VCO_BAND_SRC	BAND								
0x49	VCO_CTL3	[15:8]	RESERVED		SET_1					SET_0[8]	0x16BD	RW
		[7:0]	SET_0[7:0]									

REGISTER DETAILS

Address: 0x00, Reset: 0x0000, Name: SOFT_RESET

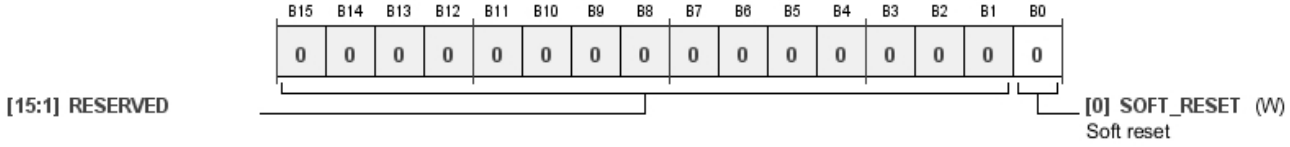


Table 15. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Settings	Description	Reset	Access
0	SOFT_RESET		Soft Reset.	0x0	W

Address: 0x01, Reset: 0xF67F, Name: ENABLES

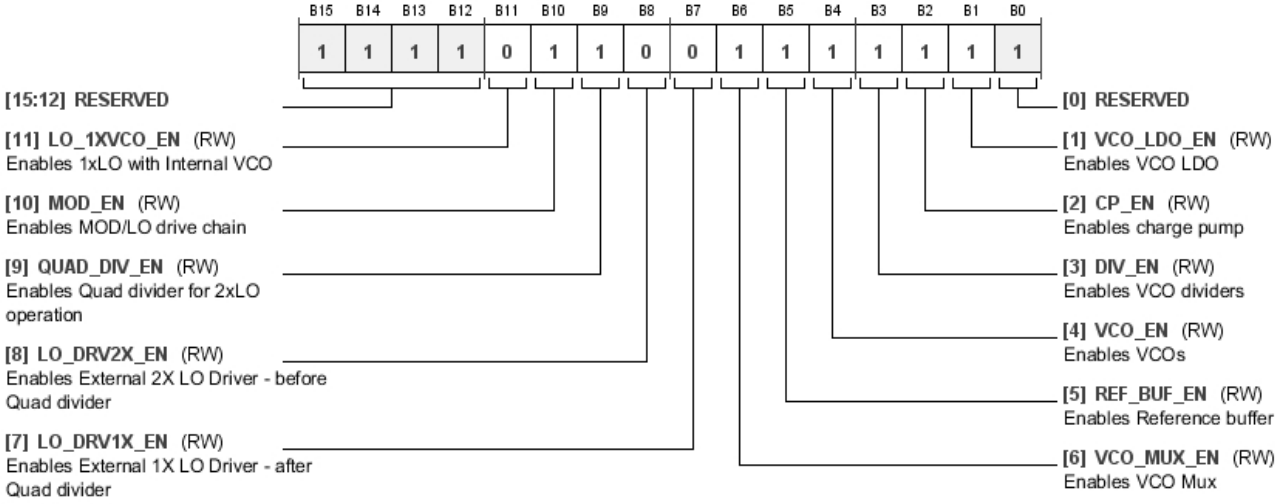


Table 16. Bit Descriptions for ENABLES

Bits	Bit Name	Settings	Description	Reset	Access
11	LO_1XVCO_EN		Enables 1 × LO with Internal VCO.	0x0	RW
10	MOD_EN		Enables MOD/LO Drive Chain.	0x1	RW
9	QUAD_DIV_EN		Enables Quad Divider for 2 × LO Operation.	0x1	RW
8	LO_DRV2X_EN		Enables External 2 × LO Driver—Before Quad Divider.	0x0	RW
7	LO_DRV1X_EN		Enables External 1 × LO Driver—After Quad Divider.	0x0	RW
6	VCO_MUX_EN		Enables VCO Mux.	0x1	RW
5	REF_BUF_EN		Enables Reference Buffer.	0x1	RW
4	VCO_EN		Enables VCOs.	0x1	RW
3	DIV_EN		Enables VCO Dividers.	0x1	RW
2	CP_EN		Enables Charge Pump.	0x1	RW
1	VCO_LDO_EN		Enables VCO LDO.	0x1	RW

Address: 0x02, Reset: 0x002C, Name: INT_DIV

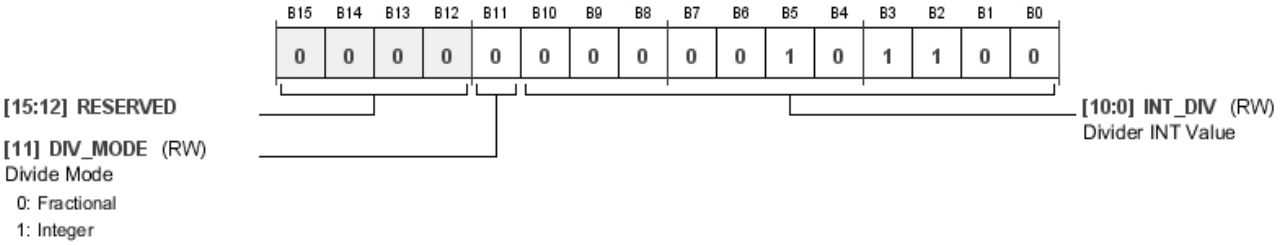


Table 17. Bit Descriptions for INT_DIV

Bits	Bit Name	Settings	Description	Reset	Access
11	DIV_MODE		Divide Mode.	0x0	RW
		0	Fractional		
		1	Integer		
[10:0]	INT_DIV		Divider INT Value.	0x2C	RW

Address: 0x03, Reset: 0x0128, Name: FRAC_DIV

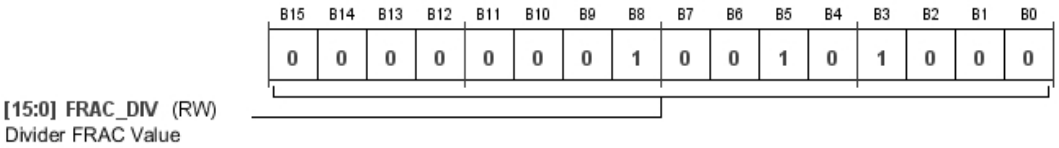


Table 18. Bit Descriptions for FRAC_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	FRAC_DIV		Divider FRAC Value.	0x128	RW

Address: 0x04, Reset: 0x0600, Name: MOD_DIV

Table 19. Bit Descriptions for MOD_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	MOD_DIV		Divider Modulus Value.	0x600	RW

Address: 0x10, Reset: 0xF67F, Name: ENBL_MASK

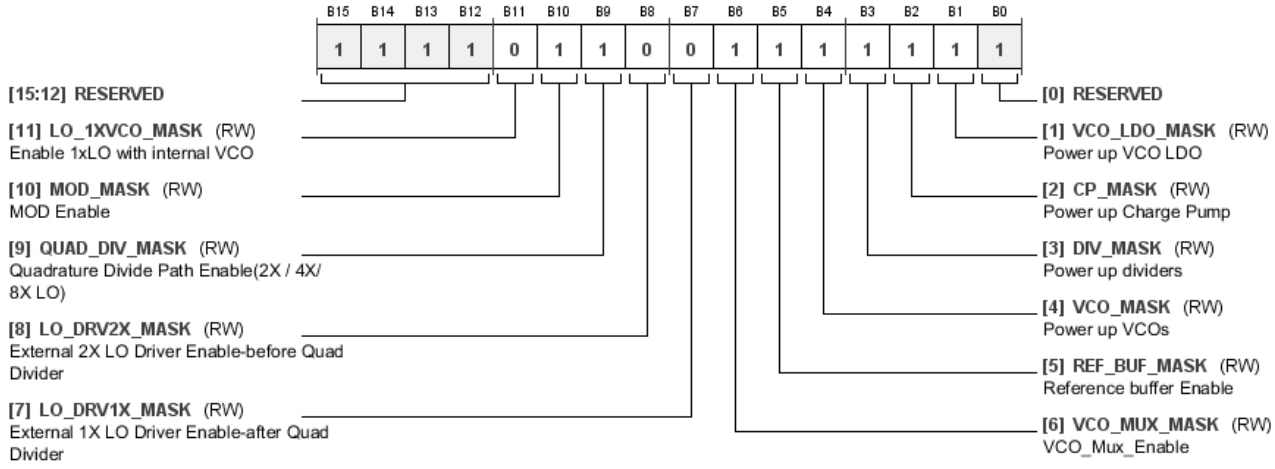


Table 20. Bit Descriptions for ENBL_MASK

Bits	Bit Name	Settings	Description	Reset	Access
11	LO_1XVCO_MASK		Enable 1 × LO with internal VCO.	0x0	RW
10	MOD_MASK		MOD Enable.	0x1	RW
9	QUAD_DIV_MASK		Quadrature Divide Path Enable (2 ×/4 ×/8 × LO).	0x1	RW
8	LO_DRV2X_MASK		External 2 × LO Driver Enable—Before Quad Divider.	0x0	RW
7	LO_DRV1X_MASK		External 1 × LO Driver Enable—After Quad Divider.	0x0	RW
6	VCO_MUX_MASK		VCO_Mux_Enable.	0x1	RW
5	REF_BUF_MASK		Reference Buffer Enable.	0x1	RW
4	VCO_MASK		Power Up VCOs.	0x1	RW
3	DIV_MASK		Power Up Dividers.	0x1	RW
2	CP_MASK		Power Up Charge Pump.	0x1	RW
1	VCO_LDO_MASK		Power Up VCO LDO.	0x1	RW

Address: 0x20, Reset: 0x0C26, Name: CP_CTL

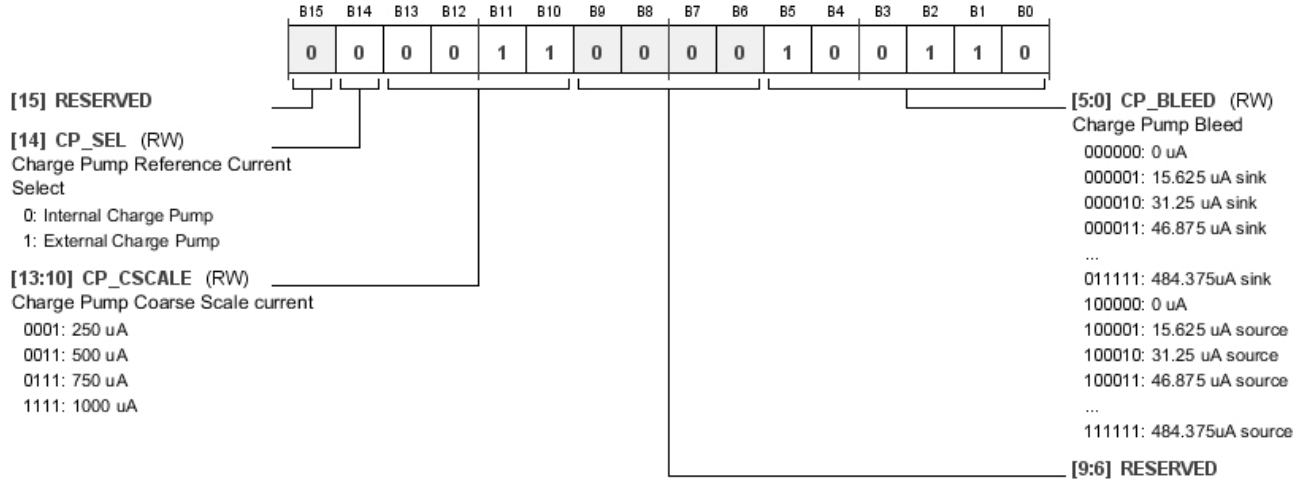


Table 21. Bit Descriptions for CP_CTL

Bits	Bit Name	Settings	Description	Reset	Access
14	CP_SEL		Charge Pump Reference Current Select.	0x0	RW
		0	Internal Charge Pump.		
		1	External Charge Pump.		
[13:10]	CP_CSCALE		Charge Pump Coarse Scale Current.	0x3	RW
		0001	250 µA.		
		0011	500 µA.		
		0111	750 µA.		
		1111	1000 µA.		
[5:0]	CP_BLEED		Charge Pump Bleed.	0x26	RW
		000000	0 µA		
		000001	15.625 µA Sink.		
		000010	31.25 µA Sink.		
		000011	46.875 µA Sink.		
		…			
		011111	484.375 µA Sink.		
		100000	0 µA.		
		100001	15.625 µA Source.		
		100010	31.25 µA Source.		
		100011	46.875 µA Source.		
		…			
		111111	484.375 µA Source.		

Address: 0x21, Reset: 0x000B, Name: PFD_CTL

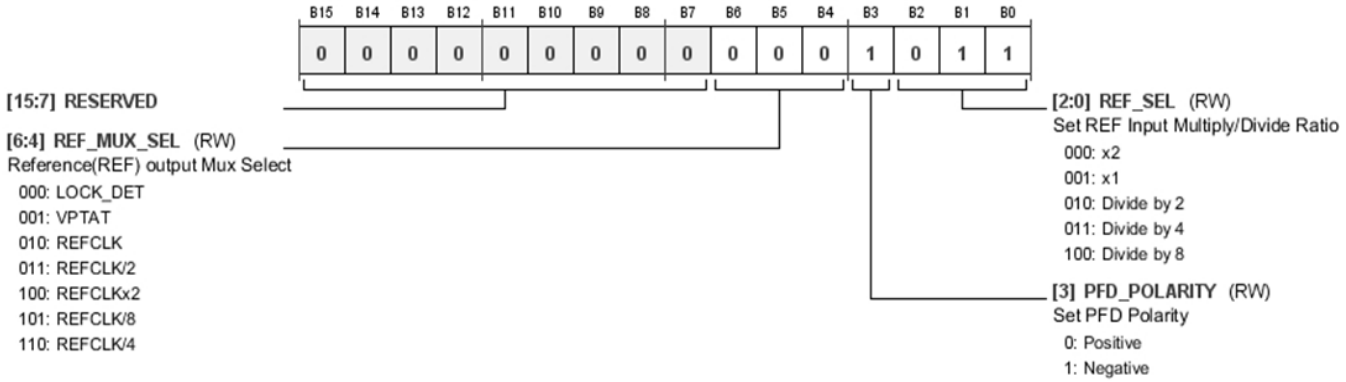


Table 22. Bit Descriptions for PFD_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	REF_MUX_SEL		Reference (REF) Output Mux Select.	0x0	RW
		000	LOCK_DET.		
		001	VPTAT.		
		010	REFCLK.		
		011	REFCLK/2.		
		100	REFCLK × 2.		
		101	REFCLK/8.		
		110	REFCLK/4.		
3	PFD_POLARITY		Set PFD Polarity.	0x1	RW
		0	Positive.		
		1	Negative.		

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	REF_SEL		Set REF Input Multiply/Divide Ratio.	0x3	RW
		000	×2.		
		001	×1.		
		010	Divide by 2.		
		011	Divide by 4.		
		100	Divide by 8.		

Address: 0x22, Reset: 0x2A03, Name: VCO_CTL

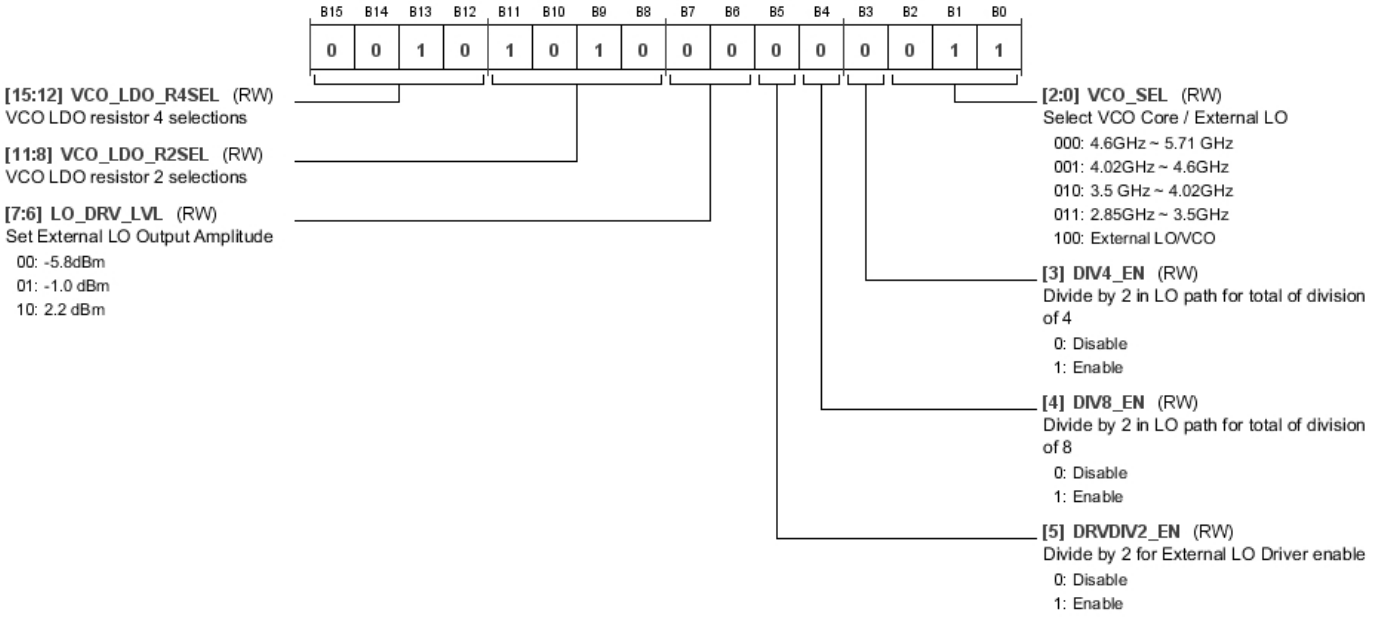


Table 23. Bit Descriptions for VCO_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	VCO_LDO_R4SEL		VCO LDO Resistor 4 Selections.	0x2	RW
[11:8]	VCO_LDO_R2SEL		VCO LDO Resistor 2 Selections.	0xA	RW
[7:6]	LO_DRV_LVL		Set External LO Output Amplitude.	0x0	RW
		00	−5.8 dBm.		
		01	−1.0 dBm.		
		10	+2.2 dBm.		
5	DRVDIV2_EN		Divide by 2 for External LO Driver Enable.	0x0	RW
		0	Disable.		
		1	Enable.		
4	DIV8_EN		Divide by 2 in LO Path for Total Division of 8.	0x0	RW
		0	Disable.		
		1	Enable.		
3	DIV4_EN		Divide by 2 in LO Path for Total Division of 4.	0x0	RW
		0	Disable.		
		1	Enable.		

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	VCO_SEL		Select VCO Core/External LO.	0x3	RW
		000	4.6 GHz to About 5.71 GHz.		
		001	4.02 GHz to About 4.6 GHz.		
		010	3.5 GHz to About 4.02 GHz.		
		011	2.85 GHz to About 3.5 GHz.		
		100	External LO/VCO.		

Address: 0x30, Reset: 0x0000, Name: BALUN_CTL

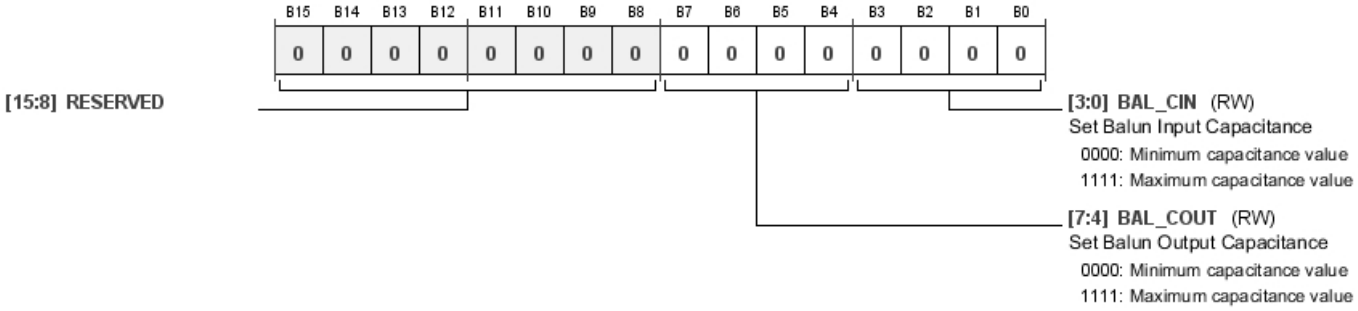


Table 24. Bit Descriptions for BALUN_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	BAL_COUT		Set Balun Output Capacitance.	0x0	RW
		0000	Minimum Capacitance Value.		
		1111	Maximum Capacitance Value.		
[3:0]	BAL_CIN		Set Balun Input Capacitance.	0x0	RW
		0000	Minimum Capacitance Value.		
		1111	Maximum Capacitance Value.		

Address: 0x31, Reset: 0x1101, Name: MOD_LIN_CTL

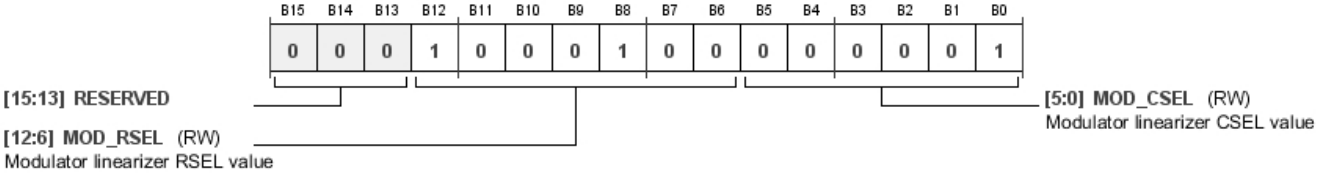


Table 25. Bit Descriptions for MOD_LIN_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[12:6]	MOD_RSEL		Modulator Linearizer RSEL Value.	0x44	RW
[5:0]	MOD_CSEL		Modulator Linearizer CSEL Value.	0x01	RW

Address: 0x32, Reset: 0x0900, Name: MOD_CTL0

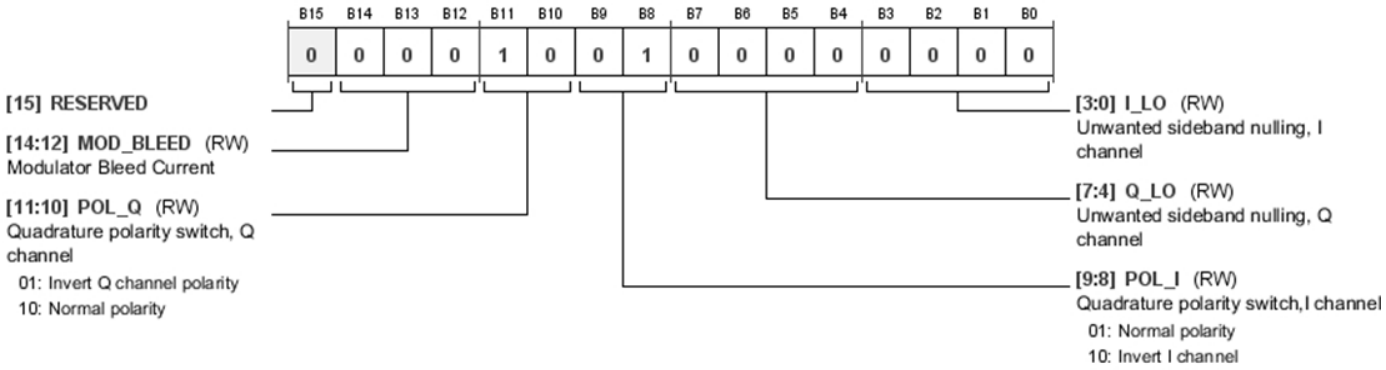


Table 26. Bit Descriptions for MOD_CTL0

Bits	Bit Name	Settings	Description	Reset	Access
[14:12]	MOD_BLEED		Modulator Bleed Current.	0x0	RW
[11:10]	POL_Q		Quadrature Polarity Switch, Q Channel.	0x2	RW
		01	Inverted Q Channel Polarity.		
		10	Normal Polarity.		
[9:8]	POL_I		Quadrature Polarity Switch, I Channel.	0x1	RW
		01	Normal Polarity.		
		10	Inverted I Channel Polarity.		
[7:4]	Q_LO		Unwanted Sideband Nulling, Q Channel.	0x0	RW
[3:0]	I_LO		Unwanted Sideband Nulling, I Channel.	0x0	RW

Address: 0x33, Reset: 0x0000, Name: MOD_CTL1

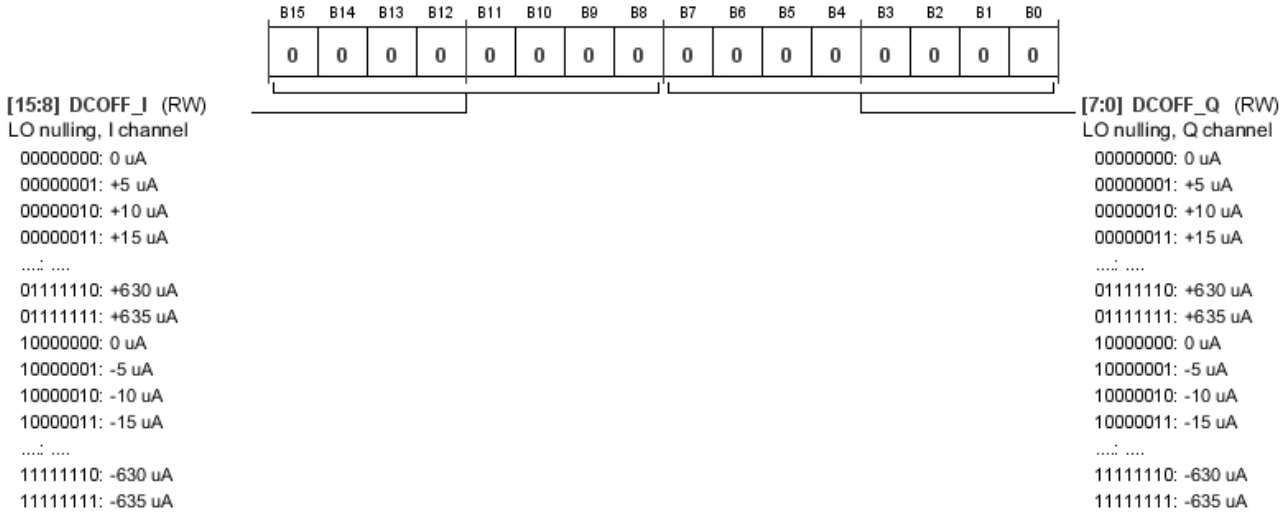


Table 27. Bit Descriptions for MOD_CTL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	DCOFF_I		LO Nulling, I Channel.	0x0	RW
		00000000	0 µA.		
		00000001	+5 µA.		
		00000010	+10 µA.		
		00000011	+15 µA.		
		…	…		
		01111110	+630 µA.		
		01111111	+635 µA.		
		10000000	0 µA.		
		10000001	−5 µA.		
		10000010	−10 µA.		
		10000011	−15 µA.		
		…	…		
		11111110	−630 µA.		
		11111111	−635 µA.		
[7:0]	DCOFF_Q		LO Nulling, Q Channel.	0x0	RW
		00000000	0 µA.		
		00000001	+5 µA.		
		00000010	+10 µA.		
		00000011	+15 µA.		
		…	…		
		01111110	+630 µA.		
		01111111	+635 µA.		
		10000000	0 µA.		
		10000001	−5 µA.		
		10000010	−10 µA.		
		10000011	−15 µA.		
		…	…		
		11111110	−630 µA.		
		11111111	−635 µA.		

Address: 0x40, Reset: 0x0010, Name: PFD_CP_CTL

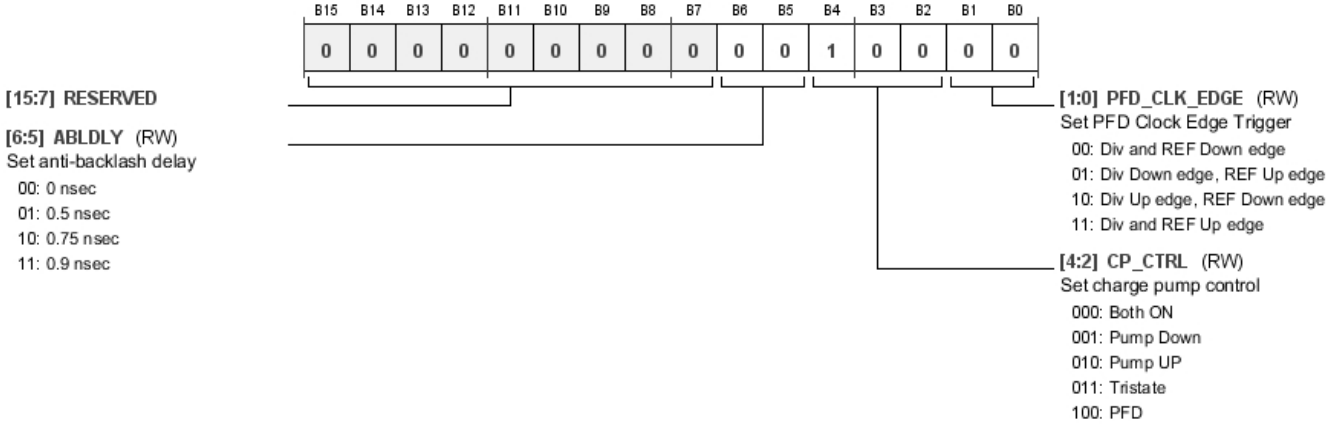


Table 28. Bit Descriptions for PFD_CP_CTL

Bits	Bit Name	Settings	Description	Reset	Access
[6:5]	ABLDLY		Set Antibacklash Delay.	0x0	RW
		00	0 ns.		
		01	0.5 ns.		
		10	0.75 ns.		
		11	0.9 ns.		
[4:2]	CP_CTRL		Set Charge Pump Control.	0x4	RW
		000	Both On.		
		001	Pump Down.		
		010	Pump Up.		
		011	Tristate.		
		100	PFD.		
[1:0]	PFD_CLK_EDGE		Set PFD Clock Edge Trigger.	0x0	RW
		00	Divide and Reference Down Edge.		
		01	Divide Down Edge, Reference Up Edge.		
		10	Divide Up Edge, Reference Down Edge.		
		11	Divide and Reference Up Edge.		

Address: 0x42, Reset: 0x000E, Name: DITH_CTL1

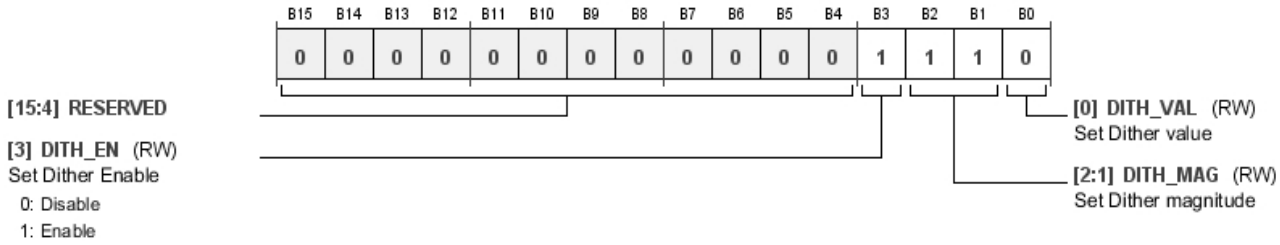


Table 29. Bit Descriptions for DITH_CTL1

Bits	Bit Name	Settings	Description	Reset	Access
3	DITH_EN		Set Dither Enable.	0x1	RW
		0	Disable.		
		1	Enable.		
[2:1]	DITH_MAG		Set Dither Magnitude.	0x3	RW
0	DITH_VAL		Set Dither Value.	0x0	RW

Address: 0x43, Reset: 0x0000, Name: DITH_CTL2

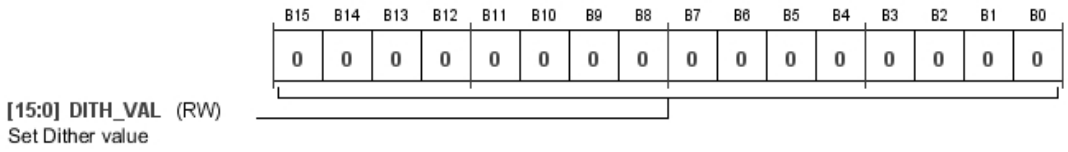


Table 30. Bit Descriptions for DITH_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DITH_VAL		Set Dither Value.	0x0	RW

Address: 0x45, Reset: 0x0000, Name: VCO_CTL2

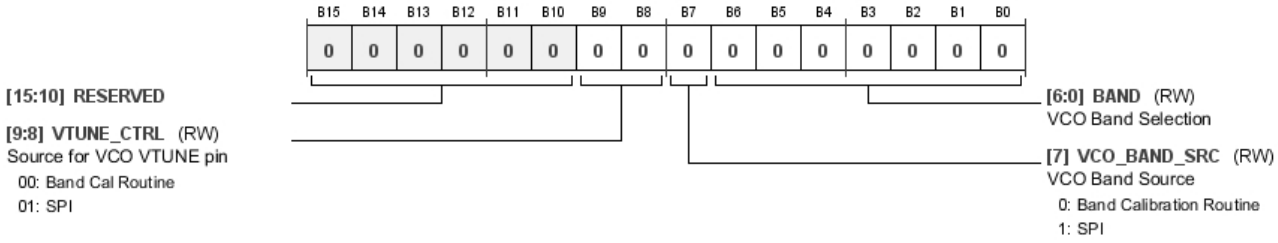


Table 31. Bit Descriptions for VCO_CTL2

Bits	Bit Name	Settings	Description	Reset	Access
[9:8]	VTUNE_CTRL		Source for VCO VTUNE Pin.	0x0	RW
		00	Band Calibration Routine.		
		01	SPI.		
7	VCO_BAND_SRC		VCO Band Source	0x0	RW
		0	Band Calibration Routine.		
		1	SPI.		
[6:0]	BAND		VCO Band Selection.	0x00	RW

Address: 0x49, Reset: 0x16BD, Name: VCO_CTL3

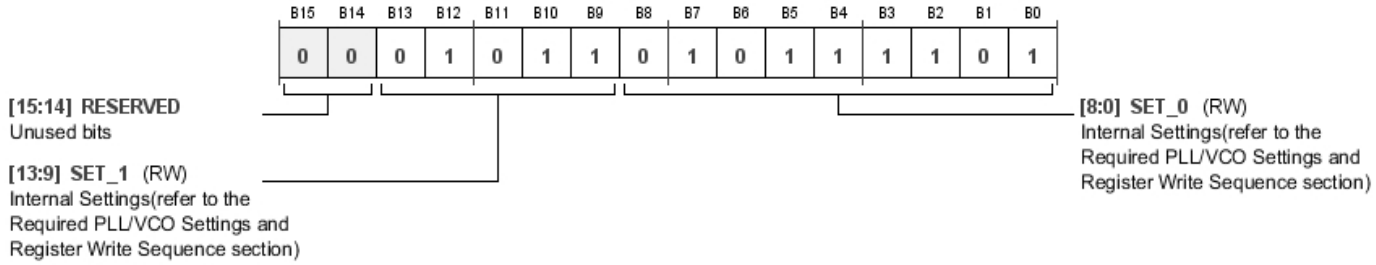
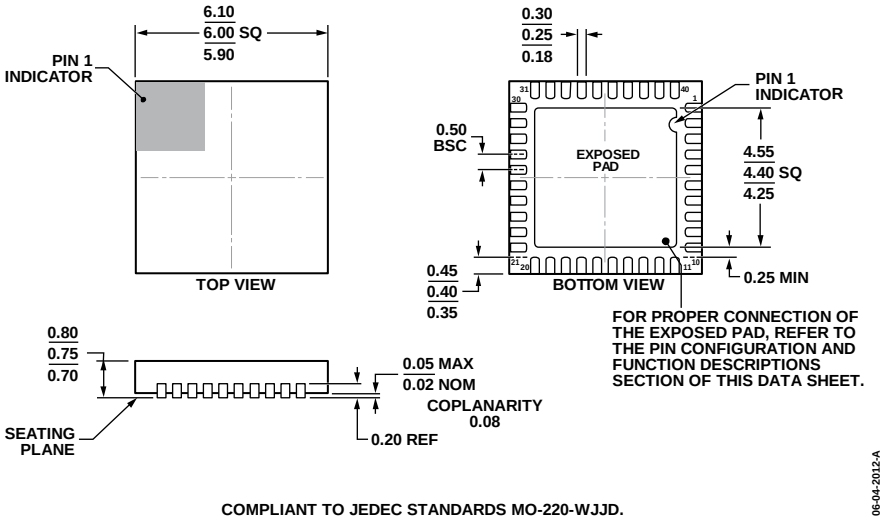


Table 32. Bit Descriptions for VCO_CTL3

Bits	Bit Name	Settings	Description	Reset	Access
[13:9]	SET_1		Internal Settings. Refer to the Required PLL/VCO Settings and Register Write Sequence section.	0x0B	RW
[8:0]	SET_0		Internal Settings. Refer to the Required PLL/VCO Settings and Register Write Sequence section.	0x0BD	RW

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.

Figure 64. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6720-27ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-11
ADRF6720-27-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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