THE DATASHEET OF

AD7879-1ACPZ-RL

Low Voltage Controller for Touch Screens

Data Sheet

AD7879/AD7889

FEATURES

- 4-wire touch screen interface
- 1.6 V to 3.6 V operation
- Median and averaging filter to reduce noise
- Automatic conversion sequencer and timer
- User-programmable conversion parameters
- Auxiliary analog input/battery monitor (0.5 V to 5 V)
- 1 optional GPIO
- Interrupt outputs ($\overline{\text{INT}}$, $\overline{\text{PENIRQ}}$)
- Touch-pressure measurement
- Wake-up on touch function
- Shutdown mode: 6 µA maximum
- 12-ball, 1.6 mm × 2 mm WLCSP
- 16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Personal digital assistants
- Smart handheld devices
- Touch screen monitors
- Point-of-sale terminals
- Medical devices
- Cell phones

FUNCTIONAL BLOCK DIAGRAM

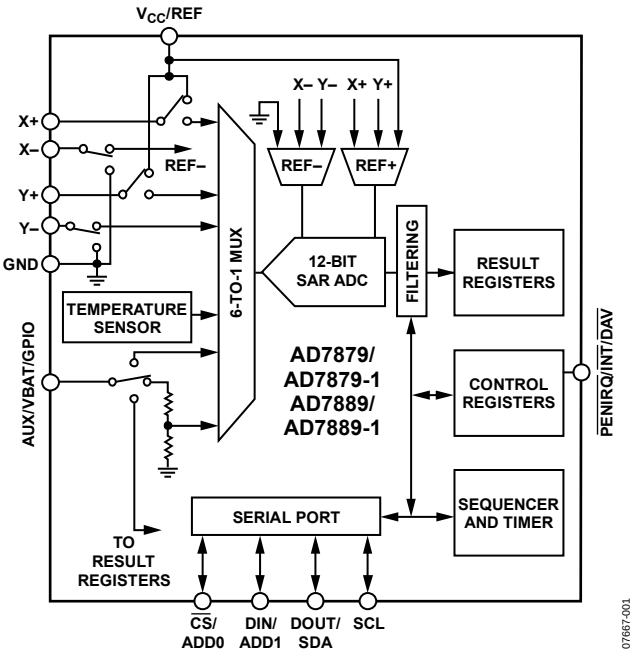

Figure 1.

GENERAL DESCRIPTION

The AD7879/AD7889 are 12-bit successive approximation analog-to-digital converters (SAR ADCs) with a synchronous serial interface and low on-resistance switches for driving 4-wire resistive touch screens. The AD7879/AD7889 work with a very low power supply—a single 1.6 V to 3.6 V supply—and feature a throughput rate of 105 kSPS. The devices include a shutdown mode that reduces current consumption to less than 6 µA.

To reduce the effects of noise from LCDs and other sources, the AD7879/AD7889 contain a preprocessing block. The preprocessing function consists of a median filter and an averaging filter. The combination of these two filters provides a more robust solution, discarding the spurious noise in the signal and keeping only the data of interest. The size of both filters is programmable. Other user-programmable conversion controls include variable acquisition time and first conversion delay; up to 16 averages can be taken per conversion. The AD7879/AD7889 can run in slave mode or standalone (master) mode, using an automatic conversion sequencer and timer.

The AD7879/AD7889 have a programmable pin that can operate as an auxiliary input to the ADCs, as a battery monitor, or as a general-purpose input/output (GPIO). In addition, a programmable interrupt output can operate in three modes: as a general-purpose interrupt to signal when new data is available ($\overline{\text{DAV}}$), as an interrupt to indicate when limits are exceeded ($\overline{\text{INT}}$), or as a pen-down interrupt when the screen is touched ($\overline{\text{PENIRQ}}$). The AD7879/AD7889 offer temperature measurement and touch pressure measurement.

The AD7879 is available in a 12-ball, 1.6 mm × 2 mm WLCSP and in a 16-lead, 4 mm × 4 mm LFCSP. The AD7889 is available in a backside coated version of the WLCSP. Both devices support an SPI interface (AD7879/AD7889) or an I²C interface (AD7879-1/AD7889-1).

Note that throughout this data sheet, multifunction pins, such as $\overline{\text{PENIRQ}}$/$\overline{\text{INT}}$/$\overline{\text{DAV}}$, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{\text{PENIRQ}}$, when only that function is relevant.

Rev. D

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8/2016—Rev. C to Rev. D

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11/2010—Rev. B to Rev. C

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1/2010—Rev. A to Rev. B

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Changes to Ordering Guide ... 38

3/2009—Rev. 0 to Rev. A

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10/2008—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 1.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	11	12		Bits	
Integral Nonlinearity (INL)[1]			±3	LSB	LSB size = 390 µV
Differential Nonlinearity (DNL)[1]					LSB size = 390 µV
Negative DNL			−0.99	LSB	
Positive DNL			2	LSB	
Offset Error[1, 2]		±2	±6	LSB	
Gain Error[1, 2]			±4	LSB	
Noise[3]		70		µV rms	
Power Supply Rejection[3]		60		dB	
Internal Clock Frequency		2		MHz	
Internal Clock Accuracy	1.8		2.2	MHz	
SWITCH DRIVERS					
On Resistance[1]					
Y+, X+		6		Ω	
Y−, X−		5		Ω	
ANALOG INPUTS					
Input Voltage Range	0		V_{CC}	V	
DC Leakage Current		±0.1		µA	
Input Capacitance		30		pF	
Accuracy		0.3		%	
TEMPERATURE MEASUREMENT					
Temperature Range	−40		+85	°C	
Resolution		0.3		°C	
Accuracy[2]		±2		°C	Calibrated at 25°C
BATTERY MONITOR					
Input Voltage Range	0.5		5	V	
Input Impedance[3]		16		kΩ	
Accuracy		2	5	%	Uncalibrated accuracy
LOGIC INPUTS (DIN, SCL, $\overline{CS}$, SDA, GPIO)					
Input High Voltage, V_{INH}	0.7 × V_{CC}			V	
Input Low Voltage, V_{INL}			0.3 × V_{CC}	V	
Input Current, I_{IN}		0.01		µA	V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN}[3]		10		pF	
LOGIC OUTPUTS (DOUT, GPIO, SCL, SDA, $\overline{INT}$)					
Output High Voltage, V_{OH}	V_{CC} − 0.2			V	
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.1		µA	
Floating State Output Capacitance[2]		5		pF	
CONVERSION RATE[3]					
Conversion Time		9.5		µs	Including 2 µs of acquisition time, median and averaging (MAV) filter off; 2 µs of additional time is required if the MAV filter is on
Throughput Rate		105		kSPS	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{CC}	1.6	2.6	3.6	V	Specified performance
I_{CC}					Digital inputs = 0 V or V_{CC}
Converting Mode		480	650	μA	ADC on, PM = 10
Static		406		μA	ADC and temperature sensor are off; the reference and oscillator are on; PM = 01 or 11
Shutdown Mode		0.5	6	μA	PM = 00

[1] See the Terminology section.
[2] Guaranteed by characterization; not production tested.
[3] Sample tested at 25°C to ensure compliance.

SPI TIMING SPECIFICATIONS (AD7879/AD7889)

V_{CC} = 1.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.4 V.

Table 2.

Parameter[1]	Limit	Unit	Description
f_{SCL}	5	MHz max	
t_1	5	ns min	$\overline{CS}$ falling edge to first SCL falling edge
t_2	20	ns min	SCL high pulse width
t_3	20	ns min	SCL low pulse width
t_4	15	ns min	DIN setup time
t_5	15	ns min	DIN hold time
t_6	20	ns max	DOUT access time after SCL falling edge
t_7	16	ns max	$\overline{CS}$ rising edge to DOUT high impedance
t_8	15	ns min	SCL rising edge to $\overline{CS}$ high

[1] Guaranteed by design; not production tested.

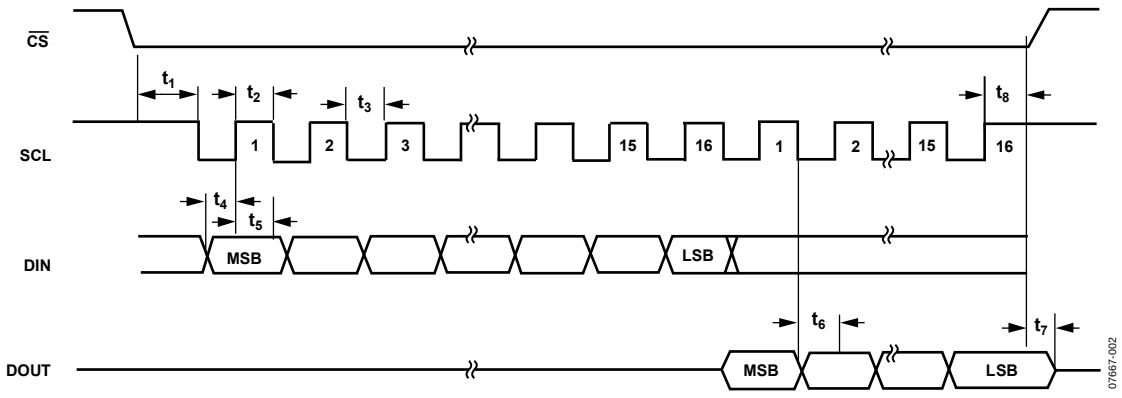


Figure 2. Detailed SPI Timing Diagram

I²C TIMING SPECIFICATIONS (AD7879-1/AD7889-1)

V_{CC} = 1.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are timed from a voltage level of 1.4 V.

Table 3.

Parameter[1]	Limit	Unit	Description
f_{SCL}	400	kHz max	
t_1	0.6	µs min	Start condition hold time, $t_{HD; STA}$
t_2	1.3	µs min	Clock low period, t_{LOW}
t_3	0.6	µs min	Clock high period, t_{HIGH}
t_4	100	ns min	Data setup time, $t_{SU; DAT}$
t_5	300	ns min	Data hold time, $t_{HD; DAT}$
t_6	0.6	µs min	Stop condition setup time, $t_{SU; STO}$
t_7	0.6	µs min	Start condition setup time, $t_{SU; STA}$
t_8	1.3	µs min	Bus-free time between stop and start conditions, t_{BUF}
t_R	300	ns max	Clock/data rise time
t_F	300	ns max	Clock/data fall time

[1] Guaranteed by design; not production tested.

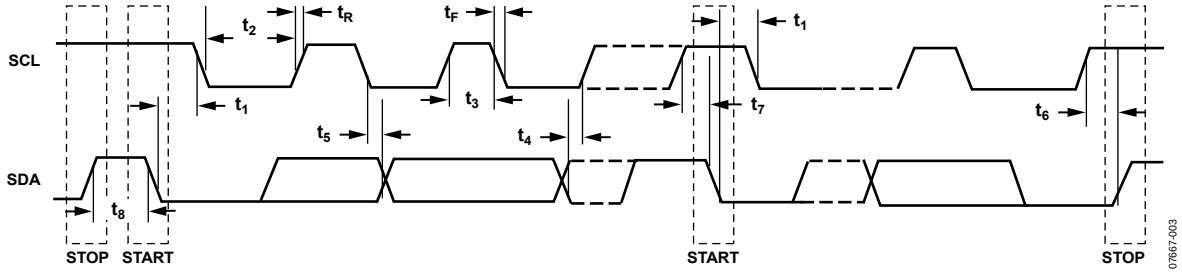


Figure 3. Detailed I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC} to GND	−0.3 V to +3.6 V
Analog Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
AUX/VBAT to GND	−0.3 V to +5 V
Digital Input Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	10 mA
ESD Rating (X+, Y+, X−, Y−)	
Air Discharge Human Body Model	15 kV
Contact Human Body Model	10 kV
ESD Rating (All Other Pins)	
Human Body Discharge	4 kV
Field-Induced Charged Device Model	1 kV
Machine Model	0.2 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation	
WLCSP (4-Layer Board)	866 mW
LFCSP (4-Layer Board)	2.138 W
IR Reflow Peak Temperature	260°C (±0.5°C)
Lead Temperature (Soldering 10 sec)	300°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
12-Ball WLCSP	75	°C/W
16-Lead LFCSP	30.4	°C/W

[1] 4-layer board.

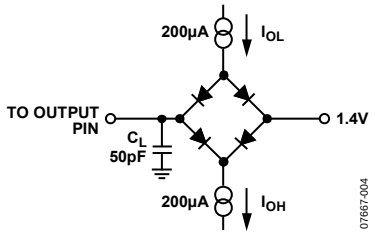


Figure 4. Circuit Used for Digital Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

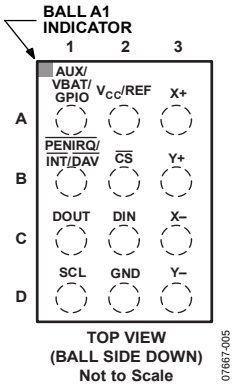


Figure 5. AD7879/AD7889 WLCSP Pin Configuration

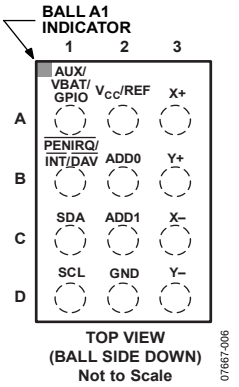
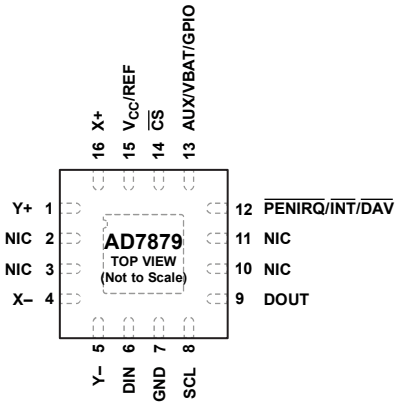


Figure 6. AD7879-1/AD7889-1 WLCSP Pin Configuration

Table 6. WLCSP Pin Function Descriptions

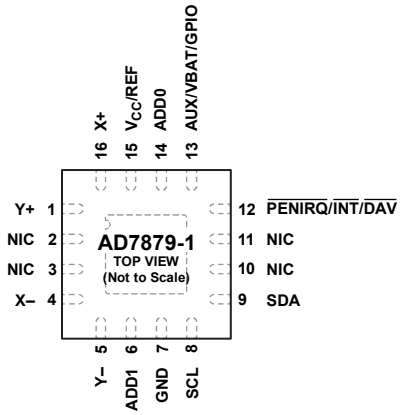
Pin No.			
AD7879/ AD7889	**AD7879-1/ AD7889-1**	**Mnemonic**	**Description**
1A	1A	AUX/VBAT/GPIO	This pin can be programmed as an auxiliary input to the ADC (AUX), as a battery measurement input to the ADC (VBAT), or as a GPIO.
1B	1B	$\overline{\text{PENIRQ}}/\overline{\text{INT}}/\overline{\text{DAV}}$	Interrupt Output. This pin is asserted when the screen is touched ($\overline{\text{PENIRQ}}$), when a measurement exceeds the preprogrammed limits ($\overline{\text{INT}}$), or when new data is available in the registers ($\overline{\text{DAV}}$). This pin is active low and has an internal 50 kΩ pull-up resistor.
1C	Not applicable	DOUT	SPI Serial Data Output for the AD7879/AD7889.
Not applicable	1C	SDA	I²C Serial Data Input and Output for the AD7879-1/AD7889-1.
1D	1D	SCL	Serial Interface Clock Input.
2A	2A	V_{CC}/REF	Power Supply Input and ADC Reference.
2B	Not applicable	$\overline{\text{CS}}$	Chip Select for the SPI Serial Interface on the AD7879/AD7889. This pin is active low.
Not applicable	2B	ADD0	I²C Address Bit 0 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
2C	Not applicable	DIN	SPI Serial Data Input to the AD7879/AD7889.
Not applicable	2C	ADD1	I²C Address Bit 1 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
2D	2D	GND	Ground. This pin is the ground reference point for all circuitry on the AD7879/AD7889. Refer all analog input signals and any external reference signal to this voltage.
3A	3A	X+	Touch Screen Input Channel.
3B	3B	Y+	Touch Screen Input Channel.
3C	3C	X–	Touch Screen Input Channel.
3D	3D	Y–	Touch Screen Input Channel.



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

07667-007

Figure 7. AD7879 LFCSP Pin Configuration



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE.

07667-008

Figure 8. AD7879-1 LFCSP Pin Configuration

Table 7. LFCSP Pin Function Descriptions

Pin No.			
AD7879	**AD7879-1**	**Mnemonic**	**Description**
1	1	Y+	Touch Screen Input Channel.
2, 3, 10, 11	2, 3, 10, 11	NIC	No Internal Connection.
4	4	X–	Touch Screen Input Channel.
5	5	Y–	Touch Screen Input Channel.
6	Not applicable	DIN	SPI Serial Data Input to the AD7879.
Not applicable	6	ADD1	I²C Address Bit 1 for the AD7879-1. Tie this pin high or low to determine an address for the AD7879-1 (see Table 25).
7	7	GND	Ground. This pin is the ground reference point for all circuitry on the AD7879. Refer all analog input signals and any external reference signal to this voltage.
8	8	SCL	Serial Interface Clock Input.
9	Not applicable	DOUT	SPI Serial Data Output for the AD7879.
Not applicable	9	SDA	I²C Serial Data Input and Output for the AD7879-1.
12	12	$\overline{\text{PENIRQ}}/\overline{\text{INT}}/\overline{\text{DAV}}$	Interrupt Output. This pin is asserted when the screen is touched ($\overline{\text{PENIRQ}}$), when a measurement exceeds the preprogrammed limits ($\overline{\text{INT}}$), or when new data is available in the registers ($\overline{\text{DAV}}$). This pin is active low and has an internal 50 kΩ pull-up resistor.
13	13	AUX/VBAT/GPIO	This pin can be programmed as an auxiliary input to the ADC (AUX), as a battery measurement input to the ADC (VBAT), or as a GPIO.
14	Not applicable	$\overline{\text{CS}}$	Chip Select for the SPI Serial Interface on the AD7879/AD7889. This pin is active low.
Not applicable	14	ADD0	I²C Address Bit 0 for the AD7879-1/AD7889-1. Tie this pin high or low to determine an address for the AD7879-1/AD7889-1 (see Table 25).
15	15	V_{CC}/REF	Power Supply Input and ADC Reference.
16	16	X+	Touch Screen Input Channel.
		EP	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.6 V, f_{SCL} = 2 MHz, unless otherwise noted.

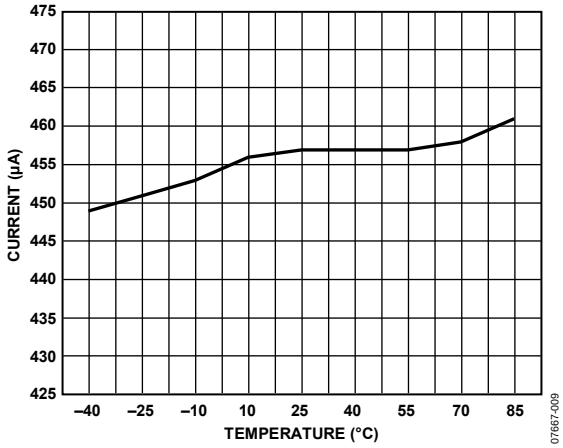


Figure 9. Supply Current vs. Temperature

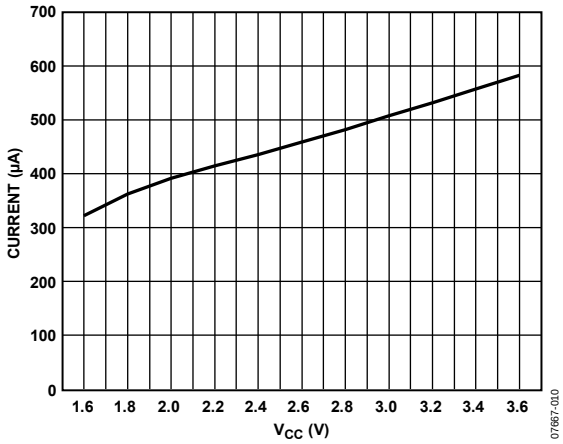


Figure 10. Supply Current vs. V_{CC}

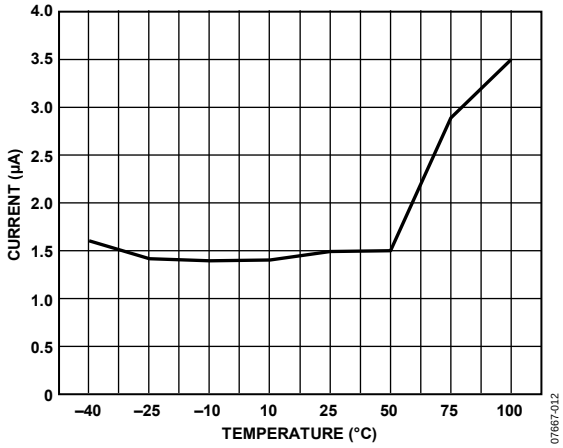


Figure 11. Full Power-Down Current (I_{DD}) vs. Temperature

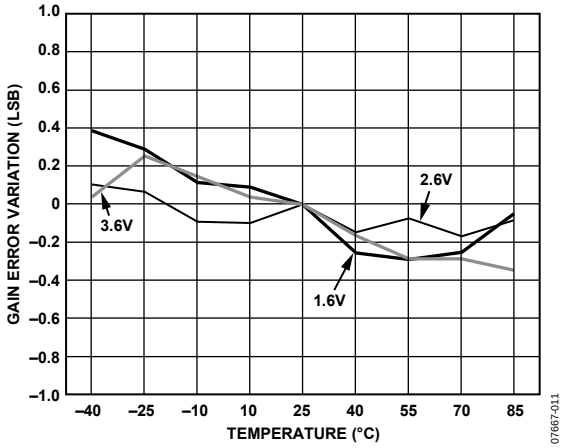


Figure 12. Change in ADC Gain vs. Temperature

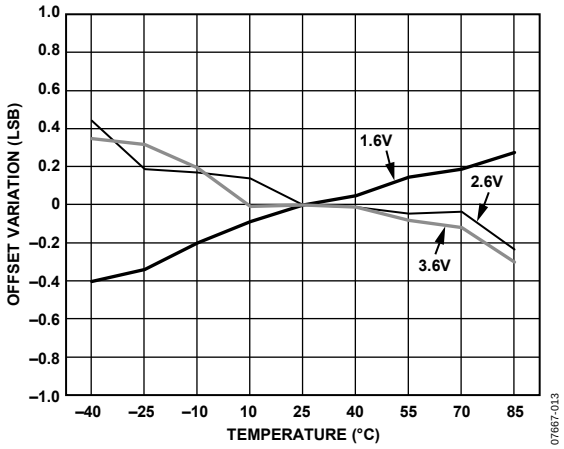


Figure 13. ADC Offset Variation vs. Temperature

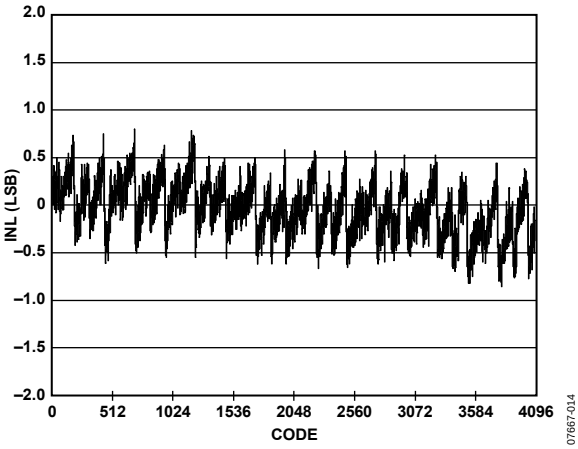


Figure 14. ADC INL

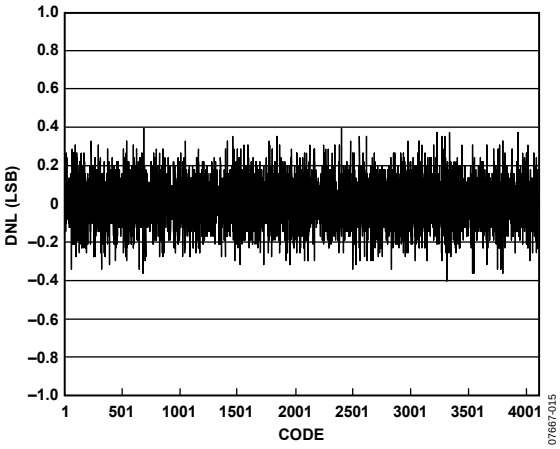


Figure 15. ADC DNL

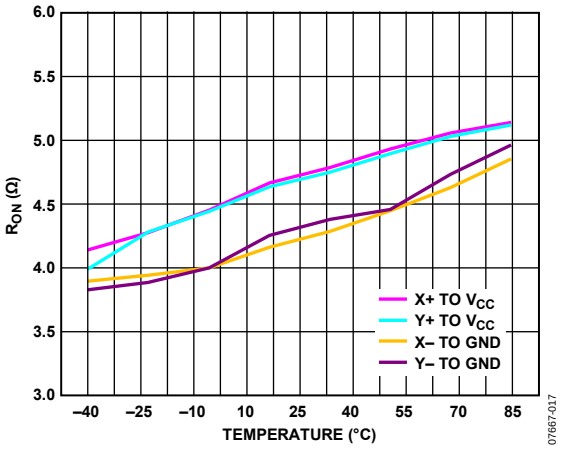


Figure 17. Switch On Resistance (R_{ON}) vs. Temperature ($X+$, $Y+$: Pin to V_{CC}; $X–$, $Y–$: Pin to GND)

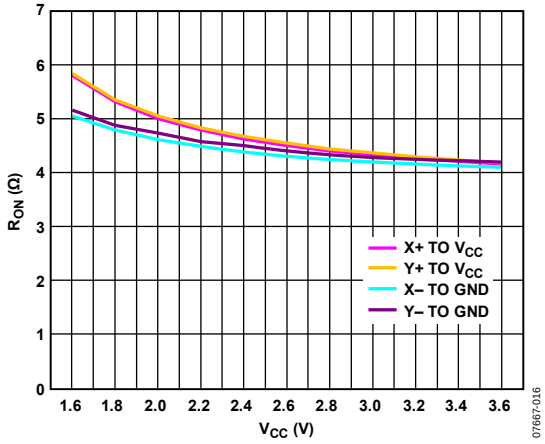


Figure 16. Switch On Resistance (R_{ON}) vs. V_{CC} ($X+$, $Y+$: Pin to V_{CC}; $X–$, $Y–$: Pin to GND)

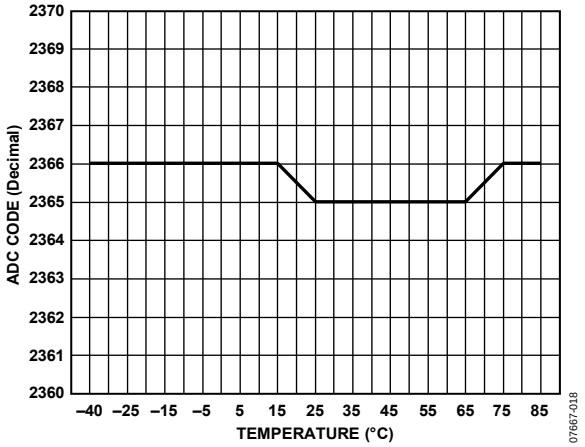


Figure 18. ADC Code vs. Temperature (Fixed Analog Input)

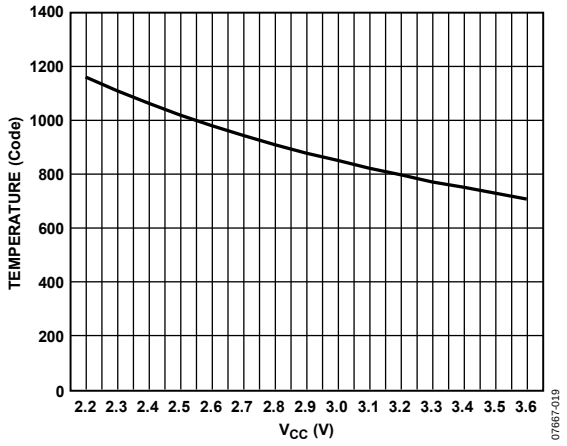


Figure 19. Temperature Code vs. V_{CC} for 25°C

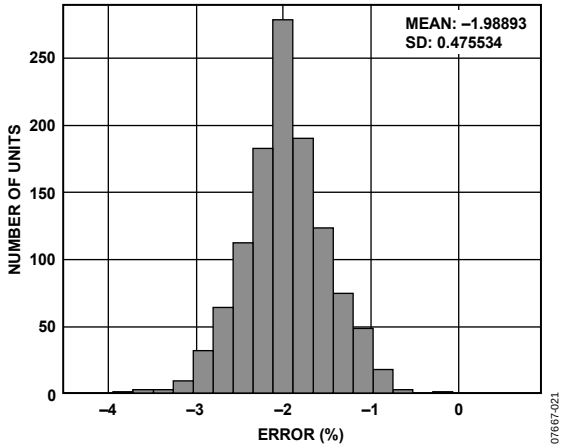


Figure 21. Typical Uncalibrated Accuracy for the Battery Channel (25°C)

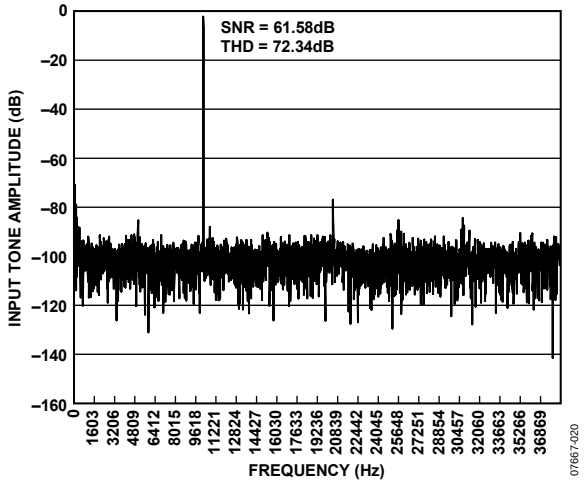


Figure 20. Typical FFT Plot for the Auxiliary Channels at a 25 kHz Sampling Rate and a 1 kHz Input Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at 1 LSB below the first code transition and full scale at 1 LSB above the last code transition.

Gain Error
Gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (V_{REF} − 1 LSB) after the offset error has been calibrated out.

Offset Error
Offset error is the deviation of the first code transition (00 … 000 to 00 … 001) from the ideal (AGND + 1 LSB).

On Resistance
On resistance is a measure of the ohmic resistance between the drain and the source of the switch drivers.

THEORY OF OPERATION

The AD7879/AD7889 are a complete 12-bit data acquisition system for digitizing positional inputs from a 4-wire resistive touch screen. To support this function, data acquisition on the AD7879/AD7889 is highly programmable to ensure accurate and noise free results from the touch screen.

The core of the AD7879/AD7889 is a high speed, low power, 12-bit ADC with an input multiplexer, on-chip track-and-hold, and an on-chip clock. Conversion results are stored in on-chip result registers. Compare the results from the auxiliary input or the battery input with high and low limits stored in the limit registers to generate an out of limit interrupt ($\overline{\text{INT}}$).

The AD7879/AD7889 also contain low resistance analog switches to switch the X and Y excitation voltages to the touch screen and to the on-chip temperature sensor. The high speed SPI serial bus provides control of the devices, as well as communication with the devices. The AD7879-1/AD7889-1 are available with an I^2C interface.

Operating from a single supply from 1.6 V to 3.6 V, the AD7879/AD7889 offer a throughput rate of 105 kHz. The device is available in a 1.6 mm × 2 mm, 12-ball wafer level chip scale package (WLCSP) and in a 4 mm × 4 mm, 16-lead, lead frame chip scale package (LFCSP).

The AD7879/AD7889 have an on-chip sequencer that schedules a sequence of preprogrammed conversions. The conversion sequence starts automatically when the screen is touched or at preset intervals, using the on-board timer.

To ensure that the AD7879/AD7889 work well with different touch screens, the user is able to select the acquisition time. A programmable delay ensures that the voltage on the touch screen settles before a measurement is taken.

To reduce noise in the system, the ADC takes up to 16 conversion results from each channel and writes the average of the results to the register. If there is noise present in the system, use the median filter to improve the performance of the AD7879/AD7889.

TOUCH SCREEN PRINCIPLES

A 4-wire touch screen consists of two flexible, transparent, resistive coated layers typically separated by a small air gap (see Figure 22). The X layer has conductive electrodes running down the left and right edges, allowing the application of an excitation voltage across the X layer from left to right.

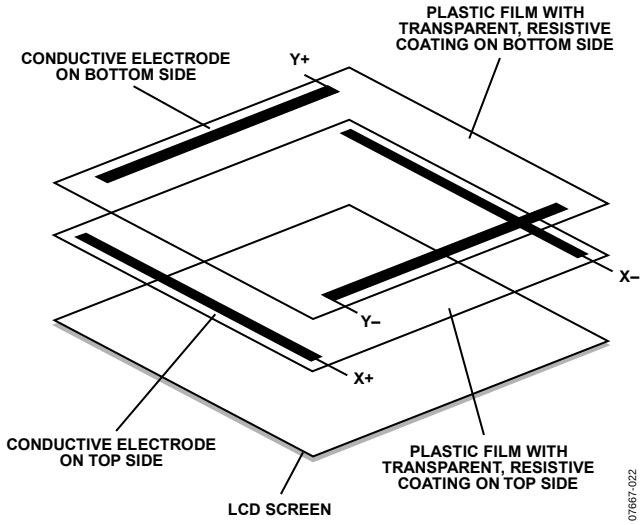


Figure 22. Basic Construction of a Touch Screen

The Y layer has conductive electrodes running along the top and bottom edges, allowing the application of an excitation voltage down the Y layer from top to bottom.

Provided that the layers are of uniform resistivity, the voltage at any point between the two electrodes is proportional to the horizontal position for the X layer and the vertical position for the Y layer.

When the screen is touched, the two layers make contact. If only the X layer is excited, the voltage at the point of contact and, therefore, the horizontal position, can be sensed at one of the Y layer electrodes. Similarly, if only the Y layer is excited, the voltage and, therefore, the vertical position, can be sensed at one of the X layer electrodes. By switching alternately between X and Y excitation and measuring the voltages, the X and Y coordinates of the contact point can be determined.

In addition to measuring the X and Y coordinates, it is also possible to estimate the touch pressure by measuring the contact resistance between the X and Y layers. The AD7879/AD7889 facilitate this measurement.

Figure 23 shows an equivalent circuit of the analog input structure of the AD7879/AD7889, including the touch screen switches, the main analog multiplexer, the ADC, and the dual 3 to 1 multiplexer that selects the reference source for the ADC.

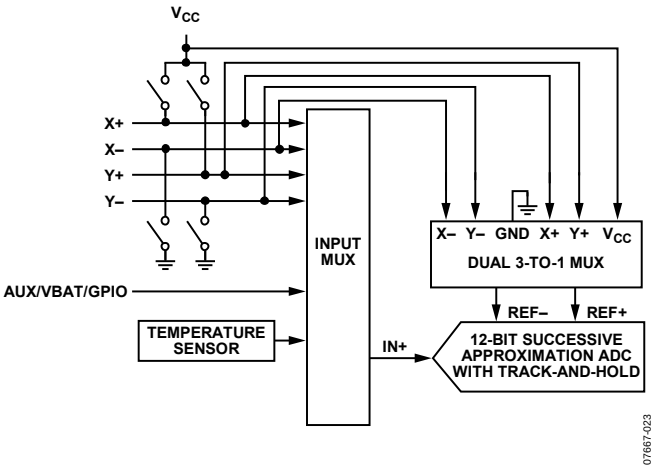


Figure 23. Analog Input Structure

The AD7879/AD7889 can be set up to automatically convert either specific input channels or a sequence of channels. The results of the ADC conversions are stored in the result registers.

When measuring the ancillary analog inputs (AUX, TEMP, or VBAT), the ADC uses a V_{CC} reference and the measurement is referred to GND.

MEASURING TOUCH SCREEN INPUTS

When measuring the touch screen inputs, it is possible to use V_{CC} as a reference or instead to use the touch screen excitation voltage as the reference and to perform a ratiometric, differential measurement. The differential method is the default method and is selected by clearing the SER/$\overline{\text{DFR}}$ bit (Bit 9 in Control Register 2) to 0. The single-ended method is selected by setting this bit to 1.

Single-Ended Method

Figure 24 shows the single-ended method for the Y position. For the X position, the excitation voltage is applied to X+ and X– and the voltage is measured at Y+.

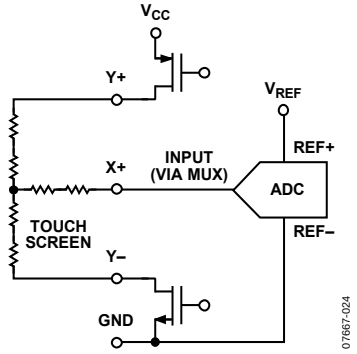


Figure 24. Single-Ended Conversion of Touch Screen Inputs

The voltage seen at the input to the ADC in Figure 24 is

$$V_{IN} = V_{CC} \times \frac{R_{Y-}}{R_{YTOTAL}} \quad (1)$$

The advantage of the single-ended method is that the touch screen excitation voltage is switched off when the signal is acquired. Because a screen can draw over 1 mA, this is a significant consideration for a battery-powered system.

The disadvantage of the single-ended method is that voltage drops across the switches can introduce errors. Touch screens can have a total end-to-end resistance ranging from 200 Ω to 900 Ω. By taking the lowest screen resistance of 200 Ω and a typical switch resistance of 14 Ω, the user can reduce the apparent excitation voltage to 200/228 × 100 = 87% of its actual value. In addition, the voltage drop across the low-side switch adds to the ADC input voltage. This introduces an offset into the input voltage; thus, it can never reach 0.

Ratiometric Method

The ratiometric method illustrated in Figure 25 shows the negative input of the ADC reference connected to Y– and the positive input connected to Y+. Thus, the screen excitation voltage provides the reference for the ADC. The input of the ADC is connected to X+ to determine the Y position.

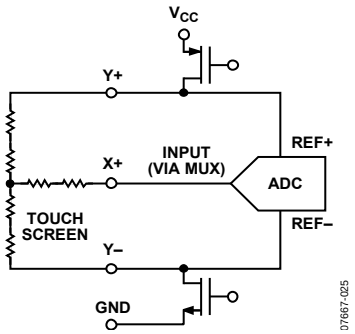


Figure 25. Ratiometric Conversion of Touch Screen Inputs

For greater accuracy, the ratiometric method has two significant advantages. One is that the reference to the ADC is provided from the actual voltage across the screen; therefore, any voltage dropped across the switches has no effect. The other advantage is that because the measurement is ratiometric, it does not matter if the voltage across the screen varies in the long term. However, it must not change after the signal has been acquired.

The disadvantage of the ratiometric method is that the screen must be powered up at all times because it provides the reference voltage for the ADC.

TOUCH PRESSURE MEASUREMENT

The pressure applied to the touch screen by a pen or a finger can also be measured with the AD7879/AD7889 by using simple calculations. The contact resistance between the X and Y plates is measured, providing a good indication of the size of the depressed area and, therefore, the applied pressure. The area of the spot that is touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

First Method for Calculating the Size of R_{TOUCH}

The first method for calculating R_{TOUCH} requires the user to know the total resistance of the X-plate tablet (R_X). Three touch screen conversions are required: the measurement of the X position, $X_{POSITION}$ (Y+ input); the measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z1 measurement); and the measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z2 measurement). These three measurements are shown in Figure 26.

The AD7879/AD7889 has two special ADC channel settings that configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The Z1 measurement is selected by setting the CHNL ADD[2:0] bits to 101 in Control Register 1 (Address 0x01); the result is stored in the X+ (Z1) result register (Address 0x0A). The Z2 measurement is selected by setting the CHNL ADD[2:0] bits to 100 in Control Register 1 (Address 0x01); the result is stored in the Y− (Z2) result register (Address 0x0B).

The touch resistance (R_{TOUCH}) can then be calculated using Equation 2:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION}/4096) \times ((Z2/Z1) - 1) \quad (2)$$

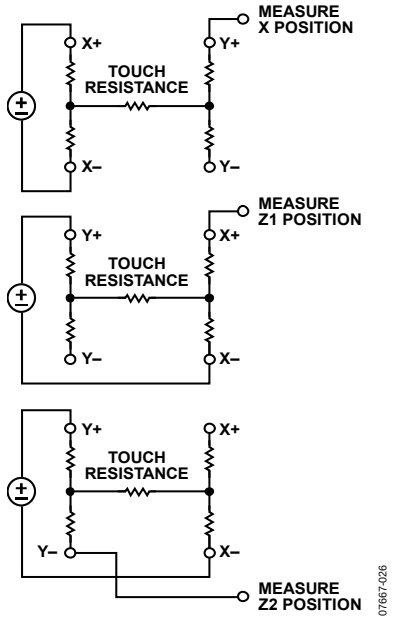


Figure 26. Three Measurements Required for Touch Pressure

Second Method for Calculating the Size of R_{TOUCH}

The second method for calculating R_{TOUCH} requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position.

Equation 3 also calculates the touch resistance (R_{TOUCH}):

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times ((4096/Z1) - 1) - R_{YPLATE} \times (1 - (Y_{POSITION}/4096)) \quad (3)$$

TEMPERATURE MEASUREMENT

A temperature measurement option called the single-conversion method is available on the AD7879/AD7889. The conversion method requires only a single measurement on ADC Channel 001. The results are stored in the temperature conversion result register (Address 0x0D). The AD7879/AD7889 do not provide an explicit output of the temperature reading; the system must perform some external calculations. This method is based on an on-chip diode measurement.

The acquisition time is fixed at 16 ms for temperature measurement.

Conversion Method

The conversion method makes use of the fact that the temperature coefficient of a silicon diode is approximately −2.1 mV/°C. However, this small change is superimposed on the diode forward voltage, which can have a wide tolerance. Therefore, it is necessary to calibrate by measuring the diode voltage at a known temperature to provide a baseline from which the change in forward voltage with temperature can be measured. This method provides a resolution of approximately 0.3°C and a predicted accuracy of ±2°C.

The temperature limit comparison is performed on the result in the temperature conversion result register (Address 0x0D), which is the measurement of the diode forward voltage. The values programmed into the high and low limits should be referenced to the calibrated diode forward voltage to make accurate limit comparisons.

Temperature Calculations

If an explicit temperature reading in degrees Celsius is required, calculate for the single measurement method as follows:

1. Calculate the scale factor of the ADC in degrees per LSB.

   Degrees per LSB = ADC LSB size/−2.1 mV = (V_{CC}/4096)/−2.1 mV
2. Save the ADC output, D_{CAL}, at the calibration temperature, T_{CAL}.
3. Take the ADC reading, D_{AMB}, at the temperature to be measured, T_{AMB}.
4. Calculate the difference in degrees between T_{CAL} and T_{AMB} by

   $\Delta T = (D_{AMB} - D_{CAL}) \times degrees\ per\ LSB$
5. Add ΔT to T_{CAL}.

Example

Using V_{CC} = 2.5 V as reference,

$Degrees\ per\ LSB = (2.5/4096)/-2.1 \times 10^{-3} = -0.291$

The ADC output is 983 decimal at 25°C, equivalent to a diode forward voltage of 0.6 V.

The ADC output at T_{AMB} is 880.

$\Delta T = (880 - 983) \times -0.291 = 30°C$

$T_{AMB} = 25 + 30 = 55°C$

MEDIAN AND AVERAGING FILTERS

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements.

The AD7879/AD7889 contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading.

The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter.

The median filter suppresses the isolated out of range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Bit 6 and Bit 5 in Control Register 2 (MED1 and MED0, respectively) set the window of the median filter and, therefore, the number of measurements taken.

Table 8. Median Filter Size

MED1	MED0	Number of Measurements
0	0	Median filter disabled
0	1	4
1	0	8
1	1	16

The averaging filter size determines the number of values to average. Bit 8 and Bit 7 in Control Register 2 (AVG1, AVG0) set the average to 2, 4, 8, or 16 samples. Only the final averaged result is written into the result register.

Table 9. Averaging Filter Size

AVG1	AVG0	Filter Size
0	0	Average of 2 middle samples
0	1	Average of 4 middle samples
1	0	Average of 8 middle samples
1	1	Average of 16 samples

When both filter values are 00, only one measurement is transferred to the register map.

The number specified with the MED1 and MED0 settings must be greater than or equal to the number specified with the AVG1 and AVG0 settings. If both settings specify the same number, the median filter is switched off.

Table 10. Median Averaging Filters (MAVF) Settings

Setting	Function
M = A	Median filter is disabled; output is the average of A converted results
M > A	Output is the average of the middle A values from the array of M measurements
M < A	Not possible because the median filter size is always larger than the averaging window size

Example

In this example, MED1, MED0 = 11 and AVG1, AVG0 = 10; the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array.

The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.

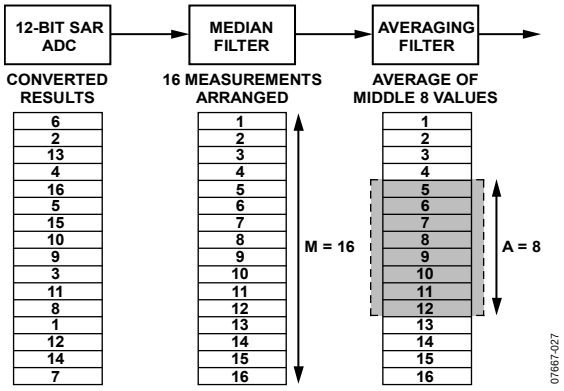


Figure 27. Median and Averaging Filter Example

It takes approximately 2 µs to sort the data in the rank filter (t_{SORT} in Figure 33); t_{SORT} adds to the update rate of the AD7879.

AUX/VBAT/GPIO PIN

The AUX/VBAT/GPIO pin on the AD7879/AD7889 can be programmed as an auxiliary input to the ADC, as a battery monitoring input or as a GPIO. To select the auxiliary measurement, set the ADC channel address to 011 (Bits[14:12] in Control Register 1, Address 0x01). To select a battery measurement, set the ADC channel address to 010. To select the GPIO function, set Bit 13 in Control Register 2 (Address 0x02) to 1.

AUXILIARY INPUT

The AD7879/AD7889 have an auxiliary analog input, AUX. When the auxiliary input function is selected, the signal on the AUX pin (AUX/VBAT/GPIO) is connected directly to the ADC input. This channel has a full-scale input range from 0 V to V_{CC}. The ADC channel address for AUX is 011 (Bits[14:12] in Control Register 1, Address 0x01), and the result is stored in the AUX/VBAT result register (Address 0x0C).

BATTERY INPUT

The AD7879/AD7889 can monitor battery voltages from 0.5 V to 5 V when the BAT measurement is selected. Figure 28 shows a block diagram of a battery voltage monitored through the VBAT pin. The voltage to the V_{CC} pin (V_{CC}/REF) of the AD7879/AD7889 is maintained at the desired supply voltage via the dc-to-dc converter, and the input to the converter is monitored. This voltage on VBAT is divided by 4 internally, so that a 5 V battery voltage is presented to the ADC as 1.25 V. To conserve power, the divider circuit is on only during the sampling of a voltage on VBAT. Note that the possible maximum input is 5 V.

The ADC channel address for VBAT is 010 (Bits[14:12] in Control Register 1, Address 0x01), and the result is stored in the AUX/VBAT result register (Address 0x0C).

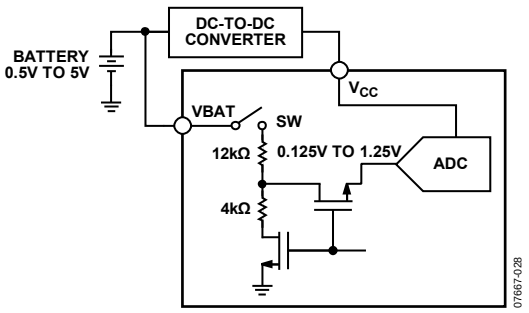


Figure 28. Block Diagram of Battery Measurement Circuit

The maximum battery voltage that the AD7879/AD7889 can measure changes when a different reference voltage is used. The maximum voltage that is measurable is $V_{CC} \times 4$ because this voltage gives a full-scale output from the ADC. Calculate the battery voltage using the following formula:

$$VBAT\ (V) = ((Register\ Value) \times V_{CC} \times 4)/4095$$

LIMIT COMPARISON

The AUX measurement and the battery measurement can be compared with high and low limits stored on chip. An out of limit result generates an alarm output at the $\overline{INT}$ pin ($\overline{PENIRQ}$/$\overline{INT}$/$\overline{DAV}$) when the $\overline{INT}$ function is enabled. The high limit for both channels is stored in the AUX/VBAT high limit register (Address 0x04), and the low limit is stored in the AUX/VBAT low limit register (Address 0x05).

After a measurement from either AUX or VBAT is taken, it is compared with the high and low limits. The out of limit comparison sets a status bit in Control Register 3. Separate status bits for the high limit and the low limit indicate which limit was exceeded. The interrupt sources can be masked by clearing the corresponding enable bit in Control Register 3.

GPIO

The AD7879/AD7889 have one general-purpose logic input/output pin, GPIO (AUX/VBAT/GPIO). To enable GPIO, set Bit 13 in Control Register 2 to 1. If this bit is set to 0, the AUX/VBAT function is active on the pin. If the GPIO is not enabled, the other GPIO configuration bits have no effect.

The GPIO data bit is Bit 12 in Control Register 2.

Direction (Bit 11, Control Register 2, Address 0x02)

Bit 11 sets the direction of the GPIO pin (AUX/VBAT/GPIO). When GPIO DIR = 0, the pin is an output. Setting or clearing the GPIO data bit (Bit 12 in Control Register 2) outputs a value on the GPIO pin.

When GPIO DIR = 1, the pin is an input. An input value on the GPIO pin sets or clears the GPIO data bit (Bit 12 in Control Register 2). GPIO data register bits are read-only when GPIO DIR = 1.

Polarity (Bit 10, Control Register 2, Address 0x02)

When GPIO POL = 0, the GPIO pin is active low. When GPIO POL = 1, the GPIO pin is active high. How this bit affects the GPIO operation also depends on the GPIO DIR bit.

If GPIO POL = 1 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data register bit to 1. A 0 at the input pin clears the corresponding GPIO data bit to 0.

If GPIO POL = 1 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 1 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 0 on the GPIO output pin.

If GPIO POL = 0 and GPIO DIR = 1, a 1 at the input pin sets the corresponding GPIO data bit to 0. A 0 at the input pin clears the corresponding GPIO data bit to 1.

If GPIO POL = 0 and GPIO DIR = 0, a 1 in the GPIO data register bit puts a 0 on the corresponding GPIO output pin. A 0 in the GPIO data register bit puts a 1 on the GPIO output pin.

GPIO Interrupt Enable (Bit 12, Control Register 3, Address 0x03)

The GPIO pin can operate as an interrupt source to trigger the $\overline{\text{INT}}$ output. This is controlled by Bit 12 in Control Register 3.

If the GPIO ALERT interrupt enable bit is set to 0, the GPIO can trigger $\overline{\text{INT}}$. If this bit is set to 1, the GPIO cannot trigger $\overline{\text{INT}}$.

$\overline{\text{INT}}$ is asserted if the GPIO data register bit is set when the GPIO is configured as an input, provided that $\overline{\text{INT}}$ is enabled. $\overline{\text{INT}}$ is triggered only when the GPIO is configured as an input, that is, when GPIO DIR = 1.

$\overline{\text{INT}}$ is cleared only when the GPIO signal or the GPIO enable bit changes.

CONVERSION TIMING

Conversion timing or update rate is the rate at which the AD7879/AD7889 provides converted values from the ADC so that the XY positions in the touch screen can be updated. In other words, the update rate is the timing required to give valid measurements in the sequencer.

Figure 29 shows conversion timing for a conversion sequence.

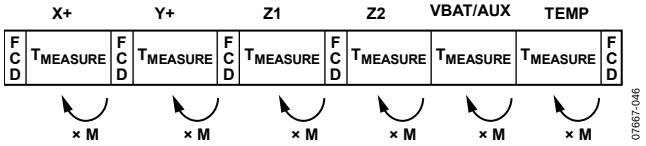


Figure 29. Conversion Timing Sequence

FCD is required before each touch screen measurement (X+, Y+, Z1, and Z2). This time is required to allow the screen inputs to settle before converting. If the sequence does not contain any screen channel (VBAT, AUX, or TEMP), only one FCD is added at the start of the sequence. At the end of the sequence, there is always another FCD.

$T_{MEASURE}$ is the time required to perform one measurement in the conversion sequence.

$$T_{MEASURE} = (ACQ\ (2\ \mu s, 4\ \mu s, 8\ \mu s, 16\ \mu s) + T_{CONV}\ (7.5\ \mu s) + T_{SORT}\ (2\ \mu s))$$

where:
ACQ is the acquisition time which is programmable in Control Register 1. For temperature measurements, ACQ is fixed at 16 µs.
T_{CONV} (typical ADC conversion time) is specified at 7.5 µs.
T_{SORT} is the time needed to sort the new sample within the median filter array. The T_{SORT} value is approximately 2 µs. If a median filter is not used (MED =0), the T_{SORT} value is 0.

$$T_{MEASURE\_MIN} = 9.5\ \mu s\ (ACQ = 2\ \mu s, \text{no median filter})$$

Conversion time per channel depends on the number of samples to be converted. The number of samples is programmed using the following median filter settings:

$$T_{CHANNEL} = T_{MEASURE} \times MED$$

$$T_{CHANNEL\_MIN} = 9.5\ \mu s\ (ACQ = 2\ \mu s, MED = 0)$$

$$T_{CHANNEL\_MAX} = 376\ \mu s\ (ACQ = 16\ \mu s, MED = 16)$$

$$Update\ Rate = (FCD + (T_{MEASURE} \times MED)) \times N + FCD + TMR$$

where:
MED = median filter setting (1, 4, 8, 16).
N = number of channels to be measured (1 to 6).
TMR = timer setting (0 µs to 9.4 ms).

The total update rate depends on the median filter settings and the number of channels in the conversion sequence. The timer setting (TMR) allows the user more flexibility to program the update rate.

For example, if

ACQ = 4 µs

MED = 8

N = 2

FCD = 1.024 ms

TMR = 620 µs

$T_{MEASURE}$ = 4 + 7.5 + 2 = 13.5 µs

$T_{CHANNEL}$ = (13.5 × 8) = 108 µs

Then, Update Rate = (1024 + 108) × 2 + 1024 + 620 = 3.9 ms

REGISTER MAP

Table 11. Register Table

Address[1]	Register Name	Description	Default Value	Type
0x00	Unused	Unused	0x0000	R/$\overline{W}$
0x01	Control Register 1	Pen interrupt enable, channel selection for manual conversion, ADC mode, acquisition time, and conversion timer	0x0000	R/$\overline{W}$
0x02	Control Register 2	ADC power management, GPIO control, pen interrupt mode, averaging, median filter, software reset, and FCD	0x4040	R/$\overline{W}$
0x03	Control Register 3	Status of high/low limit comparisons for TEMP and AUX/VBAT, and enable bits to allow them to become interrupts; channel selection for slave/master mode	0x0000	R/$\overline{W}$
0x04	AUX/VBAT high limit	AUX/VBAT high limit for comparison	0x0000	R/$\overline{W}$
0x05	AUX/VBAT low limit	AUX/VBAT low limit for comparison	0x0000	R/$\overline{W}$
0x06	TEMP high limit	TEMP high limit for comparison	0x0000	R/$\overline{W}$
0x07	TEMP low limit	TEMP low limit for comparison	0x0000	R/$\overline{W}$
0x08	X+	X+ measurement for Y position	0x0000	R
0x09	Y+	Y+ measurement for X position	0x0000	R
0x0A	X+ (Z1)	X+ measurement for touch pressure calculation (Z1)	0x0000	R
0x0B	Y− (Z2)	Y− measurement for touch pressure calculation (Z2)	0x0000	R
0x0C	AUX/VBAT	AUX/VBAT voltage measurement	0x0000	R
0x0D	TEMP	Temperature conversion measurement	0x0000	R
0x0E	Revision and device ID	Revision and device ID	0x0379 (AD7879-1/AD7889-1)	R
			0x037A (AD7879/AD7889)	R

[1] Do not write to addresses outside the register map.

DETAILED REGISTER DESCRIPTIONS

All addresses and default values are expressed in hexadecimal.

Table 12. Control Register 1

Address	Bit Name	Data Bit	Description	Default Value
0x01	Disable $\overline{\text{PENIRQ}}$	15	Pen interrupt enable. 0 = $\overline{\text{PENIRQ}}$ is enabled. 1 = $\overline{\text{PENIRQ}}$ is disabled and $\overline{\text{INT}}$ is enabled.	0x0000
	CHNL ADD[2:0]	[14:12]	ADC channel address for manual conversion (ADC mode = 01). 111 = X+ input (Y position). 110 = Y+ input (X position). 101 = X+ (Z1) input for touch-pressure calculation. 100 = Y− (Z2) input (used for touch-pressure measurement). 011 = AUX input.[1] 010 = VBAT input.[1] 001 = temperature measurement. 000 = not applicable.	
	ADC MODE[1:0]	[11:10]	ADC mode. 00 = no conversion. 01 = single conversion.[2] 10 = conversion sequence (slave mode).[2] 11 = conversion sequence (master mode).	
	ACQ[1:0]	[9:8]	ADC acquisition time. 00 = 4 clock periods (2 µs). 01 = 8 clock periods (4 µs). 10 = 16 clock periods (8 µs). 11 = 32 clock periods (16 µs). Note that the acquisition time does not apply to the temperature sensor channels; the temperature channel has a constant settling time of 16 µs.	
	TMR[7:0]	[7:0]	Conversion interval timer. Starts at 550 µs (00000001) and continues to 9.440 ms (11111111) in steps of 35 µs (see Table 18). Note that, in slave mode, the conversion interval timer starts to count as soon as the conversion sequence is finished; in master mode, it starts to count again only if the screen remains touched. If the screen is released, the timer stops counting and, on the next screen touch, a conversion starts immediately.	

[1] If GPIO is enabled in Control Register 2 (Bit 13), AUX and VBAT are both ignored. If AUX and VBAT are both selected in Control Register 3 and GPIO is disabled, AUX is ignored and VBAT is measured.

[2] Note that these bits are cleared to 00 at the end of the conversion sequence if the conversion interval timer bits in Control Register 1 (Address 0x01) Bits[7:0] = 0x00 at the end of the conversion sequence.

Table 13. Control Register 2

Address	Bit Name	Data Bit	Description	Default Value
0x02	PM[1:0]	[15:14]	ADC power management. 00 = full shutdown; the ADC, oscillator, bias, and temperature sensor are all powered down. 01 = analog blocks to be powered down depend on the ADC mode. If ADC mode is master mode, the ADC, oscillator, bias, and temperature sensor are powered down and must wake up when the user touches the screen. If ADC mode is slave mode, the ADC and temperature sensor are powered down when not being used. They wake up automatically when required. The oscillator and bias are powered up because they are needed to measure time. This also applies to the single-conversion mode. 10 = ADC, bias, and oscillator are powered up continuously, irrespective of ADC mode. 11 = same as 01.	0x4040
	GPIO EN	13	GPIO enable. 0 = AUX/VBAT channel active. 1 = GPIO enabled on AUX/VBAT/GPIO pin.	
	GPIO DAT	12	GPIO data bit.	
	GPIO DIR	11	GPIO direction. 0 = output. 1 = input.	
	GPIO POL	10	GPIO polarity. 0 = GPIO pin is active low. 1 = GPIO pin is active high.	
	SER/$\overline{\text{DFR}}$	9	Selects normal (single-ended) or ratiometric (differential) conversion. 0 = ratiometric (differential). 1 = normal (single-ended).	
	AVG[1:0]	[8:7]	ADC averaging. 00 = 2 middle values averaged (one measurement when median filter is disabled). 01 = 4 middle values averaged. 10 = 8 middle values averaged. 11 = 16 values averaged.	
	MED[1:0]	[6:5]	Median filter size. 00 = median filter disabled. 01 = 4 measurements. 10 = 8 measurements. 11 = 16 measurements.	
	SW/RST	4	Software reset; digital logic is reset when this bit is set.	
	FCD[3:0]	[3:0]	ADC first conversion delay.[1] Starts at 128 µs (default) and continues to 4.096 ms in steps of 128 µs (see Table 22).	

[1] This delay occurs before conversion of the X and Y coordinate channels (including Z1 and Z2) to allow screen settling and before the first conversion to allow the ADC to power up.

Table 14. Control Register 3

Address	Bit Name	Data Bit	Description	Default Value
0x03	TEMP MASK	15	TEMP mask bit. 0 = temperature measurement is allowed to cause interrupt. 1 = temperature measurement is not allowed to cause interrupt.	0x0000
	AUX/VBAT MASK	14	AUX/VBAT mask bit. 0 = AUX/VBAT measurement is allowed to cause interrupt. 1 = AUX/VBAT measurement is not allowed to cause interrupt.	
	INT MODE	13	$\overline{DAV}/\overline{INT}$ mode select. 0 = enable $\overline{DAV}$ mode. 1 = enable $\overline{INT}$ mode. This bit overrides any mask bits associated with individual channels.	
	GPIO ALERT	12	GPIO interrupt enable. 0 = GPIO can cause an alert on the $\overline{INT}$ output. 1 = mask GPIO from causing an alert on the $\overline{INT}$ output.	
	AUX/VBAT LOW	11	1 = AUX/VBAT below low limit.	
	AUX/VBAT HIGH	10	1 = AUX/VBAT above high limit.	
	TEMP LOW	9	1 = TEMP below low limit.	
	TEMP HIGH	8	1 = TEMP above high limit.	
	X+	7	1 = include measurement of Y position (X+ input).	
	Y+	6	1 = include measurement of X position (Y+ input).	
	Z1	5	1 = include Z1 touch-pressure measurement (X+ input).	
	Z2	4	1 = include measurement of Z2 touch-pressure measurement (Y– input).	
	AUX	3	1 = include measurement of AUX channel.[1]	
	VBAT	2	1 = include measurement of battery monitor (VBAT).[1]	
	TEMP	1	1 = include temperature measurement.	
	Not used	0	Unused.	

[1] If GPIO is enabled in Control Register 2 (Bit 13), AUX and VBAT are both ignored. If AUX and VBAT are both selected and GPIO is disabled, AUX is ignored and VBAT is measured.

Table 15. Limit Registers

Address	Register Name	Data Bit	Description	Default Value
0x04	AUX/VBAT high limit	[15:0]	User-programmable AUX/VBAT high limit register	0x0000
0x05	AUX/VBAT low limit	[15:0]	User-programmable AUX/VBAT low limit register	0x0000
0x06	TEMP high limit	[15:0]	User-programmable TEMP high limit register	0x0000
0x07	TEMP low limit	[15:0]	User-programmable TEMP low limit register	0x0000

Table 16. Measurement Result Registers (Read Only)

Address	Register Name	Data Bits	Description	Default Value
0x08	X+	[15:0]	Measured X+ input with Y excitation (Y position)	0x0000
0x09	Y+	[15:0]	Measured Y+ input with X excitation (X position)	0x0000
0x0A	X+ (Z1)	[15:0]	Measured X+ input with X− and Y+ excitation (touch-pressure calculation Z1)	0x0000
0x0B	Y− (Z2)	[15:0]	Measured Y− input with X− and Y+ excitation (touch-pressure calculation Z2)	0x0000
0x0C	AUX/VBAT	[15:0]	AUX/VBAT voltage measurement	0x0000
0x0D	TEMP	[15:0]	Temperature conversion measurement	0x0000

Table 17. Revision and Device ID Register (Read Only)

Address	Data Bits	Description	Default Value
0x0E	[15:12]	Unused	0x0379 (AD7879-1/AD7889-1)
	[11:8]	Revision and device ID bits	0x037A (AD7879/AD7889)
	[7:0]	Device ID	

CONTROL REGISTERS

CONTROL REGISTER 1

Control Register 1 (Address 0x01) contains the ADC channel address and the ADC mode bits. It sets the acquisition time and the timer. It also contains a bit to disable the pen interrupt. Control Register 1 must always be the last register programmed prior to starting conversions. Its power-on default value is 0x0000. To change any parameter after conversion has begun, the device must first be put into ADC Mode 00. Make the changes, and then reprogram Control Register 1, ensuring that it is always the last register programmed before conversions begin.

Timer (Control Register 1, Bits[7:0])

The TMR bits in Control Register 1 set the conversion interval timer, which enables the ADC to perform a conversion sequence at regular intervals from 550 µs (00000001) up to 9.440 ms (11111111) in increments of 35 µs (see Table 18). The default value of these bits is 00000000, which enables the ADC to perform one conversion only.

In slave mode, the timer starts as soon as the conversion sequence is finished. In master mode, the timer starts at the end of a conversion sequence only if the screen remains touched. If the touch is released at any stage, the timer stops. The next time that the screen is touched, a conversion sequence begins immediately.

Table 18. Timer Selection

TMR[7:0]	Conversion Interval
00000000	Convert one time only (default)
00000001	Every 550 µs
00000010	Every 585 µs
00000011	Every 620 µs
…	…
11111101	Every 9.370 ms
11111110	Every 9.405 ms
11111111	Every 9.440 ms

Acquisition Time (Control Register 1, Bits[9:8])

The ACQ bits in Control Register 1 allow the selection of acquisition times for the ADC of 2 µs (default), 4 µs, 8 µs, or 16 µs. The user can program the ADC with an acquisition time suitable for the type of signal being sampled. For example, signals with large RC time constants can require longer acquisition times.

Table 19. Acquisition Time Selection

ACQ1	ACQ0	Acquisition Time
0	0	4 clock periods (2 µs)
0	1	8 clock periods (4 µs)
1	0	16 clock periods (8 µs)
1	1	32 clock periods (16 µs)

ADC Mode (Control Register 1, Bits[11:10])

The mode bits select the operating mode of the ADC. The AD7879/AD7889 have three operating modes. These modes are selected by writing to the mode bits in Control Register 1. If the mode bits are set to 00, no conversion is performed.

Table 20. Mode Selection

ADC MODE1	ADC MODE0	Function
0	0	Do not convert (default)
0	1	Single-channel conversion; the device is in slave mode
1	0	Sequence 0; the device is in slave mode
1	1	Sequence 1; the device is in master mode

If the mode bits are set to 01, a single conversion is performed on the channel selected by writing to the channel bits of Control Register 1 (Bits[14:12]). At the end of the conversion, if the TMR bits in Control Register 1 are set to 00000000, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a value other than 00000000 causes the conversion to be repeated.

The AD7879/AD7889 can also be programmed to automatically convert a sequence of selected channels. The two modes for this type of conversion are slave mode and master mode.

For slave mode operation, the channels to be digitized are selected by setting the corresponding bits in Control Register 3. Conversion is initiated by writing 10 to the mode bits of Control Register 1. The ADC then digitizes the selected channels and stores the results in the corresponding result registers. At the end of the conversion, if the TMR bits in Control Register 1 are set to 00000000, the mode bits revert to 00 and the ADC returns to no convert mode until a new conversion is initiated by the host. Setting the TMR bits to a value other than 00000000 causes the conversion sequence to be repeated.

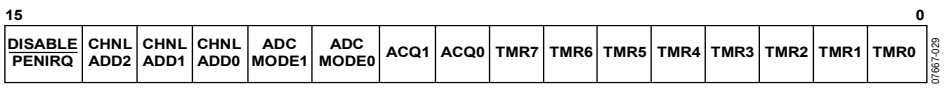


Figure 30. Control Register 1

For master mode operation, the channels to be digitized are written to Control Register 3. Master mode is then selected by writing 11 to the mode bits in Control Register 1. In this mode, the wake-up on touch feature is active; therefore, conversion does not begin immediately. The AD7879/AD7889 wait until the screen is touched before beginning the sequence of conversions. The ADC then digitizes the selected channels, and the results are written to the result registers. Before beginning another sequence of conversions, the AD7879/AD7889 wait for the screen to be touched again or for a timer event if the screen remains touched.

ADC Channel (Control Register 1, Bits[14:12])

The ADC channel address is selected by Bits[14:12] of Control Register 1 (CHNL ADD2 to CHNL ADD0). A complete list of channel addresses is given in Table 21.

For single-channel conversion, the channel address is selected by writing the appropriate code to the CHNL ADD2 to CHNL ADD0 bits in Control Register 1.

For sequential channel conversion, the channels to be converted are selected by setting the bits corresponding to the channel number in Control Register 3 for slave and master mode sequencing.

For both single-channel and sequential conversion, a normal conversion (single-ended) is selected by setting the SER/$\overline{\text{DFR}}$ bit in Control Register 2 (Bit 9). Ratiometric (differential) conversion is selected by clearing the SER/$\overline{\text{DFR}}$ bit.

$\overline{\text{PENIRQ}}$ Enable (Control Register 1, Bit 15)

The AD7879/AD7889 have a dual function output that performs as $\overline{\text{PENIRQ}}$ or $\overline{\text{INT}}$, depending on the pen interrupt enable bit (Bit 15 of Control Register 1). When this bit is set to 0, the pin functions as a pen interrupt and goes low whenever the screen is touched. When the pen interrupt enable bit is set to 1, the pen interrupt request is disabled and the pin functions as an interrupt when a measurement exceeds a preprogrammed limit ($\overline{\text{INT}}$).

Table 21. Codes for Selecting Input Channel and Normal or Ratiometric Conversion

Channel	SER/$\overline{\text{DFR}}$	CHNL ADD[2:0]	Analog Input	X Switches	Y Switches	REF+	REF−
0	0	111	X+ (Y position)	Off	On	Y+	Y−
1	0	110	Y+ (X position)	On	Off	X+	X−
2	0	101	X+ (Z1 touch pressure)	X+ off, X− on	Y+ on, Y− off	Y+	X−
3	0	100	Y− (Z2 touch pressure)	X+ off, X− on	Y+ on, Y− off	Y+	X−
4	0	011	AUX	Off	Off	V_{CC}	GND
5	0	010	VBAT	Off	Off	V_{CC}	GND
6	0	001	TEMP	Off	Off	V_{CC}	GND
	0	000	Invalid address				
7	1	111	X+ (Y position)	Off	On	V_{CC}	GND
8	1	110	Y+ (X position)	On	Off	V_{CC}	GND
9	1	101	X+ (Z1 touch pressure)	Off	Off	V_{CC}	GND
12	1	100	Y− (Z2 touch pressure)	Off	Off	V_{CC}	GND
13	1	011	AUX	Off	Off	V_{CC}	GND
14	1	010	VBAT	Off	Off	V_{CC}	GND
15	1	001	TEMP	Off	Off	V_{CC}	GND
	1	000	Invalid address				

CONTROL REGISTER 2

Control Register 2 (Address 0x02) contains the ADC power management bits, the GPIO settings, the SER/$\overline{\text{DFR}}$ bit (to choose the single-ended or differential method of touch screen measurement), the averaging and median filter settings, a bit that allows resetting of the device, and the first conversion delay bits. Its power-on default value is 0x4040. See the Detailed Register Descriptions section for more information about the control registers.

For information about the averaging and median filter settings, see the Median and Averaging Filters section. For information about the GPIO settings, see the GPIO section.

First Conversion Delay (Control Register 2, Bits[3:0])

The first conversion delay (FCD) bits in Control Register 2 program a delay from 128 µs (default) up to 4.096 ms before the first conversion to allow the ADC time to power up. This delay also occurs before conversion of the X and Y coordinate channels to allow extra time for screen settling, and after the last conversion in a sequence to precharge $\overline{\text{PENIRQ}}$.

Table 22. First Conversion Delay Selection

FCD[3:0]	Delay
0000	128 µs
0001	256 µs
0010	384 µs
0011	512 µs
0100	640 µs
0101	768 µs
0110	896 µs
0111	1.024 ms
1000	1.152 ms
1001	1.280 ms
1010	1.536 ms
1011	1.792 ms
1100	2.048 ms
1101	2.560 ms
1110	3.584 ms
1111	4.096 ms

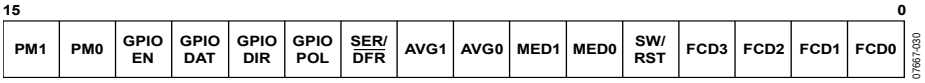


Figure 31. Control Register 2

Power Management (Control Register 2, Bits[15:14])

The power management (PM) bits in Control Register 2 allow the power management features of the ADC to be programmed (see Table 23). If the PM bits are set to 00, the ADC is in full shutdown. This setting overrides any setting of the mode bits in Control Register 1. Power management overrides the ADC modes.

Table 23. Power Management Selection

PM1	PM0	Function
0	0	Full shutdown; ADC, oscillator, bias, and temperature sensor are turned off. The only way to exit this mode is to write to the device over the serial interface and change the PM bits. This setting overrides any other setting on the device, including the ADC mode bits.
0	1	The analog blocks to be powered down depend on the ADC mode setting. In master mode, the ADC, bias, temperature sensor, and oscillator are powered down and must wake up when the user touches the screen. In slave mode, the ADC and temperature sensor are powered down when not being used. They wake up automatically when required. The oscillator and bias are powered up because they are needed to measure time. This setting also applies to the single-conversion mode.
1	0	The ADC, bias, and oscillator are powered up continuously, irrespective of ADC mode.
1	1	The analog blocks to be powered down depend on the ADC mode setting. In master mode, the ADC, bias, temperature sensor, and oscillator are powered down and must wake up when the user touches the screen. In slave mode, the ADC and temperature sensor are powered down when not being used. They wake up automatically when required. The oscillator and bias are powered up because they are needed to measure time. This setting also applies to the single-conversion mode.

CONTROL REGISTER 3

Control Register 3 (Address 0x03) includes the interrupt register (Bits[15:8]) and the sequencer bits (Bits[7:0]).

Sequencer (Control Register 3, Bits[7:0])

The sequencer bits control which channels are converted during a conversion sequence in both slave mode and master mode.

To include a measurement in a sequence, the relevant bit must be set in the sequence. Setting Bit 7 includes a measurement on the X+ channel (Y position). Setting Bit 6 includes a measurement on the Y+ channel (X position), and so on (see Table 14).

Figure 34 illustrates the correspondence between the bits in Control Register 3 and the various measurements. Bit 0 is not used.

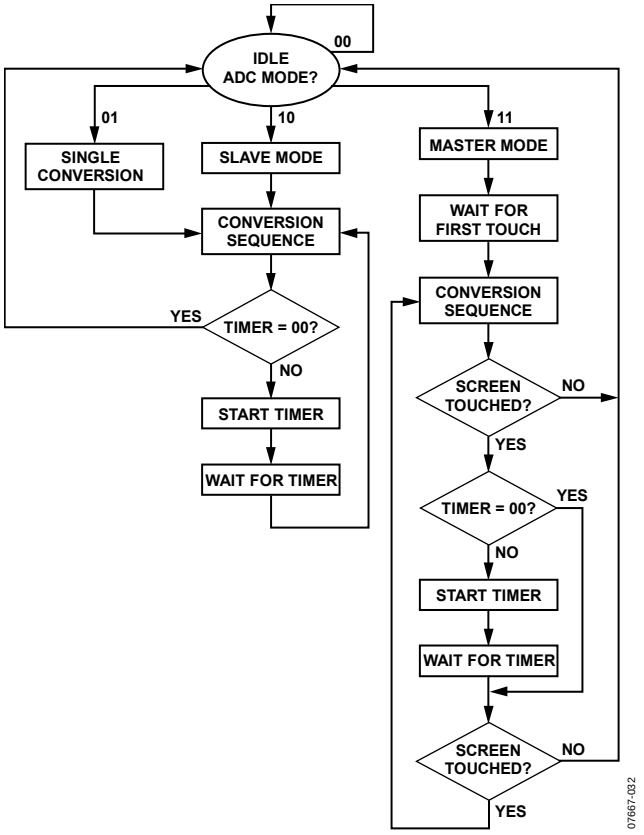


Figure 32. Conversion Modes

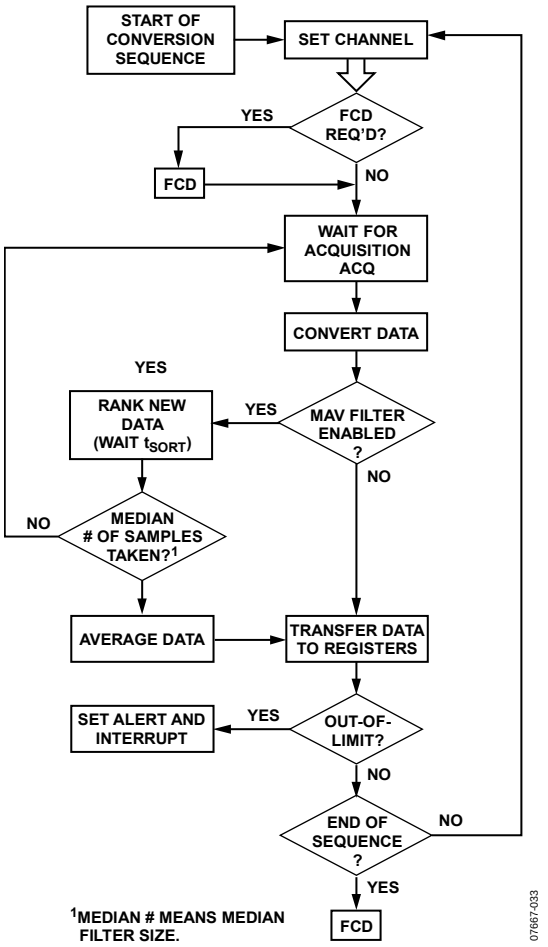


Figure 33. Conversion Sequence

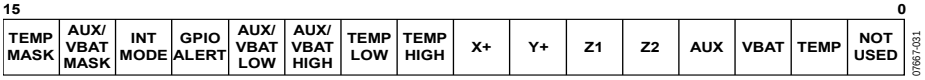


Figure 34. Control Register 3

INTERRUPTS

The AD7879/AD7889 have a dual function interrupt output, $\overline{INT}$, as well as a pen-down interrupt, $\overline{PENIRQ}$. The $\overline{INT}$ output can be configured as a data available interrupt ($\overline{DAV}$), as an out of limit interrupt ($\overline{INT}$), or as a GPIO interrupt.

$\overline{DAV}$—Data Available Interrupt

The behavior of the interrupt output is controlled by Bit 13 in Control Register 3. In default mode (Bit 13 = 0), $\overline{INT}$ operates as a data available interrupt ($\overline{DAV}$). When the AD7879/AD7889 finish a conversion or a conversion sequence, the interrupt is asserted to let the host know that new ADC data is available in the result registers.

While the ADC is idle or is converting, $\overline{DAV}$ is high. When the ADC finishes converting and new data has been written to the result registers, $\overline{DAV}$ goes low. Reading the result registers resets $\overline{DAV}$ to a high condition. $\overline{DAV}$ is also reset if a new conversion is started by the AD7879/AD7889 because the timer expired. The host reads the result registers only when $\overline{DAV}$ is low. To ensure correct operation of the $\overline{DAV}$ mode when using the SPI interface, it is necessary to write 0x0000 to Register 0x81 after a set of register reads. This write clears the internal data read signal.

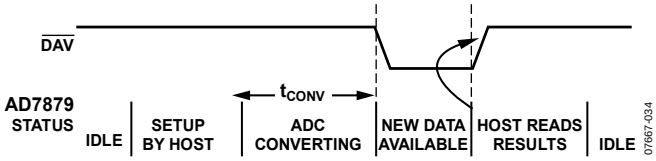


Figure 35. Operation of $\overline{DAV}$ Output

When the on-board timer is programmed to perform automatic conversions, limited time is available to the host to read the result registers before another sequence of conversions begins. The $\overline{DAV}$ signal is reset high when the timer expires, and the host should not access the result registers while $\overline{DAV}$ is high.

$\overline{INT}$—Out of Limit Interrupt

The $\overline{INT}$ pin operates as an alarm or interrupt output when Bit 13 in Control Register 3 (Address 0x03) is set to 1. The output goes low if any one of the interrupt sources is asserted. The results of high and low limit comparisons on the AUX, VBAT, and TEMP channels are interrupt sources. An out of limit comparison sets a status bit in the interrupt register. A separate status bit for the high limit and the low limit on each channel indicates which limit was exceeded. The interrupt sources can be masked by setting the corresponding enable bit in this register to 1. There is one enable bit per channel.

$\overline{PENIRQ}$—Pen Interrupt

The pen interrupt request output ($\overline{PENIRQ}$) goes low whenever the screen is touched and the $\overline{PENIRQ}$ enable bit is set to 0 (Control Register 1, Bit 15). When $\overline{PENIRQ}$ enable is set to 1, the pen interrupt request output is disabled.

The pen interrupt equivalent output circuitry is shown in Figure 36. This digital logic output has an internal 50 kΩ pull-up resistor, so it does not need an external pull-up. The $\overline{PENIRQ}$ output idles high, and the $\overline{PENIRQ}$ circuitry is always enabled in master mode (ADC mode = 11), except during conversions.

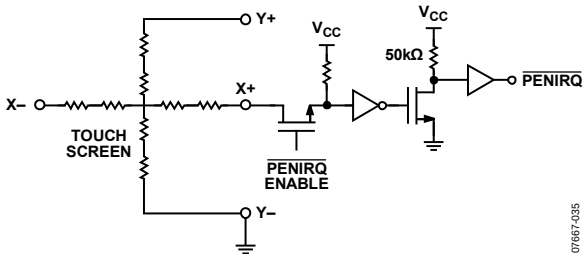


Figure 36. $\overline{PENIRQ}$ Output Equivalent Circuit

When the screen is touched, $\overline{PENIRQ}$ goes low. This generates an interrupt request to the host. When the screen touch ends, $\overline{PENIRQ}$ immediately goes high if the ADC is idle. If the ADC is converting, $\overline{PENIRQ}$ goes high when the ADC becomes idle. The $\overline{PENIRQ}$ operation for these two conditions is shown in Figure 37.

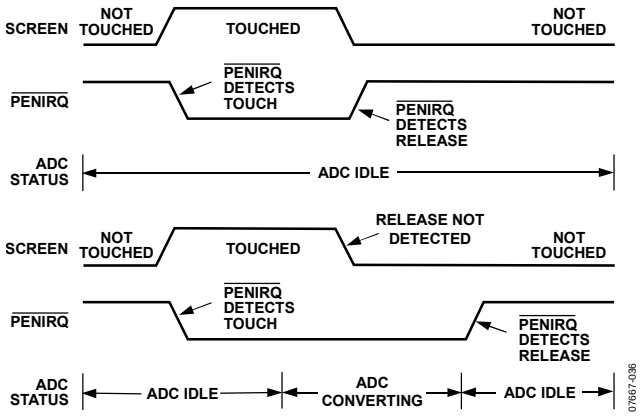


Figure 37. $\overline{PENIRQ}$ Operation for ADC Idle and ADC Converting

SYNCHRONIZING THE AD7879/AD7889 TO THE HOST CPU

The two methods for synchronizing the AD7879/AD7889 to the host CPU are slave mode (in which the mode bits are set to 01 or 10) and master mode (in which the mode bits set to 11).

In master mode (ADC mode bits = 11), $\overline{\text{PENIRQ}}$ can be used as an interrupt to the host. When $\overline{\text{PENIRQ}}$ goes low to indicate that the screen has been touched, the host is awakened. The host can then program the AD7879/AD7889 to convert in any mode and read the results after the conversions are completed.

In master mode, $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ can also be used as an interrupt to the host. The host must first define a conversion sequence in Control Register 3, initialize the AD7879/AD7889 in Mode 11, and enable $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ using Bit 15 in Control Register 1 and Bit 13 in Control Register 3. The host can then enter sleep mode to conserve power. The wake-up on touch feature of the AD7879/AD7889 is active in this mode; therefore, when the screen is touched, the programmed sequence of conversions automatically begins. When the $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ signal is asserted, the host reads the new data available in the AD7879/AD7889 result registers and returns to sleep mode. This method can significantly reduce the load on the host.

Figure 38 shows how the $\overline{\text{PENIRQ}}$ circuit is enabled. The wake-up on touch circuit and the $\overline{\text{PENIRQ}}$ circuit are enabled only in master mode (ADC mode = 11). In slave mode, the $\overline{\text{PENIRQ}}$/$\overline{\text{INT}}$/$\overline{\text{DAV}}$ pin can output only $\overline{\text{INT}}$ or $\overline{\text{DAV}}$ signals.

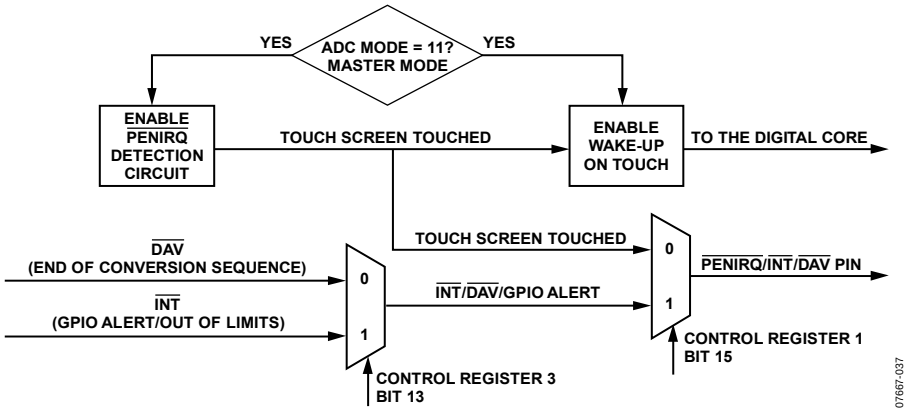


Figure 38. Master Mode Operation

SERIAL INTERFACE

The AD7879 and AD7879-1 (AD7889 and AD7889-1) differ only in the serial interface provided on the device. The AD7879 and the AD7889 are available with a serial peripheral interface (SPI). The AD7879-1 and the AD7889-1 are available with an I²C-compatible interface. It is recommended that addresses outside the register map not be written to.

SPI INTERFACE

The AD7879/AD7889 have a 4-wire SPI. The SPI has a data input pin (DIN) for inputting data to the device, a data output pin (DOUT) for reading data back from the device, and a data clock pin (SCL) for clocking data into and out of the device. A chip select pin ($\overline{CS}$) enables or disables the serial interface. $\overline{CS}$ is required for correct operation of the SPI interface. Data is clocked out of the AD7879/AD7889 on the falling edge of SCL, and data is clocked into the device on the rising edge of SCL.

SPI Command Word

All data transactions on the SPI bus begin with the master taking $\overline{CS}$ from high to low and sending out the command word. This indicates to the AD7879/AD7889 whether the transaction is a read or a write and gives the address of the register from which to begin the data transfer. The bit map in Table 24 shows the SPI command word.

Table 24. SPI Command Word

MSB						LSB
15	**14**	**13**	**12**	**11**	**10**	**[9:0]**
1	1	1	0	0	R/$\overline{W}$	Register address

Bits[15:11] of the command word must be set to 11100 to successfully begin a bus transaction.

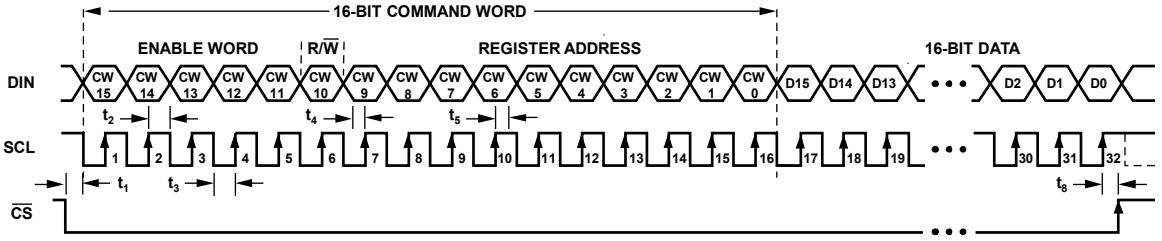
Bit 10 is the read/write bit; 1 indicates a read, and 0 indicates a write.

Bits[9:0] contain the target register address. When reading or writing to more than one register, this address indicates the address of the first register to be written to or read from.

Writing Data

Data is written to the AD7879/AD7889 in 16-bit words. The first word written to the device is the command word, with the read/write bit set to 0. The master then supplies the 16-bit input data-word on the DIN line. The AD7879/AD7889 clock the data into the register addressed in the command word. If there is more than one word of data to be clocked in, the AD7879/AD7889 automatically increment the address pointer and clocks the next data-word into the following register.

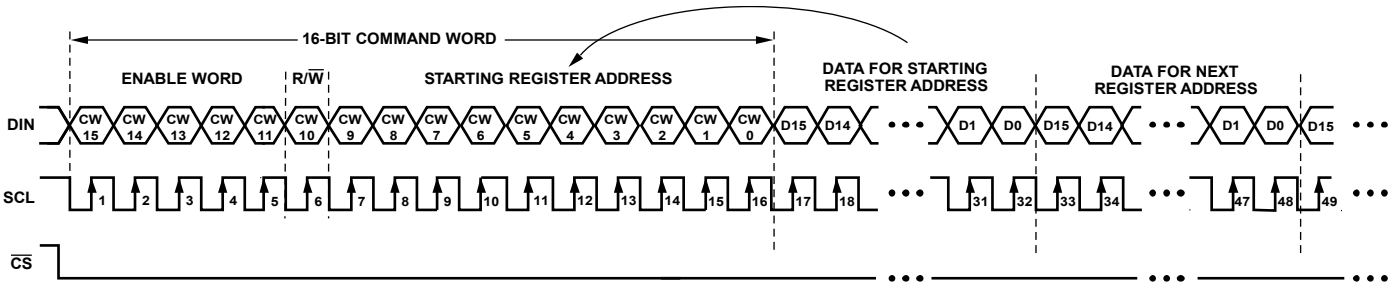
The AD7879/AD7889 continue to clock in data on the DIN line until the master ends the write transition by pulling $\overline{CS}$ high or until the address pointer reaches its maximum value. The AD7879/AD7889 address pointer does not wrap. When the address pointer reaches its maximum value, any data provided by the master on the DIN line is ignored by the AD7879/AD7889.



NOTES
1. DATA BITS ARE LATCHED ON SCL RISING EDGES. SCL CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 32 BITS MUST BE WRITTEN: 16 BITS FOR THE COMMAND WORD AND 16 BITS FOR DATA.
3. 16-BIT COMMAND WORD SETTINGS FOR SINGLE WRITE OPERATION:
CW[15:11] = 11100 (ENABLE WORD)
CW[10] = 0 (R/$\overline{W}$)
CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

07667-038

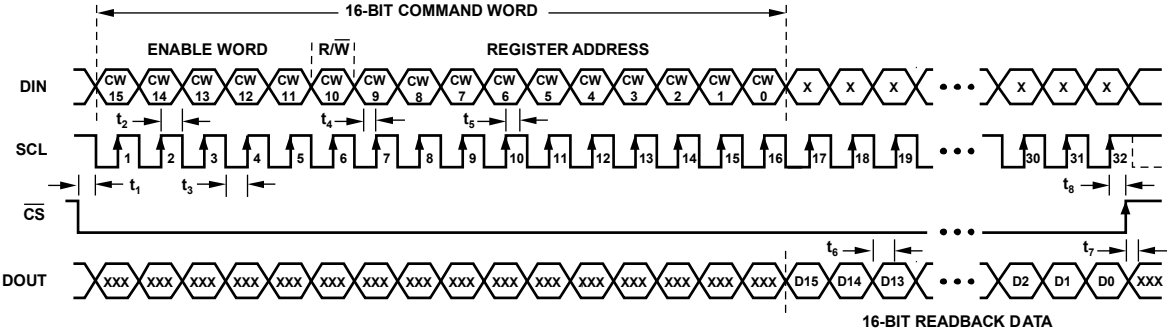
Figure 39. Single Register Write, SPI Timing



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS CAN BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 16-BIT DATA-WORDS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD (ALL 16 BITS MUST BE WRITTEN).
4. CS IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/W)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB JUSTIFIED REGISTER ADDRESS)

07667-039

Figure 40. Sequential Register Write, SPI Timing



NOTES
1. DATA BITS ARE LATCHED ON SCL RISING EDGES. SCL CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. THE 16-BIT COMMAND WORD MUST BE WRITTEN ON DIN: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/W, AND 10 BITS FOR REGISTER ADDRESS.
3. THE REGISTER DATA IS READ BACK ON THE DOUT PIN.
4. X DENOTES DON'T CARE.
5. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
6. CS IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
7. 16-BIT COMMAND WORD SETTINGS FOR SINGLE READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/W)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB JUSTIFIED REGISTER ADDRESS)

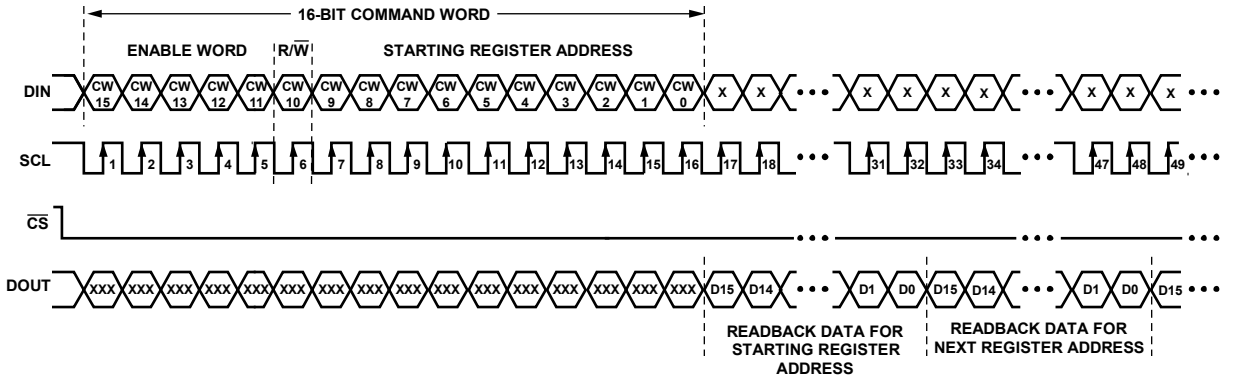
07667-040

Figure 41. Single Register Readback, SPI Timing

Reading Data

A read transaction begins when the master writes the command word to the AD7879/AD7889 with the read/write bit set to 1. The master then supplies 16 clock pulses per data-word to be read, and the AD7879/AD7889 clock out data from the addressed register on the DOUT line. The first data-word is clocked out on the first falling edge of SCL following the command word, as shown in Figure 41.

The AD7879/AD7889 continue to clock out data on the DOUT line, provided that the master continues to supply the clock signal on SCL. The read transaction ends when the master takes CS high. If the AD7879/AD7889 address pointer reaches its maximum value, the AD7879/AD7889 repeatedly clock out data from the addressed register. The address pointer does not wrap.



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS CAN BE READ BACK CONTINUOUSLY.
2. THE 16-BIT COMMAND WORD MUST BE WRITTEN ON DIN: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/$\overline{W}$, AND 10 BITS FOR REGISTER ADDRESS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD BEING READ BACK ON THE DOUT PIN.
4. $\overline{CS}$ IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
5. X DENOTES DON'T CARE.
6. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
7. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB JUSTIFIED REGISTER ADDRESS)

Figure 42. Sequential Register Readback, SPI Timing

I²C-COMPATIBLE INTERFACE

The AD7879-1/AD7889-1 support the industry standard 2-wire I²C serial interface protocol. The two wires associated with the I²C timing are the SCL and SDA inputs. SDA is an input output pin that allows both register write and register readback operations. The AD7879-1/AD7889-1 are always a slave device on the I²C serial interface bus.

The devices have a 7-bit device address, Address 0101 1XX. The lower two bits are set by tying the ADD0 and ADD1 pins high or low. The AD7879-1/AD7889-1 respond when the master device sends the device address over the bus. The AD7879-1/AD7889-1 cannot initiate data transfers on the bus.

Table 25. I²C Device Addresses for the AD7879-1/AD7889-1

ADD1	ADD0	I²C Address
0	0	0101 100
0	1	0101 101
1	0	0101 110
1	1	0101 111

Data Transfer

Data is transferred over the I²C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows.

All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus then remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in a sequence of nine clock pulses (eight bits of data followed by an acknowledge bit from the slave device). Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If the AD7879-1/AD7889-1 encounter a stop condition, they return to the idle condition.

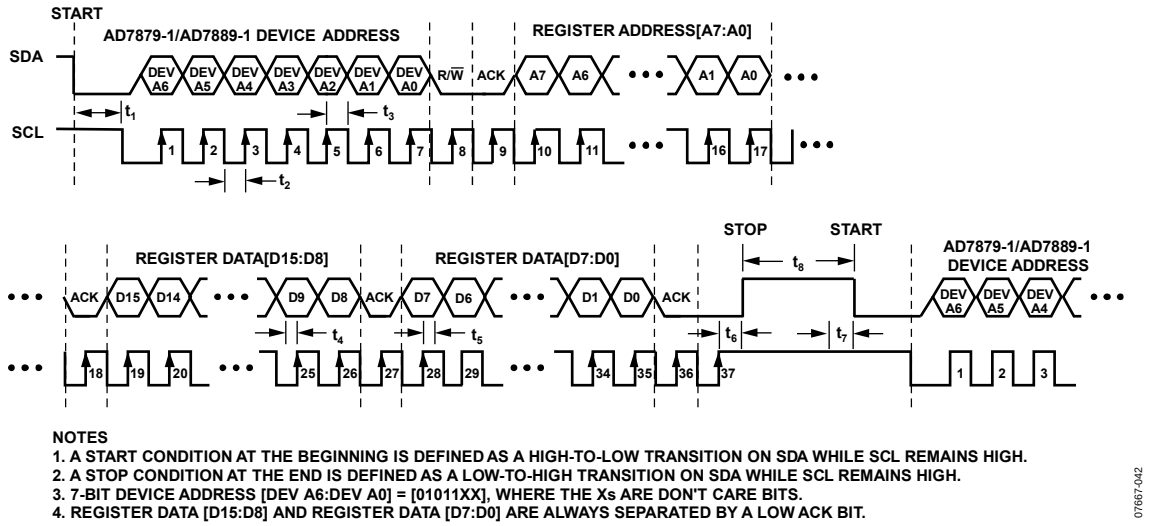


Figure 43. Example of I²C Timing for Single Register Write Operation

Writing Data over the I²C Bus

The process of writing to the AD7879-1/AD7889-1 over the I²C bus is shown in Figure 43 and Figure 45. The device address is sent over the bus followed by the R/$\overline{W}$ bit set to 0. This is followed by one byte of data that contains the 8-bit address of the internal data register to be written. The bit map in Table 26 shows the register address byte.

Table 26. I²C Register Address Byte

MSB							LSB
7	6	5	4	3	2	1	0
Register Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The third data byte contains the eight MSBs of the data to be written to the internal register. The fourth data byte contains the eight LSBs of data to be written to the internal register.

The AD7879-1/AD7889-1 address pointer register automatically increments after each write. This allows the master to sequentially write to all registers on the AD7879-1/AD7889-1 in the same write transaction. However, the address pointer register does not wrap after the last address.

Any data written to the AD7879-1/AD7889-1 after the address pointer has reached its maximum value is discarded.

All registers on the AD7879-1/AD7889-1 have 16 bits. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

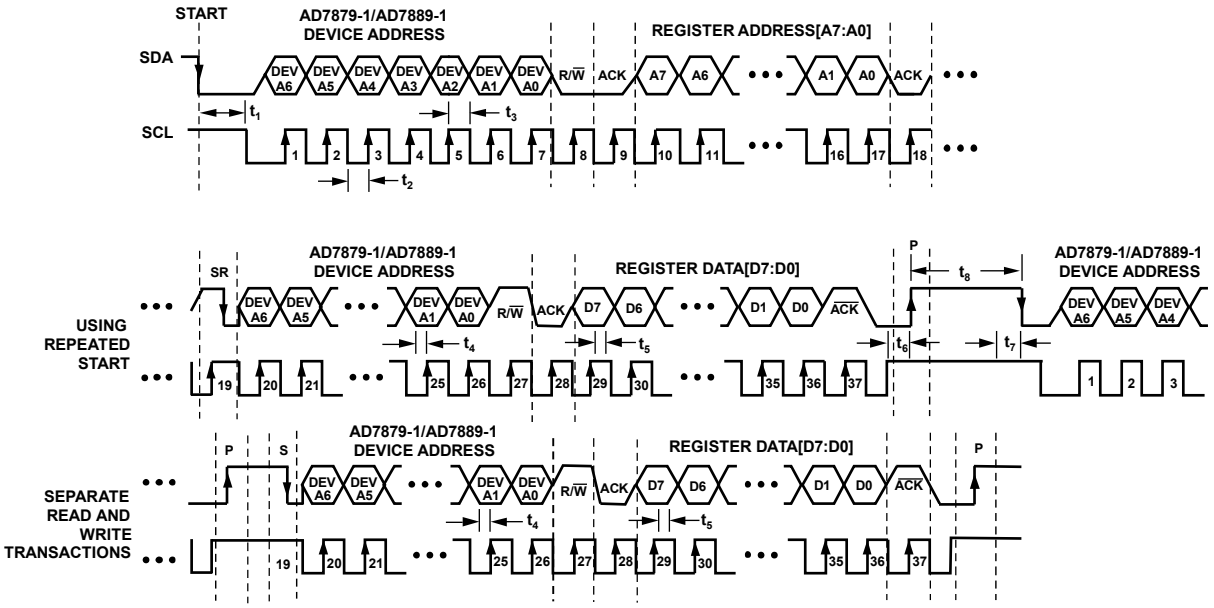
To end the transaction, the master generates a stop condition on SDA, or it generates a repeat start condition if the master is to maintain control of the bus.

Reading Data over the I²C Bus

To read from the AD7879-1/AD7889-1, the address pointer register must first be set to the address of the required internal register. The master performs a write transaction and writes to the AD7879-1/AD7889-1 to set the address pointer. The master then outputs a repeat start condition to keep control of the bus or, if this is not possible, the master ends the write transaction with a stop condition. A read transaction is initiated, with the R/$\overline{W}$ bit set to 1.

The AD7879-1/AD7889-1 supply the upper eight bits of data from the addressed register in the first readback byte, followed by the lower eight bits in the next byte. This is shown in Figure 44 and Figure 45.

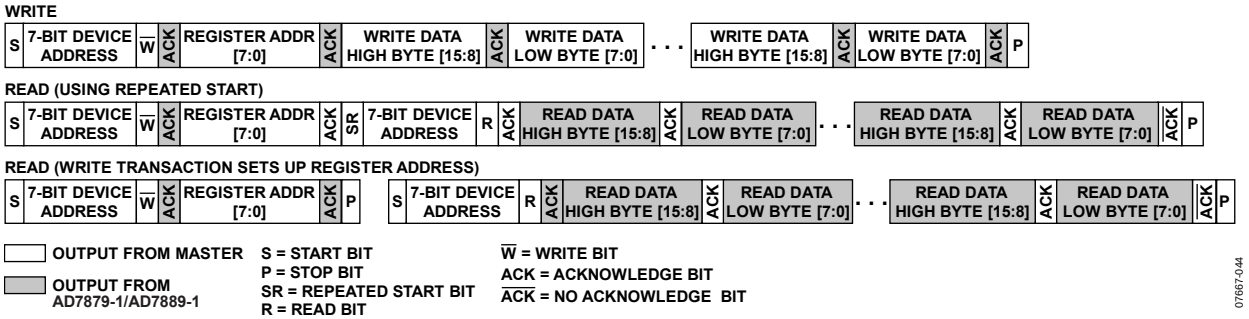
Because the address pointer automatically increments after each read, the AD7879-1/AD7889-1 continue to output readback data until the master puts a no acknowledge and a stop condition on the bus. If the address pointer reaches its maximum value and the master continues to read from the device, the AD7879-1/AD7889-1 repeatedly send data from the last register addressed.



NOTES
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCL REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCL REMAINS HIGH.
3. THE MASTER GENERATES THE $\overline{ACK}$ AT THE END OF THE READBACK TO SIGNAL THAT IT DOES NOT WANT ADDITIONAL DATA.
4. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [01011XX], WHERE THE TWO LSB Xs ARE DON'T CARE BITS.
5. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
6. THE R/$\overline{W}$ BIT IS SET TO 1 TO INDICATE A READBACK OPERATION.

07667-043

Figure 44. Example of I²C Timing for Single Register Readback Operation



07667-044

Figure 45. Example of Sequential I²C Write and Readback Operation

GROUNDING AND LAYOUT

For detailed information on grounding and layout considerations for the AD7879/AD7889, refer to the AN-577 Application Note, *Layout and Grounding Recommendations for Touch Screen Digitizers*.

LEAD FRAME CHIP SCALE PACKAGES

The lands on the lead frame chip scale package (CP-16-20) are rectangular. The printed circuit board (PCB) pad for these lands should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad to maximize the solder joint size.

The bottom of the lead frame chip scale package has a central thermal pad. The thermal pad on the PCB should be at least as large as this exposed pad. To avoid shorting, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the land pattern on the PCB. Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, incorporate them into the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. of copper to plug the via.

Connect the PCB thermal pad to GND.

WLCSP ASSEMBLY CONSIDERATIONS

For detailed information on the WLCSP PCB assembly and reliability, see the AN-617 Application Note, *Wafer Level Chip Scale Package*.

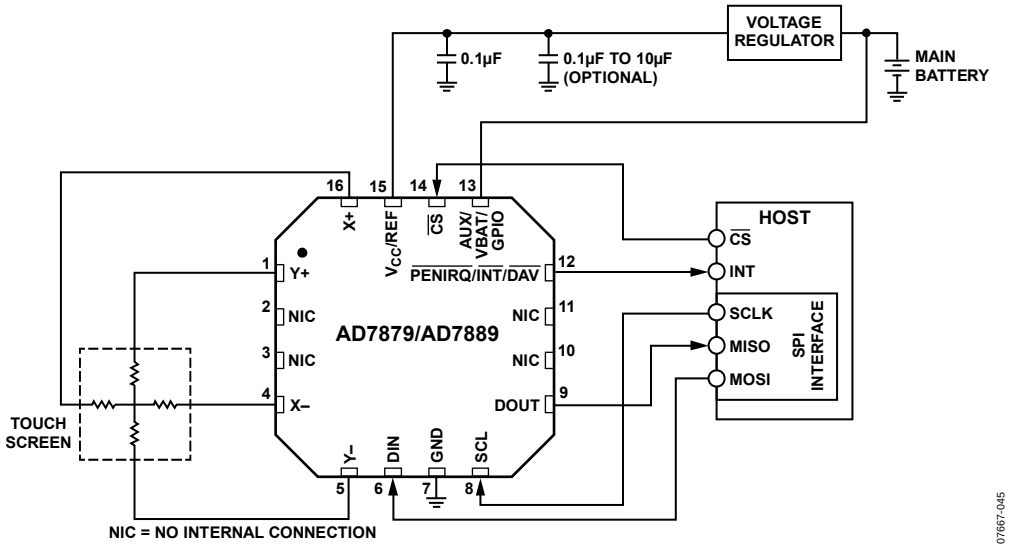


Figure 46. Typical Application Circuit

OUTLINE DIMENSIONS

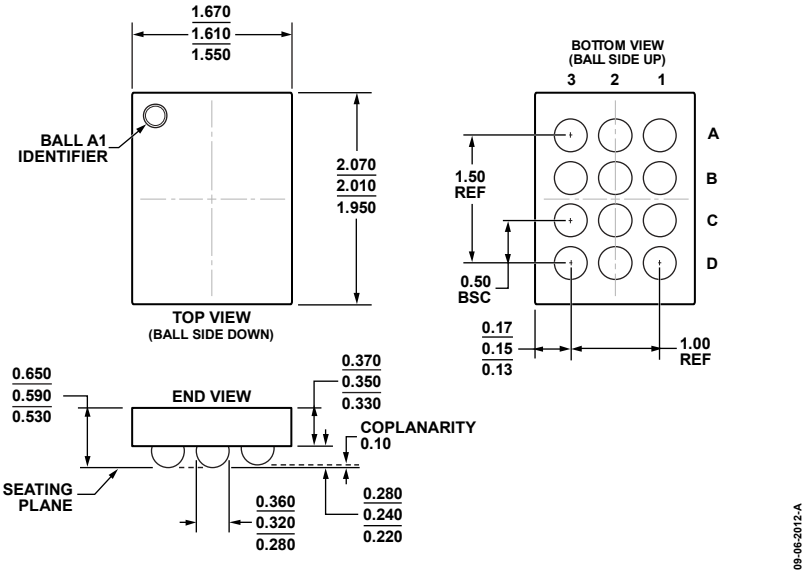


Figure 47. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-1)
Dimensions shown in millimeters

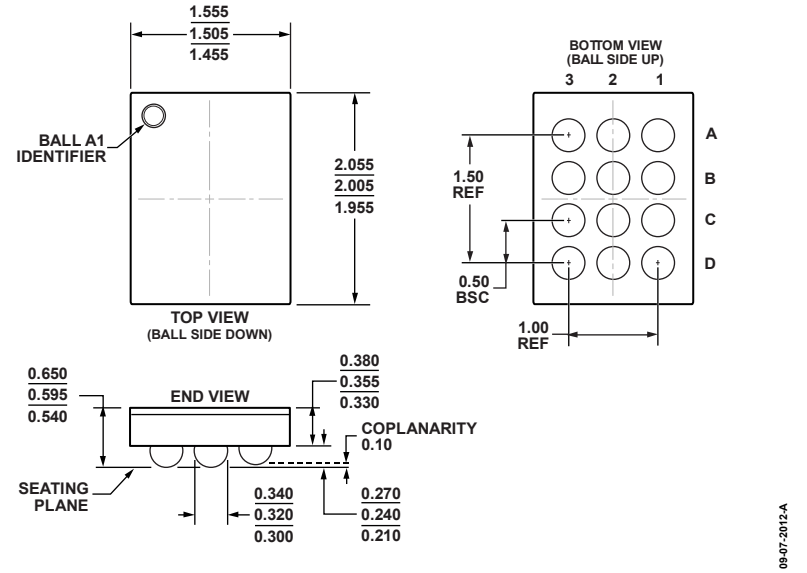


Figure 48. 12-Ball, Backside-Coated Wafer Level Chip Scale Package [WLCSP]
(CB-12-5)
Dimensions shown in millimeters

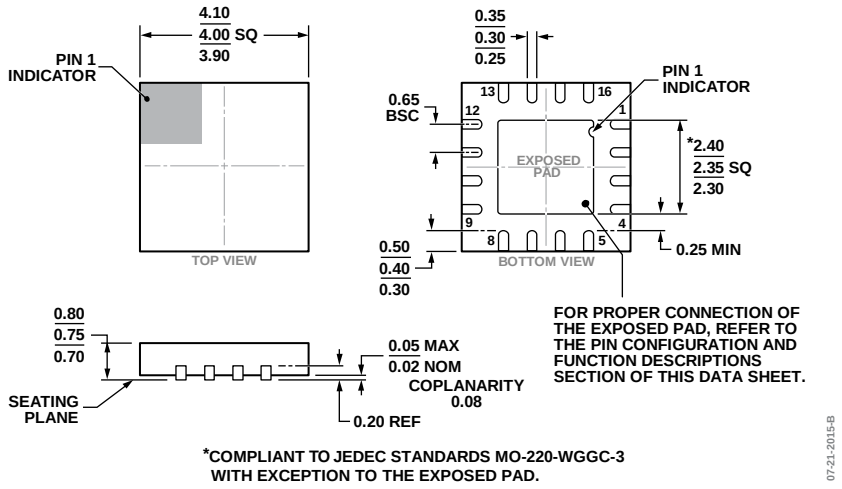


Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm and 0.75 mm Package Height
(CP-16-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Serial Interface Description	Package Description	Package Option	Branding
AD7879ACBZ-RL	−40°C to +85°C	SPI Interface	12-Ball WLCSP	CB-12-1	T2Y
AD7879ACBZ-500R7	−40°C to +85°C	SPI Interface	12-Ball WLCSP	CB-12-1	T2Y
AD7879ACPZ-RL	−40°C to +85°C	SPI Interface	16-Lead LFCSP	CP-16-20	
AD7879ACPZ-500R7	−40°C to +85°C	SPI Interface	16-Lead LFCSP	CP-16-20	
AD7879-1ACBZ-RL	−40°C to +85°C	I²C Interface	12-Ball WLCSP	CB-12-1	T0Q
AD7879-1ACBZ-500R7	−40°C to +85°C	I²C Interface	12-Ball WLCSP	CB-12-1	T0Q
AD7879-1ACPZ-RL	−40°C to +85°C	I²C Interface	16-Lead LFCSP	CP-16-20	
AD7879-1ACPZ-500R7	−40°C to +85°C	I²C Interface	16-Lead LFCSP	CP-16-20	
AD7889ACBZ-RL	−40°C to +85°C	SPI Interface	12-Ball, Backside-Coated WLCSP	CB-12-5	T3R
EVAL-AD7879EBZ		SPI Interface	Evaluation Board		
EVAL-AD7879-1EBZ		I²C Interface	Evaluation Board		

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

Looking for pricing, stock, or lifecycle information?

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