THE DATASHEET OF

AD5293BRUZ-50-RL7

Single-Channel, 1024-Position, 1% R-Tolerance Digital Potentiometer

Data Sheet **AD5293**

FEATURES

- Single-channel, 1024-position resolution
- 20 kΩ, 50 kΩ, and 100 kΩ nominal resistance
- Calibrated 1% nominal resistor tolerance (resistor performance mode)
- Rheostat mode temperature coefficient: 35 ppm/°C
- Voltage divider temperature coefficient: 5 ppm/°C
- Single-supply operation: 9 V to 33 V
- Dual-supply operation: ±9 V to ±16.5 V
- SPI-compatible serial interface
- Wiper setting readback

APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacements
- Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

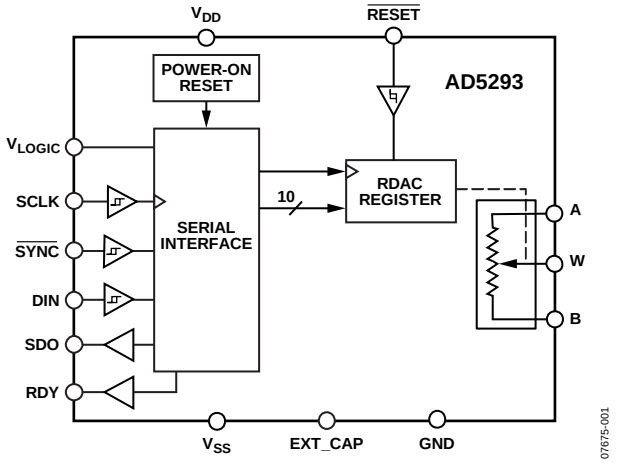

Figure 1.

GENERAL DESCRIPTION

The AD5293 is a single-channel, 1024-position digital potentiometer (in this data sheet, the terms digital potentiometer and RDAC are used interchangeably) with a <1% end-to-end resistor tolerance error. The AD5293 performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. This device is capable of operating at high voltages and supporting both dual-supply operation at ±10.5 V to ±15 V and single-supply operation at 21 V to 30 V.

The AD5293 offers guaranteed industry-leading low resistor tolerance errors of ±1% with a nominal temperature coefficient of 35 ppm/°C. The low resistor tolerance feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5293 is available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +105°C.

Rev. E
Document Feedback

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4/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—20 kΩ VERSIONS

V_{DD} = 21 V to 33 V, V_{SS} = 0 V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = −10.5 V to −16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	$\lvert V_{DD} - V_{SS} \rvert$ = 26 V to 33 V	−2		+2	LSB
	R-INL	$\lvert V_{DD} - V_{SS} \rvert$ = 21 V to 26 V	−3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode)[3]	$\Delta R_{AB}/R_{AB}$	See Table 2	−1	±0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)	$\Delta R_{AB}/R_{AB}$			±7		%
Resistance Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W			60	100	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[5]	DNL		−1		+1	LSB
Integral Nonlinearity[5]	INL		−1.5		+1.5	LSB
Voltage Divider Temperature Coefficient[4]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−8		0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		8	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[6]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[4]	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		85		pF
Capacitance W[4]	C_W	f = 1 MHz, measured to GND, code = half-scale		65		pF
Common-Mode Leakage Current	I_{CM}	$V_A = V_B = V_W$		±1		nA
DIGITAL INPUTS				JEDEC compliant		
Input Logic High	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	2.0			V
Input Logic Low	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input Capacitance[4]	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	V_{LOGIC} − 0.4			V
Output Low Voltage	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}			GND + 0.4	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[4]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±9		±16.5	V
Positive Supply Current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V		0.1	2	µA
Negative Supply Current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V	−2	−0.1		µA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		1	10	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		8	110	µW
Power Supply Rejection Ratio[4]	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%		0.103		%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[4, 8]						
Bandwidth	BW	−3 dB		520		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz,		−93		dB
V_W Settling Time	t_S	V_A = 30 V, V_B = 0 V, ±0.5 LSB error band, initial code = zero scale				
		Code = full scale, R-normal mode		750		ns
		Code = full scale, R-perf mode		2.5		µs
		Code = half scale, R-normal mode		2.5		µs
		Code = half scale, R-perf mode		5		µs
Resistor Noise Density	e_{N_WB}	R_{WB} = 10 kΩ, T_A = 25°C, 0 kHz to 200 kHz		10		nV/√Hz

[1] Typicals represent average readings at 25°C; V_{DD} = +15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between R_{WB} at Code 0x00B to Code 0x3FF or between R_{WA} at Code 0x3F3 to Code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.
[3] The terms resistor performance mode and R-perf mode are used interchangeably.
[4] Guaranteed by design; not subject to production test.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] The A, B, and W resistor terminals have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[8] All dynamic characteristics use V_{DD} = +15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE MODE CODE RANGE—20 kΩ VERSIONS

Table 2.

Resistor Tolerance per Code	R_{AB} = 20 kΩ							
	$\|V_{DD} - V_{SS}\|$ = 30 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 30 V		$\|V_{DD} - V_{SS}\|$ = 22 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 22 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x15E to 0x3FF	From 0x000 to 0x2A1	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x8C to 0x3FF	From 0x000 to 0x373	From 0xB4 to 0x3FF	From 0x000 to 0x34B	From 0xFA to 0x3FF	From 0x000 to 0x305	From 0xFA to 0x3FF	From 0x000 to 0x305
3% R-Tolerance	From 0x5A to 0x3FF	From 0x000 to 0x3A5	From 0x64 to 0x3FF	From 0x000 to 0x39B	From 0x78 to 0x3FF	From 0x000 to 0x387	From 0x78 to 0x3FF	From 0x000 to 0x387

ELECTRICAL CHARACTERISTICS—50 kΩ AND 100 kΩ VERSIONS

V_{DD} = 21 V to 33 V, V_{SS} = 0 V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = −10.5 V to −16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL		−2		+2	LSB
Nominal Resistor Tolerance (R-Perf Mode)[3]	$\Delta R_{AB}/R_{AB}$	See Table 4	−1	±0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)	$\Delta R_{AB}/R_{AB}$			±20		%
Resistance Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W			60	100	Ω
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[5]	DNL		−1		+1	LSB
Integral Nonlinearity[5]	INL		−1.5		+1.5	LSB
Voltage Divider Temperature Coefficient[4]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−8		+1	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		8	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[6]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[4]	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		85		pF
Capacitance W[4]	C_W	f = 1 MHz, measured to GND, code = half-scale		65		pF
Common-Mode Leakage Current	I_{CM}	$V_A = V_B = V_W$		±1		nA
DIGITAL INPUTS			JEDEC compliant			
Input Logic High	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	2.0			V
Input Logic Low	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input Capacitance[4]	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	V_{LOGIC} − 0.4			V
Output Low Voltage	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}			GND + 0.4	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[4]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±9		±16.5	V
Positive Supply Current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V		0.1	2	µA
Negative Supply Current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V	−2	−0.1		µA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		1	10	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		8	110	µW
Power Supply Rejection Ratio[4]	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%				
		R_{AB} = 50 kΩ		0.039		%/%
		R_{AB} = 100 kΩ		0.021		%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[4, 8]						
Bandwidth	BW	−3 dB				kHz
		R_{AB} = 50 kΩ		210		
		R_{AB} = 100 kΩ		105		
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 50 kΩ		−101		dB
		R_{AB} = 100 kΩ		−106		dB
V_W Settling Time	t_S	V_A = 30 V, V_B = 0 V, ±0.5 LSB error band, initial code = zero scale				
		Code = full scale, R-normal mode		750		ns
		Code = full scale, R-perf mode		2.5		µs
		Code = half scale, R-normal mode, R_{AB} = 50 kΩ		7		µs
		Code = half scale, R-normal mode, R_{AB} = 100 kΩ		14		µs
		Code = half scale, R-perf mode, R_{AB} = 50 kΩ		9		µs
		Code = half scale, R-perf mode, R_{AB} = 100 kΩ		16		µs
Resistor Noise Density	e_{N_WB}	Code = half scale, T_A = 25°C, 0 kHz to 200 kHz,				
		R_{AB} = 50 kΩ		18		nV/√Hz
		R_{AB} = 100 kΩ		27		nV/√Hz

[1] Typicals represent average readings at 25°C; V_{DD} = +15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between R_{WB} at Code 0x00B to Code 0x3FF or between R_{WA} at Code 0x3F3 to Code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.
[3] The terms resistor performance mode and R-perf mode are used interchangeably.
[4] Guaranteed by design; not subject to production test.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] The A, B, and W resistor terminals have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[7] P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{SS} × V_{SS}) + (I_{LOGIC} × V_{LOGIC}).
[8] All dynamic characteristics use V_{DD} = +15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE MODE CODE RANGE—50 kΩ AND 100 kΩ VERSIONS

Table 4.

Resistor Tolerance per Code	R_{AB} = 50 kΩ				R_{AB} = 100 kΩ			
	$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x08C to 0x3FF	From 0x000 to 0x35F	From 0x0B4 to 0x3FF	From 0x000 to 0x31E	From 0x04B to 0x3FF	From 0x000 to 0x3B4	From 0x064 to 0x3FF	From 0x000 to 0x39B
2% R-Tolerance	From 0X03C to 0x3FF	From 0x000 to 0x3C3	From 0x050 to 0x3FF	From 0x000 to 0x3AF	From 0x028 to 0x3FF	From 0x000 to 0x3D7	From 0x028 to 0x3FF	From 0x000 to 0x3D7
3% R-Tolerance	From 0X028 to 0x3FF	From 0x000 to 0x3D7	From 0x032 to 0x3FF	From 0x000 to 0x3CD	From 0x019 to 0x3FF	From 0x000 to 0x3E6	From 0x019 to 0x3FF	From 0x000 to 0x3E6

INTERFACE TIMING SPECIFICATIONS

V_{DD} = V_{SS} = ±15 V, V_{LOGIC} = 2.7 V to 5.5 V, and −40°C < T_A < +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	1	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	400[3]	ns min	Minimum $\overline{SYNC}$ high time
t_9	14	ns min	$\overline{SYNC}$ rising edge to next SCLK fall ignored
t_{10}[4]	1	ns min	RDY rise to $\overline{SYNC}$ falling edge
t_{11}[4]	40	ns max	$\overline{SYNC}$ rise to RDY fall time
t_{12}[4]	2.4	µs max	RDY low time, RDAC register write command execute time (resistor performance mode)
t_{12}[4]	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
t_{12}[4]	1.5	ms max	Software\hardware reset
t_{13}[4]	450	ns max	RDY low time, RDAC register read command execute time
t_{14}[4]	450	ns max	SCLK rising edge to SDO valid
t_{RESET}	20	ns min	Minimum $\overline{RESET}$ pulse width (asynchronous)
$t_{POWER-UP}$[5]	2	ms max	Power-on time to half scale

[1] All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency = 50 MHz.
[3] Refer to t_{12} and t_{13} for RDAC register commands operations.
[4] R_{PULL_UP} = 2.2 kΩ to V_{LOGIC} with a capacitance load of 168 pF.
[5] Typical power supply voltage slew-rate of 2 V/ms.

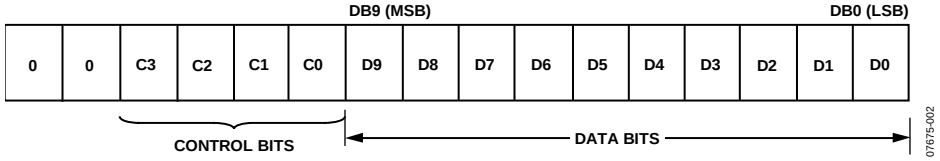

Figure 2. Shift Register Contents

TIMING DIAGRAMS

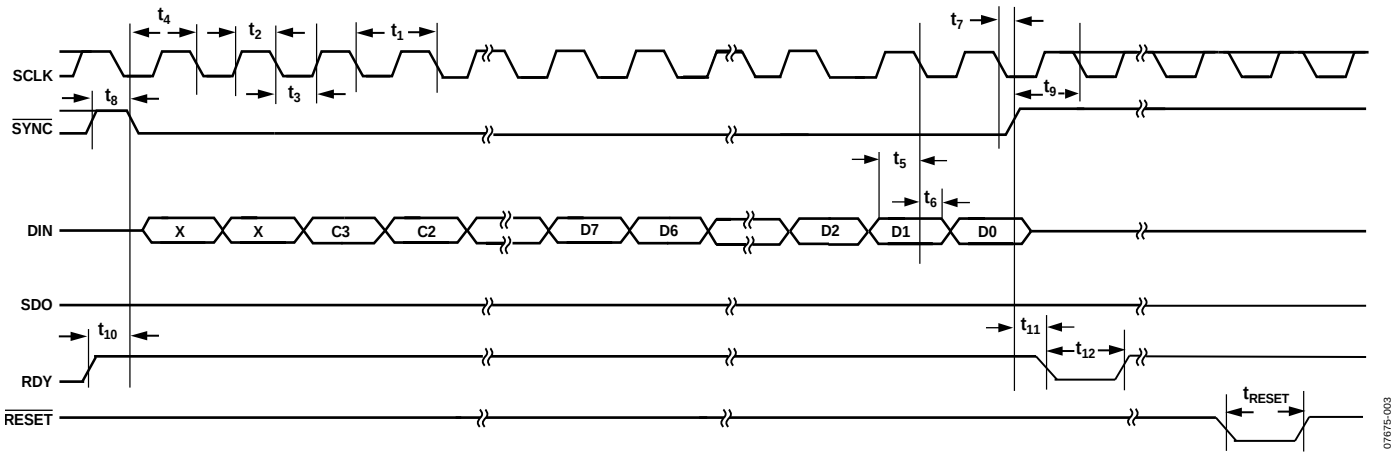

Figure 3. Write Timing Diagram, CPOL = 0, CPHA =1

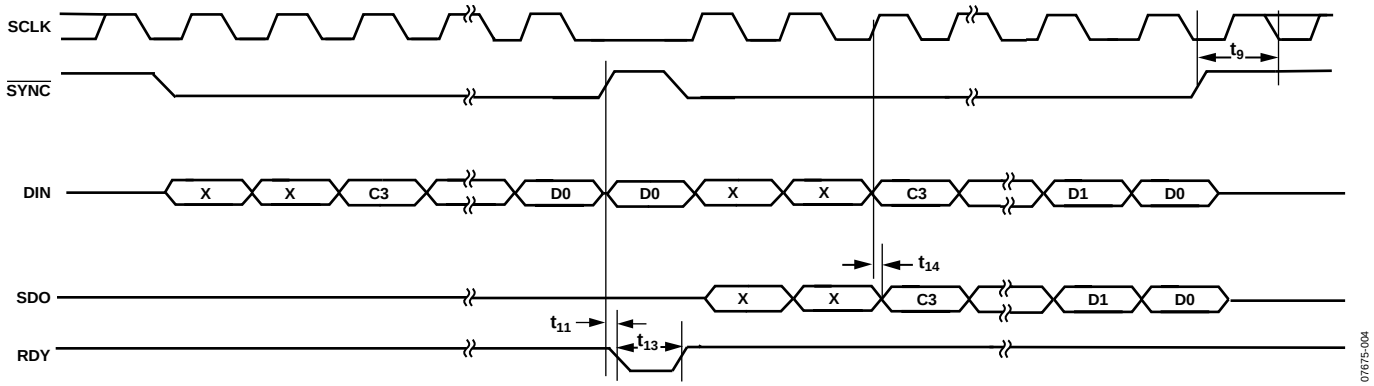

Figure 4. Read Timing Diagram, CPOL = 0, CPHA =1

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +35 V
V_{SS} to GND	+0.3 V to −25 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{DD} to V_{SS}	35 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{LOGIC} +0.3 V
EXT_CAP Voltage to GND	−0.3 V to +7 V
I_A, I_B, I_W	
Continuous	
R_{AB} = 20 kΩ	±3 mA
R_{AB} = 50 kΩ, 100 kΩ	±2 mA
Pulsed[1]	
Frequency > 10 kHz	MCC^2/d^3
Frequency ≤ 10 kHz	$MCC^2/\sqrt{d^3}$
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	(T_J max − T_A)/θ_{JA}

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Maximum continuous current.
[3] Pulse duty factor.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP	93[1]	20	°C/W

[1] JEDEC 2S2P test board, still air (from 0 m/sec to 1 m/sec of air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

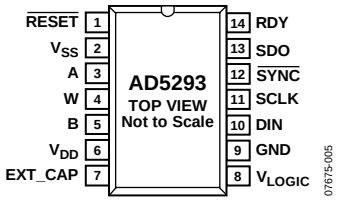

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Hardware Reset Pin. Sets the RDAC register to midscale. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
4	W	Wiper Terminal W of RDAC. $V_{SS} \le V_W \le V_{DD}$.
5	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$.
6	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
7	EXT_CAP	Connect a 1 µF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.
8	V_{LOGIC}	Logic Power Supply, 2.7 V to 5.5 V. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. This part has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register, and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$, following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the serial register in daisy-chain mode or in readback mode.
14	RDY	Ready Pin. This active-high, open-drain output identifies the completion of a write or read operation to or from the RDAC register.

TYPICAL PERFORMANCE CHARACTERISTICS

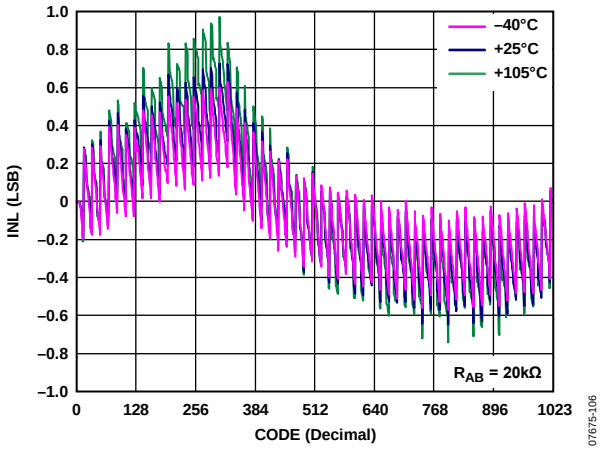

Figure 6. R-INL in R-Perf Mode vs. Code vs. Temperature

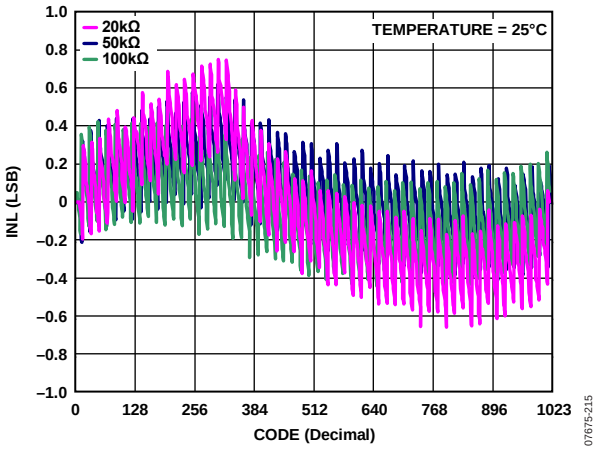

Figure 9. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance

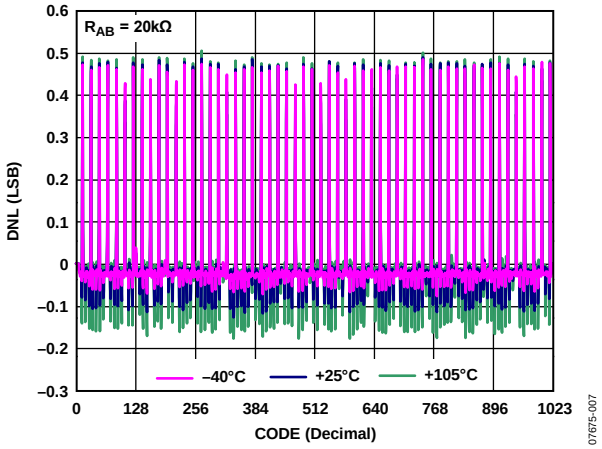

Figure 7. R-DNL in R-Perf Mode vs. Code vs. Temperature

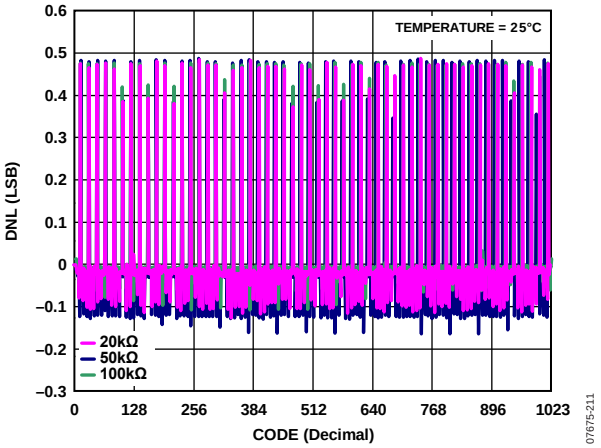

Figure 10. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance

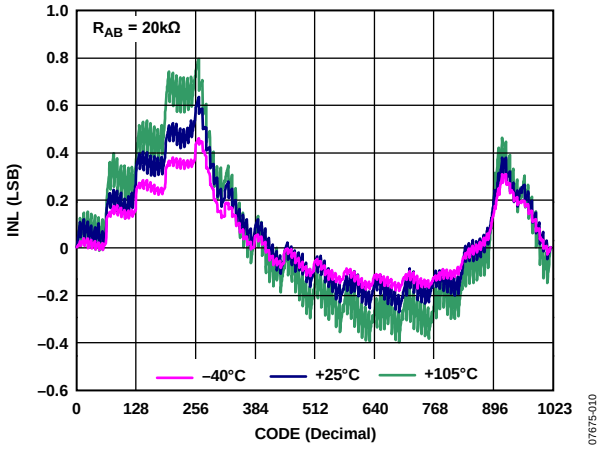

Figure 8. R-INL in Normal Mode vs. Code vs. Temperature

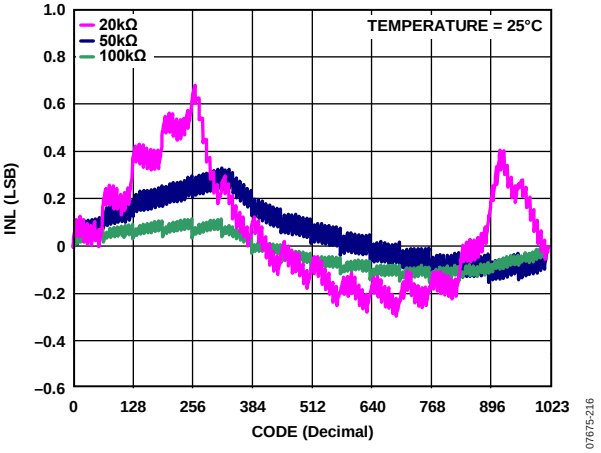

Figure 11. R-INL in Normal Mode vs. Code vs. Nominal Resistance

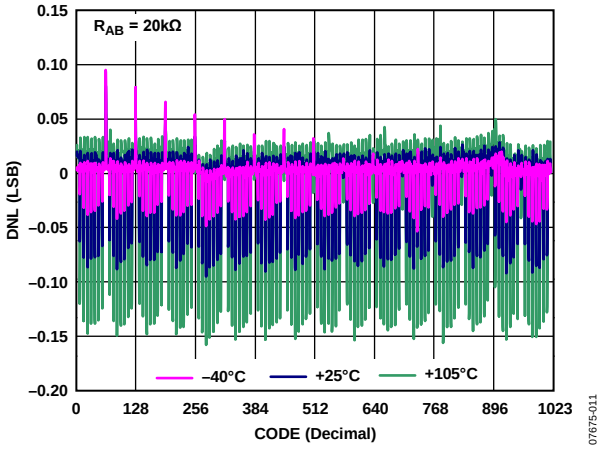

Figure 12. R-DNL in Normal Mode vs. Code vs. Temperature

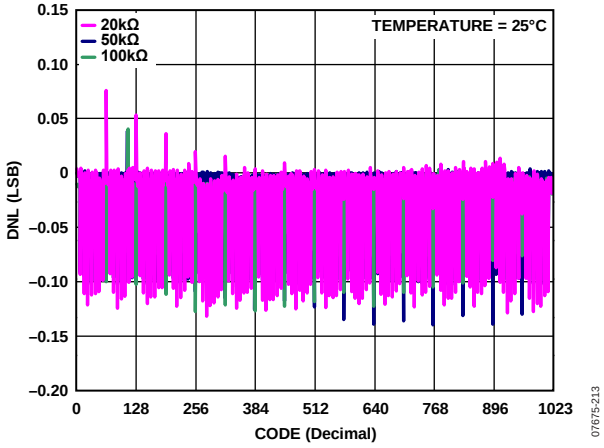

Figure 15. R-DNL in Normal Mode vs. Code vs. Nominal Resistance

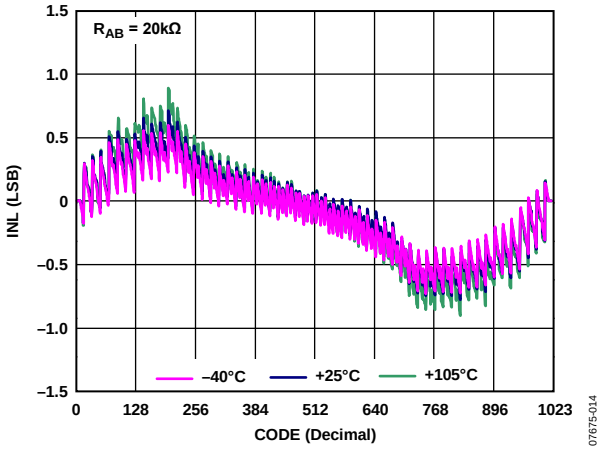

Figure 13. INL in R-Perf Mode vs. Code vs. Temperature

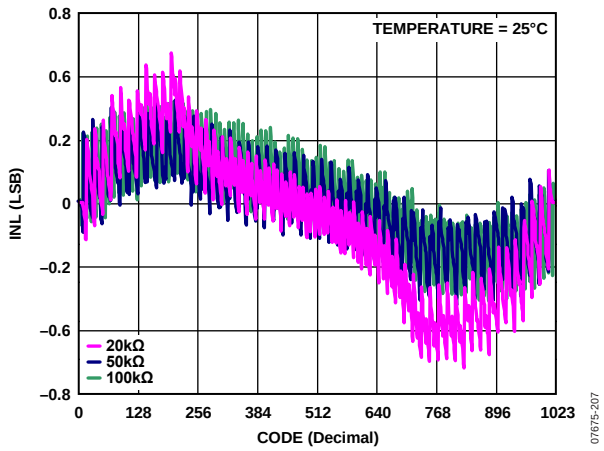

Figure 16. INL in R-Perf Mode vs. Code vs. Nominal Resistance

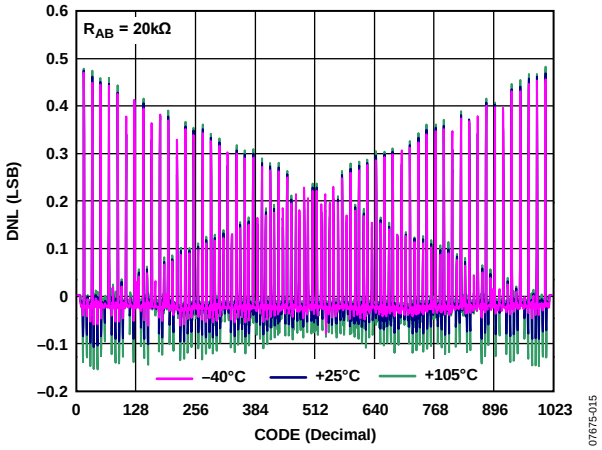

Figure 14. DNL in R-Perf Mode vs. Code vs. Temperature

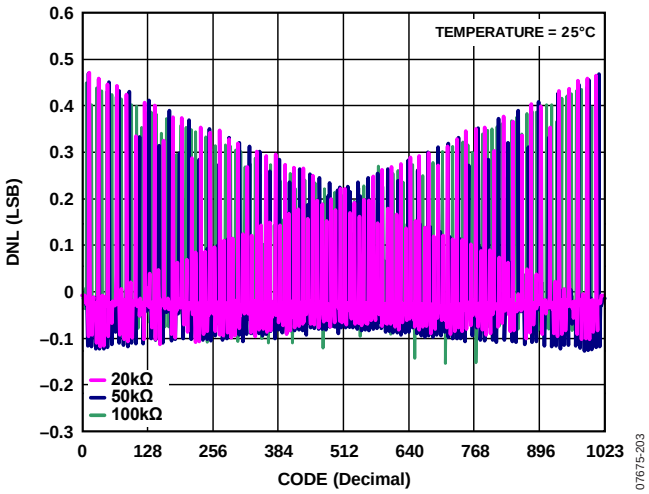

Figure 17. DNL in R-Perf Mode vs. Code vs. Nominal Resistance

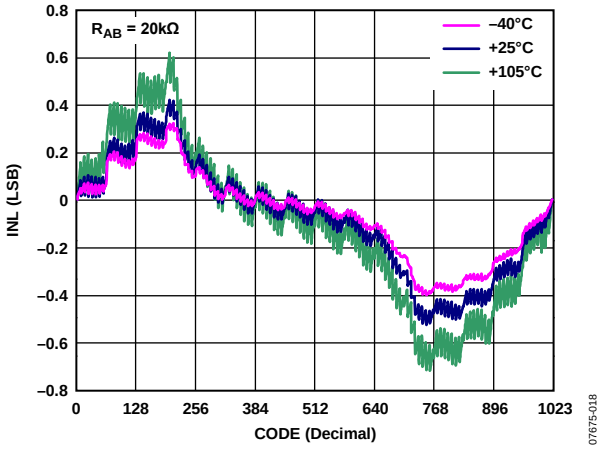

Figure 18. INL in Normal Mode vs. Code vs. Temperature

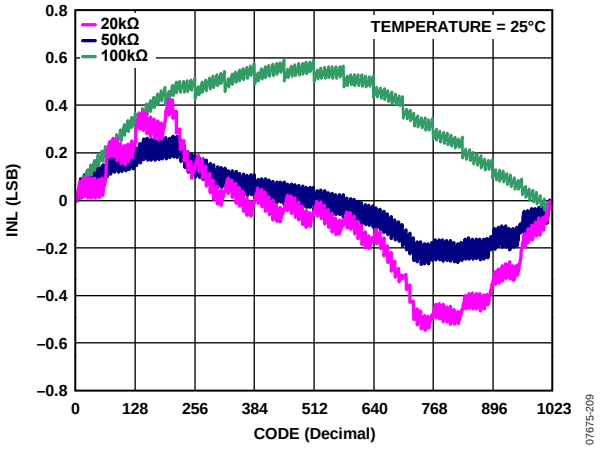

Figure 21. INL in Normal Mode vs. Code vs. Nominal Resistance

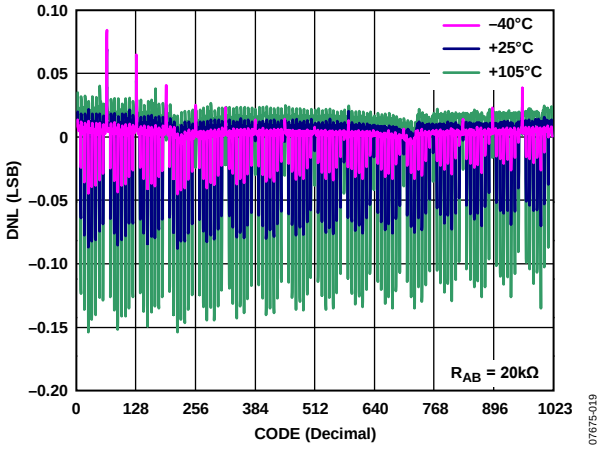

Figure 19. DNL in Normal Mode vs. Code vs. Temperature

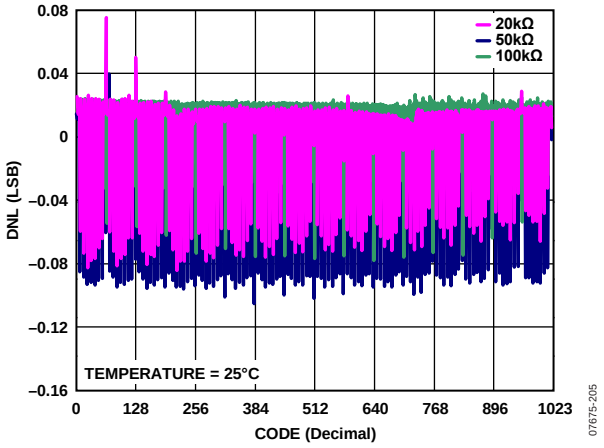

Figure 22. DNL in Normal Mode vs. Code vs. Nominal Resistance

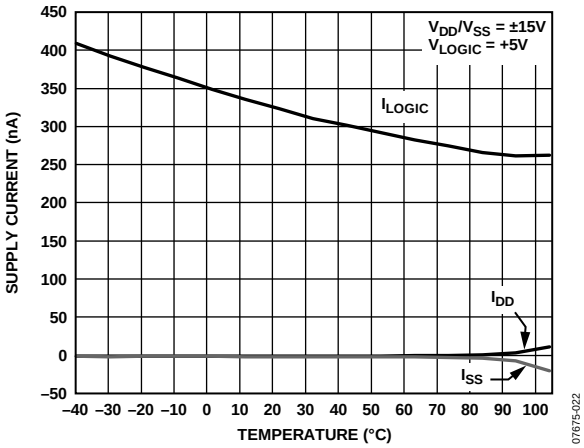

Figure 20. Supply Current vs. Temperature

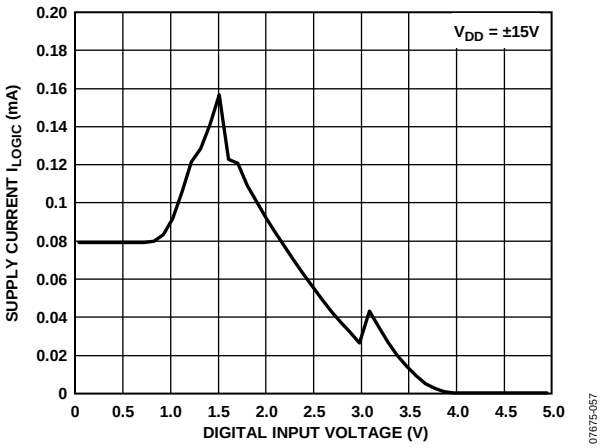

Figure 23. Supply Current, I_{LOGIC}, vs. Digital Input Voltage.

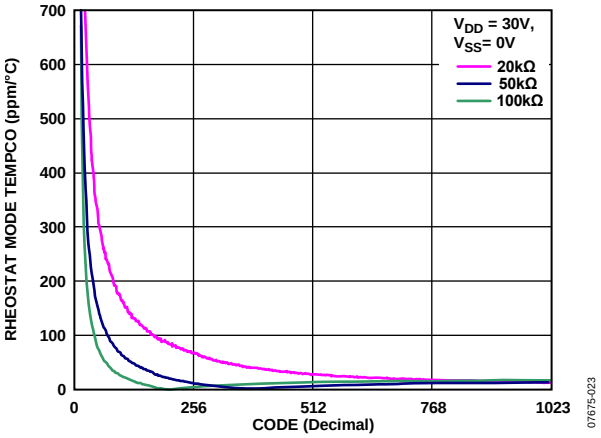

Figure 24. Rheostat Mode Tempco ΔRWB/ΔT vs. Code

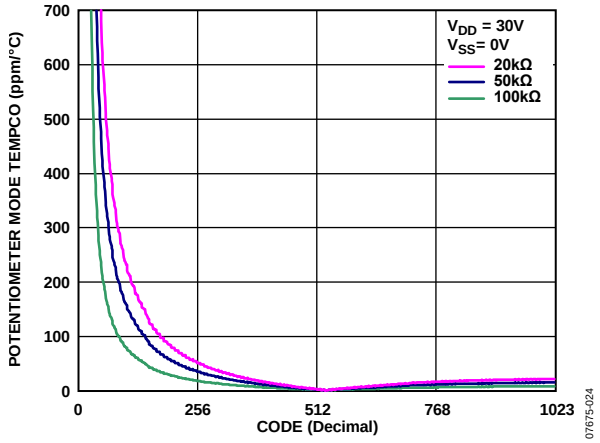

Figure 27. Potentiometer Mode Tempco ΔRWB/ΔT vs. Code

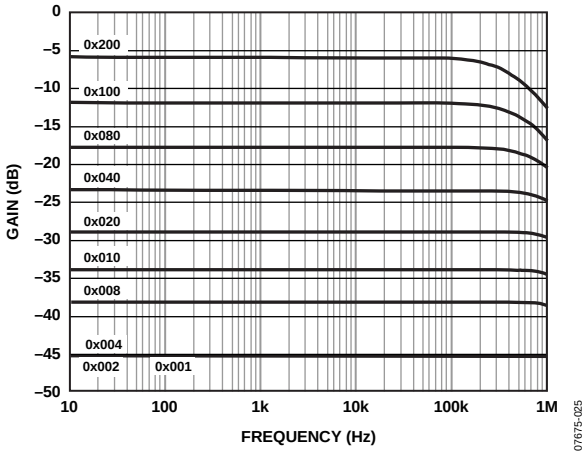

Figure 25. 20 kΩ Gain vs. Frequency vs. Code

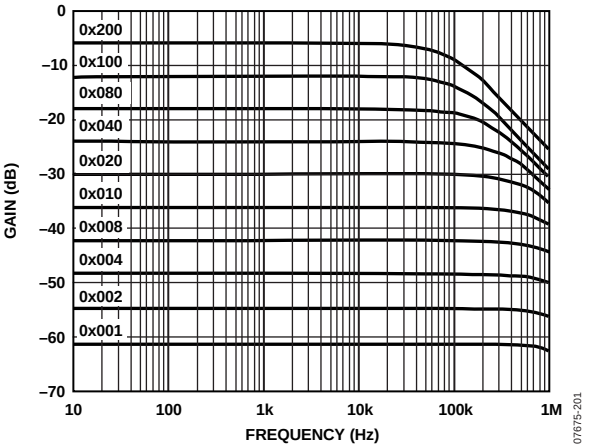

Figure 28. 100 kΩ Gain vs. Frequency vs. Code

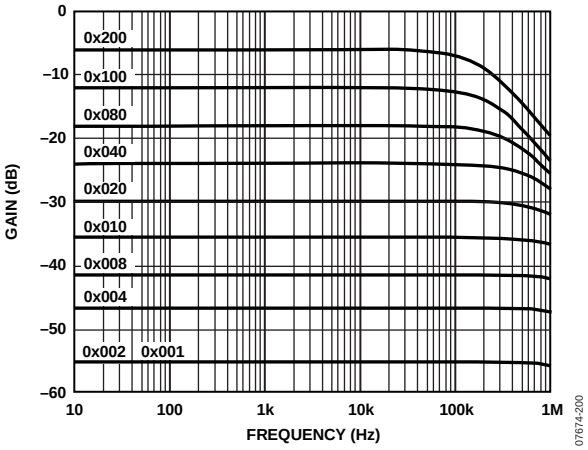

Figure 26. 50 kΩ Gain vs. Frequency vs. Code

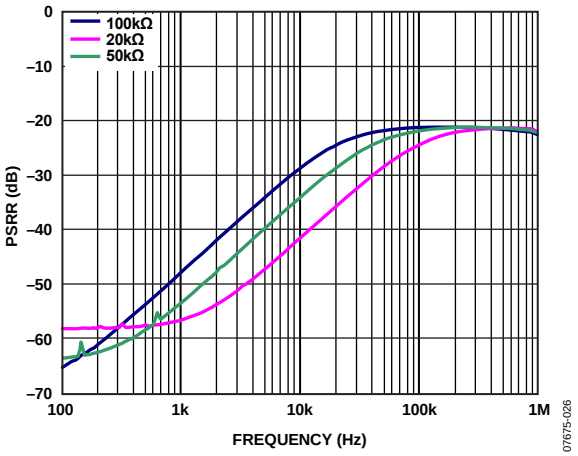

Figure 29. Power Supply Rejection Ratio (PSRR) vs. Frequency

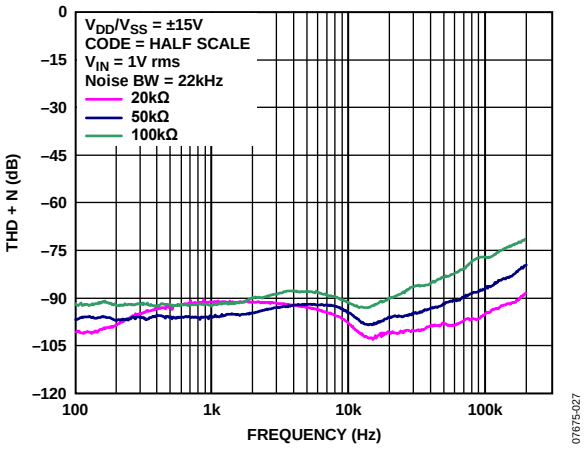

Figure 30. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

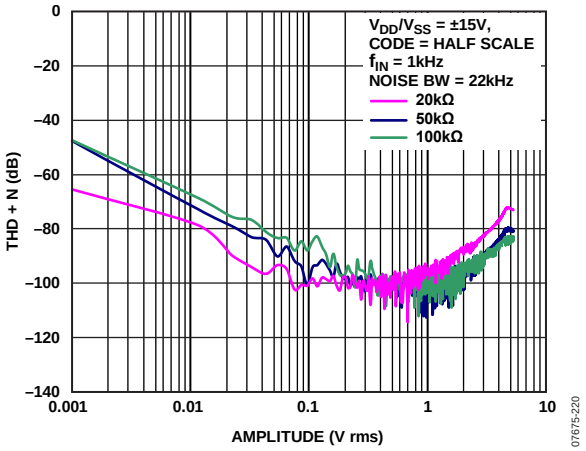

Figure 33. Total Harmonic Distortion + Noise (THD + N) vs. Amplitude

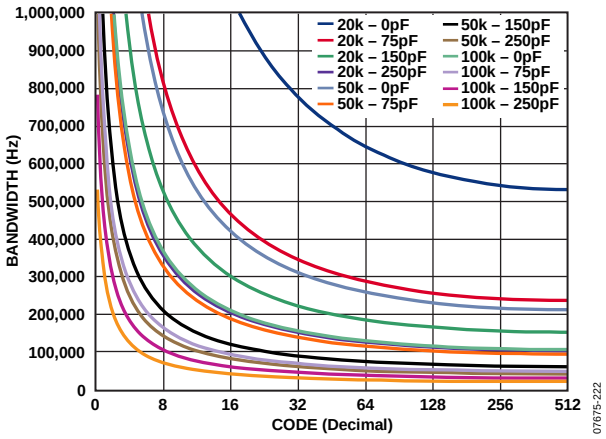

Figure 31. Maximum Bandwidth vs. Code vs. Net Capacitance

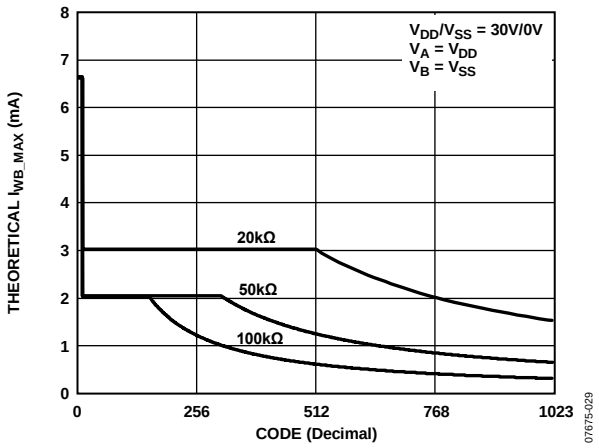

Figure 34. Theoretical Maximum Current vs. Code

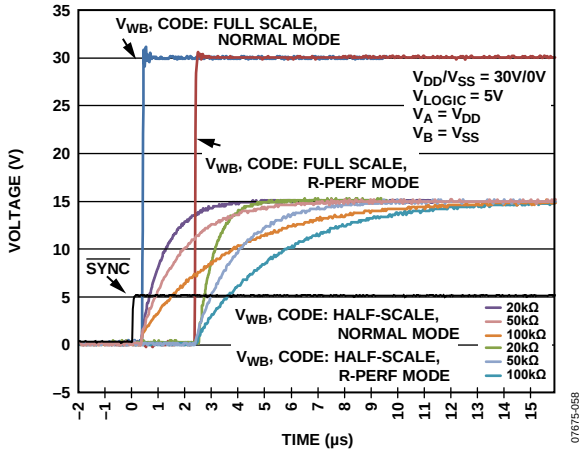

Figure 32. Large Signal Settling Time, Code from Zero Scale to Full Scale

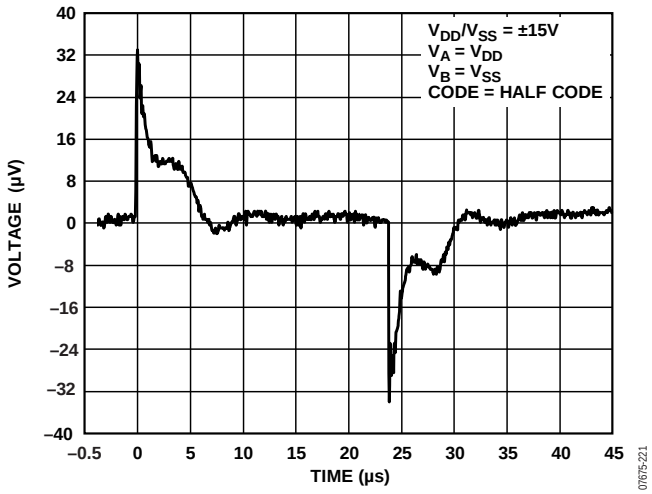

Figure 35. Digital Feedthrough

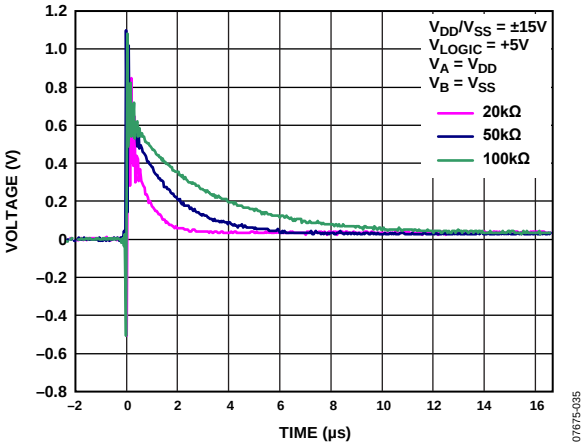

Figure 36. Maximum Transition Glitch

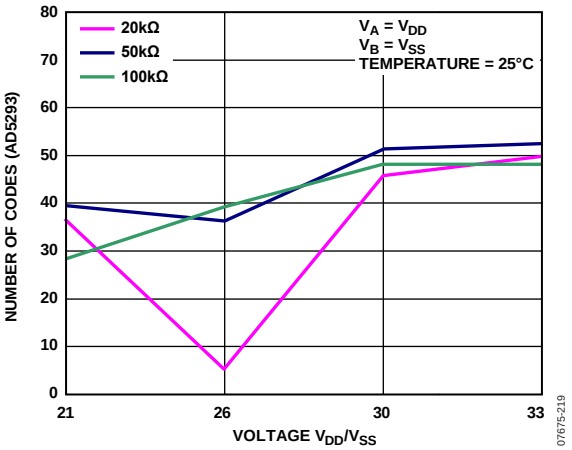

Figure 38. Code Range > 1% R-Tolerance Error vs. Voltage

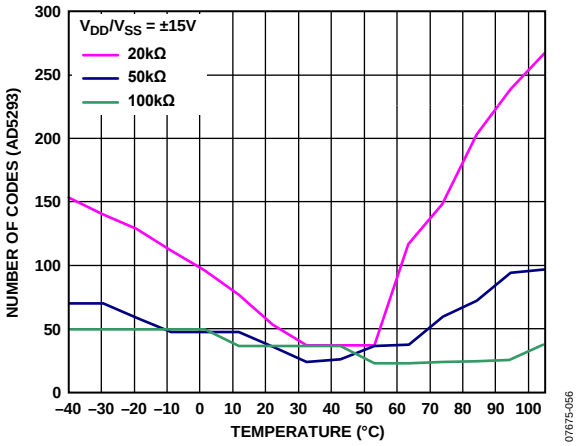

Figure 37. Code Range > 1% R-Tolerance Error vs. Temperature

TEST CIRCUITS

Figure 39 to Figure 44 define the test conditions used in the Specifications section.

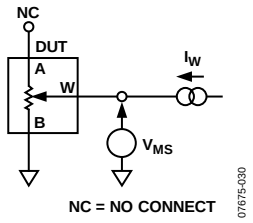

Figure 39. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

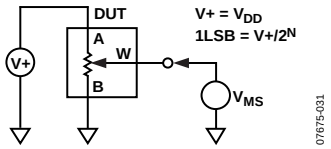

Figure 40. Potentiometer Divider Nonlinearity Error (INL, DNL)

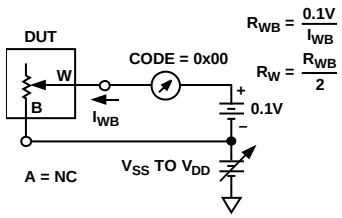

Figure 41. Wiper Resistance

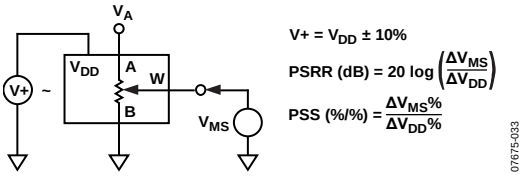

Figure 42. Power Supply Sensitivity (PSS, PSRR)

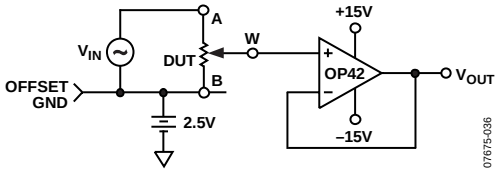

Figure 43. Gain vs. Frequency

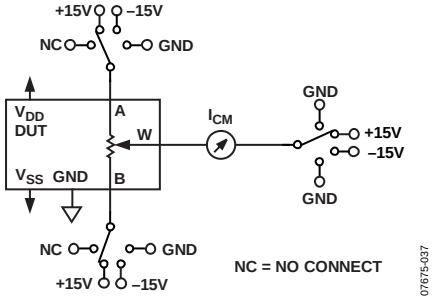

Figure 44. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5293 digital potentiometer is designed to operate as a true variable resistor for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The patented ±1% resistor tolerance feature helps to minimize the total RDAC resistance error, which reduces the overall system error by offering better absolute matching and improved open-loop performance. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The RDAC register can be programmed with any position setting via the standard serial peripheral interface (SPI) by loading the 16-bit data-word.

SERIAL DATA INTERFACE

The AD5293 contains a serial interface ($\overline{SYNC}$, SCLK, DIN, and SDO) that is compatible with SPI standards, as well as most DSPs. The device allows data to be written to every register via the SPI.

SHIFT REGISTER

The AD5293 shift register is 16 bits wide (see Figure 2). The 16-bit data-word consists of two unused bits, which are set to 0, followed by four control bits and 10 RDAC data bits. Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command (see Table 11). Figure 3 shows a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. The $\overline{SYNC}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{SYNC}$ returns high, the serial data-word is decoded according to the instructions in Table 11. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5293 has an internal counter that counts a multiple of 16 bits (per frame) for proper operation. For example, the AD5293 works with a 32-bit word, but it cannot work properly with a 31- or 33-bit word. The AD5293 does not require a continuous SCLK, when $\overline{SYNC}$ is high, and all interface pins should be operated close to the supply rails to minimize power consumption in the digital input buffers.

RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal B of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed. The RDY pin can be used to monitor the completion of a write to or read from the RDAC register. The AD5293 presets to midscale on power-up.

WRITE PROTECTION

On power-up, the serial data input register write command for the RDAC register is disabled. The RDAC write protect bit, C1 of the control register (see Table 12 and Table 13), is set to 0 by default. This disables any change of the RDAC register content, regardless of the software commands, except that the RDAC register can be refreshed to midscale using the software reset command (Command 3, see Table 11) or through hardware, using the $\overline{RESET}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit, C1 of the control register, must first be programmed. This is accomplished by loading the serial data input register with Command 4 (see Table 11).

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the serial data input register with Command 1 (see Table 11) and the desired wiper position data. The RDY pin can be used to monitor the completion of this RDAC register write command. Command 2 can be used to read back the contents of the RDAC register (see Table 11). After issuing the readback command, the RDY pin can be monitored to indicate when the data is available to be read out on SDO in the next SPI operation. Instead of monitoring the RDY pin, a minimum delay can be implemented when executing a write or read command (see Table 5). Table 9 provides an example listing of a sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format for an RDAC write and read.

Table 9. RDAC Register Write and Read

DIN	SDO	Action
0x1802	0xXXXX[1]	Enable update of wiper position.
0x0500	0x1802	Write 0x100 to the RDAC register. Wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from RDAC register.
0x0000	0x0100	NOP (Instruction 0) sends a 16-bit word out of SDO, where the last 10 bits contain the contents of the RDAC register.

[1] X = unknown.

SHUTDOWN MODE

The AD5293 can be placed in shutdown mode by executing the software shutdown command (see Command 6 in Table 11), and setting the LSB to 1. This feature places the RDAC in a special state in which Terminal A is open-circuited and Wiper W is connected to Terminal B. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 11 are supported while in shutdown mode.

RESET

A low-to-high transition of the hardware $\overline{\text{RESET}}$ pin loads the RDAC register with midscale. The AD5293 can also be reset through software by executing Command 3 (see Table 11). The control register is restored with default bits (see Table 13).

RESISTOR PERFORMANCE MODE

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a ±1% resistor tolerance on each code, that is, code = half scale, R_{WB} =10 kΩ ± 100 Ω. See Table 2 and Table 4 to verify which codes achieve ±1% resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register (see Table 12 and Table 13). The typical settling time is shown in Figure 32.

SDO PIN AND DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes: it can be used to read the contents of the wiper setting and control register using Command 2, and Command 5, respectively (see Table 11) or the SDO pin can be used in daisy-chain mode. Data is clocked out of SDO on the rising edge of SCLK. The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor if this pin is used. To place the pin in high impedance and minimize the power dissipation when the pin is used, the 0x8001 data word followed by Command 0 should be sent to the part. Table 10 provides a sample listing for the sequence of the serial data input (DIN). Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 45, users need to tie the SDO pin of one package to the DIN pin of the next package. Users may need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO-to-DIN interface may require additional time delay between subsequent devices.

When two AD5293s are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. The $\overline{\text{SYNC}}$ pin should be held low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

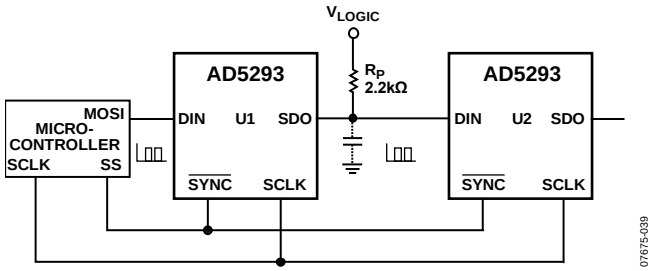

Figure 45. Daisy-Chain Configuration Using SDO

Table 10. Minimize Power Dissipation at the SDO Pin

DIN	SDO[1]	Action
0xXXXX	0xXXXX	Last user command sent to the digital potentiometer
0x8001	0xXXXX	Prepares the SDO pin to be placed in high impedance mode
0x0000	High impedance	The SDO pin is placed in high impedance

[1] X = don't care.

Table 11. Command Operation Truth Table

	Command Bits[B13:B10]				Data Bits[B9:B0][1]										
Command	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP command. Do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of serial register data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read RDAC wiper setting from SDO output in the next frame.
3	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Reset. Refresh RDAC with midscale code.
4	0	1	1	0	X	X	X	X	X	X	X	D2	D1	X	Write contents of serial register data to control register.
5	0	1	1	1	X	X	X	X	X	X	X	X	X	X	Read control register from SDO output in the next frame.
6	1	0	0	0	X	X	X	X	X	X	X	X	X	D0	Software power-down. D0 = 0 (normal mode). D0 = 1 (device placed in shutdown mode).

[1] X = don't care.

Table 12. Control Register Bit Map

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	C2	C1	X[1]

[1] X = don't care.

Table 13. Control Register Function

Register Name	Bit Name	Description
Control	C2	Calibration enable. 0 = resistor performance mode (default). 1 = normal mode.
	C1	RDAC register write protect. 0 = locks the wiper position through the digital interface (default). 1 = allows update of wiper position through digital interface.

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices, Inc., has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5293 employs a 3-stage segmentation approach, as shown in Figure 46. The AD5293 wiper switch is designed with transmission gate CMOS topology and with the gate voltage derived from V_{DD}.

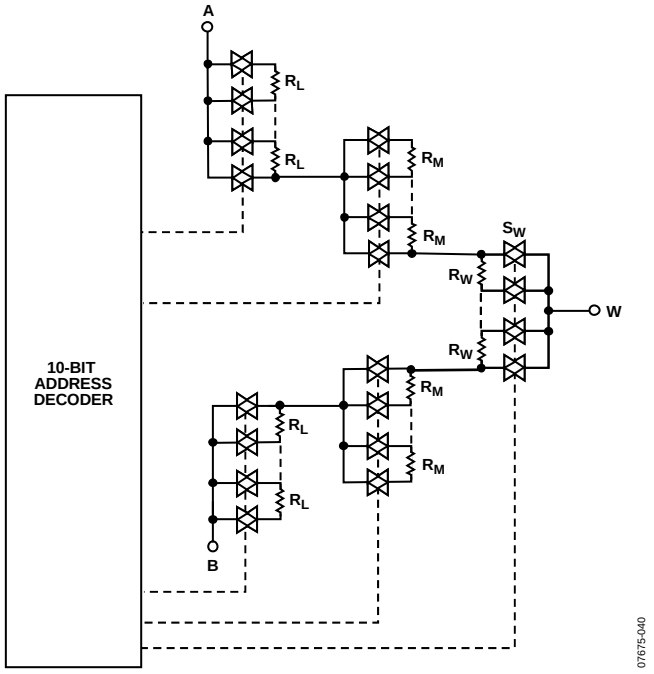

Figure 46. Simplified RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—1% Resistor Tolerance

The AD5293 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be left floating or it can be tied to the W terminal, as shown in Figure 47.

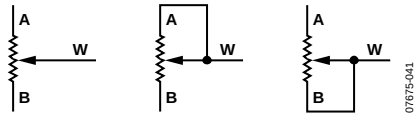

Figure 47. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 20 kΩ, 50 kΩ, and 100 kΩ and has 1024 tap points that are accessed by the wiper terminal. The 10-bit data in the RDAC latch is decoded to select one of the 1024 possible wiper settings. The AD5293 contains an internal ±1% resistor tolerance calibration feature that can be enabled or disabled, enabled by default by programming Bit C2 of the control register (see Table 12 and Table 13).

The digitally programmed output resistance between the W terminal and the A terminal, R_{WA}, and the W terminal and B terminal, R_{WB}, is calibrated to give a maximum of ±1% absolute resistance error over both the full supply and temperature ranges. As a result, the general equation for determining the digitally programmed output resistance between the W terminal and B terminal is

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB} \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.
R_{AB} is the end-to-end resistance.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} is also calibrated to give a maximum of 1% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equation for this operation is

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} \quad (2)$$

where:
D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.
R_{AB} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of the setting in which the part is operating, care should be taken to limit the current between the A terminal to B terminal, the W terminal to the A terminal, and the W terminal to the B terminal to the maximum continuous current of ±3 mA or to the pulse current specified in Table 6. Otherwise, degradation, or possible destruction of the internal switch contact, can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B terminal and wiper-to-A terminal that is proportional to the input voltage at A to B, as shown in Figure 48. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

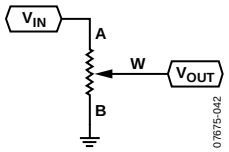

Figure 48. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B that ranges from 0 V to 30 V − 1 LSB. Each LSB of voltage is equal to the voltage applied across the A terminal and B terminal, divided by the 1024 positions of the potentiometer divider. The general equation defining the output voltage at V_W, with respect to ground for any valid input voltage applied to Terminal A and Terminal B, is

$$V_W(D) = \frac{D}{1024} \times V_A + \frac{1024 - D}{1024} \times V_B \quad (3)$$

To optimize the wiper position update rate when in voltage divider mode, it is recommended that the internal ±1% resistor tolerance calibration feature be disabled by programming Bit C2 of the control register (see Table 11).

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not on the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

EXT_CAP CAPACITOR

A 1 µF capacitor to GND must be connected to the EXT_CAP pin (see Figure 49) on power-up and throughout the operation of the AD5293. This capacitor must have a voltage rating of ≥7 V.

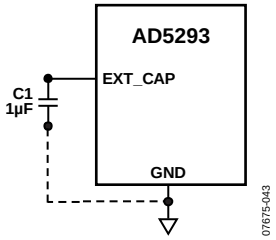

Figure 49. Hardware Setup for the EXT_CAP Pin

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5293 define the boundary conditions for proper 3-terminal, digital potentiometer operation. Supply signals present on the A, B, and W terminals that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 50).

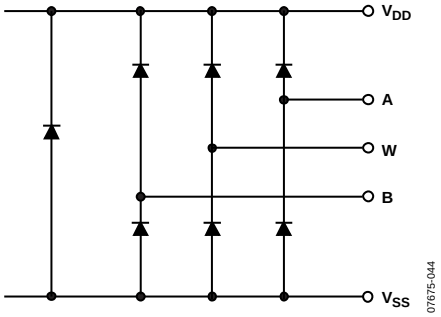

Figure 50. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5293 is primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5293 ground pin should be joined remotely to common ground. The digital input control signals to the AD5293 must be referenced to the device ground pin (GND) to satisfy the logic level defined in the Specifications section.

Power-Up Sequence

Because there are diodes to limit the voltage compliance at the A, B, and W terminals (see Figure 50), it is important to power V_{DD} and V_{SS} first, before applying any voltage to the A, B, and W terminals. Otherwise, the diode is forward-biased such that V_{DD} and V_{SS} are powered up unintentionally. The ideal power-up sequence is GND, V_{SS}, V_{LOGIC}, V_{DD}, the digital inputs, and then V_A, V_B, and V_W. The order of powering up V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}, V_{SS}, and V_{LOGIC}.

Regardless of the power-up sequence and the ramp rates of the power supplies, the power-on preset activates after V_{LOGIC} is powered, restoring midscale to the RDAC register.

APPLICATIONS INFORMATION

HIGH VOLTAGE DAC

The AD5293 can be configured as a high voltage DAC, with an output voltage as high as 33 V. The circuit is shown in Figure 51. The output is

$$V_{OUT}(D) = \frac{D}{1024} \times \left[1.2\ \text{V} \times \left(1 + \frac{R_2}{R_1} \right) \right] \quad (4)$$

where D is the decimal code from 0 to 1023.

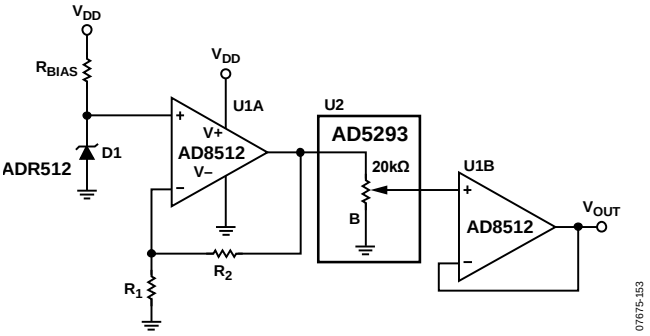

Figure 51. High Voltage DAC

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustments, such as a laser diode or tunable laser, a boosted voltage source can be considered (see Figure 52).

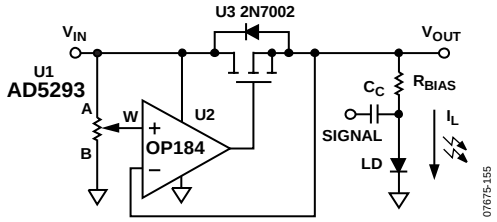

Figure 52. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET (U3). The N-channel FET power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 33 V supply.

HIGH ACCURACY DAC

It is possible to configure the AD5293 as a high accuracy DAC by optimizing the resolution of the device over a specific reduced voltage range. This is achieved by placing external resistors on either side of the RDAC, as shown in Figure 53. The improved ±1% resistor tolerance specification greatly reduces error associated with matching to discrete resistors.

$$V_{OUT}(D) = \frac{R_3 + (D/1024 \times R_{AB}) \times V_{DD}}{R_1 + ((1024-D)/1024) \times R_{AB} + R_3} \quad (5)$$

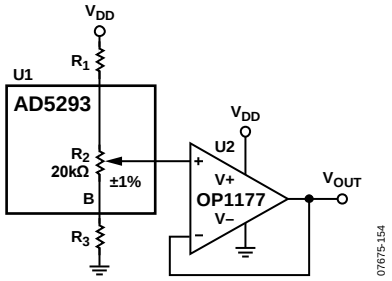

Figure 53. Optimizing Resolution

VARIABLE GAIN INSTRUMENTATION AMPLIFIER

The AD8221 in conjunction with the AD5293 and the ADG1207, as shown in Figure 54, make an excellent instrumentation amplifier for use in data acquisition systems. The data acquisition system is low distortion and low noise enable it to condition signals in front of a variety of ADCs.

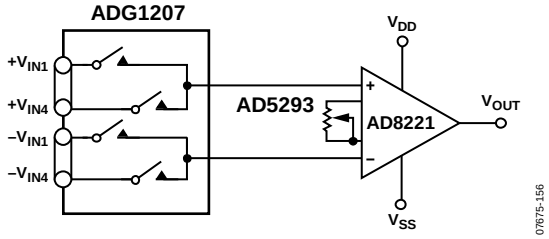

Figure 54. Data Acquisition System

The gain can be calculated by using Equation 6, as follows:

$$G(D) = 1 + \frac{49.4\ \text{k}\Omega}{(D/1024) \times R_{AB}} \quad (6)$$

AUDIO VOLUME CONTROL

The excellent THD performance and high voltage capability of the AD5293 make it ideal for digital volume control. The AD5293 is used as an audio attenuator; it can be connected directly to a gain amplifier. A large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $\overline{CS}$ line to delay the device update until the audio signal crosses the window. Because the input signal can operate on top of any dc level, rather than absolute 0 V level, zero crossing in this case means the signal is ac-coupled, and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise is shown in Figure 56, and the results of using this configuration are shown in Figure 55.

The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by U2, U3, and U4B. U6 is used to establish the signal as zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the chip select signal such that the AD5293 updates whenever the signal crosses the window. To avoid a constant update of the device, program the chip select signal as two pulses instead of one.

In Figure 55, the lower trace shows that the volume level changes from a quarter-scale to full-scale when a signal change occurs near the zero-crossing window.

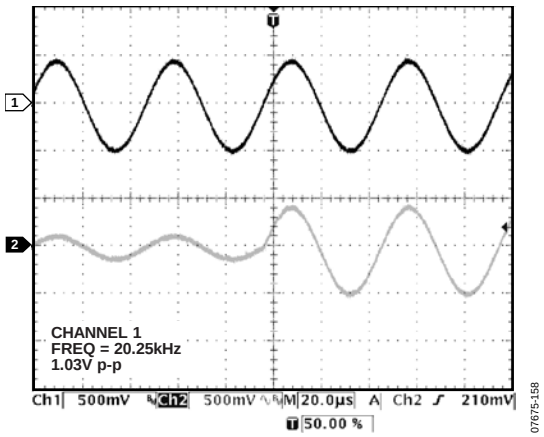

Figure 55. Zipper Noise Detector

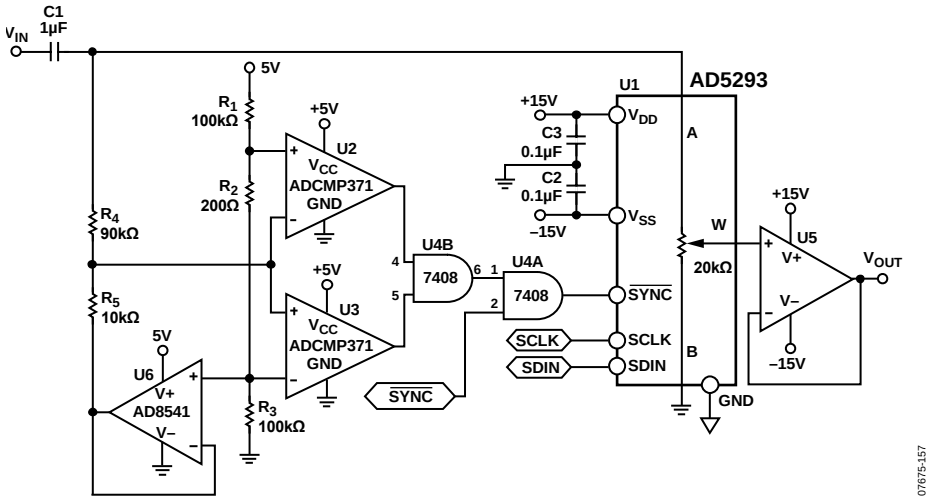

Figure 56. Audio Volume Control with Zipper Noise Reduction.

OUTLINE DIMENSIONS

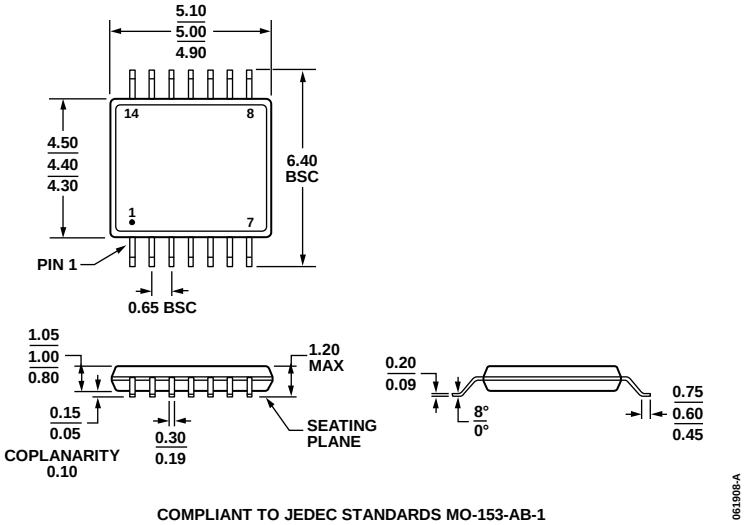

Figure 57. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option
AD5293BRUZ-20	20	1024	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-20-RL7	20	1024	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-50	50	1024	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-50-RL7	50	1024	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-100	100	1024	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5293BRUZ-100-RL7	100	1024	−40°C to +105°C	14-Lead TSSOP	RU-14

[1] Z = RoHS Compliant Part.

D07675-0-3/16(E)

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