THE DATASHEET OF

A4939KLPTR-T

Automotive Three Phase MOSFET Driver

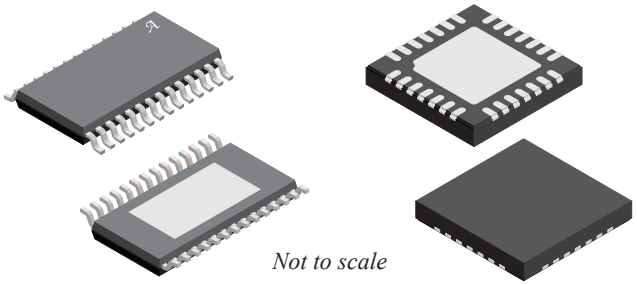
FEATURES AND BENEFITS

- High current 3-phase gate drive for N-channel MOSFETs
- Cross-conduction protection
- 5.5 to 50 V supply voltage range
- Regulated logic supply voltage output option
- Motor phase short to supply and short to ground detection
- Undervoltage, overtemperature monitors
- Low current Sleep mode option

APPLICATIONS

- Electronic power steering (EPS, EHPS, EAS)
- Hydraulic pumps
- Engine cooling fan
- Gearbox actuator

PACKAGES



Not to scale

28-pin TSSOP with exposed thermal pad (LP package)

28-contact QFN 5 mm × 5 mm × 0.85 mm (ET package)

DESCRIPTION

The A4939 is a three-phase controller for use with N-channel external power MOSFETs and is specifically designed for automotive applications.

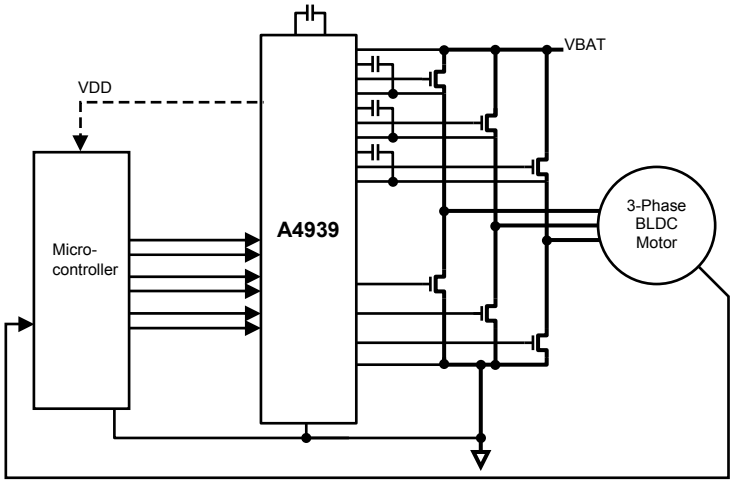
A unique charge pump regulator provides full (>10 V) gate drive at battery voltages down to 7 V and allows the A4939 to operate with reduced gate drive at battery voltages down to 5.5 V. A bootstrap capacitor is used to provide the above battery supply voltage required for N-channel MOSFETs.

One logic level input is provided for each of the six power MOSFETs in the 3-phase bridge, allowing motors to be driven with any commutation scheme defined by an external controller. The power MOSFETs are protected from cross-conduction by integrated crossover control.

Motor phase short-to-supply and short-to-ground detection is provided by independent drain-source voltage monitors on each MOSFET. Short faults, supply undervoltage, and chip overtemperature conditions are indicated by a single open drain fault output.

Product variants incorporating a low drop out (LDO) regulator to source either 5.0 V or 3.3 V to external circuitry are available. All A4939 variants are available in a 28-pin TSSOP power package with an exposed thermal pad (package type LP) or a 28-pin wettable flank QFN package with an exposed thermal pad (package type ET). Both packages are lead (Pb) free, with 100% matte-tin leadframe plating (suffix T).

Typical Application Diagram



SELECTION GUIDE

Part Number	Sleep Mode	Regulator	Packing	Package
A4939KLPTR-T	Yes	–	4000 pieces per 13-in. reel	9.7 mm × 4.4 mm, 1.2 mm nominal height 28-pin TSSOP with exposed thermal pad
A4939KLPTR-3-T	–	3.3 V		
A4939KLPTR-5-T	–	5 V		
A4939KETTR-T	Yes	–	7000 pieces per 13-in. reel	5 mm × 5 mm, 0.85 mm nominal height, 28-pin wettable flank QFN with exposed thermal pad
A4939KETTR-3-T	–	3.3 V		
A4939KETTR-5-T	–	5 V		

Table of Contents

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ABSOLUTE MAXIMUM RATINGS with respect to GND

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Monitor or Supply	V_{DDM}, V_3, V_5	V_{DDM} if no internal LDO regulator, V_3 or V_5 if LDO regulator present	–0.3 to 7	V
Terminal VREG			–0.3 to 16	V
Terminals CP1, CP2			–0.3 to 16	V
Logic Inputs AHI, ALO, BHI, BLO, CHI, CLO			–0.3 to 6.5	V
Terminal VBRG			–5 to 55	V
Terminal LSS			–4 to 6.5	V
Terminals SA, SB, SC			–5 to 55	V
Terminals GHA, GHB, GHC			S_x to S_x+15	V
Terminals GLA, GLB, GLC			–5 to 16	V
Terminals CA, CB, CC			–0.3 to S_x + 15	V
Terminal FAULT			–0.3 to 6.5	V
Terminal VDSTH			–0.3 to 6.5	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		165	°C
Transient Junction Temperature	T_{tJ}	Over temperature event not exceeding 10s, lifetime duration not exceeding 10hours, determined by design characterization.	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
LP PACKAGE				
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	°C/W
		On 2-layer PCB with 3.8 in^2 copper each side	32	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W
ET PACKAGE				
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	32	°C/W
		On 2-layer PCB with 0.7 in^2 copper each side	64	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro website.

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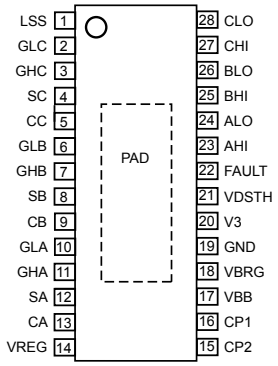
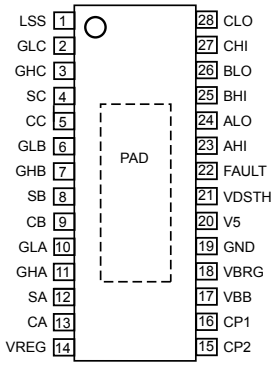
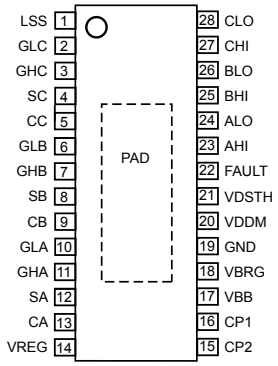
Pinout Diagrams



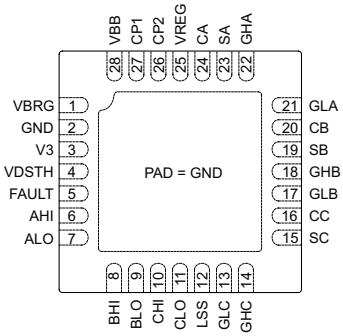
LP Package
A4939x-3 variant



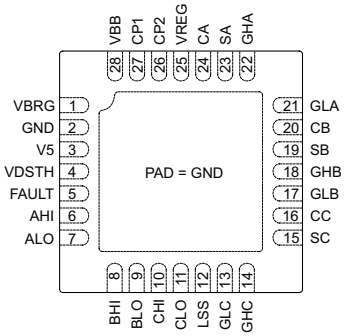
LP Package
A4939x-5 variant



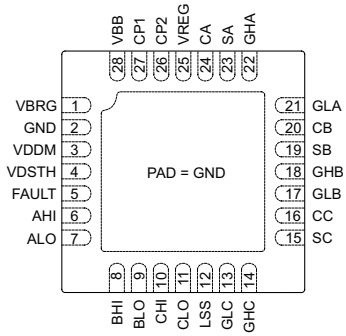
LP Package
A4939x (No LDO) variant



ET Package
A4939x-3 Variant



ET Package
A4939x-5 Variant



ET Package
A4939x (No LDO) Variant

Terminal List Table

Name	Number		Function
	LP Pkg	ET Pkg	
LSS	1	12	Low-side Source
GLC	2	13	Low-side Gate Drive Phase C
GHC	3	14	High-side Gate Drive Phase C
SC	4	15	Motor Connection Phase C
CC	5	16	Bootstrap Capacitor Phase C
GLB	6	17	Low-side Gate Drive Phase B
GHB	7	18	High-side Gate Drive Phase B
SB	8	19	Motor Connection Phase B
CB	9	20	Bootstrap Capacitor Phase B
GLA	10	21	Low-side Gate Drive Phase A
GHA	11	22	High-side Gate Drive Phase A
SA	12	23	Motor Connection Phase A
CA	13	24	Bootstrap Capacitor Phase A
VREG	14	25	Gate Drive Supply Output
CP2	15	26	Pump Capacitor

Name	Number		Function
	LP Pkg	ET Pkg	
CP1	16	27	Pump Capacitor
VBB	17	28	Main Power Supply
VBRG	18	1	High-side bridge voltage sense
GND	19	2	Ground
V3 V5 VDDM	20	3	Voltage Supply (Output) – A4939x-3 Voltage Supply (Output) – A4939x-5 Monitor Input – A4939x (No LDO)
VDSTH	21	4	VDS Monitor Threshold Voltage
FAULT	22	5	Programmable diagnostic output
AHI	23	6	Phase A high-side control input
ALO	24	7	Phase A low-side control input
BHI	25	8	Phase B high-side control input
BLO	26	9	Phase B low-side control input
CHI	27	10	Phase C high-side control input
CLO	28	11	Phase C low-side control input
Pad	–	–	Exposed thermal pad on underside

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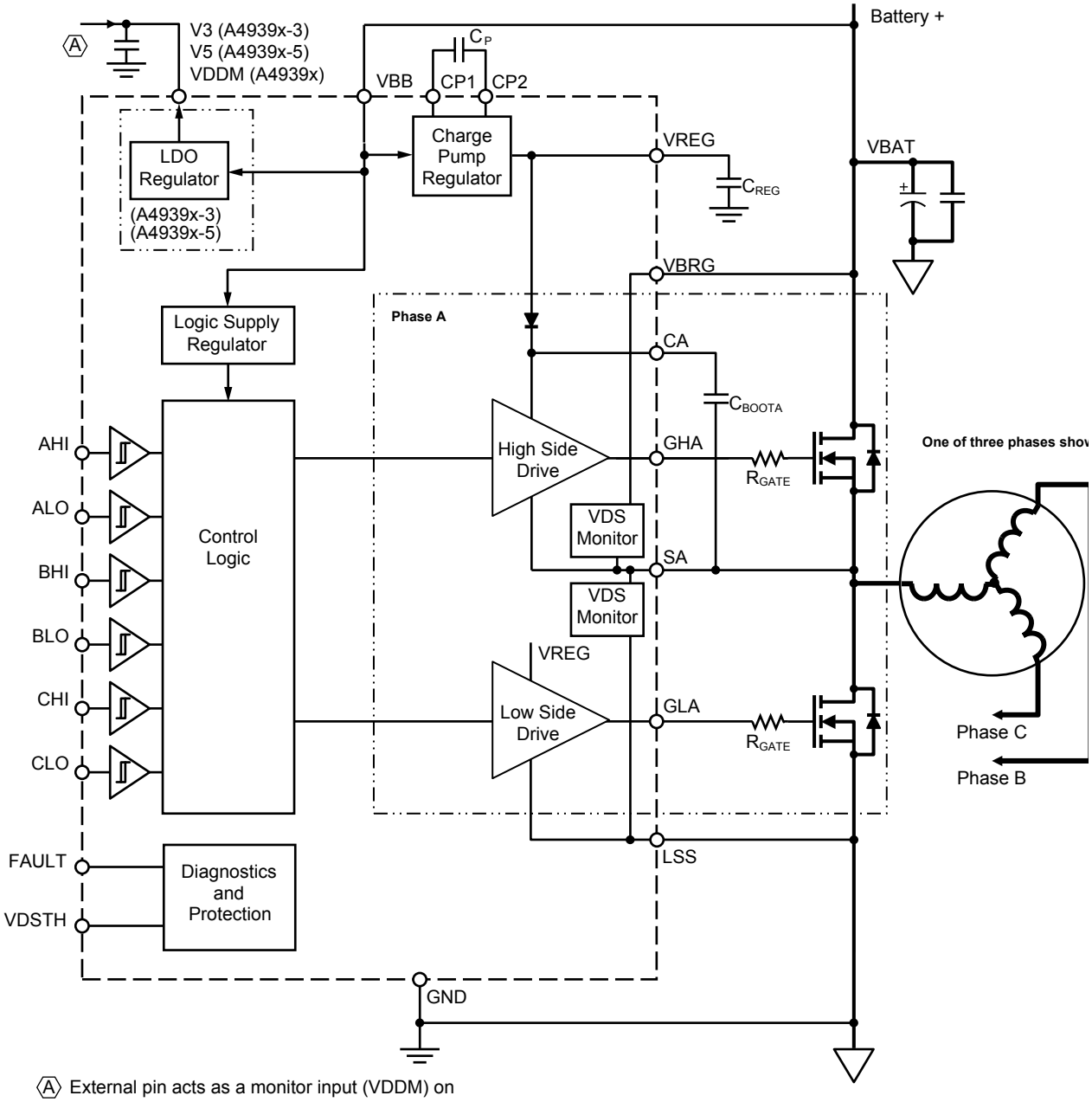

A External pin acts as a monitor input (VDDM) on variants without LDO regulator, and a supply voltage output on variants with LDO regulator (designated V3 or V5 for 3.3 V and 5.0 V variants respectively)

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 50 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
V_{BB} Functional Operating Range [2]	V_{BB}	Correct function, parameters not guaranteed	5.5	–	50	V
VBB Quiescent Current [3]	I_{BBQ}	Operational mode, outputs low, V_{BB} = 12 V	–	10	14	mA
	I_{BBS}	Sleep mode, V_{BB} = 12 V (A4939x, No LDO, variant)	–	–	15	µA
VREG Output Voltage	V_{REG}	V_{BB} > 9 V, I_{REG} = 0 to 15 mA	12.5	13	13.75	V
		7.5 V < $V_{BB} \leq$ 9 V, I_{REG} = 0 to 10 mA	12	13	13.75	V
		6 V < $V_{BB} \leq$ 7.5 V, I_{REG} = 0 to 9 mA	$2 \times V_{BB}$ – 3.0	–	–	V
		5.5 V < $V_{BB} \leq$ 6 V, I_{REG} < 8 mA	8.5	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	3.1	V
Bootstrap Diode Resistance	r_D	$r_{D(100mA)} = (V_{fBOOT(150mA)} - V_{fBOOT(50mA)}) /$ 100 (mA)	6	13	28	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
GATE OUTPUT DRIVE						
Turn-On Time	t_r	CLOAD = 1nF, 20% to 80%	–	35	–	ns
Turn-Off Time	t_f	CLOAD = 1nF, 80% to 20%	–	20	–	ns
Pull-Up On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –150 mA	5	8	13	Ω
		T_J = 150°C, I_{GHx} = –150 mA	10	15	24	Ω
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 150 mA	1.5	2.4	4.6	Ω
		T_J = 150°C, I_{GLx} = 150 mA	2.5	4	6.5	Ω
GHx Output Voltage – High	V_{GHH}	Bootstrap capacitor fully charged	V_{Cx} – 0.2	–	–	V
GHx Output Voltage – Low	V_{GHL}		–	–	V_{SX} + 0.3	V
GLx Output Voltage – High	V_{GLH}		V_{REG} – 0.2	–	–	V
GLx Output Voltage – Low	V_{GLL}		–	–	V_{LSS} + 0.3	V
GHx Passive Pull-Down Resistance	R_{GHPD}	$V_{GHx} - V_{Sx}$ < 0.3 V	–	400	–	kΩ
GLx Passive Pull-Down Resistance	R_{GLPD}	$V_{GLx} - V_{LSS}$ < 0.3 V	–	400	–	kΩ
Turn-Off Propagation Delay [4]	$t_{P(off)}$	Input change to unloaded gate output change	60	90	180	ns
Turn-On Propagation Delay [4]	$t_{P(on)}$	Input change to unloaded gate output change	60	90	180	ns
Propagation Delay Matching – Phase to Phase	Δt_{PP}	Same phase change	–	10	–	ns
Propagation Delay Matching – On to Off	Δt_{OO}	Single phase	–	30	–	ns

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 50 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	–	V
Input Hysteresis	V_{Ihys}		100	300	–	mV
Input Pull-Down Resistor (xHI, xLO)	R_{PD}		–	50	–	kΩ
Input Pulse Filter Time (xHI, xLO)	t_{PIN}		–	35	–	ns
VDS Disable Voltage	V_{DSD}		–	–	100	mV
Fault Disable Voltage	V_{FLTD}		–	–	0.5	V
Output Low Voltage (FAULT)	V_{OL}	I_{OL} = 1 mA, no fault indicated	–	0.2	0.4	V
Output Leakage (FAULT) [5]	I_O	0 V < V_O < 5.5 V, fault indicated	–1	–	1	µA
PROTECTION						
VREG Undervoltage Lockout	V_{REGON}	VREG rising	7.5	8	8.5	V
	V_{REGOFF}	VREG falling	6.75	7.25	7.75	V
Bootstrap Undervoltage Threshold	V_{BOOTUV}	VBOOT falling, VCx – VSx	62	–	75	%V_{REG}
Bootstrap Undervoltage Hysteresis	$V_{BOOTHys}$		–	9	–	%V_{REG}
VDDM / V3 / V5 Undervoltage Threshold [6]	V_{DDUV}	Voltage falling	2.45	2.7	2.85	V
VDDM / V3 / V5 Undervoltage Hysteresis [6]	$V_{DDUVHys}$		40	100	160	mV
VDS Threshold – Internal	V_{DSTHI}	V_{DSTH} > 2.7 V	1.1	1.2	1.3	V
VDS Threshold Range	V_{DSTH}		0.2	–	2	V
VDS Threshold Input Leakage	V_{DSTHL}	0 V < V_{DSTH} < 5.5 V	– 3	–	3	µA
VBRG Input Voltage	V_{BRG}		V_{BB} – 1	V_{BB}	V_{BB} + 1	V
VBRG Input Current	I_{VBRG}	V_{DSTH} = 2 V, V_{BB} = 12 V, 0 V < V_{BRG} < V_{BB}	–	–	250	µA
Short-to-Ground Threshold Offset	V_{STGO}	V_{DSTH} ≥ 1 V	–	±100	–	mV
		V_{DSTH} < 1 V	–150	±50	+150	mV
Short-to-Battery Threshold Offset	V_{STBO}	V_{DSTH} ≥ 1 V	–	±100	–	mV
		V_{DSTH} < 1 V	–150	±50	+150	mV
VDS Fault Blank Time	t_{BL}		1.5	2.3	4.5	µs
Overtemperature Warning	T_{JF}	Temperature increasing	170	–	180	°C
Overtemperature Hysteresis	T_{JHyst}	Recovery = T_{JF} – T_{JHyst}	–	15	–	°C
VARIANT WITHOUT LDO REGULATOR ONLY (A4939X)						
Input Low Voltage For Sleep Mode	V_{ILS}	xHI, xLO	–	–	0.5	V
Sleep Mode Activation Timeout (xHI, xLO) [3]	t_{SLT}	From all xHI, xLO < V_{IL}	7.5	10	12.5	ms
Wake-Up from Sleep Delay [3]	t_{WK}	Any xHI, xLO > V_{IH}, C_{REG} < 1 µF	–	–	1	ms
Gate Drive Disable Threshold	V_{GDD}		–	1.5	–	V
VDDM Pull-Down Resistor	R_{VDDM}		–	60	–	kΩ

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 50 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
5 V LDO REGULATOR VARIANT ONLY (A4939X-5) [7]						
V5 Output Voltage	V_5	I_{V5} < 70 mA, V_{BB} > 6 V	4.85	–	5.25	V
		5 mA < I_{V5} < 25 mA	4.9	5.0	5.2	V
V5 Output Overcurrent Limit	$I_{LDOOC(V5)}$		130	–	260	mA
V5 Shutdown Voltage Threshold	$V_{LDOSD(V5)}$	Voltage falling	450	–	850	mV
V5 Shutdown Voltage Hysteresis	$V_{LDOHys(V5)}$		80	–	200	mV
V5 Pilot Current [8]	$I_{LDOP(V5)}$	LDO regulator shut down	–	2	–	mA
V5 Shutdown Lockout Period	$t_{LDOL(V5)}$	From V_5 < $V_{LDOSD(V5)}$	–	2	–	ms
3 V LDO REGULATOR VARIANT ONLY (A4939X-3) [7]						
V3 Output Voltage	V_3	I_{V3} < 70 mA, V_{BB} > 6 V	3.15	–	3.53	V
		5 mA < I_{V3} < 25 mA	3.2	3.3	3.5	V
V3 Output Overcurrent Limit	$I_{LDOOC(V3)}$		130	–	260	mA
V3 Shutdown Voltage Threshold	$V_{LDOSD(V3)}$	Voltage falling	450	–	850	mV
V3 Shutdown Voltage Hysteresis	$V_{LDOHys(V3)}$		80	–	200	mV
V3 Pilot Current [8]	$I_{LDOP(V3)}$	LDO regulator shut down	–	2	–	mA
V3 Shutdown Lockout Period	$t_{LDOL(V3)}$	From V_3 < $V_{LDOSD(V3)}$	–	2	–	ms

[1] Specifications presented apply to all product variants except where variant-specific limitations are explicitly defined.
[2] Function is correct but parameters are not guaranteed below the general limits (7 V).
[3] Sleep mode entered after logic low (less than V_{IL}) simultaneously detected on all xLO and xHI inputs for a period of t_{SLT}. Operating mode resumed within t_{WK} of logic high (greater than V_{IL}) being detected on any of the xLO or xHI pins.
[4] See figure 1 for gate drive output timing.
[5] For input and output current specifications, negative current is defined as coming out of (sourced by) the specified device terminal.
[6] On product variants with LDO regulator (A4939x-3 and A4939x-5), an undervoltage trip sets all gate drive outputs low and an unlatched fault state on the FAULT pin. On product variants without LDO regulator (A4939x), an undervoltage trip has no effect on device operation but sets an unlatched fault state on the FAULT pin.
[7] A capacitance of at least 1 µF with an ESR of no more than 250 mΩ should be fitted between the LDO V3 / V5 output and GND to ensure stability.
[8] Pilot current is disabled while the overtemperature warning is active.

Figure 1: Gate Drive Timing

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Functional Description

The A4939 provides six high current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three high-side drives and three low-side. The six gate drives are controlled by individual TTL-threshold logic inputs which may be driven from 3.3 V or 5 V logic outputs.

The A4939 provides all necessary circuitry to ensure that the gate-source turn-on voltages of both high-side and low-side external MOSFETs are driven above 10 V at supply voltages down to 7 V. For extreme low battery voltage conditions, correct functional operation is maintained down to 5.5 V but with a reduced gate drive.

The control inputs to the A4939 provide a simple solution for many motor drive applications controlled by an external microcontroller or DSP. Phase commutation and PWM control must be managed by the external system controller.

Specific device functions are described more fully in the following sections.

Input and Output Terminal Functions

VBB. Power supply for all device functions including internal logic and charge pump. Also used to power the LDO regulator where present.

System power should be connected to VBB through a reverse voltage protection circuit. The VBB pin should be decoupled to ground with ceramic capacitors mounted physically close to the device pins.

VDDM. Unique to parts without an LDO regulator. It does not provide power to support external circuitry and must be connected to the system logic supply voltage or similar.

If the voltage applied on VDDM drops below the VDDUV undervoltage threshold (2.7 V typ) an unlatched fault condition is set on the FAULT pin. If it rises above V_{DDUV} +$V_{DDUVHys}$ the fault condition is cleared. Additionally, if the voltage on VDDM drops below the V_{GDD} gate drive disable threshold (1.5 V typ) the charge pump is turned off and all gate drive outputs are disabled. If it rises above V_{GDD} the charge pump restarts and all gate drives are enabled. A pull-down resistance (60 kΩ typical) is connected from VDDM to ground within the device

V3. Unique to A4939x-3 variant (has a 3.3 V LDO regulator). Sources 3.3 V to power external circuitry but does not power any on-chip functions. Must be loaded with appropriate capacitance as detailed in the Electrical Characteristics table.

V5. Unique to A4939x-5 variant (has a 5 V LDO regulator). Sources 5 V to power external circuitry but does not power any on-chip functions. Must be loaded with appropriate capacitance as detailed in the Electrical Characteristics table.

CP1, CP2. Pump capacitor connection for charge pump. Connect a minimum 220 nF capacitor, typically 470 nF, between CP1 and CP2.

VREG. Regulated voltage, nominally 13 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.

GND. Analog reference, digital, and power ground. Connect to supply ground (see Layout Recommendations section).

CA, CB, CC. High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC. High-side, gate-drive outputs for external N-channel MOSFETs.

SA, SB, SC. Motor phase connections. Used to sense the voltages switched across the load. Also connected to the negative side of the bootstrap capacitors and constitute the negative supply connections for the floating high-side drivers.

GLA, GLB, GLC. Low-side, gate-drive outputs for external N-channel MOSFETs.

LSS. Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs through a low impedance PCB trace.

VBRG. Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drains of the high side MOSFETs.

AHI, BHI, CHI. Input to control the high-side gate drives. A logic high on the pin commands the relevant high-side gate drive to be activated.

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ALO, BLO, CLO. Input to control the low-side gate drives. A logic high on the pin commands the relevant low-side gate drive to be activated.

FAULT. Open drain active-high fault output. If a fault is present the open-drain pull-down is off and the FAULT output may be pulled high by an external pull-up resistor connected to any voltage up to a maximum of 5.5 V.

VDSTH. Drain source fault threshold programming pin. The VDS fault threshold may be set by applying an externally generated analog voltage. VDS fault reporting is disabled if VDSTH is driven to less than V_{DSD} (for example, shorted to ground). The VDS fault threshold is set to an internally hardwired value, V_{DSTHI}, if VDSTH is driven to a voltage above its specified analog input range (for example, pulled-up to the system logic supply voltage).

Power Supplies

A single supply voltage applied to the VBB pin powers all device functions including on-chip logic, analog circuitry, output drivers and the LDO regulator (where present). The supply should be connected to VBB through a reverse voltage protection circuit and decoupled by way of a ceramic capacitor mounted close to the VBB and GND terminals. All variants of the A4939 will operate within specified performance limits with V_{BB} between 7 and 50 V, and will function correctly with V_{BB} as low as 5.5 V.

CP1, CP2, VREG

The gate drivers are powered by an internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. For VBB supply greater than approximately 16 V, the regulator is a simple buck regulator. Below 16 V, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals. The regulated voltage, nominally 13 V, is available on the VREG terminal. A sufficiently large storage capacitor (see the Applications Information section) must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors.

Sleep Mode

A low power Sleep mode is available on the A4939x (no LDO regulator) variant. It is activated after logic low states compatible with the Input Logic Low Voltage For Sleep (V_{ILS}) are detected simultaneously on all xLO and xHI inputs for a period equal to the Sleep Mode Activation Timeout (t_{SLT}). In Sleep mode all outputs are switched to a high impedance state.

Operating mode is activated within a period equal to the Wake-up from Sleep Delay (t_{WK}) from when a logic high is detected on any of the xLO or xHI pins. In operating mode logic low control states applied on the xHI, xLO inputs need only comply with the Input Low Voltage (V_{IL}) and not the lower Input Logic Low Voltage For Sleep (V_{ILS}). It is recommended that all xLO inputs are simultaneously driven to logic high (GLx turned on) when waking from Sleep mode, in order to recharge the bootstrap capacitors and enable subsequent high-side turn on.

Sleep mode is not available on A4939x-3 and A4939-5 (LDO regulator) variants. If all logic inputs are taken low, power consumption remains unchanged and all functions remain operational.

Gate Drives

The A4939 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitances in order to reduce dissipation in the external MOSFET during switching. Charge current for the low-side drives is provided directly by the capacitor on the VREG terminal. Charge current for the high-side drives is delivered via the bootstrap capacitors connected, one per phase, across the Cx – Sx terminal pairs. Charge and discharge rate can be controlled by incorporating an external resistor in series with each MOSFET gate drive (GHx, GLx).

High-Side Gate Drives (GHA, GHB, GHC)

These are the high-side gate drive outputs for external N-channel MOSFETs. An external resistor between the GHx gate drive output and the MOSFET gate terminal (mounted as close to the latter as possible) may be used to control the slew rate at the gate, thereby controlling the di/dt and dv/dt at the Sx terminals. Setting GHx high turns-on the upper half of the driver, sourcing current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. Setting GHx low turns-on the lower half of the driver, sinking current from the external MOSFET gate circuit to the respective Sx terminal, turning it off.

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Bootstrap Charge Management

Bootstrap capacitors are charged to approximately V_{REG} when the associated Sx terminal is driven low. When the Sx terminal subsequently goes high, the capacitor provides the necessary voltage for high-side N-channel power MOSFET turn-on. At system start-up it is necessary to turn on each low-side drive (GLx) prior to attempting to turn on the complementary high-side (GHx), in order to charge the bootstrap capacitors.

Low-Side Gate Drive (GLA, GLB, GLC)

The low-side, gate-drive outputs on GLA, GLB, and GLC are referenced to the LSS terminal. These outputs are designed to drive external N-channel power MOSFETs. An external resistor between the GLx gate drive output and the MOSFET gate terminal (mounted as close to the latter as possible) may be used to control the slew rate at the gate, thereby providing some control of the di/dt and dv/dt at the Sx terminals. Setting GLx high turns-on the upper half of the driver, sourcing current to the gate of the low-side MOSFET in the external motor-driving bridge, turning it on. Setting GLx low turns-on the lower half of the driver, sinking current from the external MOSFET gate circuit to the to the LSS terminal, turning it off.

Drain Source Voltage Monitor

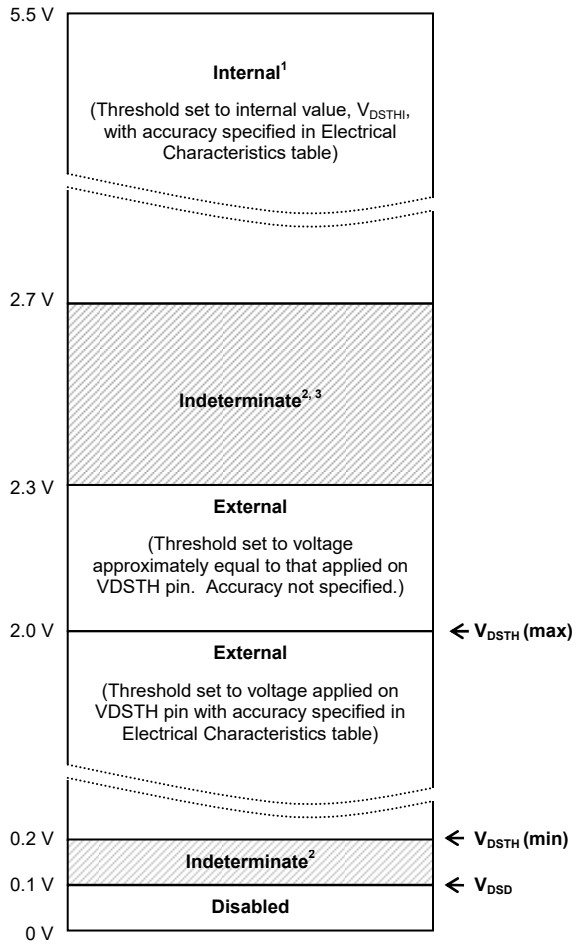
The VDS fault threshold is set by applying a control voltage on the VDSTH pin, as detailed in figure 2. If a voltage between 0.2 and 2.0 V is applied, the threshold follows this level, subject to the Short to Ground Threshold (V_{STGO}) and Short to Battery Threshold (V_{STBO}) offsets detailed in the Electrical Characteristics table.

If a voltage between 2.0 and 2.3 V is applied, the threshold approximates the applied level, but accuracy is not specified.

If the VDSTH pin is driven below the VDS Disable Voltage (V_{DSD}), 0.1 V (such as when shorted to ground), VDS fault reporting is disabled.

If the VDSTH pin is taken above 2.7 V (such as when pulled up to the system logic supply voltage) the threshold is set to the VDS Threshold Internal voltage (V_{DSTH}), detailed in the Electrical Characteristics table (typically 1.2 V).

The VDSTH pin presents a high impedance at all voltages across its permissible input range (per the VDS Threshold Input Leakage limits, V_{DSTHL}, detailed in the Electrical Characteristics table) allowing a wide range of programming circuits to be used including simple resistive dividers.



[1] VDSTH pin typically tied to system logic supply voltage (for example, V3 or V5)

[2] Behavior indeterminate due to threshold detection uncertainty

[3] Threshold range confirmed by design

Figure 2: V_{DSTH} Pin Voltage versus V_{DS} Monitor Function

The VDSTH input has an internal passive first-order filter with a time constant of approximately 0.01 ms. Additional filter capacitance may be added externally if required.

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Logic Control Inputs

A set of discrete digital inputs (xHI and xLO) provides direct control of the six gate drive outputs (GHx and GLx). TTL input threshold levels ensure these can be driven from 3.3 V or 5 V logic systems. Setting a logic input high causes the corresponding gate drive output to go high, thereby commanding the associated external MOSFET to turn on. Conversely, setting a logic input low causes the corresponding gate drive to go low, commanding the MOSFET to turn off.

Internal lock-out logic, detailed in table 1, ensures that the high-side output drive and low-side output drive cannot be active simultaneously.

Table 1: Phase Control Truth Table

Input		Output		Phase	
xHI	xLO	GHx	GLx	Sx	Comment
0	0	L	L	Z	Phase disabled
0	1	L	H	LO	Low-side active
1	0	H	L	HI	High-side active
1	1	L	L	Z	Phase disabled

HI = high-side MOSFET active
LO = low-side MOSFET active
Z = high impedance, both MOSFETs off

Diagnostics

Several diagnostic features are integrated into the A4939 to indicate fault conditions. In addition to system-wide faults such as undervoltage and overtemperature, the A4939 integrates individual monitors for each bootstrap capacitor voltage and each external MOSFET drain-source voltage.

The presence of a fault condition is indicated on the FAULT pin. This is an open drain output that should be pulled to any voltage, up to 5.5 V, by an external resistor, typically 10 to 47 kΩ. The definition of the individual fault states and the effects on the gate drive outputs (GHx and GLx) are shown in table 2 and described below.

Fault States

It is recommended that any external control circuitry remaining active in the event of a fault state being flagged be configured to take appropriate action to prevent damage to the A4939 and associated motor drive components.

Overtemperature. If the junction temperature exceeds the overtemperature warning threshold (T_{JF}), the A4939 enters the overtemperature warning state and FAULT goes high. When the junction temperature drops below the recovery level (T_{JF} – $T_{JF\,hys}$), the overtemperature warning state is cleared and the FAULT output returned to logic low.

While an overtemperature warning state is being asserted, no on-chip circuitry or functions are disabled, with the exception of the LDO regulator on the A3939x-3 and A4939x-5 variants, which is shut down immediately and remains off until the overtemperature warning state is cleared.

Table 2: Fault Definitions

FAULT Pin State	Fault Description	Outputs Disabled	Fault Latched
Low	No fault	No	–
High	Overtemperature	No	No
High	VDDM undervoltage (A4939x variant, without LDO) V3 or V5 undervoltage (A4939x-3 and A4939x-5 variants, with LDO)	All gate drives enabled for $V_{DDM} > V_{GDD}$. All gate drives low (external MOSFETs off) for $V_{DDM} \le V_{GDD}$ All gate drives low (external MOSFETs off)	No
High	VREG undervoltage	All gate drives low (external MOSFETs off)	No
High	VDS overvoltage	No	No
High	Bootstrap undervoltage	High-side drive of the output phase that is generating the fault condition is set low (external MOSFET off). Other outputs unaffected.	Yes

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VREG Undervoltage. The charge pump generates V_{REG} to provide low-side gate driver and bootstrap charge current. It is necessary to ensure that this voltage is high enough prior to enabling any of the gate drive outputs. If the voltage at the VREG pin drops below the VREG Undervoltage Lockout Threshold (falling), V_{REGOFF}, the A4939 enters the VREG undervoltage fault state, FAULT is set high, and all gate drive outputs (GHx and GLx) are disabled. The VREG undervoltage fault state is cleared and FAULT goes low when VREG rises above the VREG Undervoltage Lockout Threshold (rising), V_{REGON}.

During power-up, the VREG undervoltage monitor circuit is active and the A4939 remains in the VREG undervoltage fault state until VREG is greater than the rising VREG Undervoltage Lockout Threshold (V_{REGON}, rising).

VDDM / V3 / V5 Undervoltage. The voltage on the VDDM / V3 / V5 pin is monitored on all part variants. If it drops below the VDDM / V3 / V5 undervoltage threshold, V_{DDUV}, the A4939 enters the VDDM/V3/V5 undervoltage state and FAULT is set high. On part variants with LDO regulator functionality all gate drive outputs (GHx, GLx) are disabled. On the part variant without LDO functionality all gate drive outputs remain active unless the applied voltage also drops below the gate drive disable threshold, V_{GDD}. The VDDM/V3/V5 undervoltage fault state is cleared and FAULT goes low when the voltage on VDDM / V3 / V5 pin rises above V_{DDUV}+$V_{DDUVhys}$.

During power-up the VDDM/V3/V5 undervoltage monitor circuit is active and all variants of the A4939 remain in the VDDM/V3/V5 undervoltage fault state until the voltage on the VDDM/V3/V5 pin is greater than the VDDM/V3/V5 undervoltage threshold plus hysteresis, V_{DDUV}+$V_{DDUVhys}$.

VDS Overvoltage. When a gate drive output is commanded to turn on (GHx or GLx high), the drain-source voltage of the corresponding external MOSFET is monitored between VBRG and Sx, or between Sx and LSS, as appropriate. If the measured voltage exceeds the threshold value programmed on the VDSTH pin, the FAULT output is set high but none of the gate drive outputs is disabled.

Propagation of any fault states to the FAULT output is disabled for the VDS Fault Blank Time (t_{BL}) commencing at every external MOSFET turn-on event to avoid reporting spurious faults in response to switching transients. If a fault is reported on the FAULT pin it will be cleared as soon as the measured drain-source voltage drops below the programmed VDSTH level.

Bootstrap Capacitor Undervoltage. Each bootstrap capacitor is monitored to ensure sufficient high-side gate drive voltage is available to initiate and maintain external MOSFET turn-on.

High-side gate drive outputs turn on only if the relevant bootstrap capacitor voltage is higher than the bootstrap turn-on voltage threshold, V_{BOOTUV} + $V_{BOOTHys}$. If the bootstrap voltage is below this threshold when turn-on is commanded (on the xHI pin), the corresponding gate drive, GHx, is not switched on and FAULT is set high. The output remains off and FAULT remains high until either the affected gate drive is commanded to turn off, or the FAULT pin is pulled low by external means (see the FAULT Disable description, below).

After a high-side gate drive has been successfully turned on, the appropriate bootstrap capacitor voltage must remain above the Bootstrap Undervoltage Threshold, V_{BOOTUV}. If the bootstrap capacitor voltage drops below V_{BOOTUV}, the high-side driver in question is switched off and FAULT goes high. The driver will remain off and FAULT will remain high until either the affected high-side gate drive turn-on command is removed from xHI or the FAULT pin is pulled low by external means (see the FAULT Disable description below).

If a bootstrap capacitor fault condition is detected, only the driver in question is disabled. All other gate drives continue to respond to control inputs on xHI and xLO.

FAULT Disable. If the FAULT pin is held low (below the Fault Disable Voltage, V_{FLTD}) by external means, the bootstrap undervoltage monitor feature is disabled. In this condition, if the bootstrap capacitor voltage fails to reach V_{BOOTUV} + $V_{BOOTHys}$ for turn-on, or if it drops below V_{BOOTUV} after turn-on, the driver in question is not forced into the off state. A fault state is not flagged because the FAULT pin is held low.

While the FAULT pin is held low (to disable the bootstrap undervoltage monitor), any other fault conditions that might arise are undetectable outside the A4939. However, internal fault actions are unaffected and gate drive outputs are still disabled in response to other faults in accordance with table 2.

Low Drop Out (LDO) Regulator

The A4939x-3 and A4939x-5 variants have a linear regulator that provides a low-voltage DC supply to power external circuitry. It is derived from VBB and incorporates a number of protection features.

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An overcurrent circuit limits the output of the regulator in the event of an excessively high load demand being made (load current > I_{LDOOC}).

If the output voltage falls below the regulator undervoltage threshold (V_{DDUV}), a fault state is flagged on the FAULT output to provide an external warning, but device operation remains otherwise unchanged.

If the output voltage falls below the regulator shutdown threshold (V_{LDOSD}, which is lower than the regulator undervoltage threshold) for a period exceeding the Shutdown Lockout Period (t_{LDOL}), the regulator is turned off but all other device functions remain active. In this state a small pilot current (I_{LDOP}), is driven through the regulator output to detect load resistance. If the resultant voltage rises above the regulator shutdown threshold plus hysteresis ($V_{LDOSD} + V_{LDOHys}$), the regulator immediately attempts to restart.

At device power-up, full output current is delivered for a period equal to the Shutdown Lockout Period regardless of output voltage to facilitate reliable regulator startup.

If the device internal temperature rises high enough to generate an Overtemperature Warning ($T > T_{JF}$), the regulator is immediately shut down and the FAULT flag is set. All device functions other than the regulator remain active. When the Overtemperature Warning is cleared ($T < T_{JF} - T_{JHyst}$), the pilot current is turned on and the regulator attempts to restart.

If an undervoltage shutdown ($< V_{LDOSD}$) and an Overtemperature Warning ($T > T_{JF}$) occur simultaneously, both must be cleared to allow the regulator to restart.

Internal device circuitry is not powered from the LDO regulator and remains fully operational regardless of whether the LDO regulator is running normally or is shut down.

As detailed in the Electrical Characteristics table, a minimum capacitance must be connected between the LDO regulator output and ground to ensure stability. Running the device with significantly less than the stated minimum capacitance may result in oscillation and voltage excursions exceeding the specified V3 or V5 output voltage range. In some applications the use of redundant output capacitors may be advisable to avoid such a condition in the event of a single-point, capacitor-high-impedance failure.

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Applications Information

Power Bridge Management Using PWM Control

The A4939 provides individual high-side and low-side controls for each phase through the six digital control inputs. The only restriction imposed by the A4939 is to prevent both the high-side and low-side gate drives of the same phase from being on at the same time, in order to avoid cross-conduction. This design approach allows almost all 3-phase BLDC bridge control schemes to be implemented. This includes fast and slow decay, synchronous rectification and diode rectification, and edge-aligned and center-aligned PWM.

Figure 3A shows an example of the path of the bridge and load current. In this example, the high-side MOSFETs are switched off during the current decay time (PWM off-time) and load current recirculates through the low-side MOSFETs. This is commonly referred to as high-side chopping or high-side PWM. During the PWM off-time, the complementary MOSFETs are turned on to short the body diode and provide synchronous rectification. Figure 3A only shows one combination of phase states, but the same principal applies to any of the possible phase states. The same principal also applies when the low-side MOSFETs are turned off during the PWM off-time and the load current recirculates through the high-side MOSFETs as in figure 3B. In this control scheme, the microcontroller has full control over the current decay method, load current recirculation paths, braking, and coasting.

The A4939 provides exceptional propagation delay matching from logic input to gate drive output for high performance motor control applications. These advanced applications usually require high-resolution PWM control on each phase. This must be provided by an external controller, which must also provide the necessary dead time to avoid shoot through in the power bridge.

Bootstrap Capacitor Selection

C_{BOOT} must be correctly selected to ensure proper operation of the device. If it is too large, time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency. If it is too small, there can be a large voltage drop at the time the charge is transferred from CBOOT to the MOSFET gate.

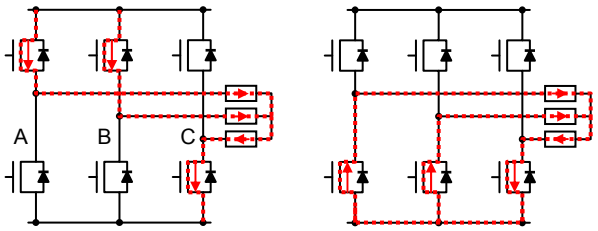
To keep the voltage drop due to charge sharing small, the charge on the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} >> Q_{GATE} \quad (1)$$

A factor of 20 is a reasonable value. C_{BOOT} can then be calculated as:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20, \text{ or} \quad (2)$$
$$C_{BOOT} = (Q_{GATE} \times 20) / V_{BOOT}$$

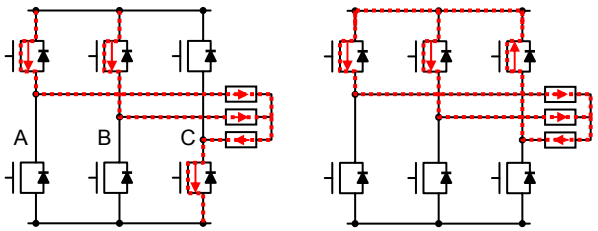
where V_{BOOT} is the voltage across the bootstrap capacitor.



Phase	A	B	C
xH	1	1	0
xL	0	0	1
GHx	H	H	L
GLx	L	L	H

Phase	A	B	C
xH	0	0	0
xL	1	1	1
GHx	L	L	L
GLx	H	H	H

(A) High-side PWM with slow decay and synchronous rectification



Phase	A	B	C
xH	1	1	0
xL	0	0	1
GHx	H	H	L
GLx	L	L	H

Phase	A	B	C
xH	1	1	1
xL	0	0	0
GHx	H	H	H
GLx	L	L	L

(B) Low-side PWM with slow decay and synchronous rectification

Figure 3: Power Bridge Control

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The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on can be approximated by:

$$\Delta V = Q_{GATE} / C_{BOOT} \quad (3)$$

so for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG} (max). However, in some circumstances the voltage may transiently reach 18 V, which is the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications, with a good ceramic capacitor the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = (C_{BOOT} \times \Delta V) / 500 \quad (4)$$

Where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor.

At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can become completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx terminal is pulled low and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

VREG Capacitor Selection

The internal reference, V_{REG}, supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high, transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but instead must be supplied by an external capacitor connected to VREG.

The turn-on current for the high-side MOSFET is similar in value, but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from the VREG regulator output.

Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of the capacitor connected between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. For block commutation motor control, where the number of MOSFETs switching at any one time is limited, a value of 20 × C_{BOOT} is a reasonable value. For sinusoidal or vector motor control (SVM), where several MOSFETs may be switching at the same time, a value of 40 × C_{BOOT} is recommended. The maximum working voltage will never exceed V_{REG} so the capacitor can be rated as low as the terminal. This capacitor should be placed as close as possible to the VREG terminal.

LDO Regulator Capacitor Selection

A capacitor of at least 1 µF, ESR < 250 mΩ should be connected between the V3 / V5 pin and GND on A4939x-3 and A4939x-5 variants to ensure LDO stability.

Supply Decoupling

The switching action associated with device operation will result in current spikes on VBB at each transition. Consequently, VBB should be decoupled to GND with a ceramic capacitor, typically 220 nF, mounted as close to the A4939 pins as possible.

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Input / Output Structures

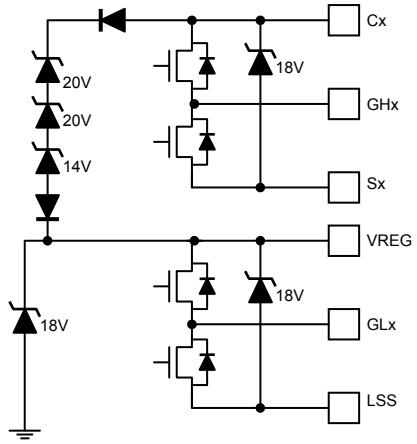

Figure 4a: Gate Drive Outputs

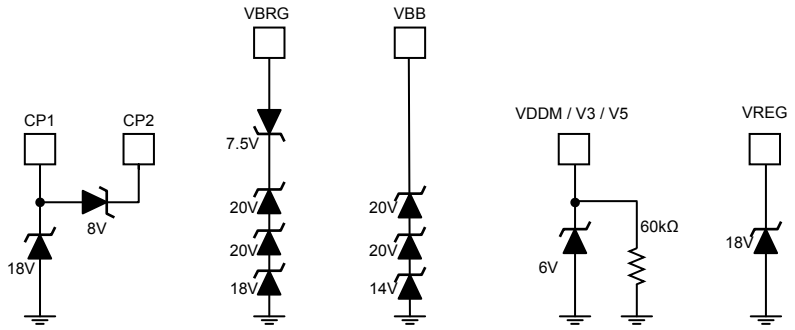

Figure 4b: Supplies

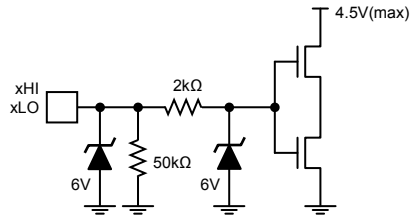

Figure 4c: xHI,xLO Inputs

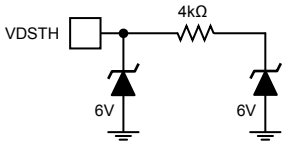

Figure 4d: VDSTH Input

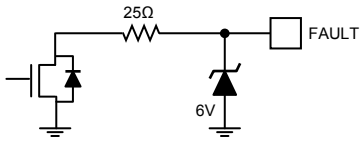

Figure 4e: FAULT Output

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Layout Recommendations

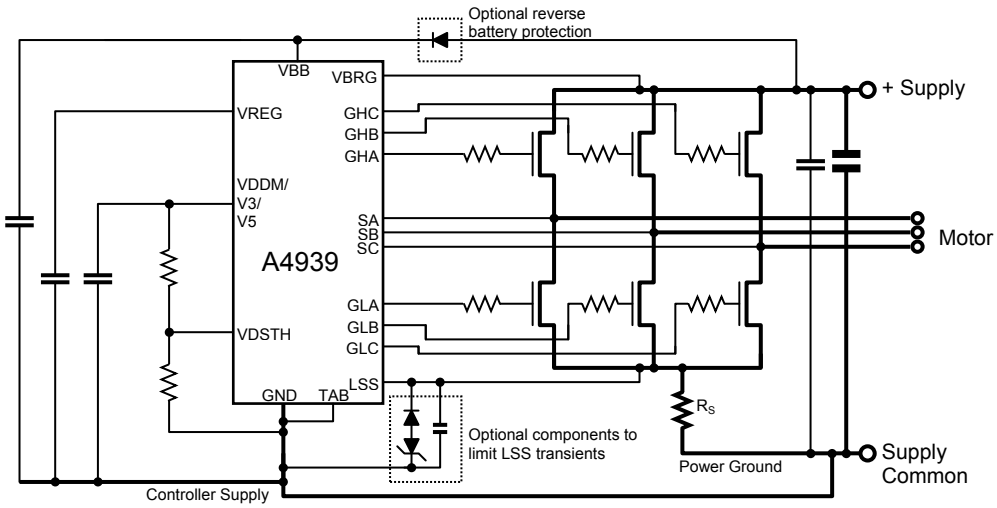

Figure 5: Supply Routing Suggestions

Careful consideration must be given to PCB layout when designing high frequency, fast-switching, high-current circuits:

• The A4939 ground, GND, and the high-current return of the external MOSFETs should return separately to the negative side of the motor supply filtering (DC-link) capacitor. This will minimize the effect of bridge switching noise on the A4939.

• The exposed thermal pad should be connected to GND.

• Minimize stray inductance by using short, wide copper PCB traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

• Consider the use of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by circuit trace inductance.

• Keep the gate discharge return connections Sx and LSS as short as possible. Any inductance on these traces will cause negative transitions on the corresponding A4939 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to GND.

• The threshold programming network associated with the VDSTH input, including suitable supply decoupling, should be located as close to the device pins as possible. All connections should take the form of short, dedicated traces. If VDSTH is directly strapped to a logic supply or GND, this should similarly be by way of a short, dedicated trace.

• Check the peak voltage excursion of the transients on the LSS terminal with reference to the GND terminal using a close-grounded (tip and barrel) probe. If the voltage at LSS exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSS terminal and the GND terminal as shown.

• Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore, the traces from GHx, GLx, Sx (x = A, B or C) and LSS should be a short as possible to minimize trace inductance.

• Provide an independent connection from LSS to the common point of the power bridge. It is not recommended to connect LSS directly to the GND terminal as this may inject noise into sensitive functions such as the various voltage monitors.

• A low-cost diode can be placed in the connection to VBB to provide reverse battery protection. In reverse battery conditions it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case the additional diode in the VBB connection will prevent damage to the A4939 and the VBRG terminal will survive the reverse voltage.

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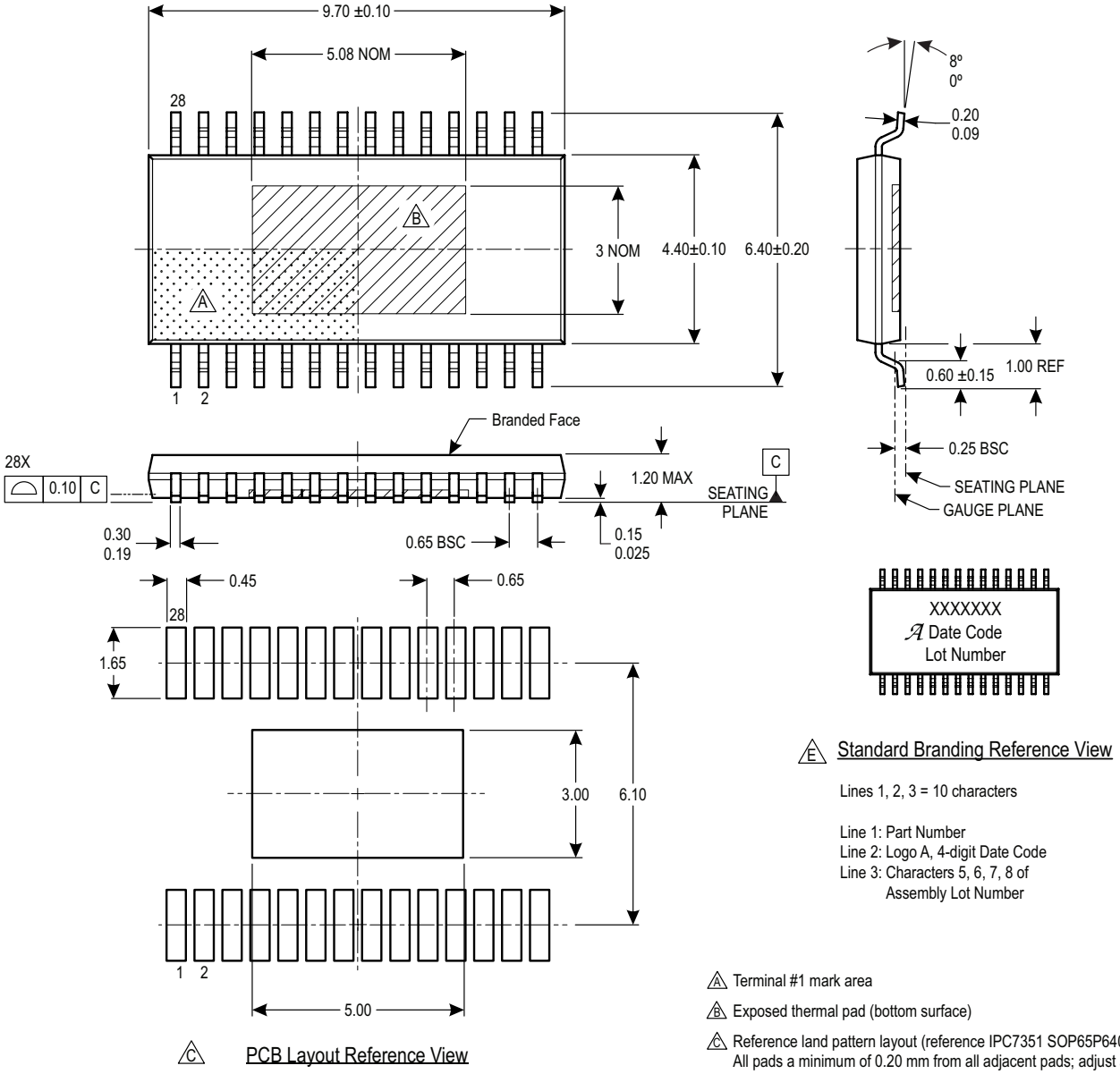
Package Outline Drawings

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153AET)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

E Standard Branding Reference View

Lines 1, 2, 3 = 10 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion.

Figure 6: Package LP, 28-Pin TSSOP with Exposed Thermal Pad

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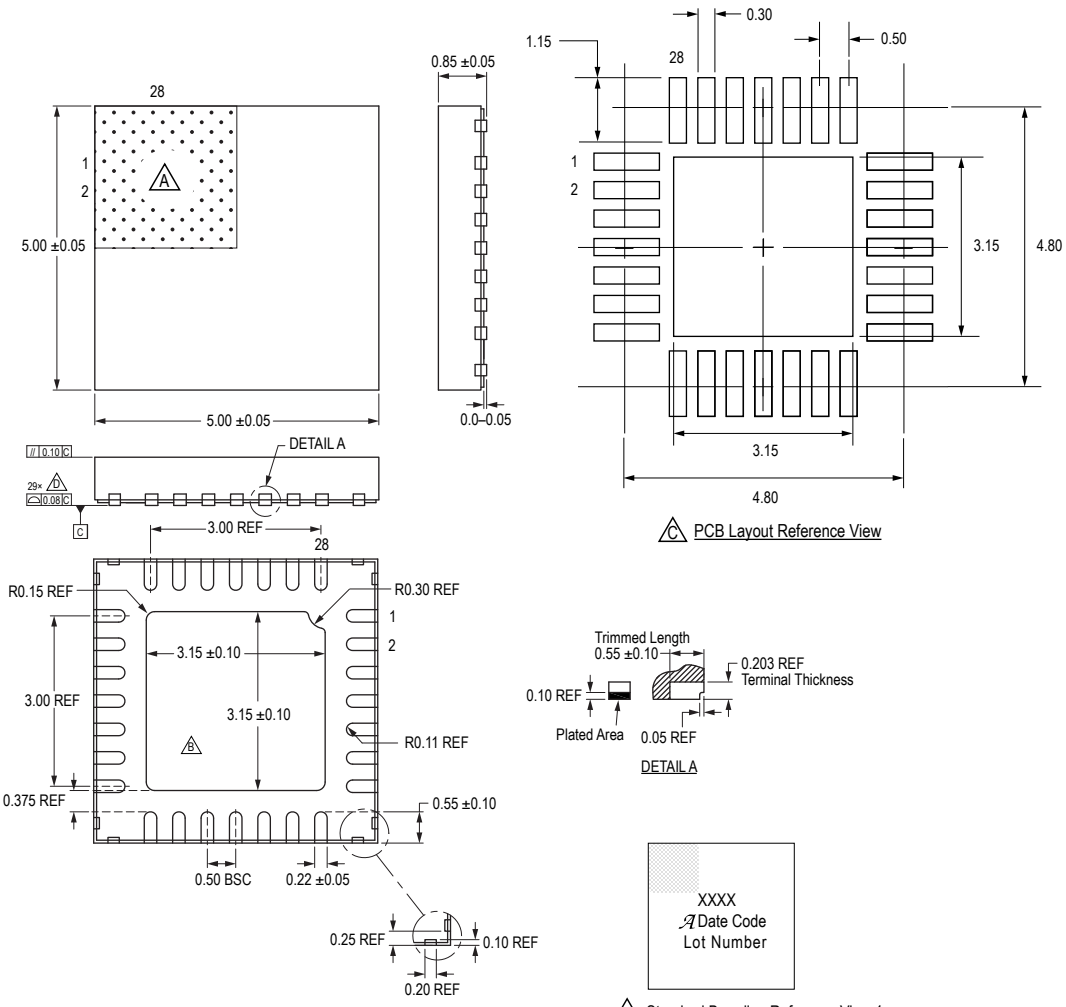

For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 7: Package ET, 28-Pin QFN with Exposed Thermal Pad and Wettable Flank

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REVISION HISTORY

Number	Date	Description
1	March 21, 2014	Revised Electrical Characteristics table
2	November 11, 2014	Added new V_{GDD} parameter and new JET package
3	February 13, 2020	Minor editorial updates
4	February 8, 2022	Updated package drawings (pages 19-20)

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