



**THE DATASHEET OF  
74LV165AD,118**





# 74LV165A

## 8-bit parallel-in/serial-out shift register

Rev. 5 — 18 April 2024

Product data sheet

### 1. General description

The 74LV165A is an 8-bit parallel-load or serial-in shift register with complementary serial outputs ( $Q7$  and  $\overline{Q7}$ ) available from the last stage. When the parallel-load input ( $\overline{PL}$ ) is LOW, parallel data from the inputs  $D0$  to  $D7$  are loaded into the register asynchronously. When input  $\overline{PL}$  is HIGH, data enters the register serially at the input  $DS$ . It shifts one place to the right ( $Q0 \rightarrow Q1 \rightarrow Q2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output  $Q7$  to the input  $DS$  of the succeeding stage.

The clock input is a gate-OR structure which allows one input to be used as an active LOW clock enable input ( $\overline{CE}$ ) input. The pin assignment for the inputs  $CP$  and  $\overline{CE}$  is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input  $\overline{CE}$  should only take place while  $CP$  HIGH for predictable operation.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times. It is fully specified for partial-power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging current backflow through the device when it is powered down.

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- CMOS LOW power consumption
- 5.5 V tolerant inputs/outputs
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
  - JESD8-1A (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LV165AD</a>	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">74LV165APW</a>	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>

### 4. Functional diagram

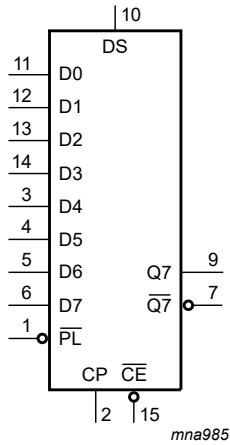


Fig. 1. Logic symbol

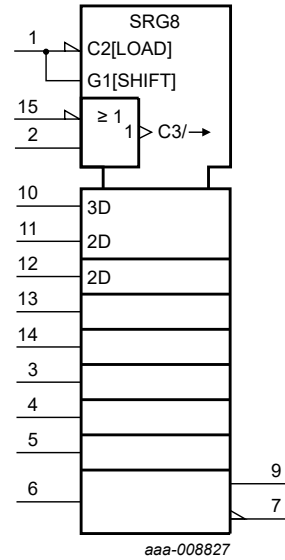


Fig. 2. IEC logic symbol

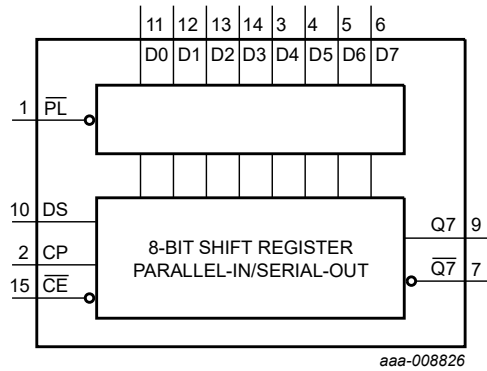


Fig. 3. Functional diagram

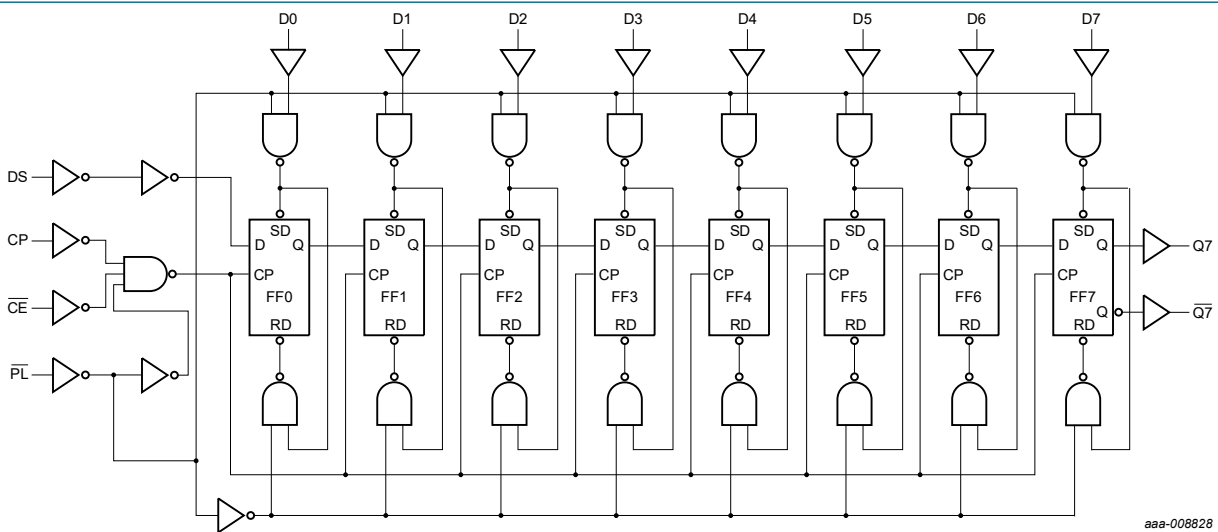
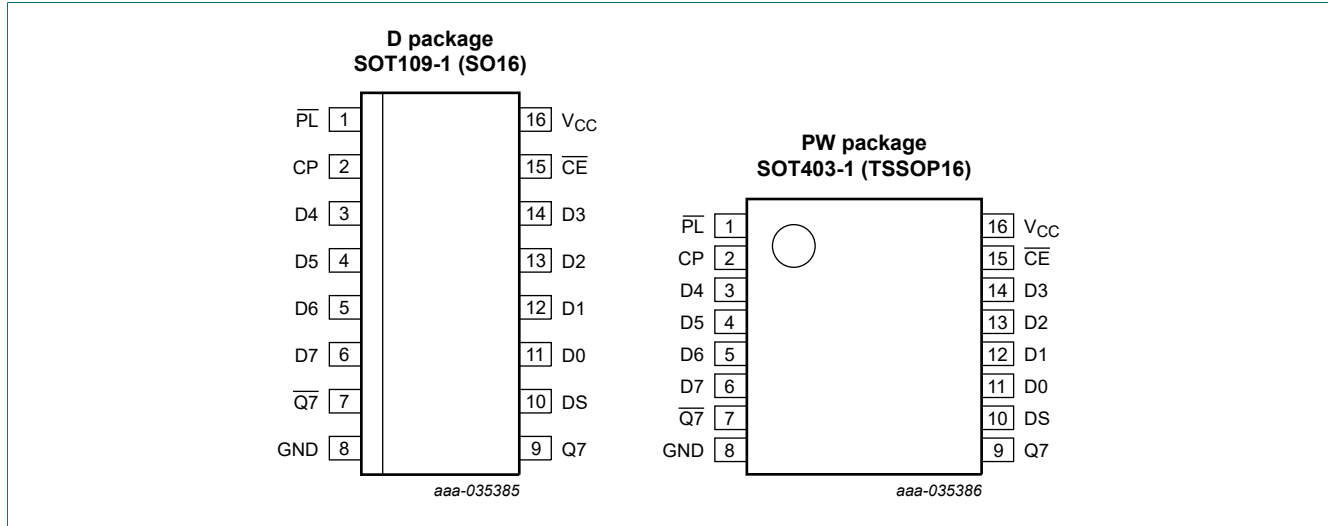


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

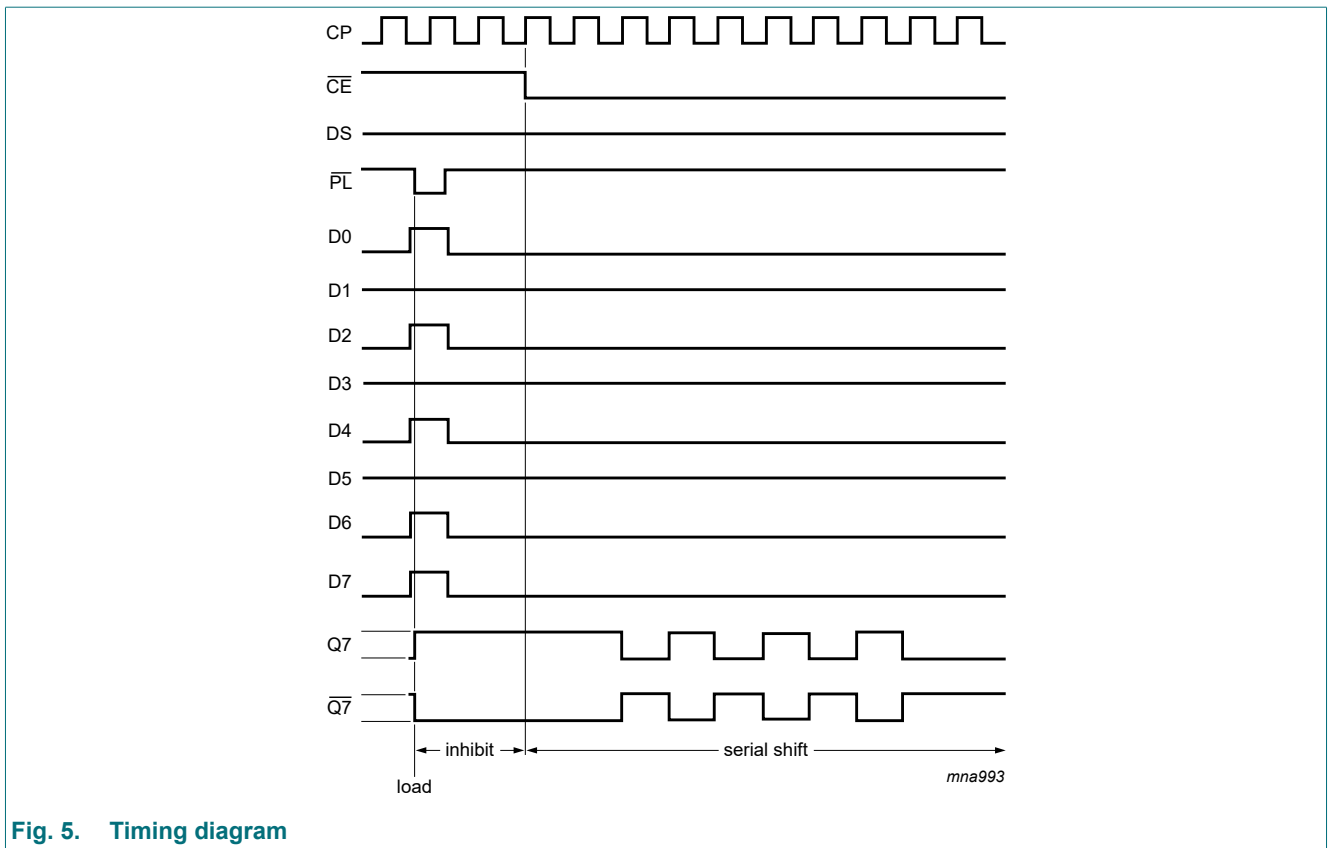
Symbol	Pin	Description
PL	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
Q7	7	complementary serial output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
CE	15	clock enable input (active LOW)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;  
 X = don't care; ↑ = LOW-to-HIGH clock transition.*

Operating modes	Inputs					Qn registers		Output	
	PL	CE	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	Q7
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$



**Fig. 5. Timing diagram**

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V) [1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-20	mA
$V_I$	input voltage		-0.5	+7	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage		-0.5	$V_{CC} + 0.5$	V
		power-down mode	-0.5	+7	V
$I_O$	output current	$0$ V $< V_O < V_{CC}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	-	200	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	100	ns/V
		$V_{CC} = 4.5$ V to 5.5 V	0	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +85 °C			Unit
			Min	Typ	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	$0.7V_{CC}$	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	$0.7V_{CC}$	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	$0.3V_{CC}$	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	$0.3V_{CC}$	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3V_{CC}$	V

## 8-bit parallel-in/serial-out shift register

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -2.0 mA; V <sub>CC</sub> = 2.3 V	2.0	-	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 3.0 V	2.48	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V to 5.5 V	-	-	0.10	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 2.3 V	-	-	0.40	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.44	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	±0.01	±1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.05	±5	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	0.2	20	μA
C <sub>I</sub>	input capacitance		-	3.0	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V); for test circuit, see Fig. 11

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t <sub>pd</sub>	propagation delay	$\overline{CE}$ , CP to Q7, $\overline{Q7}$ ; C <sub>L</sub> = 15 pF; see Fig. 6 and Fig. 7 [2]				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	11.0	22.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	7.5	18.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	5.5	11.5	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; C <sub>L</sub> = 15 pF; see Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	11.5	23.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	8.0	18.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	5.5	11.5	ns
		D7 to Q7, $\overline{Q7}$ ; C <sub>L</sub> = 15 pF; see Fig. 8				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	12.0	24.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	8.5	16.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	6.0	10.5	ns
		$\overline{CE}$ , CP to Q7, $\overline{Q7}$ ; see Fig. 6 and Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	13.0	26.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	9.0	21.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	6.1	13.5	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; see Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	14.0	28.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	10.0	22.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	6.5	13.5	ns
D7 to Q7, $\overline{Q7}$ ; see Fig. 8						
V <sub>CC</sub> = 2.3 V to 2.7 V [3]	1.0	14.0	28.0	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V [4]	1.0	10.0	20	ns		
V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	6.5	12.5	ns		
t <sub>w</sub>	pulse width	CP input HIGH to LOW; see Fig. 6				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	9.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	7.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	4.0	-	-	ns
		$\overline{PL}$ input LOW; see Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	13.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	9.0	-	-	ns
V <sub>CC</sub> = 4.5 V to 5.5 V [5]	6.0	-	-	ns		
t <sub>rec</sub>	recovery time	$\overline{PL}$ to CP, $\overline{CE}$ ; see Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	8.5	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	6.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	4.0	-	-	ns

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t <sub>su</sub>	set-up time	DS to CP, $\overline{CE}$ ; see Fig. 9				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	6.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	4.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	7.0	-	-	ns
		$\overline{CE}$ to CP, CP to $\overline{CE}$ ; see Fig. 9				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	7.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	5.0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	3.5	-	-	ns
		D7 to $\overline{PL}$ ; see Fig. 10				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	12	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	8.5	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	5.0	-	-	ns
t <sub>h</sub>	hold time	DS to CP, $\overline{CE}$ ; $\overline{PL}$ to CP, $\overline{CE}$ ; see Fig. 9				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	0	-	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	0.5	-	-	ns
		Dn to $\overline{PL}$ ; see Fig. 10				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	0.5	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	0.5	-	-	ns
V <sub>CC</sub> = 4.5 V to 5.5 V [5]	1.0	-	-	ns		
f <sub>max</sub>	maximum frequency	CP input; C <sub>L</sub> = 15 pF; see Fig. 6				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	45	80	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	50	115	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V [5]	90	165	-	MHz
		CP input; see Fig. 6				
		V <sub>CC</sub> = 2.3 V to 2.7 V [3]	35	65	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V [4]	50	90	-	MHz
V <sub>CC</sub> = 4.5 V to 5.5 V [5]	85	125	-	MHz		
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V [6]	-	24	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.

[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[3] Typical values are measured at V<sub>CC</sub> = 2.5 V.

[4] Typical values are measured at V<sub>CC</sub> = 3.3 V.

[5] Typical values are measured at V<sub>CC</sub> = 5.0 V.

[6] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) (P<sub>D</sub> in μW), where:

f<sub>i</sub> = input frequency in MHz;

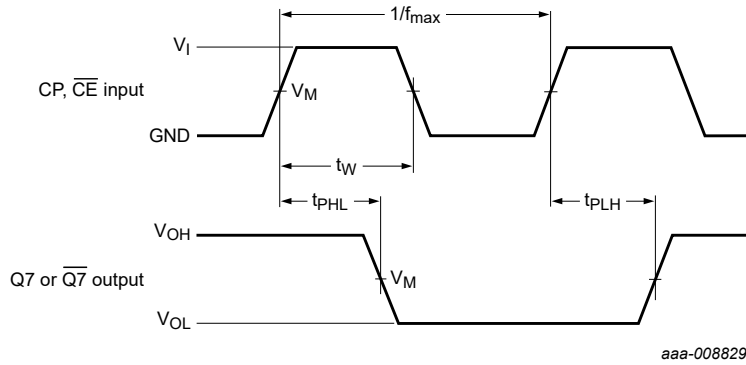
f<sub>o</sub> = output frequency in MHz;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

10.1. Waveforms and test circuit

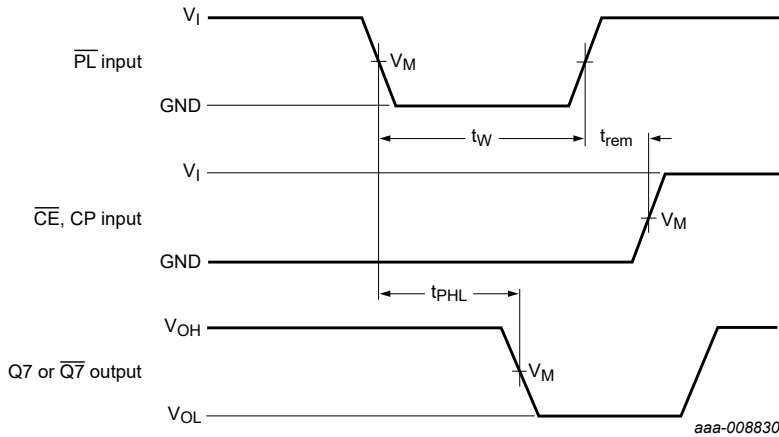


aaa-008829

Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

**Fig. 6. Clock pulse (CP) and clock enable (CE) to output (Q7 or Q7) propagation delays, clock pulse width and maximum clock frequency**

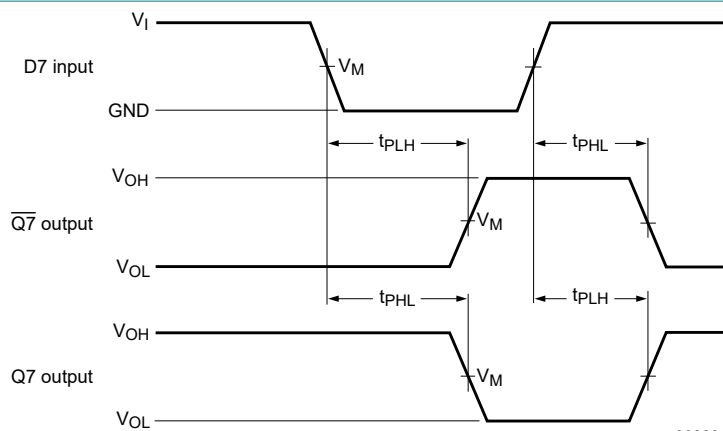


aaa-008830

Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

**Fig. 7. Parallel load (PL) pulse width, parallel load to output (Q7 or Q7) propagation delays, parallel load to clock (CP) and clock enable (CE) recovery time**

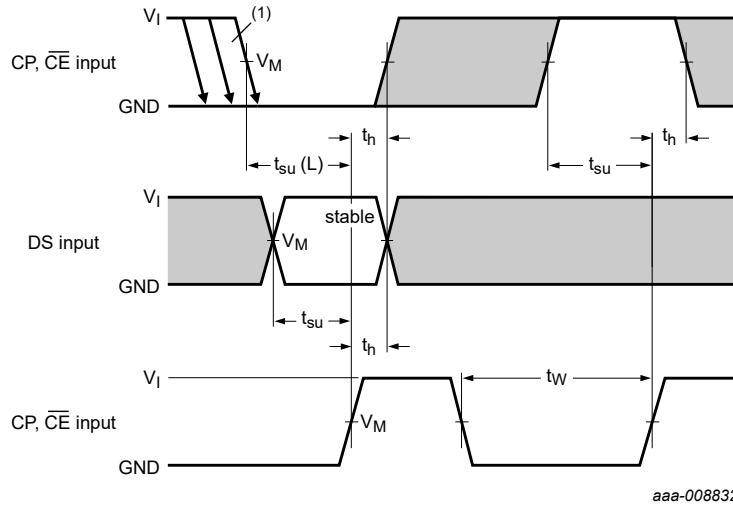


aaa-008831

Measurement points are given in [Table 8](#).

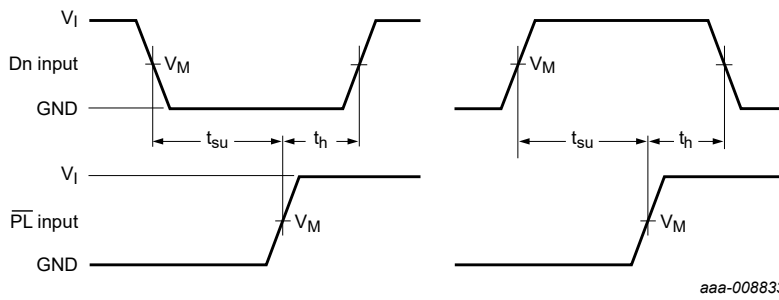
The changing to output assumes that internal Q6 is opposite state from Q7.

**Fig. 8. Data input (D7) to output (Q7 or Q7) propagation delays when PL is LOW**



Measurement points are given in [Table 8](#).  
 (1) CE may change only from HIGH-to-LOW while CP is LOW.  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 9. Set-up and hold times**

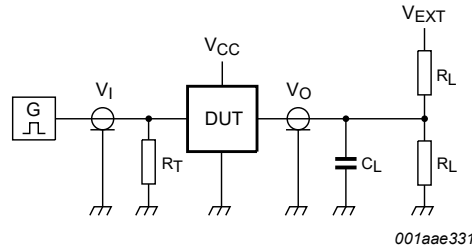
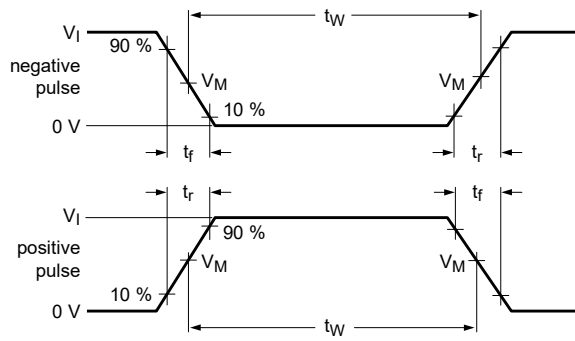


Measurement points are given in [Table 8](#).

**Fig. 10. Set-up and hold times from the data inputs (Dn) to the parallel load input ( $\overline{PL}$ )**

**Table 8. Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
2.0 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



001aee331

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 11. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
2.0 V to 5.5 V	$V_{CC}$	3.0 ns	50 pF, 15 pF	1 k $\Omega$	open

### 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

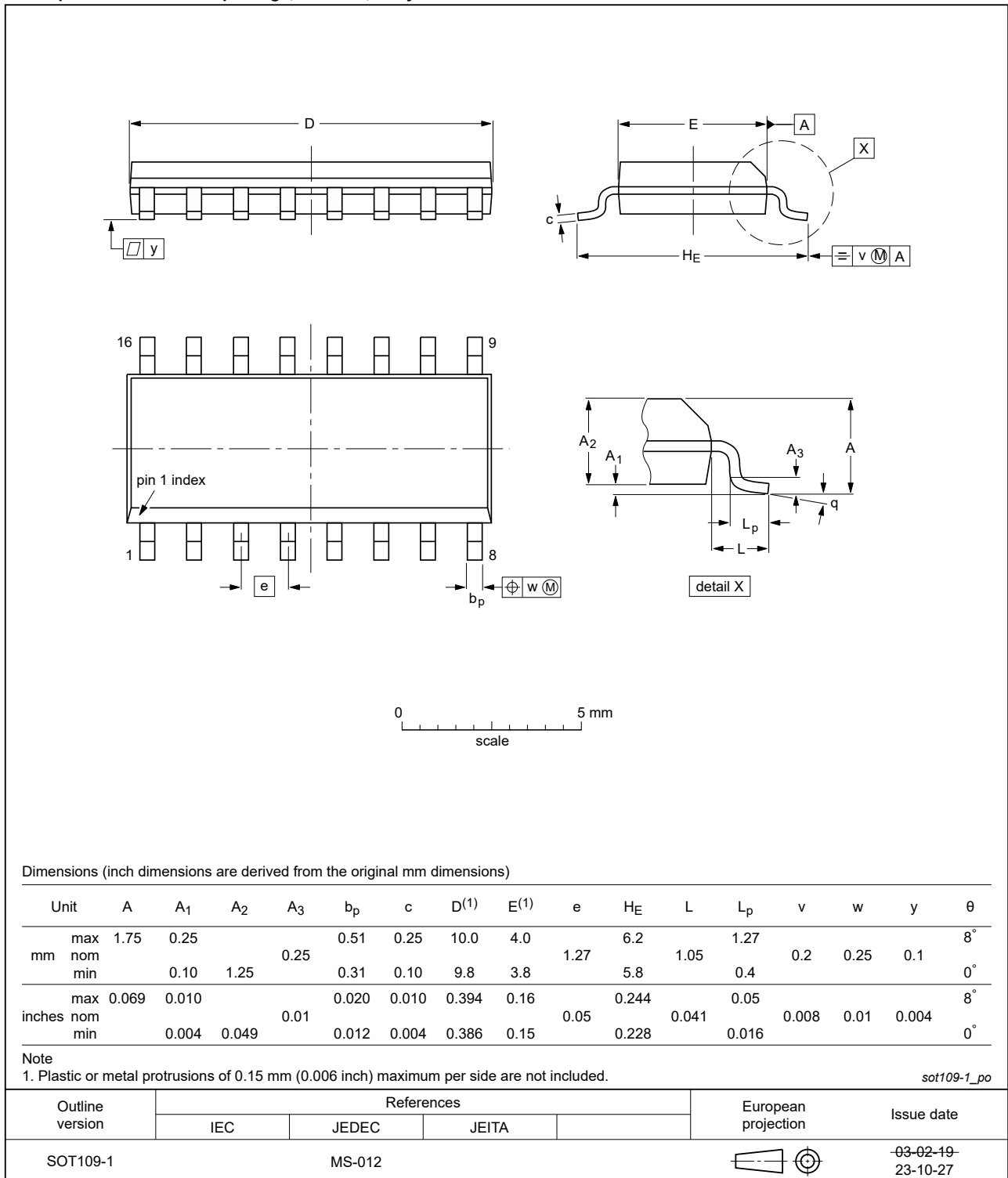


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

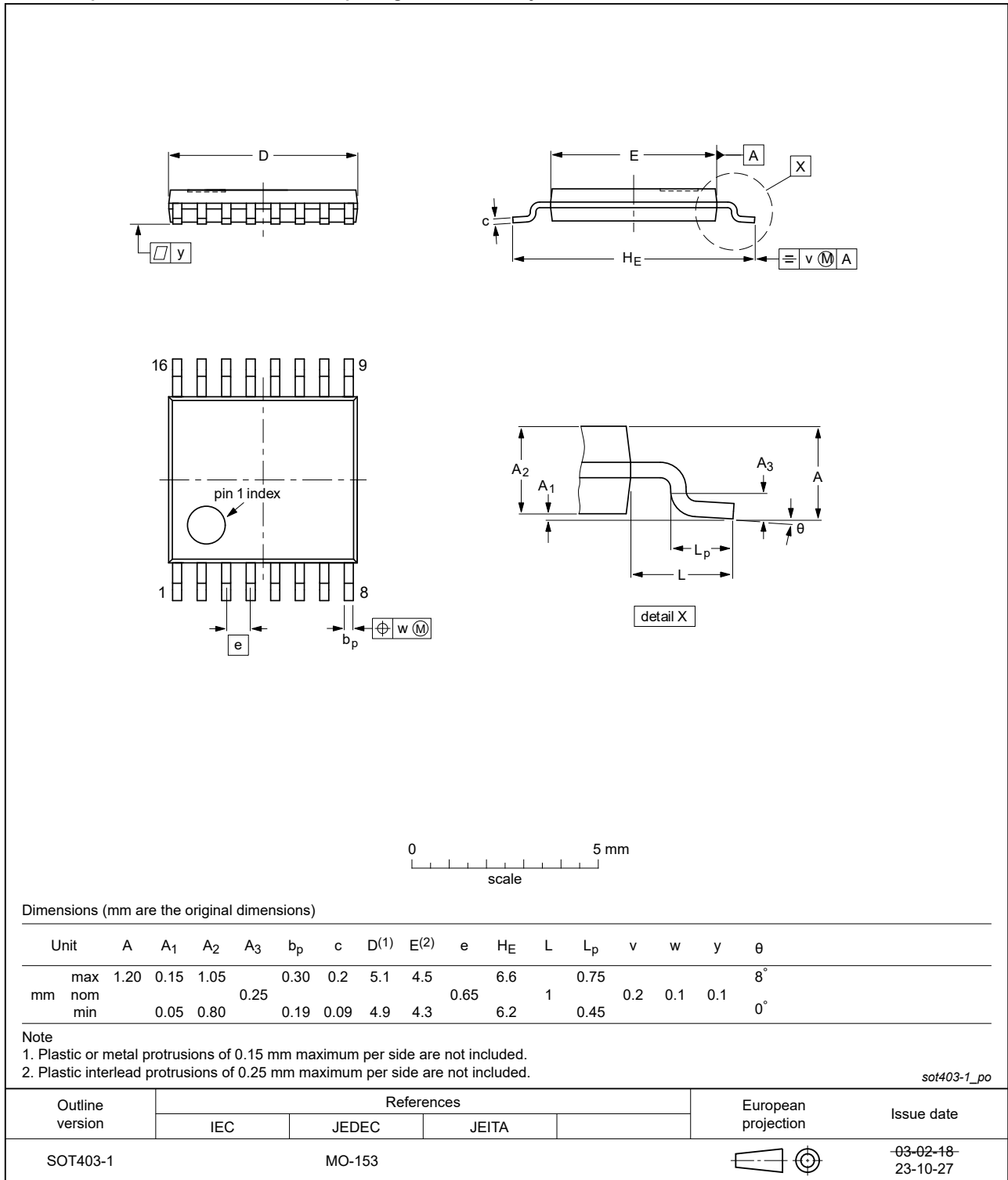


Fig. 13. Package outline SOT403-1 (TSSOP16)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV165A v.5	20240418	Product data sheet	-	74LV165A v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Fig. 12</a>, <a href="#">Fig. 13</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153</li> </ul>			
74LV165A v.4	20140328	Product data sheet	-	74LV165A v.3
Modifications:	<ul style="list-style-type: none"> <li>• Minimum limit <math>V_{OH}</math> for <math>V_{CC} = 4.5</math> V corrected from 3.0 V to 3.8 V (errata) in <a href="#">Table 6</a></li> </ul>			
74LV165A v.3	20140220	Product data sheet	-	74LV165A v.2
Modifications:	<ul style="list-style-type: none"> <li>• Typo corrected in <a href="#">Table 2</a></li> </ul>			
74LV165A v.2	20130904	Product data sheet	-	74LV165A_CNV_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Family data added, see <a href="#">Section 9</a></li> </ul>			
74LV165A v.1	December 1990	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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