



**THE DATASHEET OF  
74HCT165BQ,115**





# 74HC165; 74HCT165

8-bit parallel-in/serial out shift register

Rev. 8 — 30 May 2024

Product data sheet

## 1. General description

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The 74HC165; 74HCT165 are 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and  $\overline{Q7}$ ). When the parallel load input ( $\overline{PL}$ ) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When  $\overline{PL}$  is HIGH data enters the register serially at DS. When the clock enable input ( $\overline{CE}$ ) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on  $\overline{CE}$  will disable the CP input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

## 2. Features and benefits

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- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Input levels:
  - For 74HC165: CMOS level
  - For 74HCT165: TTL level
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

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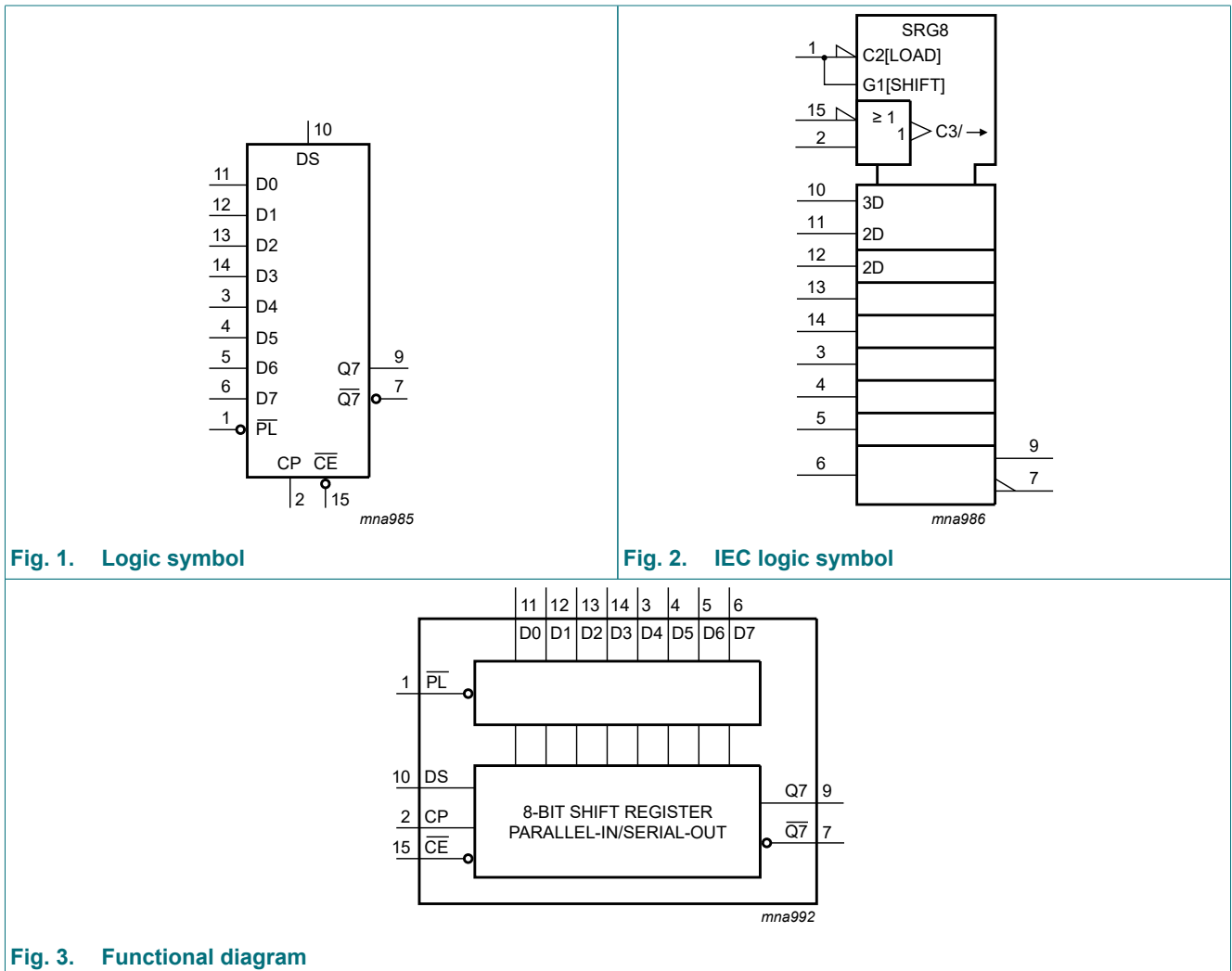
- Parallel-to-serial data conversion

### 4. Ordering information

Table 1. Ordering information

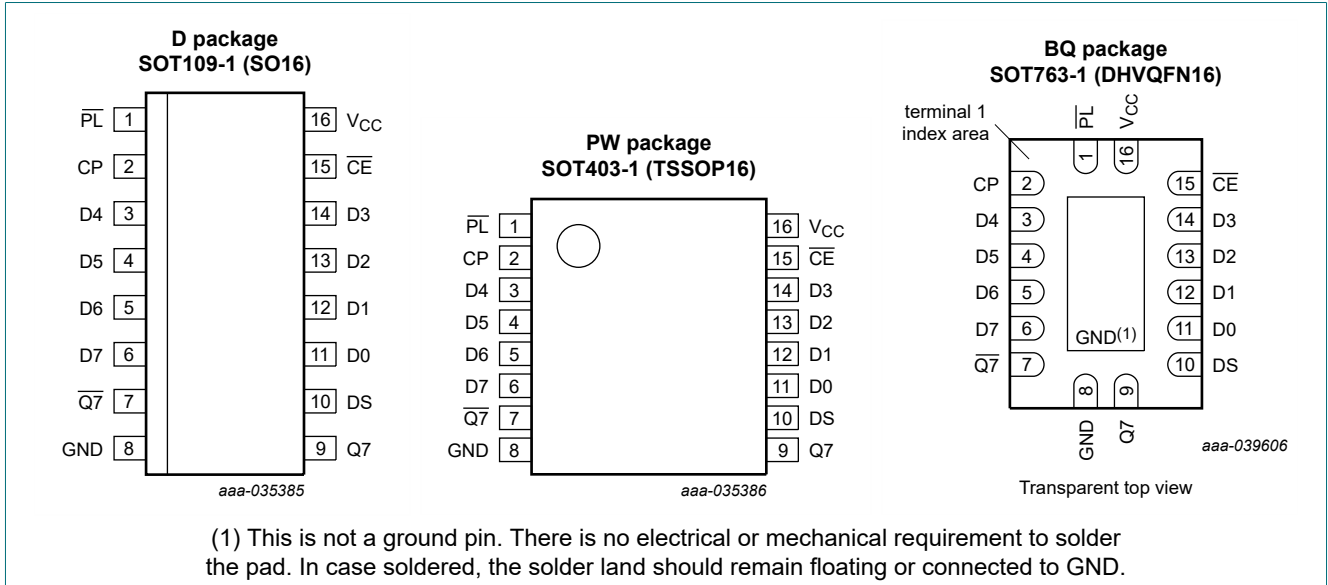
Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74HC165D</a> <a href="#">74HCT165D</a>	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">74HC165PW</a> <a href="#">74HCT165PW</a>	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>
<a href="#">74HC165BQ</a> <a href="#">74HCT165BQ</a>	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	<a href="#">SOT763-1</a>

### 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

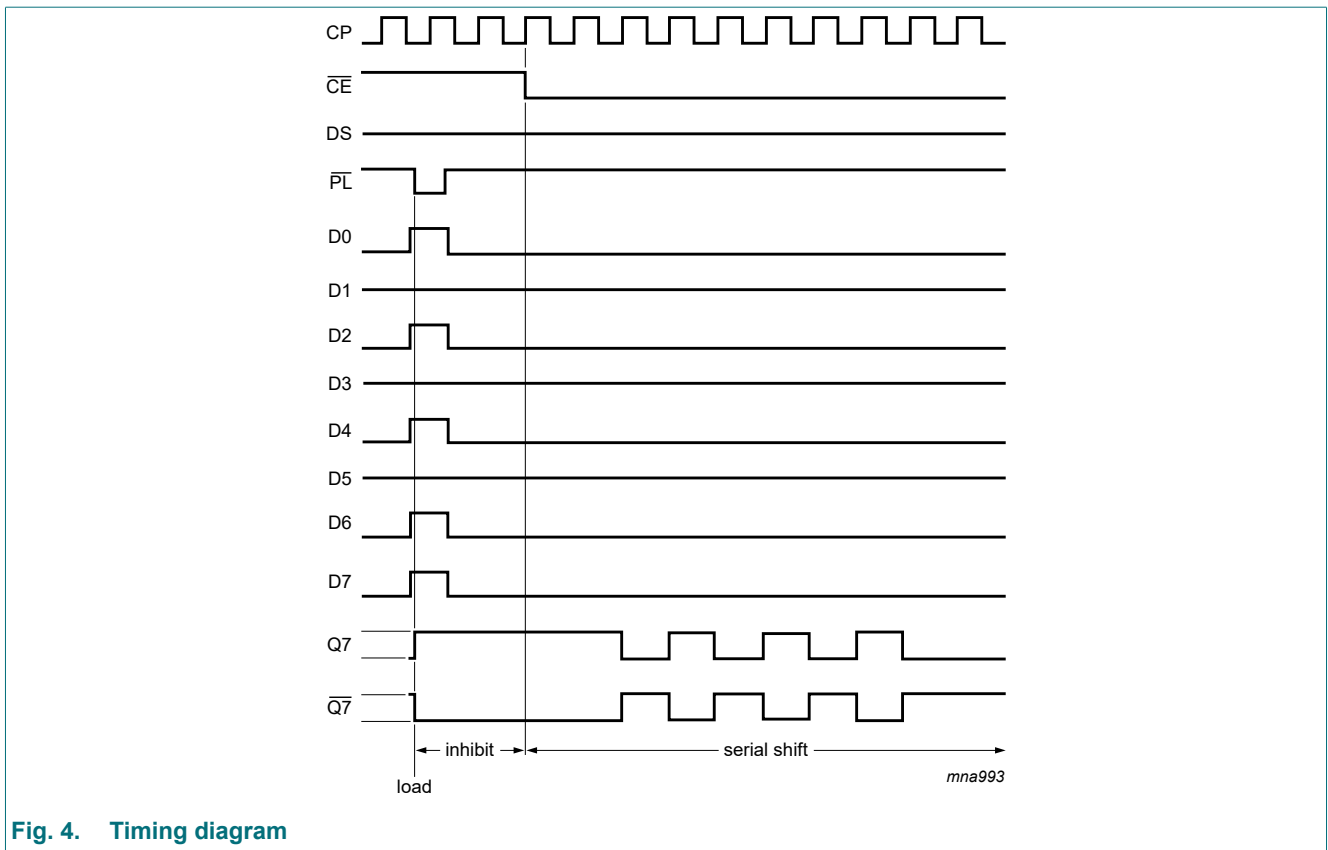
Symbol	Pin	Description
PL	1	asynchronous parallel load input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
Q7	7	complementary output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs (also referred to as Dn)
CE	15	clock enable input (active LOW)
VCC	16	positive supply voltage

## 7. Functional description

**Table 3. Function table**

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;  
 X = don't care; ↑ = LOW-to-HIGH clock transition.*

Operating modes	Inputs					Qn registers		Outputs	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$



**Fig. 4. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
 For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.  
 For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC165			74HCT165			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC165</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT165</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		Dn and DS inputs	-	35	126	-	157.5	-	171.5	μA
		CP, $\overline{CE}$ , and $\overline{PE}$ inputs	-	65	234	-	292.5	-	318.5	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  
 $C_L = 50$  pF unless otherwise specified; for test circuit, see [Fig. 10](#)

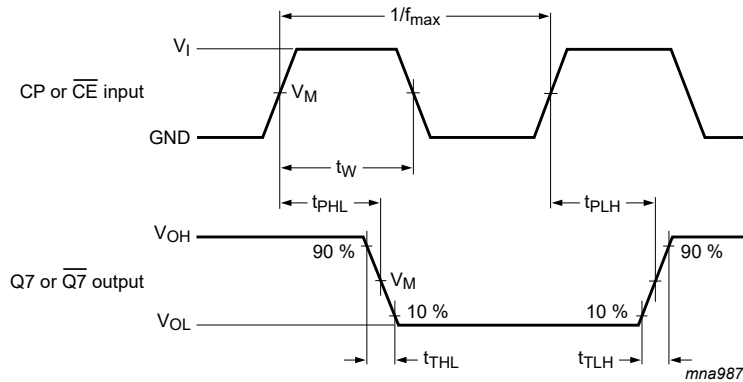
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC165</b>										
$t_{pd}$	propagation delay	CP or $\overline{CE}$ to Q7, $\overline{Q7}$ ; see <a href="#">Fig. 5</a> [1]								
		$V_{CC} = 2.0$ V	-	52	165	-	205	-	250	ns
		$V_{CC} = 4.5$ V	-	19	33	-	41	-	50	ns
		$V_{CC} = 6.0$ V	-	15	28	-	35	-	43	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; see <a href="#">Fig. 6</a>								
		$V_{CC} = 2.0$ V	-	50	165	-	205	-	250	ns
		$V_{CC} = 4.5$ V	-	18	33	-	41	-	50	ns
		$V_{CC} = 6.0$ V	-	14	28	-	35	-	43	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns
		D7 to Q7, $\overline{Q7}$ ; see <a href="#">Fig. 7</a>								
		$V_{CC} = 2.0$ V	-	36	120	-	150	-	180	ns
		$V_{CC} = 4.5$ V	-	13	24	-	30	-	36	ns
$V_{CC} = 6.0$ V	-	10	20	-	26	-	31	ns		
$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns		
$t_t$	transition time	Q7, $\overline{Q7}$ output; see <a href="#">Fig. 5</a> [2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
$t_w$	pulse width	CP input HIGH or LOW; see <a href="#">Fig. 5</a>								
		$V_{CC} = 2.0$ V	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	5	-	17	-	20	-	ns
		$\overline{PL}$ input LOW; see <a href="#">Fig. 6</a>								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns		
$t_{rec}$	recovery time	$\overline{PL}$ to CP, $\overline{CE}$ ; see <a href="#">Fig. 6</a>								
		$V_{CC} = 2.0$ V	100	22	-	125	-	150	-	ns
		$V_{CC} = 4.5$ V	20	8	-	25	-	30	-	ns
		$V_{CC} = 6.0$ V	17	6	-	21	-	26	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	DS to CP, $\overline{CE}$ ; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	11	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	4	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	3	-	17	-	20	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	17	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	5	-	17	-	20	-	ns
		Dn to $\overline{PL}$ ; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>h</sub>	hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	5	2	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	2	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	2	-	5	-	5	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	5	-17	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	-6	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	-5	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	CP input; see Fig. 5								
		V <sub>CC</sub> = 2.0 V	6	17	-	5	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V	30	51	-	24	-	20	-	MHz
		V <sub>CC</sub> = 6.0 V	35	61	-	28	-	24	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	56	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	35	-	-	-	-	-	pF
<b>74HCT165</b>										
t <sub>pd</sub>	propagation delay	$\overline{CE}$ , CP to Q7, $\overline{Q7}$ ; see Fig. 5 [1]								
		V <sub>CC</sub> = 4.5 V	-	17	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	14	-	-	-	-	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$ ; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	-	20	40	-	50	-	60	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	17	-	-	-	-	-	ns
		D7 to Q7, $\overline{Q7}$ ; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	-	14	28	-	35	-	42	ns
V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns		

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>t</sub>	transition time	Q7, $\overline{Q7}$ output; see Fig. 5 [2]								
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>W</sub>	pulse width	CP input; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
		$\overline{PL}$ input; see Fig. 6								
t <sub>rec</sub>	recovery time	$\overline{PL}$ to CP, $\overline{CE}$ ; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	20	8	-	25	-	30	-	ns
t <sub>su</sub>	set-up time	DS to CP, $\overline{CE}$ ; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	2	-	25	-	30	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$ ; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	7	-	25	-	30	-	ns
		Dn to $\overline{PL}$ ; see Fig. 9								
t <sub>h</sub>	hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$ ; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	7	-1	-	9	-	11	-	ns
f <sub>max</sub>	maximum frequency	CP input; see Fig. 5								
		V <sub>CC</sub> = 4.5 V	26	44	-	21	-	17	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	48	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [3]	-	35	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.  
 [2] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.  
 [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V.

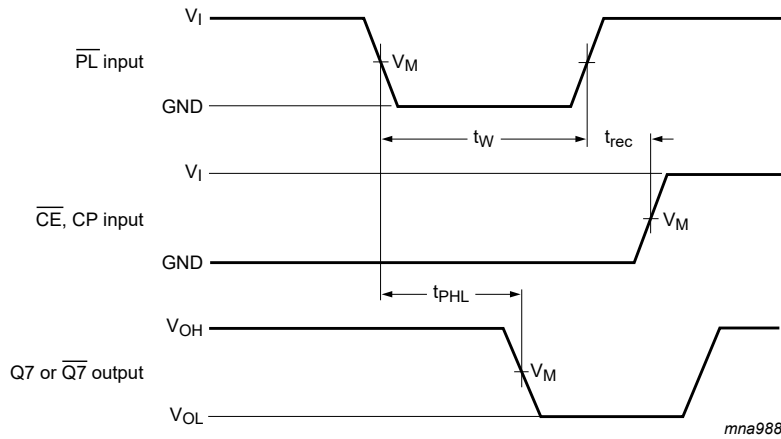
11.1. Waveforms and test circuit



Measurement points are given in Table 8.

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

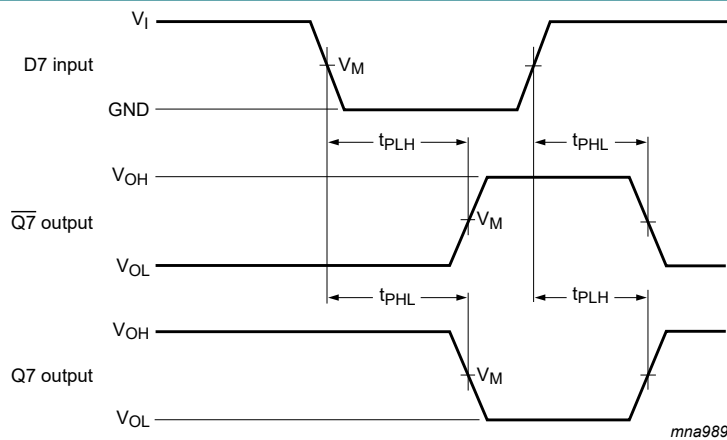
Fig. 5. The clock (CP) or clock enable ( $\overline{CE}$ ) to output (Q7 or  $\overline{Q7}$ ) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in Table 8.

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

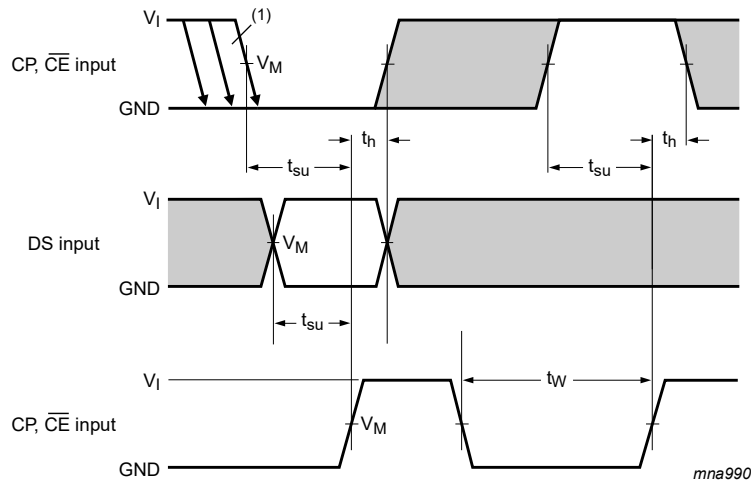
Fig. 6. The parallel load ( $\overline{PL}$ ) pulse width, the parallel load to output (Q7 or  $\overline{Q7}$ ) propagation delays, the parallel load to clock (CP) and clock enable ( $\overline{CE}$ ) recovery time



Measurement points are given in Table 8.

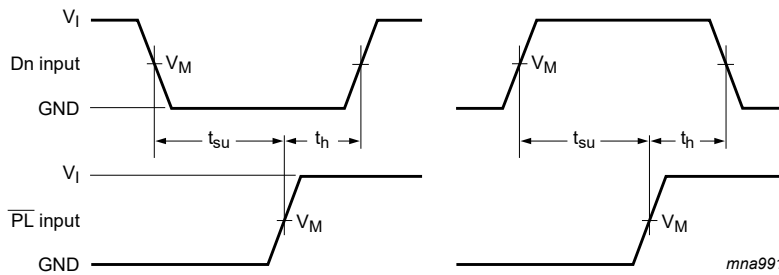
$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 7. The data input (D7) to output (Q7 or  $\overline{Q7}$ ) propagation delays when  $\overline{PL}$  is LOW



(1)  $\overline{CE}$  may change only from HIGH-to-LOW while CP is LOW.  
 The shaded areas indicate when the input is permitted to change for predictable output performance  
 Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 8.** The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable ( $\overline{CE}$ ) inputs, from the clock enable input ( $\overline{CE}$ ) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE)



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 9.** The set-up and hold times from the data inputs (Dn) to the parallel load input (PL)

**Table 8. Measurement points**

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74HC165	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT165	3 V	1.3 V	1.3 V

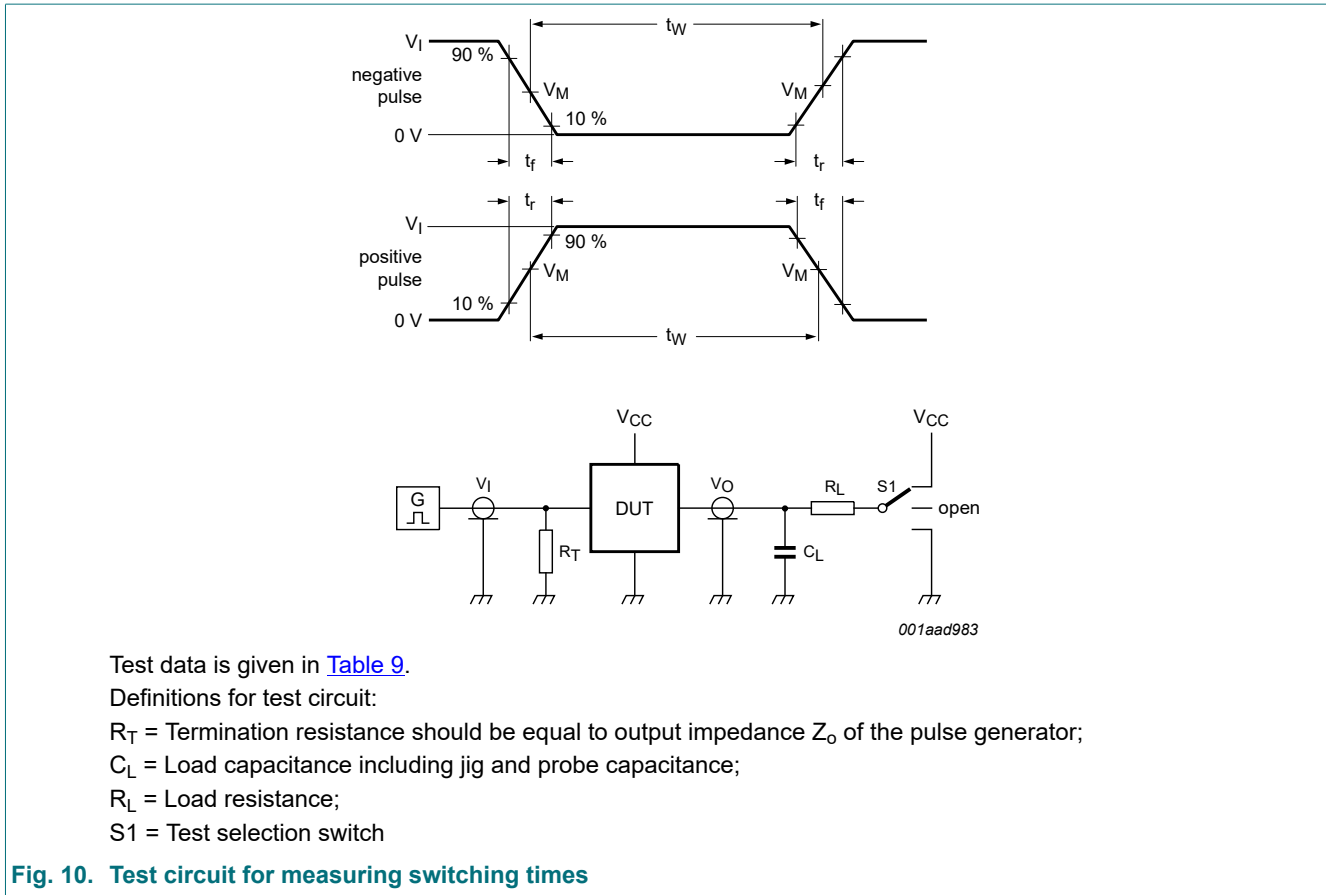


Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
74HC165	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open
74HCT165	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

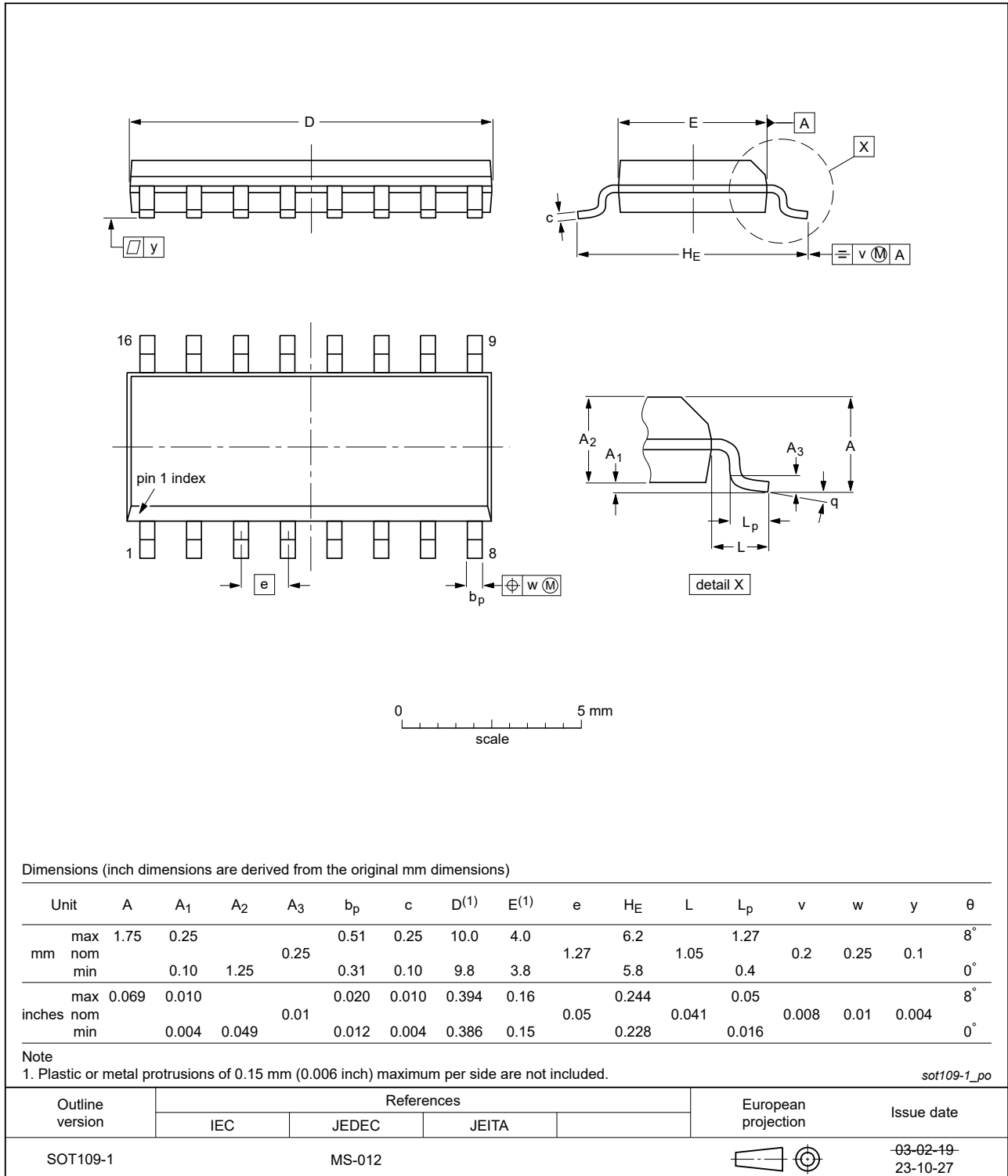


Fig. 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig. 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

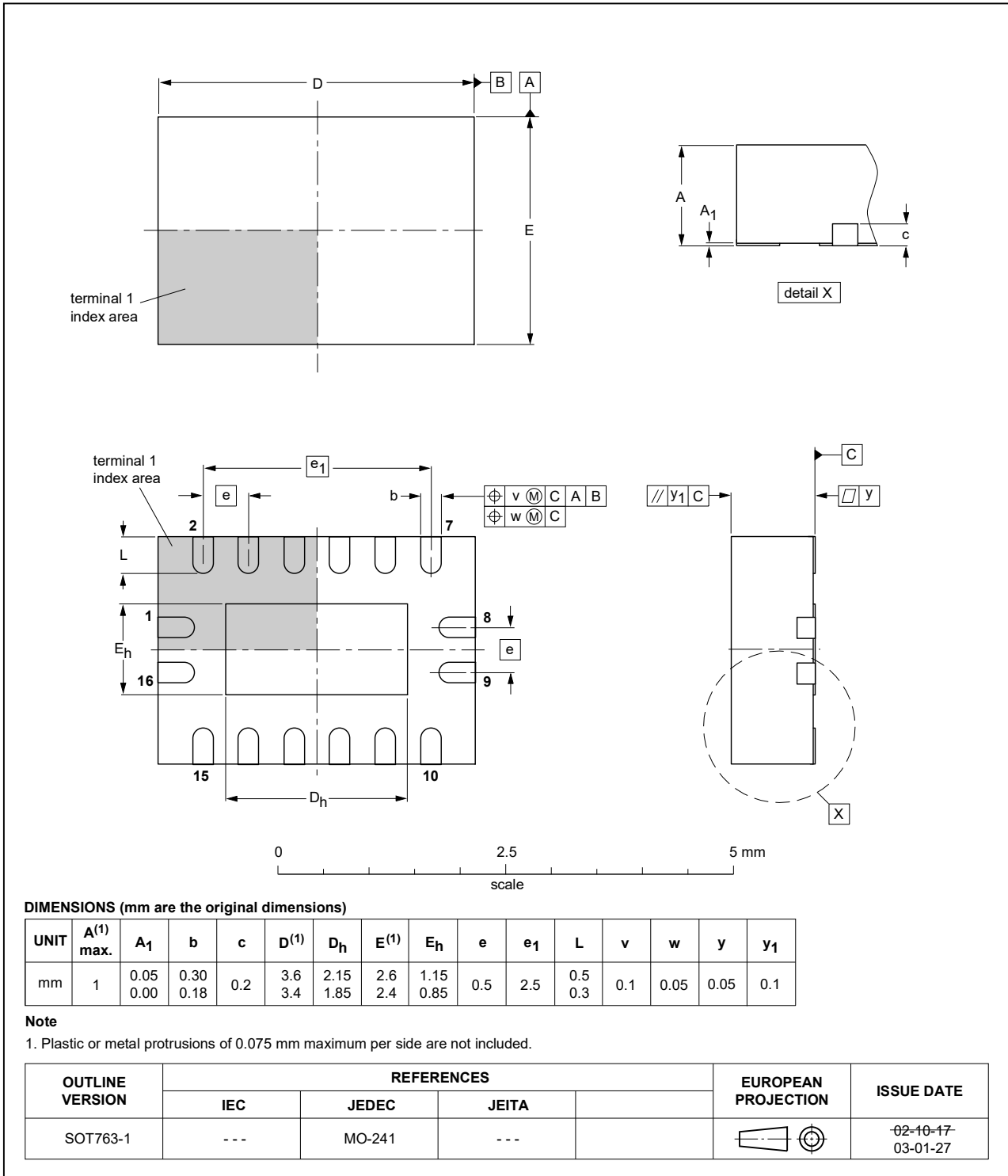


Fig. 13. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT165 v.8	20240530	Product data sheet	-	74HC_HCT165 v.7
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Fig. 11</a>, <a href="#">Fig. 12</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74HC_HCT165 v.7	20210901	Product data sheet	-	74HC_HCT165 v.6
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a> updated.</li> <li>• Type numbers 74HC165DB and 74HCT165DB (SOT338-1/SSOP16) removed.</li> </ul>			
74HC_HCT165 v.6	20200423	Product data sheet	-	74HC_HCT165 v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC_HCT165 v.5	20170821	Product data sheet	-	74HC_HCT165 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 7</a>: Hold time for 74HC165 has been updated.</li> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT165 v.4	20151228	Product data sheet	-	74HC_HCT165 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Type numbers 74HC165N and 74HCT165N (SOT38-4) removed.</li> </ul>			
74HC_HCT165 v.3	20080314	Product data sheet	-	74HC_HCT165_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Package SOT763-1 (DHVQFN16) added to <a href="#">Section 4</a> and <a href="#">Section 12</a>.</li> <li>• Family data added, see <a href="#">Section 10</a></li> </ul>			
74HC_HCT165_CNV v.2	December 1990	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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