



**THE DATASHEET OF
74AUP1T98GW-Q100H**



74AUP1T98-Q100

Low-power configurable gate with voltage-level translator

Rev. 5 — 17 July 2023

Product data sheet

1. General description

The 74AUP1T98-Q100 is a configurable multiple function gate with level translating, Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Low threshold Schmitt trigger inputs allow these devices to be driven by 1.8 V logic levels in 3.3 V applications.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.3 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standards
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- Low static power consumption; $I_{CC} = 1.5 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1T98GW-Q100	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2

4. Marking

Table 2. Marking

Type number	Marking code
74AUP1T98GW-Q100	aR

5. Functional diagram

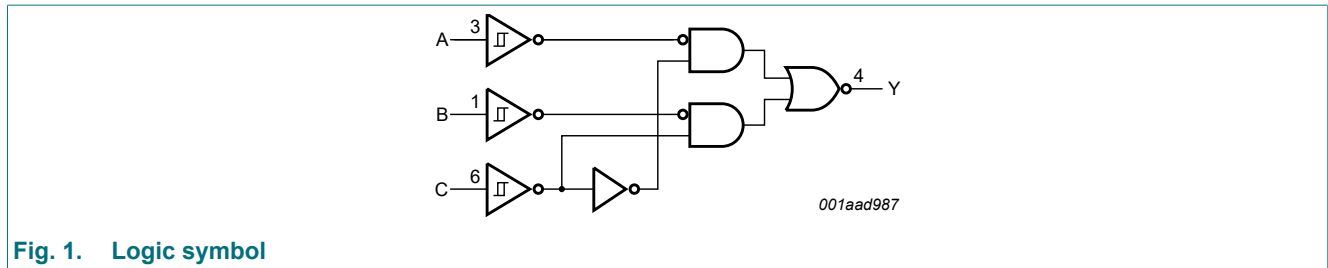


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

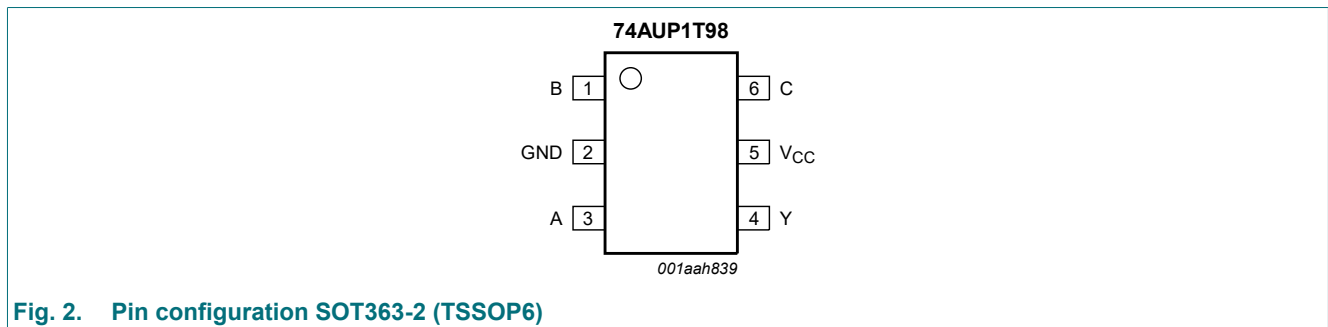


Fig. 2. Pin configuration SOT363-2 (TSSOP6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX (inverting)	see Fig. 3
2-input NAND	see Fig. 4
2-input NOR with one input inverted	see Fig. 5
2-input AND with one input inverted	see Fig. 5
2-input NAND with one input inverted	see Fig. 6
2-input OR with one input inverted	see Fig. 6
2-input NOR	see Fig. 7
Buffer	see Fig. 8
Inverter	see Fig. 9

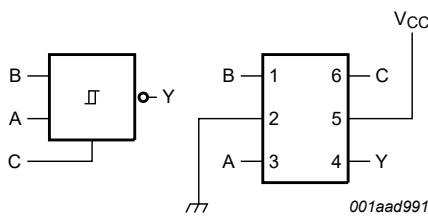


Fig. 3. 2-input MUX (inverting)

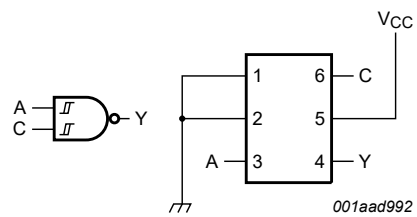


Fig. 4. 2-input NAND gate

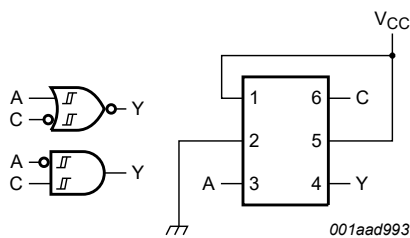


Fig. 5. 2-input AND gate with input A inverted or 2-input NOR gate with input C inverted

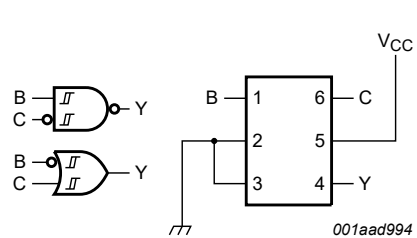
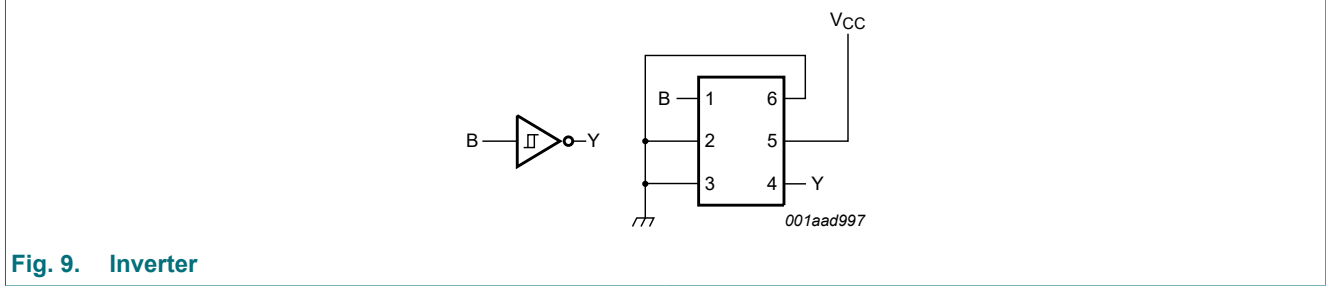
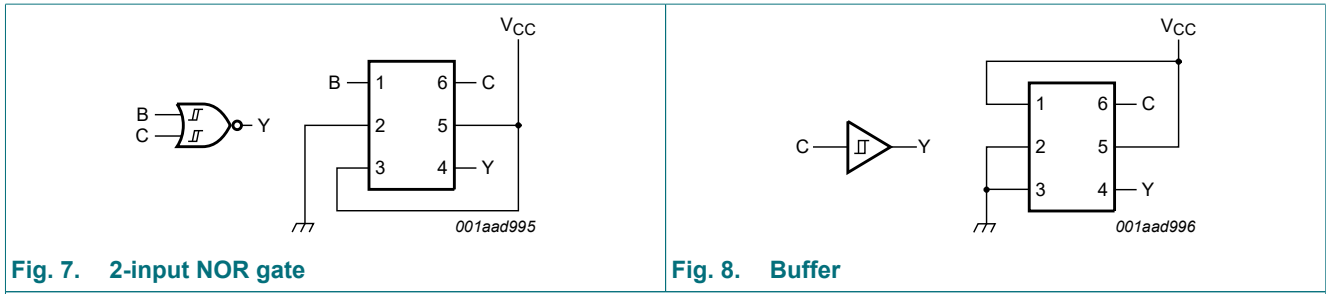


Fig. 6. 2-input OR gate with input B inverted or 2-input NAND gate with input C inverted



8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode and Power-down mode	-0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	V _H = V _{T+} - V _{T-}				
		V _{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.1	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.2	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.7	-	pF

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	V _H = V _{T+} - V _{T-}				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.5	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.5	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A; One input at 0.3 V or 1.1 V, other inputs at V _{CC} or GND	-	-	4	μA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A; One input at 0.45 V or 1.2 V, other inputs at V _{CC} or GND	-	-	12	μA

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
		V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V _H	hysteresis voltage	V _H = V _{T+} - V _{T-}				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.11	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	3.5	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A; One input at 0.3 V or 1.1 V, other inputs at V _{CC} or GND	-	-	7	μA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A; One input at 0.45 V or 1.2 V, other inputs at V _{CC} or GND	-	-	22	μA

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
V_{CC} = 2.3 V to 2.7 V; V_I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	2.0	3.6	5.7	0.5	6.8	0.5	7.5	ns
		C _L = 10 pF	2.5	4.2	6.3	1.0	7.9	1.0	8.7	ns
		C _L = 15 pF	2.9	4.6	6.9	1.0	8.7	1.0	9.6	ns
		C _L = 30 pF	3.9	5.8	8.3	1.5	10.8	1.5	11.9	ns

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
V_{CC} = 2.3 V to 2.7 V; V_I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	1.7	3.4	5.6	0.5	6.0	0.5	6.6	ns
		C _L = 10 pF	2.1	4.0	6.3	1.0	7.1	1.0	7.9	ns
		C _L = 15 pF	2.5	4.5	6.9	1.0	7.9	1.0	8.7	ns
		C _L = 30 pF	3.4	5.6	8.4	1.5	10.0	1.5	11.0	ns
V_{CC} = 2.3 V to 2.7 V; V_I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	1.3	3.2	5.2	0.5	5.5	0.5	6.1	ns
		C _L = 10 pF	1.8	3.7	5.9	1.0	6.5	1.0	7.2	ns
		C _L = 15 pF	2.2	4.2	6.5	1.0	7.4	1.0	8.2	ns
		C _L = 30 pF	3.1	5.4	7.9	1.5	9.5	1.5	10.5	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	2.0	2.9	4.1	0.5	8.0	0.5	8.8	ns
		C _L = 10 pF	2.4	3.5	4.8	1.0	8.5	1.0	9.4	ns
		C _L = 15 pF	2.8	3.9	5.4	1.0	9.1	1.0	10.1	ns
		C _L = 30 pF	3.6	5.1	6.9	1.5	9.8	1.5	10.8	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	1.5	2.8	4.4	0.5	5.3	0.5	5.9	ns
		C _L = 10 pF	2.0	3.4	5.1	1.0	6.1	1.0	6.8	ns
		C _L = 15 pF	2.4	3.9	5.7	1.0	6.8	1.0	7.5	ns
		C _L = 30 pF	3.4	5.0	7.2	1.5	8.5	1.5	9.4	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C _L = 5 pF	1.3	2.8	4.4	0.5	4.7	0.5	5.2	ns
		C _L = 10 pF	1.7	3.3	5.2	1.0	5.7	1.0	6.3	ns
		C _L = 15 pF	2.1	3.8	5.8	1.0	6.2	1.0	6.9	ns
		C _L = 30 pF	3.1	5.0	7.2	1.5	7.8	1.5	8.6	ns
T_{amb} = 25 °C										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	4.3	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuits

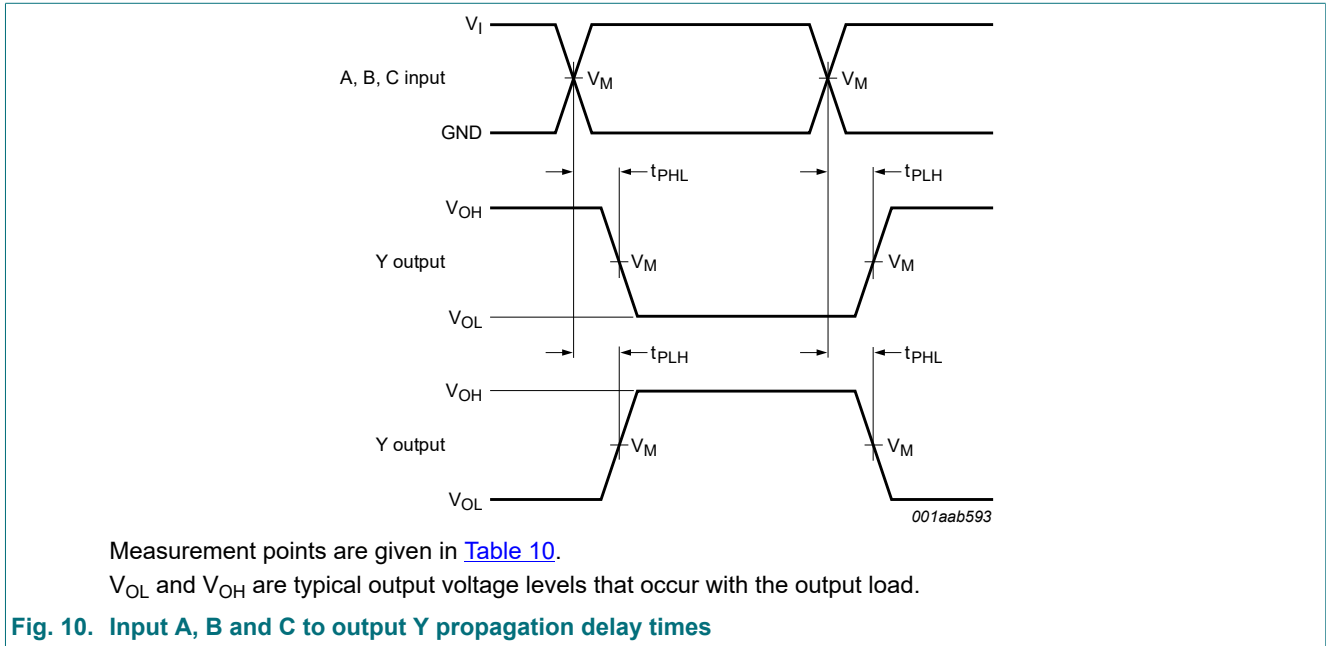


Table 10. Measurement points

Supply voltage	Input			Output
V_{CC}	V_M	V_I	$t_r = t_f$	V_M
2.3 V to 3.6 V	$0.5 \times V_I$	1.65 V to 3.6 V	≤ 3.0 ns	$0.5 \times V_{CC}$

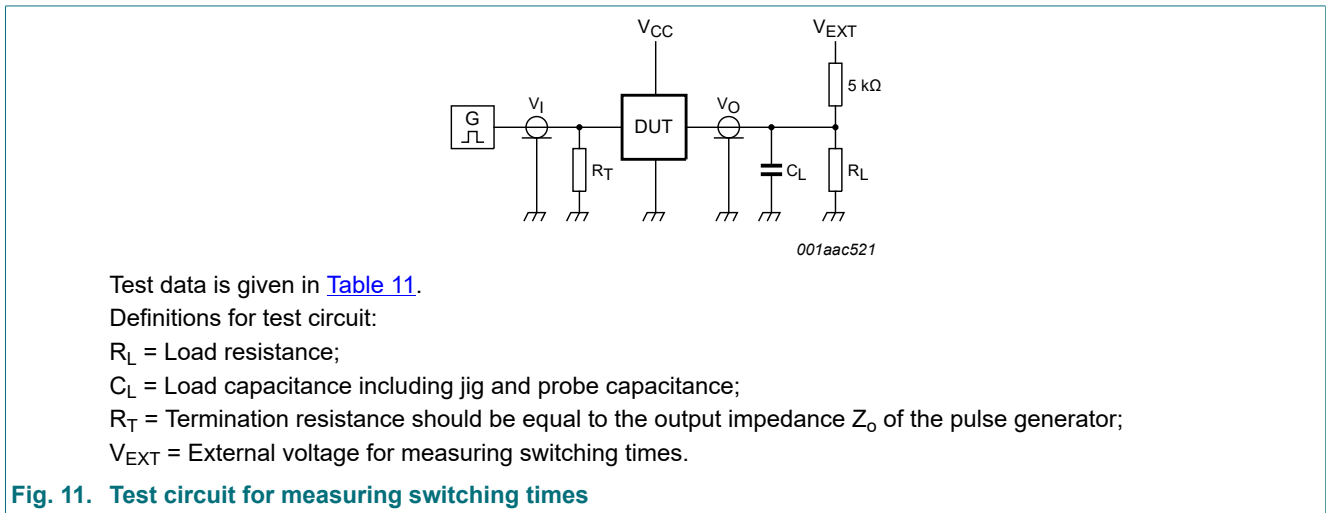


Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5$ k Ω .
 For measuring propagation delays, setup and hold times and pulse width $R_L = 1$ M Ω .

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2



Fig. 12. Package outline SOT363-2 (TSSOP6)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T98_Q100 v.5	20230717	Product data sheet	-	74AUP1T98_Q100 v.4
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AUP1T98_Q100 v.4	20220127	Product data sheet	-	74AUP1T98_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Section 2 updated. SOT363 (SC-88) package changed to SOT363-2 (TSSOP6) package. 			
74AUP1T98_Q100 v.3	20201209	Product data sheet	-	74AUP1T98_Q100 v.2
Modifications:	<ul style="list-style-type: none"> Section 1 updated. Table 6: Derating values for P_{tot} total power dissipation updated. 			
74AUP1T98_Q100 v.2	20181005	Product data sheet	-	74AUP1T98_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74AUP1T98_Q100 v.1	20140519	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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