



THE DATASHEET OF 50RIA60





SOLID STATE INC.

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50RIA SERIES

80 Amp RMS SCR_s

Major Ratings and Characteristics

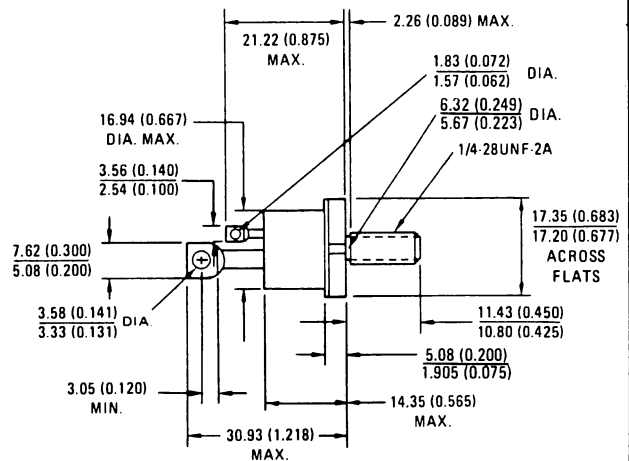
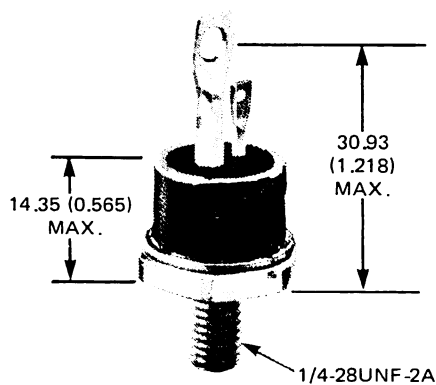
	50RIA . . .	Units
$I_T(RMS)$	80	A
$I_T(AV)$	50	A
@ Max. T_C	94	°C
I_{TSM} @ 50 Hz	1200	A
@ 60 Hz	1255	
I^2_t @ 50 Hz	7200	A ² _s
@ 60 Hz	6560	
I_{GT}	100	mA
dv/dt	200	V/μs
di/dt	200	A/μs
t_q (typ.)	110	μs
T_J	-40 to 125	°C
V_{RRM}	50 to 1200	V

Description/Features

This series of medium power thyristors is intended for general purpose phase control applications in converters, lighting circuits, battery chargers, regulated power supplies and temperature and speed control circuits.

- High current rating.
- Excellent dynamic characteristics.
- dv/dt = 1000V/μs option.
- For general purpose applications.
- Superior surge capabilities.
- Standard package.
- Metric thread version available.
- Types up to 1200V V_{RRM} , V_{DRM}

CASE STYLE AND DIMENSIONS



Conforms to JEDEC : TO-208AC (TO-65)

All Dimensions in Millimeters and (Inches)

50RIA Series

VOLTAGE RATINGS (Applied gate voltage zero or negative.)

Part Number ④	V_{RRM}, V_{DRM} – Max. Repetitive Peak Reverse or Off-State Voltage (V) ②	V_{RSM} – Max. Non-Repetitive Peak Reverse Voltage (V) ①	I_{RM}, I_{DM} – Max. Peak Reverse and Off-State Current at Rated V_{RRM} and V_{DRM} Zero Gate Bias Voltage, Gate Open Circuited (mA)
	$T_J = -40^{\circ}\text{C}$ to 125°C	$T_J = 25^{\circ}\text{C}$ to 125°C	$T_J = 125^{\circ}\text{C}$
50RIA5	50	100	15
50RIA10	100	150	15
50RIA20	200	300	15
50RIA40	400	500	15
50RIA60	600	700	15
50RIA80	800	900	15
50RIA100	1000	1100	15
50RIA120	1200	1300	15

ELECTRICAL SPECIFICATIONS

		Units	Conditions
ON-STATE			
$I_T(\text{RMS})$	Max. RMS on-state current	80	A
$I_T(\text{AV})$	Max. average on-state current	50	A $T_C = 94^{\circ}\text{C}$ max., 180° sinusoidal conduction.
I_T^{TSM}	Max. peak one cycle, non-repetitive surge current	1200	A 50 Hz half cycle sine wave or 6 ms rectangular pulse Following any rated load condition, and with rated V_{RRM} applied following surge. SCR turned fully on.
		1255	
		1430	A 50 Hz half cycle sine wave or 6 ms rectangular pulse Following any rated load condition, and with V_{RRM} following surge = 0.
		1490	
$I^2 t$	Max. $I^2 t$ capability, for fusing	7200	$A^2 s$ $t = 10$ ms Rated V_{RRM} applied following surge, initial $T_J = 125^{\circ}\text{C}$.
		6560	
$I^2 t$	Max. $I^2 t$ capability, for individual device fusing	10180	$A^2 s$ $t = 10$ ms V_{RRM} following surge = 0, initial $T_J = 125^{\circ}\text{C}$.
		9300	
$I^2 \sqrt{t}$	Max. $I^2 \sqrt{t}$ capability, for individual device fusing ③	101,800	$A^2 \sqrt{s}$ $t = 0.1$ to 10 ms, V_{RRM} following surge = 0, initial $T_J = 125^{\circ}\text{C}$.
V_{TM}	Max. peak on-state voltage	1.6	V $T_J = 25^{\circ}\text{C}$, $I_T(\text{AV}) = 50\text{A}$ (157A peak)
I_H	Max. holding current	200	mA $T_J = 25^{\circ}\text{C}$, anode supply = 22V, initial $I_T = 2.0\text{A}$.
I_L	Max. latching current	400	mA Anode supply = 6V, resistive load
BLOCKING			
dv/dt	Min. critical rate-of-rise of off-state voltage	200	$V/\mu s$ $T_J = 125^{\circ}\text{C}$. Exponential to 100% rated V_{DRM} $T_J = 125^{\circ}\text{C}$. Exponential to 67% rated V_{DRM} Zero gate bias voltage, gate open circuited.
		500†	

① For voltage pulses with $t_p \leq 5$ ms.

② Units may be broken over non-repetitively in the off-state direction without damage, if di/dt does not exceed $20 \text{ A}/\mu\text{s}$.

③ $I^2 t$ for time $t_x = I^2 \sqrt{t} \cdot \sqrt{t_x}$

④ For M6 threads add "M" to code, e.g., 50RIA60M.

† Available with dv/dt = $1000 \text{ V}/\mu\text{s}$, ($T_J = 125^{\circ}\text{C}$, exponential to 67% V_{DRM}). Add S90 to part number, e.g. 50RIA60S90.

ELECTRICAL SPECIFICATIONS (Continued)

		Units	Conditions	
SWITCHING				
t_d	Typical delay time	0.9	μs	$T_C = 25^\circ C$, $V_{DM} = \text{rated } V_{DRM}$, $I_{TM} = 10A$ dc resistive circuit, Gate pulse: 10V, 15 Ω source, $t_p = 20 \mu s$.
di/dt	Max. non-repetitive rate of rise of turned-on current $V_{RRM} = 50 \text{ to } 600V$ $= 700 \text{ to } 1200V$	200	$A/\mu s$	$T_C = 125^\circ C$, $V_{DM} = \text{rated } V_{DRM}$, $I_{TM} = 2 \times \text{rated } di/dt$, Gate pulse: 20V, 15 Ω , $t_p = 6 \mu s$, $t_r = 0.1 \mu s$ max. Per JEDEC standard RS-397, 5.2.7.6.
		100		
t_q	Typical turn-off time	110	μs	$T_C = 125^\circ C$, $I_{TM} = 50A$, $di/dt = -10 A/\mu s$, V_R during turn-off interval = 50V min., reapplied $dv/dt = 20 V/\mu s$ linear to rated V_{DRM} . Gate bias: 0V, 100 Ω .
TRIGGERING				
P_{GM}	Max. peak gate power	10	W	$t_p \leq 5ms$
$P_{G(AV)}$	Max. average gate power	2.5	W	
I_{GM}	Max. peak positive gate current	2.5	A	
$+V_{GM}$	Max. peak positive gate voltage	20	V	
$-V_{GM}$	Max. peak negative gate voltage	10	V	
I_{GT}	Max. required DC gate current to trigger	250	mA	$T_J = -40^\circ C$
		100		$T_J = 25^\circ C$
		50		$T_J = 125^\circ C$
V_{GT}	Max. required DC gate voltage to trigger	3.5	V	$T_J = -40^\circ C$
		2.5		$T_J = 25^\circ C$
V_{GD}	Max. DC gate voltage not to trigger	0.2	V	$T_J = 125^\circ C$
I_{GD}	Max. DC gate current not to trigger	5.0	mA	$T_J = 125^\circ C$, $V_{DRM} = \text{rated voltage}$
Max. required gate trigger current is the lowest value which will trigger all units with +6V anode-to-cathode.				
Max. required gate trigger voltage is the lowest value which will trigger all units with +6V anode-to-cathode.				
Max. gate current or voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode-to-cathode.				

THERMAL-MECHANICAL SPECIFICATIONS

T_J	Operating junction temperature range	-40 to 125	$^\circ C$	
T_{stg}	Storage temperature range	-40 to 125	$^\circ C$	
R_{thJC}	Max. internal thermal resistance, junction to case	0.35	deg. C/W	DC operation
R_{thCS}	Thermal resistance, case to sink	0.25	deg. C/W	Mounting surface smooth, flat and greased.
T	Mounting torque	Min.	2.8 (25)	N • m (lbf-in)
		Max.	3.4 (30)	
wt	Approximate weight	28 (1.0)	g (oz.)	
	Case Style	TO-208AC (TO-65)		
Non-lubricated threads				

50RIA Series

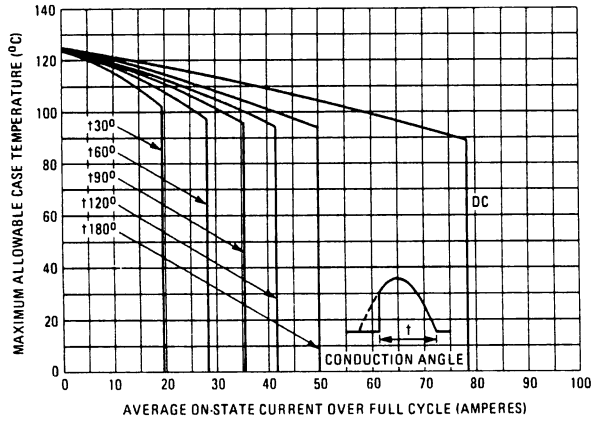


Fig. 1 – On-State Current Vs. Case Temperature (Sinusoidal Current Waveform, 50 to 400 Hz)

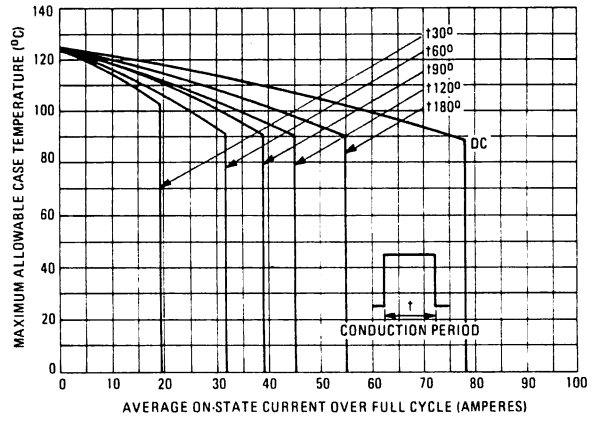


Fig. 2 – On-State Current Vs. Case Temperature (Rectangular Current Waveform, 50 to 400 Hz)

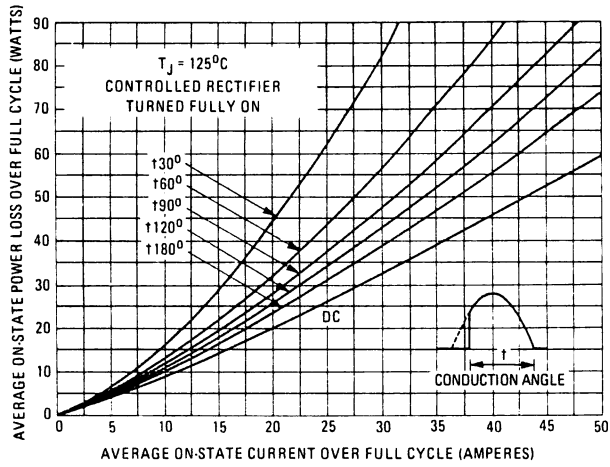


Fig. 3 – Maximum Low-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

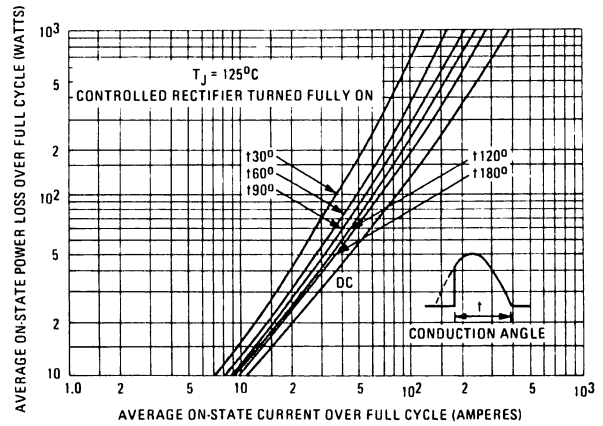


Fig. 4 – Maximum High-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

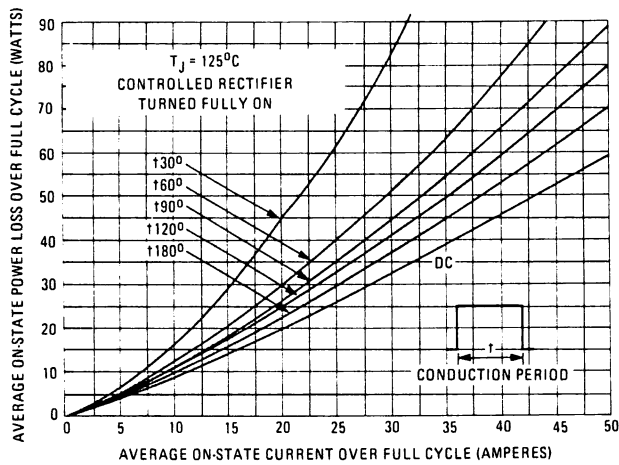


Fig. 5 – Maximum Low-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

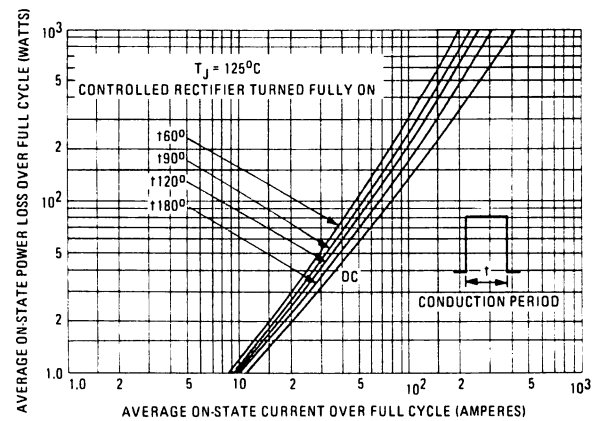


Fig. 6 – Maximum High-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

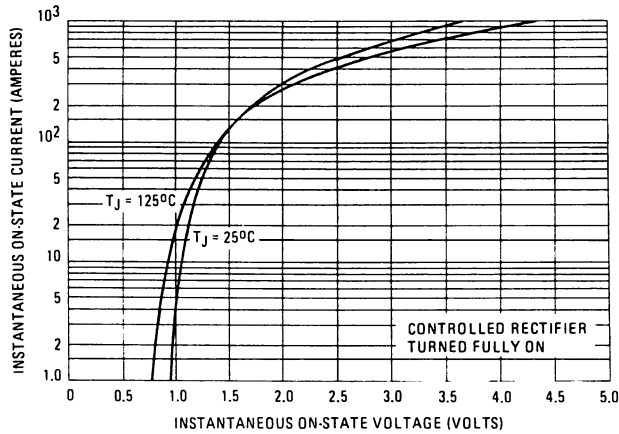


Fig. 7 – Maximum On-State Voltage Vs. Current

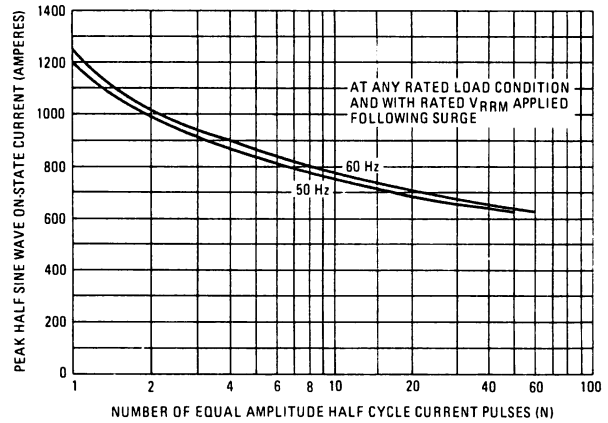


Fig. 8 – Maximum Non-Repetitive Surge Current Vs. Number of Current Pulses

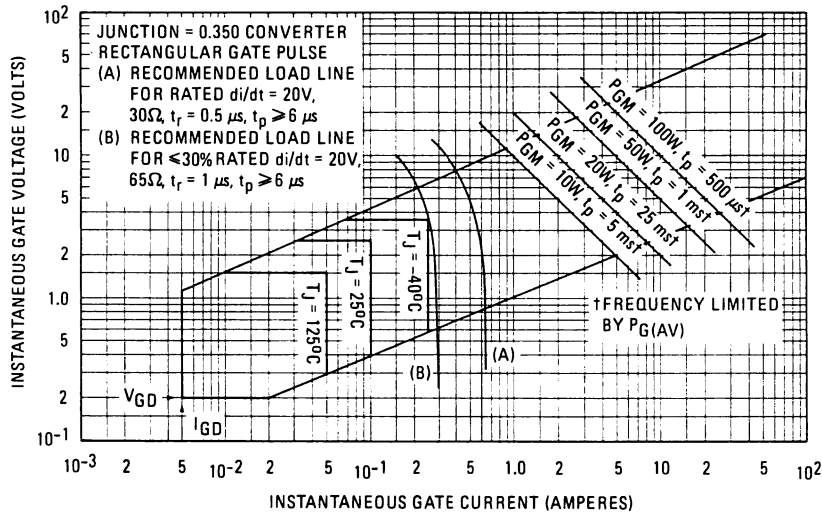


Fig. 9 – Gate Characteristics

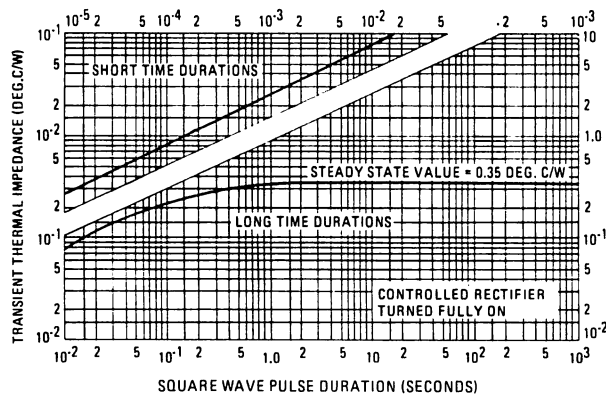


Fig. 10 – Maximum Transient Thermal Impedance, Junction-To-Case Vs. Square Wave Pulse Duration

50RIA Series

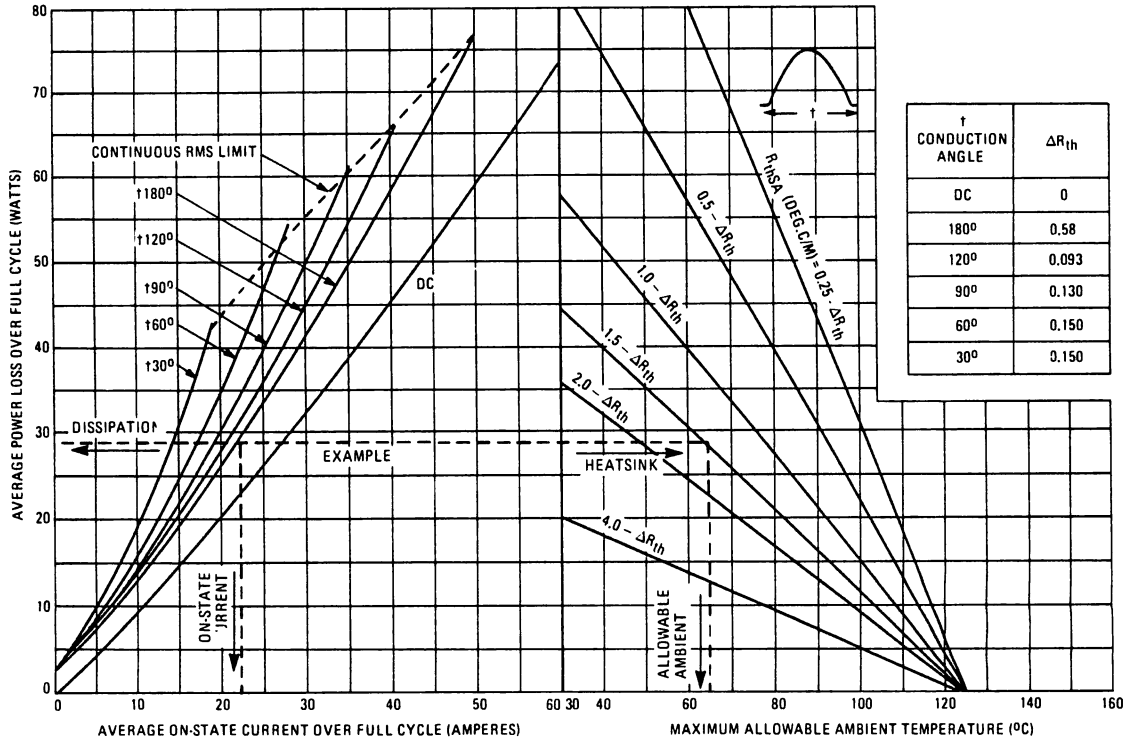


Fig. 11 – Thermal Nomogram (Sinusoidal Current Waveform, 40 to 400 Hz)

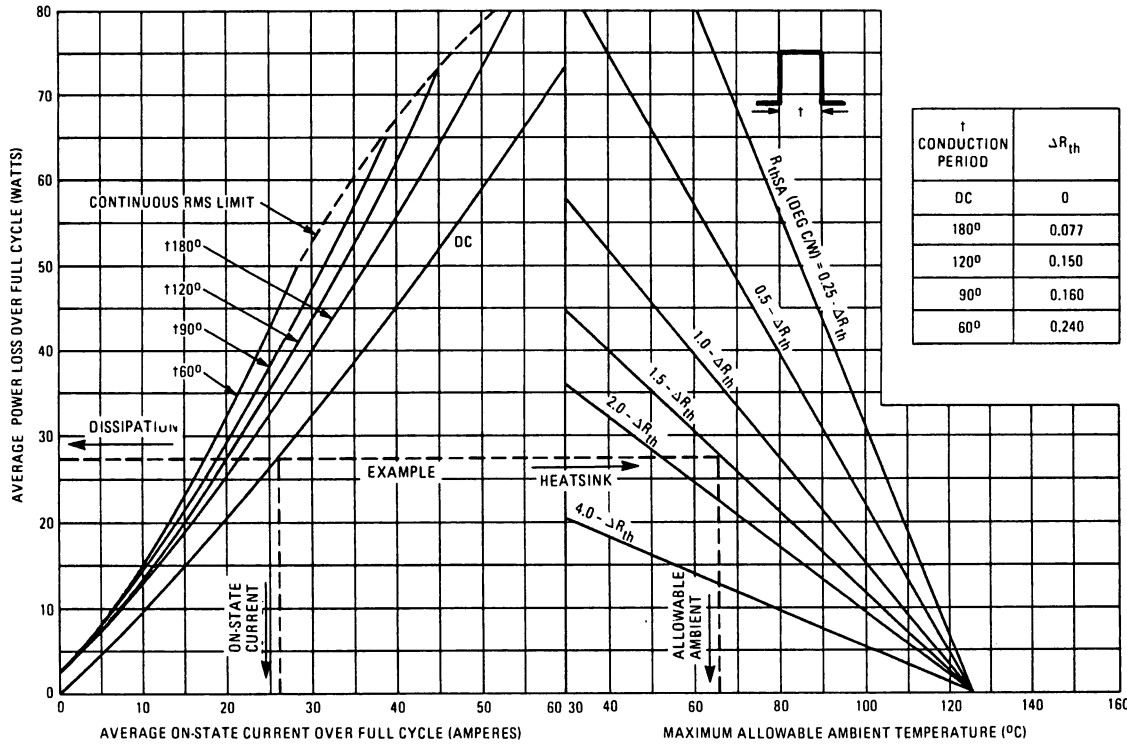




Fig. 12 – Thermal Nomogram (Rectangular Current Waveform, 40 to 400 Hz)

- Notes: A. Maximum allowable heatsink thermal resistance, R_{thSA} , equals the graph value minus the ΔR_{th} factor which allows for instantaneous T_J excursion.
- B. Caution. Data assumes that the controlled rectifier is mounted with thermally conductive grease to achieve $R_{thCS} = 0.25 \text{ deg.C/W}$.

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