



**THE DATASHEET OF
XRT8000IDTR-F**



FEATURES

- Clock Adaptation for Most Popular Telecommunication Frequencies
- Wide Input Frequency Range
- Programmable Output Frequencies
- Less than 0.05UI Wide Band Output Jitter
- Low Power Operation (5V and 3.3V)
- Maximum Lock Time of 45mS

- Cascadable
- No External Components Needed
- Lock Detect Indication Pin

APPLICATIONS

- DSU's, CSU's and Access Equipment
- ISDN Terminals
- Concentrators and Multiplexers

GENERAL DESCRIPTION

The XRT8000 is a dual phase-locked loop chip that generates two simultaneous, very low jitter, output clocks for synchronization applications in wide area networking systems. The outputs are phase locked to the input signal. The chip has four basic modes of operation; referred to as master (FORWARD, REVERSE) and slave (FORWARD, REVERSE) modes (See Figure 1). In the FORWARD mode it accepts up to 16th harmonic of either 1.544MHz or 2.048MHz as input reference and generates 1.2kHz and multiples of 2.4kHz, 56kHz or 64kHz. In the REVERSE mode an input clock of 56kHz or 64kHz is used

to generate 1.544MHz or 2.048MHz output clocks. The SLAVE (FORWARD, REVERSE) modes generate the same output frequencies as the MASTER (FORWARD/REVERSE MODES) except that the input frequency (F_{IN}) is 8kHz. An optional divide by eight can be enabled at each of the outputs.

The input and output frequency selection can be done through a serial microprocessor interface. The XRT8000 is available in either 18 pin SOIC package or 18 pin plastic DIP.

ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|-----------|----------------------------|-----------------------------|
| XRT8000IP | 18 Lead 300 Mil PDIP | -40°C to +85°C |
| XRT8000JD | 18 Lead 300 Mil JEDEC SOIC | -40°C to +85°C |

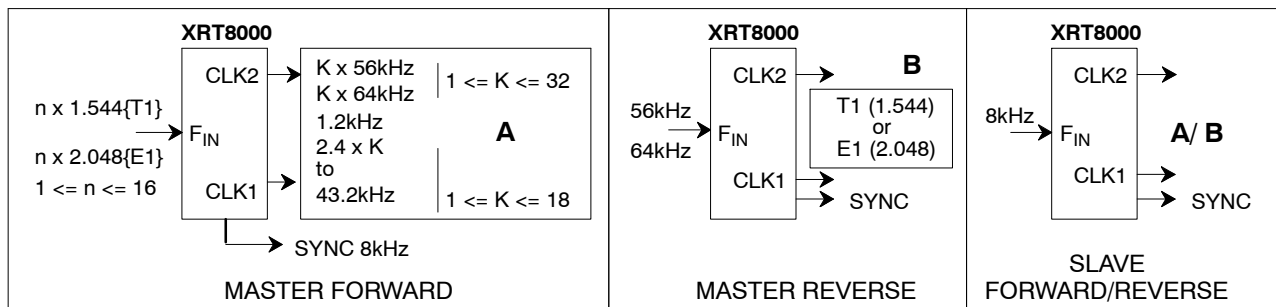


Figure 1. System Diagram

BLOCK DIAGRAM

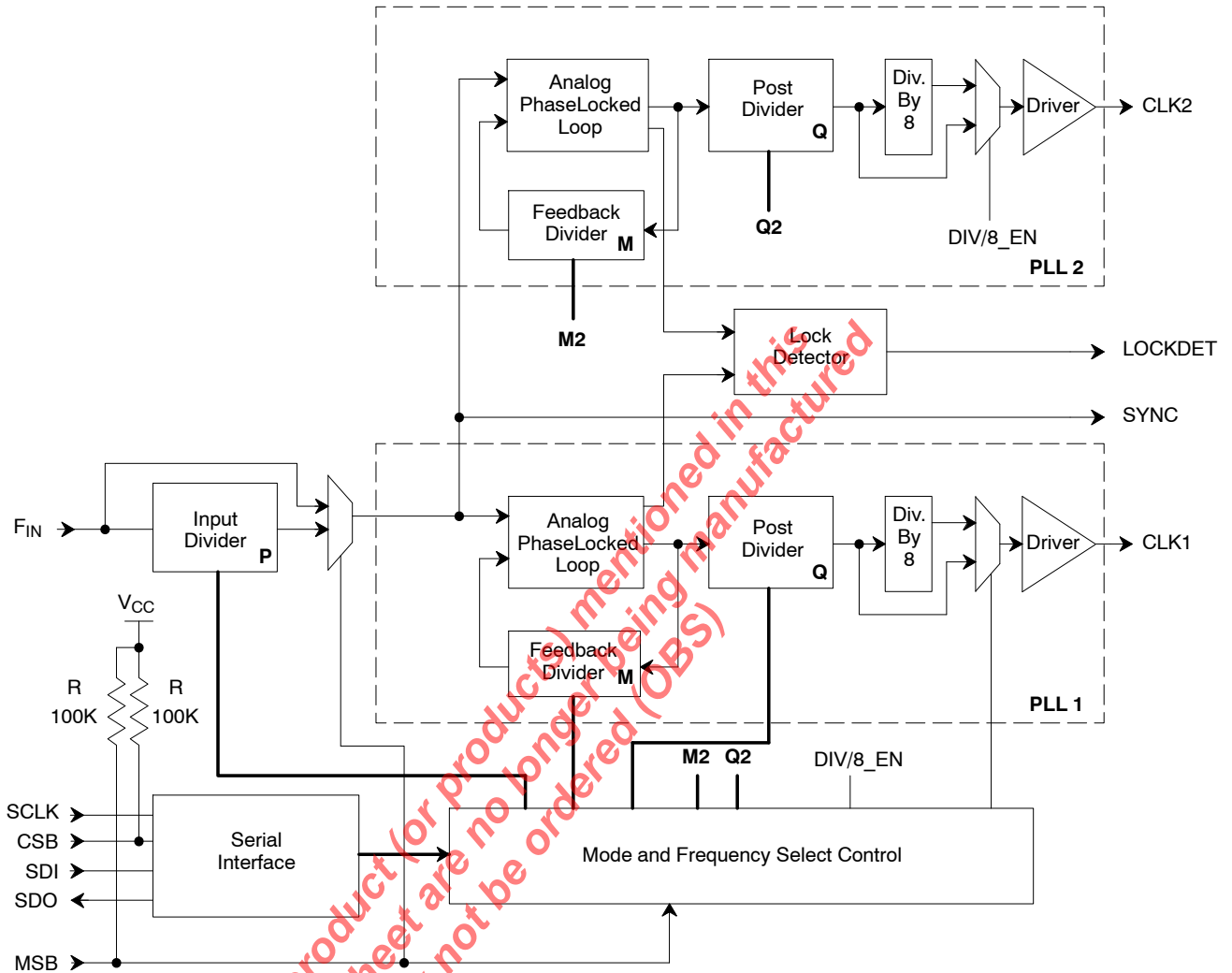
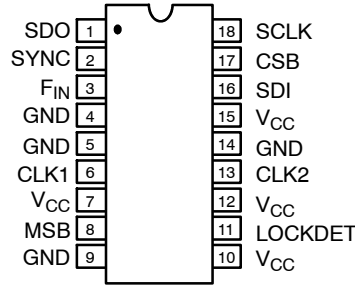
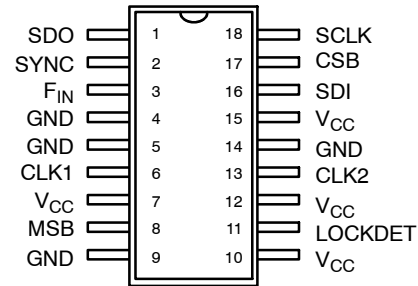


Figure 2. Block Diagram

PIN CONFIGURATION



18 Lead PDIP (0.300")



18 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

| Symbol | Pin# | Type | Description |
|---------|------|------|--|
| SDO | 1 | O | Serial Data Output (Microprocessor Serial Interface). Data output from the command registers. |
| SYNC | 2 | O | An 8kHz Signal SubDivided From FIN. This output can be threestated via CR5. SYNC can be used to synchronize other XRT8000 which are configured in slave modes. |
| FIN | 3 | I | Reference Frequency Input. |
| GND | 4 | | Digital Ground. |
| GND | 5 | | Digital Ground. |
| CLK1 | 6 | O | Clock 1. Output of the phase-locked loop 1. |
| VCC | 7 | | Digital Positive Power Supply. |
| MSB | 8 | I | Master/Slave Mode Select Input. If this input is high, then the MASTER mode is selected. If this input is low, then the SLAVE mode is enabled. This pin is internally pulled up via 100KΩ resistor. |
| GND | 9 | | Analog Ground. |
| VCC | 10 | | Analog Positive Supply. |
| LOCKDET | 11 | O | Lock Detect. This output is high when both phase-locked loops are in lock and will go low if either one of the phase locked loops loses lock. |
| VCC | 12 | | Digital Positive Power Supply. |
| CLK2 | 13 | O | Clock 2. Output of the phase-locked loop 2. |
| GND | 14 | | Digital Ground. |
| VCC | 15 | | Digital Positive Power Supply. |
| SDI | 16 | I | Serial Data Input (Microprocessor Serial Interface) Data input to the command registers. |
| CSB | 17 | I | Chip Select Not (Microprocessor Serial Interface) . When this input is low the data in and out will be shifted in the appropriate registers. Internal pull up (100K). |
| SCLK | 18 | I | Serial Clock Input (Microprocessor Serial Interface) . This clock will serve as a reference to the data streams to SDI and SDO (the positive edge of SCLK is used to latch the data). |

DC ELECTRICAL CHARACTERISTICS (Except Serial Interface) Operating Temperature: -40°C to 85°C
Test Conditions: T_A = 25°C, V_{CC} = 5.0V ± 5% Unless Otherwise Specified

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|-----------------|-------------------------------------|-----|-----|------|------|-----------------------------------|
| V _{IL} | Input low level | | | 0.8 | V | |
| V _{IH} | Input high level | 2.0 | | | V | |
| V _{OL} | Output low level (CLK1,CLK2) | | | 0.4 | V | I _{OL} = -6.0 mA |
| V _{OH} | Output high level (CLK1,CLK2) | 2.4 | | | V | I _{OH} = 6.0 mA |
| V _{OL} | Output low level (LOCKDET,SYNC) | | | 0.4 | V | I _{OL} = -3.0 mA |
| V _{OH} | Output high level (LOCKDET,SYNC) | 2.4 | | | V | I _{OH} = 3.0 mA |
| I _{IL} | Input low current (CSB,MSB) | | | -150 | μA | |
| I _{IH} | Input high current (CSB,MSB) | | | 10 | μA | V _{IN} = V _{CC} |
| I _{IL} | Input low current (except CSB,MSB) | -10 | | | μA | |
| I _{IH} | Input high current (except CSB,MSB) | | | 10 | μA | V _{IN} = V _{CC} |
| I _{CC} | Operating current | | 20 | 35 | mA | No load. Clock = 2.1 MHz |
| R _{IN} | Input pull-up resistance (CSB,MSB) | 50 | 100 | 150 | kΩ | |

AC ELECTRICAL CHARACTERISTICS (See Figure 3)

| Symbol | Parameter | Spec. ³ | Min | Typ | Max | Unit | Conditions |
|------------------------------|--|--------------------|-------|-------|------|------|--|
| T ₁ | Input frequency | | 0.008 | | 32.7 | MHz | |
| T ₂ | Minimum input signal high to low duration | | 12 | | | ns | |
| T ₃ | Output frequency | | 1.2 | | 2.1 | KHz | |
| T ₆ ¹ | Duty cycle CLK1, CLK2 | | 47.5 | 50 | 52.5 | % | V _{CC} /2 switch point. 30pF load. |
| T ₇ ⁴ | Jitter added 8KHz-40KHz | 0.025 | | 0.007 | 0.02 | UI | Output = 1.544MHz |
| T ₇ ⁴ | Jitter added 10Hz-40KHz | 0.025 | | 0.022 | | UI | Output = 1.544MHz |
| T ₇ ⁴ | Broad Band-jitter | 0.05 | | 0.03 | 0.05 | UI | Output = 1.544MHz |
| T ₇ ⁴ | Jitter added 20Hz-100KHz | 1.5 | | 0.05 | 0.07 | UI | Output = 2.048MHz |
| T ₇ ⁴ | Jitter added 18kHz-100KHz | 0.2 | | 0.01 | 0.03 | UI | Output = 2.048MHz |
| T ₈ | Capture time | | | | 40 | ms | |
| T ₉ | Clock output rise time | | | | 10 | ns | 30pF load. Measured at 20/80 % |
| T ₁₀ | Clock output fall time | | | | 10 | ns | 30pF load. Measured at 20/80 % |
| T ₁₁ ² | Duty cycle SYNC | | 40 | | 60 | % | V _{CC} /2 switch point (in master forward mode). 30pF load. |
| T ₁₄ | Delay time between the rising edge of SYNC and the rising edge of CLK1 or CLK2 | | T-20 | T | T+20 | ns | See table 12 for values of T |

Notes:

$$^1 T_6 = \frac{T_4}{(T_4 + T_5)}$$

$$^2 T_{11} = \frac{T_{12}}{(T_{12} + T_{13})}$$

³ Specifications from AT&T Publication 62411 and ITU-T Recommendations G-823 (for 1.544MHz and 2.048MHz, respectively).

⁴ T₇ is guaranteed by characterization, not tested.

Specifications are subject to change without notice.

DC ELECTRICAL CHARACTERISTICS (Except Serial Interface) Operating Temperature: -40°C to 85°C
Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% Unless Otherwise Specified

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|-----------------|-------------------------------------|-----|-----|------|------|-----------------------------------|
| V _{IL} | Input low level | | | 0.8 | V | |
| V _{IH} | Input high level | 2.0 | | | V | |
| V _{OL} | Output low level (CLK1,CLK2) | | | 0.4 | V | I _{OL} = -3 mA |
| V _{OH} | Output high level (CLK1,CLK2) | 2.4 | | | V | I _{OH} = 3 mA |
| V _{OL} | Output low level (LOCKDET,SYNC) | | | 0.4 | V | I _{OL} = -2.5 mA |
| V _{OH} | Output high level (LOCKDET,SYNC) | 2.4 | | | V | I _{OH} = 2.5 mA |
| I _{IL} | Input low current (CSB,MSB) | | | -150 | μA | |
| I _{IH} | Input high current (CSB,MSB) | | | 10 | μA | V _{IN} = V _{CC} |
| I _{IL} | Input low current (except CSB,MSB) | -10 | | | μA | |
| I _{IH} | Input high current (except CSB,MSB) | | | 10 | μA | V _{IN} = V _{CC} |
| I _{CC} | Operating current | | 11 | 30 | mA | No load. Clock = 2.1 MHz |
| R _{IN} | Input pull-up resistance (CSB,MSB) | 50 | 100 | 150 | KΩ | |

AC ELECTRICAL CHARACTERISTICS (See Figure 3)

| Symbol | Parameter | Spec. ³ | Min | Typ | Max | Unit | Conditions |
|------------------------------|---|--------------------|-------|-------|------|------|--|
| T ₁ | Input frequency | | 0.008 | | 32.7 | MHz | |
| T ₂ | Minimum input signal high to low duration | | 12 | | | ns | |
| T ₃ | Output frequency | | 1.2 | | 2.1 | KHz | |
| T ₆ ¹ | Duty cycle CLK1, CLK2 | | 47.5 | 50 | 52.5 | % | V _{CC} /2 switch point. 30pF load. |
| T ₇ ⁴ | Jitter added 8KHz-40KHz | 0.025 | | 0.01 | 0.02 | UI | Output = 1.544MHz |
| T ₇ ⁴ | Jitter added 10Hz-40KHz | 0.025 | | 0.030 | | UI | Output = 1.544MHz |
| T ₇ ⁴ | Broad Band | 0.05 | | 0.035 | 0.05 | UI | Output = 1.544MHz |
| T ₇ ⁴ | Jitter added 20Hz-100KHz | 1.5 | | 0.045 | 0.07 | UI | Output = 2.048MHz |
| T ₇ ⁴ | Jitter added 18kHz-100KHz | 0.2 | | 0.010 | 0.03 | UI | Output = 2.048MHz |
| T ₈ | Capture time | | | | 40 | ms | |
| T ₉ | Clock output rise time | | | | 14 | ns | 30pF load. Measured at 20/80 % |
| T ₁₀ | Clock output fall time | | | | 14 | ns | 30pF load. Measured at 20/80 % |
| T ₁₁ ² | Duty cycle SYNC | | 40 | | 60 | % | V _{CC} /2 switch point (in master forward mode). 30pF load. |
| T ₁₄ | Delay time between SYNC and CLK1 or CLK2 | | T-20 | T | T+20 | ns | See table 12 for values of T |

Notes:

$$^1 T_6 = \frac{T_4}{(T_4 + T_5)}$$

$$^2 T_{11} = \frac{T_{12}}{(T_{12} + T_{13})}$$

³ Specifications from AT&T Publication 62411 and ITUT Recommendations G-823 (for 1.544MHz and 2.048MHz, respectively)

⁴ T₇ is guaranteed by characterization, not tested.

Specifications are subject to change without notice.

AC ELECTRICAL CHARACTERISTICS (See Figure 5).

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---------------------------------|------|------|------|------|------------|
| AC Electrical Characteristics (See Figure 5) | | | | | | |
| T ₂₁ | CSB to SCLK Setup Time | 50 | | | ns | |
| T ₂₂ | SCLK to CSB Hold Time | 20 | | | ns | |
| T ₂₃ | SDI to SCLK Setup Time | 50 | | | ns | |
| T ₂₄ | SCLK to SDI Hold Time | 50 | | | ns | |
| T ₂₅ | SCLK Low Time | 240 | | | ns | |
| T ₂₆ | SCLK High Time | 240 | | | ns | |
| T ₂₇ | SCLK Period | 500 | | | ns | |
| T ₂₈ | SCLK to CSB Hold Time | 50 | | | ns | |
| T ₂₉ | CSB Inactive Time | 250 | | | ns | |
| T ₃₀ | SCLK to SDO Valid | | | 200 | ns | |
| T ₃₁ | SCLK to SDOx Delay | | | 100 | ns | |
| T ₃₂ | SCLK Edge or CSB Edge to SDO Hz | | 100 | | ns | |
| T ₃₃ | Rise/Fall Time SDO Output | | | 40 | ns | |

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

| | | | |
|--------------------|---|-----------------------|----------------------|
| Supply Range | 7V | Operating Temperature | 40°C to +85°C |
| Voltage at Any Pin | GND-0.3V to V _{CC} +0.3V | Storage Temperature | 40°C to +150°C |
| | | Package Dissipation | 500mW |

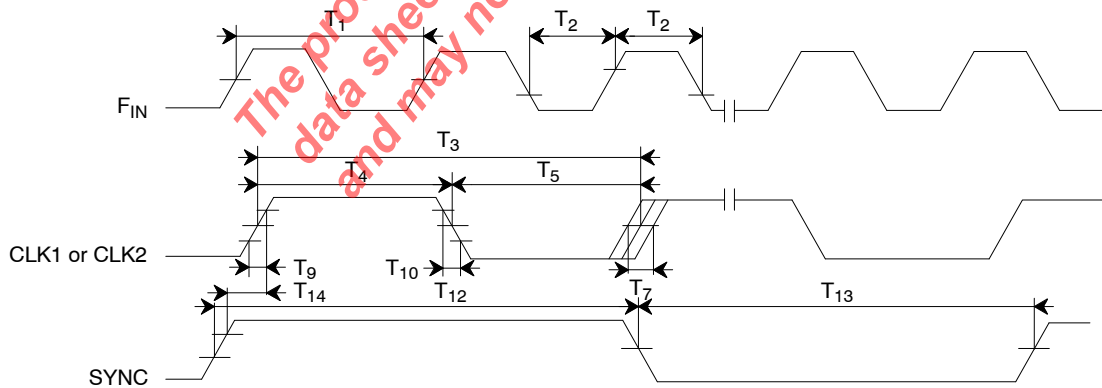


Figure 3. Clocks Timing

SYSTEM DESCRIPTION

On power up the clock outputs of XRT8000 will be tri-stated. This means that no clocks will be seen at the outputs and lock detect output will be low. After power up the XRT8000 needs to be initialized. Therefore a serial interface is provided to load the internal registers. These registers will define the modes of operation, the output frequencies and enabling the clock outputs.

Master/Forward Mode of Operation

When the XRT8000 device is operating in the “Master/Forward” Mode, it will receive either an “ $n \times 2.048 \text{ MHz}$ ” or “ $n \times 1.544 \text{ MHz}$ ” clock signal at the FIN input (pin3); where “ n ” can range from 1 to 16. From this input signal, the XRT8000 device will internally divide and synthesize the following signals.

At the CLK1 and/or CLK2 output pins:

- $k \times 56 \text{ kHz}$
- $k \times 64 \text{ kHz}$
- $(k \times 56 \text{ kHz})/8$
- $(k \times 64 \text{ kHz})/8$

where k can range from 1 to 32.

At the SYNC Output pin:

- 8kHz

The user selects and configures the XRT8000 device to generate these clock frequencies by writing the appropriate values into the Command Registers (CR1, CR2, CR3, CR4 and CR5), via the Microprocessor Serial Interface.

Reverse Mode of Operation

When the XRT8000 device is operating in the “Reverse” Mode, it will receive either a 56 kHz or 64 kHz clock signal

at the FIN input. From this input signal, the XRT8000 device will synthesize any of the following clock signal frequencies.

At the CLK1 and/or CLK2 output pins:

- 1.544 MHz
- 2.048 MHz
- $1.544 \text{ MHz}/8 = 193 \text{ kHz}$
- $2.048 \text{ MHz}/8 = 256 \text{ kHz}$

At the SYNC output pin:

- 8 kHz

The user can configure the XRT8000 device to generate these clock frequencies by writing the appropriate values into the Command Registers (CR1, CR2, CR3, CR4 and CR5), via the Microprocessor Serial Interface.

Note: in the REVERSE mode the contents of CR3 and CR4 has to be all one's.

Slave (Forward, Reverse) Mode of Operation

To activate the slave modes of operations the input MSB must be tied low. In these modes an 8kHz signal must be applied to the FIN input in order to obtain output frequencies at T1 or E1 rates. The output frequencies can be selected via the serial interface in a similar fashion as described in the master forward and reverse modes.

The Lock Detect Output Pin

If both PLL's are enabled and in locked state then LOCKDET will be active. If one PLL loses lock then LOCKDET will be false. If only one PLL is enabled then only the active PLL will control the state of LOCKDET.

The Command Registers

Between the MSB input pin and the Command Registers, the user can configure the XRT8000 device into any of the operating modes that have been described in this data sheet. The user can access these Command Registers

via the Microprocessor Serial Interface.

Table 1 presents the Address Location and Format for each of the Command Registers, within the XRT8000 device.

| AD2~0 | Register | D4 | D3 | D2 | D1 | D0 |
|-------|----------|----------|----------|----------|----------|----------|
| 000 | CR1 | IOC4 | IOC3 | IOC2 | IOC1 | PL1EN |
| 001 | CR2 | M4 | M3 | M2 | M1 | PL2EN |
| 010 | CR3 | SEL14 | SEL13 | SEL12 | SEL11 | SEL10 |
| 011 | CR4 | SEL24 | SEL23 | SEL22 | SEL21 | SEL10 |
| 100 | CR5 | SYNCEN | CLK1EN | CLK2EN | PL2/8 | PL1/8 |
| 101 | CR6 | Reserved | Reserved | Reserved | Reserved | Reserved |
| 110 | CR7 | Reserved | Reserved | Reserved | Reserved | Reserved |
| 111 | CR8 | Reserved | Reserved | Reserved | Reserved | Reserved |

Table 1. Control Registers

The next few pages describe the role/functionality of each bit-field within the Command Registers.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

CR1 Register (Power On State = “00000”)

D0 (PL1EN):

Enable control for PLL1. If PL1EN = “1”, then PLL1 is enabled. Otherwise, if PL1EN = “0”, then PLL1 is disabled.

D1~D4 (IOC1~IOC4):

These four bit-fields function as the control bits for PLL1 and PLL2 operation modes. These bits select FORWARD, REVERSE, DATA, Kx56 or Kx64 clock rates. Multiplier “K” in Kx56 and Kx64 refers to harmonics of

56kHz or 64kHz clocks, this notation is extended to 1,544kHz and 2,048kHz frequencies in the following table (Table 2).

Note: The value of “K” for PLL1 and PLL2 are independent of each other.

Table 2

Table 2 creates the values of D1 through D4 within the CRI command register to the operating mode of the XRT8000 device.

| IOC4 | IOC3 | IOC2 | IOC1 | Input Freq. [kHz] | PLL1 Output [kHz] | PLL2 Output [kHz] | Mode |
|------|------|------|------|-------------------|-------------------|-------------------|---------|
| 0 | 0 | 0 | 0 | nx1544 | Kx56 | Kx56 | Forward |
| 0 | 0 | 0 | 1 | nx1544 | Kx56 | Kx64 | Forward |
| 0 | 0 | 1 | 0 | nx1544 | Kx64 | Kx64 | Forward |
| 0 | 0 | 1 | 1 | nx1544 | Kx56 | DATA | Forward |
| 0 | 1 | 0 | 0 | nx1544 | Kx64 | DATA | Forward |
| 0 | 1 | 0 | 1 | nx1544 | DATA | DATA | Forward |
| 0 | 1 | 1 | 0 | 56 | 1544 | 1544 | Reverse |
| 0 | 1 | 1 | 1 | 8K | 1544 | 2048 | Reverse |
| 1 | 0 | 0 | 0 | nx2048 | Kx56 | Kx56 | Forward |
| 1 | 0 | 0 | 1 | nx2048 | Kx56 | Kx64 | Forward |
| 1 | 0 | 1 | 0 | nx2048 | Kx64 | Kx64 | Forward |
| 1 | 0 | 1 | 1 | nx2048 | Kx56 | DATA | Forward |
| 1 | 1 | 0 | 0 | nx2048 | Kx64 | DATA | Forward |
| 1 | 1 | 0 | 1 | nx2048 | DATA | DATA | Forward |
| 1 | 1 | 1 | 0 | 8 | 1544 | 2048 | Reverse |
| 1 | 1 | 1 | 1 | 64 | 2048 | 2048 | Reverse |

Table 2. Operation Mode/Output Clock Frequency Select Options Via the D1 Through D4 Bits within the CRI Register

Note:

- ¹ The values of “n” are selected via the M1 through M4 bits, within the CR2 Register (see Table 3).
- ² The values of “k” are selected via the Sel14 through SelP bits within the CR3 Register (see Table 4).

CR2 Register (Power On State = “00000”)

D0 (PL2EN):

Enable control for PLL2. If PL2EN = “1”, then PLL2 is enabled. Otherwise, if PL2EN = “0”, PLL2 is disabled.

D1~D4 (M1~M4):

Control bits for prescaler divider. These bits will set the divide ratio of the prescaler such that in MASTER/FORWARD or REVERSE modes the output of this block is always at 8kHz. The settings for M4~M1 bits is based on the input frequency and the mode of operation (which is determined by the state of IOC4~IOC1 bits) is provided in Table 3.

| M4 | M3 | M2 | M1 | Mode | Input Freq.[kHz] |
|----|----|----|----|---------|-------------------|
| 0 | 0 | 0 | 0 | Forward | 1x(1544 or 2048) |
| 0 | 0 | 0 | 1 | Forward | 2x(1544 or 2048) |
| 0 | 0 | 1 | 0 | Forward | 3x(1544 or 2048) |
| 0 | 0 | 1 | 1 | Forward | 4x(1544 or 2048) |
| 0 | 1 | 0 | 0 | Forward | 5x(1544 or 2048) |
| 0 | 1 | 0 | 1 | Forward | 6x(1544 or 2048) |
| 0 | 1 | 1 | 0 | Forward | 7x(1544 or 2048) |
| 0 | 1 | 1 | 1 | Forward | 8x(1544 or 2048) |
| 1 | 0 | 0 | 0 | Forward | 9x(1544 or 2048) |
| 1 | 0 | 0 | 1 | Forward | 10x(1544 or 2048) |
| 1 | 0 | 1 | 0 | Forward | 11x(1544 or 2048) |
| 1 | 0 | 1 | 1 | Forward | 12x(1544 or 2048) |
| 1 | 1 | 0 | 0 | Forward | 13x(1544 or 2048) |
| 1 | 1 | 0 | 1 | Forward | 14x(1544 or 2048) |
| 1 | 1 | 1 | 0 | Forward | 15x(1544 or 2048) |
| 1 | 1 | 1 | 1 | Forward | 16x(1544 or 2048) |
| x | x | x | x | Reverse | 56 |
| x | x | x | x | Reverse | 64 |

Note:

This table applies to MASTER (FORWARD, REVERSE) mode only

Table 3. CR2 Register

CR3 Register (Power On State = “00000”)

SEL14~SEL10:

These bits control two parameters:

1.) The frequency multiplier “K” for the PLL1, after selecting Kx56, Kx64 or DATA mode through register CR1 ($1 < K < 32$), and

2.) The delay time between the rising edge of the sync output signal (Pin 2) and the rising edge of the CLK1 or CLI 2 output signals (See Table 6).

Table 4 provides the settings for SEL14~10 bits to generate harmonic of 56kHz, 64kHz or 1.2kHz at the output of PLL1.

| SEL14~SEL10 | PLL1 Output Frequency (kHz) | | | |
|-------------|-----------------------------|-----------|-----------|-----------|
| | K factor | Kx56 MODE | Kx64 MODE | DATA MODE |
| 00000 | 1 | 56 | 64 | 1.2 |
| 00001 | 2 | 112 | 128 | 2.4 |
| 00010 | 3 | 168 | 192 | 4.8 |
| 00011 | 4 | 224 | 256 | 7.2 |
| 00100 | 5 | 280 | 320 | 9.6 |
| 00101 | 6 | 336 | 384 | 12 |
| 00110 | 7 | 392 | 448 | 14.4 |
| 00111 | 8 | 448 | 512 | 16.8 |
| 01000 | 9 | 504 | 576 | 19.2 |
| 01001 | 10 | 560 | 640 | 21.6 |
| 01010 | 11 | 616 | 704 | 24 |
| 01011 | 12 | 672 | 768 | 26.4 |
| 01100 | 13 | 728 | 832 | 28.8 |
| 01101 | 14 | 784 | 896 | 31.2 |
| 01110 | 15 | 840 | 960 | 33.6 |
| 01111 | 16 | 896 | 1024 | 36 |
| 10000 | 17 | 952 | 1088 | 38.4 |
| 10001 | 18 | 1008 | 1152 | 40.8 |
| 10010 | 19 | 1064 | 1216 | 43.2 |
| 10011 | 20 | 1120 | 1280 | 43.2 |
| 10100 | 21 | 1176 | 1344 | 43.2 |
| 10101 | 22 | 1232 | 1408 | 43.2 |
| 10110 | 23 | 1288 | 1472 | 43.2 |
| 10111 | 24 | 1344 | 1536 | 43.2 |
| 11000 | 25 | 1400 | 1600 | 43.2 |
| 11001 | 26 | 1456 | 1664 | 43.2 |
| 11010 | 27 | 1512 | 1728 | 43.2 |
| 11011 | 28 | 1568 | 1792 | 43.2 |
| 11100 | 29 | 1624 | 1856 | 43.2 |
| 11101 | 30 | 1680 | 1920 | 43.2 |
| 11110 | 31 | 1736 | 1984 | 43.2 |
| 11111 | 32 | 1792 | 2048 | 43.2 |

Note:

This table applies to forward or slave modes only

Table 4. CR3 Register

CR4 Register (Power On State = “00000”)

SEL24~SEL20:

These bits control the frequency multiplier “K” for the PLL2, after selecting Kx56, Kx64 or DATA mode through register CR1 (1 < K < 32).

Table 5 provides the settings for SEL24~20 bits to generate harmonic of 56kHz, 64kHz or 1.2kHz at the output of PLL2.

| SEL24~SEL20 | PLL2 Output Frequency (kHz) | | | |
|-------------|-----------------------------|-----------|-----------|-----------|
| | K factor | Kx56 MODE | Kx64 MODE | DATA MODE |
| 00000 | 1 | 56 | 64 | 1.2 |
| 00001 | 2 | 112 | 128 | 2.4 |
| 00010 | 3 | 168 | 192 | 4.8 |
| 00011 | 4 | 224 | 256 | 7.2 |
| 00100 | 5 | 280 | 320 | 9.6 |
| 00101 | 6 | 336 | 384 | 12 |
| 00110 | 7 | 392 | 448 | 14.4 |
| 00111 | 8 | 448 | 512 | 16.8 |
| 01000 | 9 | 504 | 576 | 19.2 |
| 01001 | 10 | 560 | 640 | 21.6 |
| 01010 | 11 | 616 | 704 | 24 |
| 01011 | 12 | 672 | 768 | 26.4 |
| 01100 | 13 | 728 | 832 | 28.8 |
| 01101 | 14 | 784 | 896 | 31.2 |
| 01110 | 15 | 840 | 960 | 33.6 |
| 01111 | 16 | 896 | 1024 | 36 |
| 10000 | 17 | 952 | 1088 | 38.4 |
| 10001 | 18 | 1008 | 1152 | 40.8 |
| 10010 | 19 | 1064 | 1216 | 43.2 |
| 10011 | 20 | 1120 | 1280 | 43.2 |
| 10100 | 21 | 1176 | 1344 | 43.2 |
| 10101 | 22 | 1232 | 1408 | 43.2 |
| 10110 | 23 | 1288 | 1472 | 43.2 |
| 10111 | 24 | 1344 | 1536 | 43.2 |
| 11000 | 25 | 1400 | 1600 | 43.2 |
| 11001 | 26 | 1456 | 1664 | 43.2 |
| 11010 | 27 | 1512 | 1728 | 43.2 |
| 11011 | 28 | 1568 | 1792 | 43.2 |
| 11100 | 29 | 1624 | 1856 | 43.2 |
| 11101 | 30 | 1680 | 1920 | 43.2 |
| 11110 | 31 | 1736 | 1984 | 43.2 |
| 11111 | 32 | 1792 | 2048 | 43.2 |

Note:

This table applies to forward or slave forward mode only

Table 5. CR4 Register

Table 6 presents information on the delay between the rising edge of SYNC and the CLK1 or CLKL output signals. It is important to note that this delay behaves as a function of the settings within the CR3 register.

| T values (nS) | | | |
|---------------|----|-----------|-----------|
| SEL14-SEL10 | K | Kx56 MODE | Kx64 MODE |
| 00000 | 1 | 372 | 326 |
| 00001 | 2 | 372 | 326 |
| 00010 | 3 | 372 | 326 |
| 00011 | 4 | 372 | 326 |
| 00100 | 5 | 446 | 391 |
| 00101 | 6 | 372 | 326 |
| 00110 | 7 | 319 | 279 |
| 00111 | 8 | 279 | 244 |
| 01000 | 9 | 496 | 434 |
| 01001 | 10 | 446 | 301 |
| 01010 | 11 | 406 | 355 |
| 01011 | 12 | 372 | 326 |
| 01100 | 13 | 343 | 301 |
| 01101 | 14 | 319 | 279 |
| 01110 | 15 | 298 | 260 |
| 01111 | 16 | 279 | 244 |
| 10000 | 17 | 525 | 460 |
| 10001 | 18 | 496 | 434 |
| 10010 | 19 | 470 | 411 |
| 10011 | 20 | 446 | 391 |
| 10100 | 21 | 425 | 372 |
| 10101 | 22 | 406 | 355 |
| 10110 | 23 | 388 | 340 |
| 10111 | 24 | 372 | 326 |
| 11000 | 25 | 357 | 312 |
| 11001 | 26 | 343 | 301 |
| 11010 | 27 | 331 | 289 |
| 11011 | 28 | 319 | 279 |
| 11100 | 29 | 308 | 279 |
| 11101 | 30 | 298 | 260 |
| 11110 | 31 | 288 | 252 |
| 11111 | 32 | 279 | 244 |

Notes:

¹ This table does not apply to the data mode or to Kx56 mode with the divide by eight enabled.

² This table does not apply when the XRT8000 device is operating in the REVERSE Mode.

Table 6. Delay Time Between SYNC and CLK1 or CLK2

CR5 Register (Power On State = “00000”)

D0 : (PL1/8) :

Select the divider by 8 for PLL1,
 PL1/8 = “1” CLK1 output frequency is divided by 8.
 PL1/8 = “0” CLK1 output frequency is as per table 4.

D1 : (PL2/8) :

Select the divider by 8 for PLL2,
 PL2/8 = “1” CLK2 output frequency is divided by 8.
 PL2/8 = “0” CLK2 output frequency is as per table 5.

D2 : (CLK2EN) , PLL2:

Output enable bit,
 CLK2EN = “1” CLK2 output is enabled.
 CLK2EN = “0” CLK2 output is Tri State D.

D3 : (CLK1EN) , PLL1:

Output enable bit,
 CLK1EN = “1” CLK1 output is enabled.
 CLK1EN = “0” CLK1 output is Tri State D.

D4 : (SYNCEN) , 8kHz SYNC enable bit:

SYNCEN = “1” SYNC output is enabled.
 SYNCEN = “0” SYNC output is Tri State D.

CR6 to CR7 Register

Register reserved for future use.

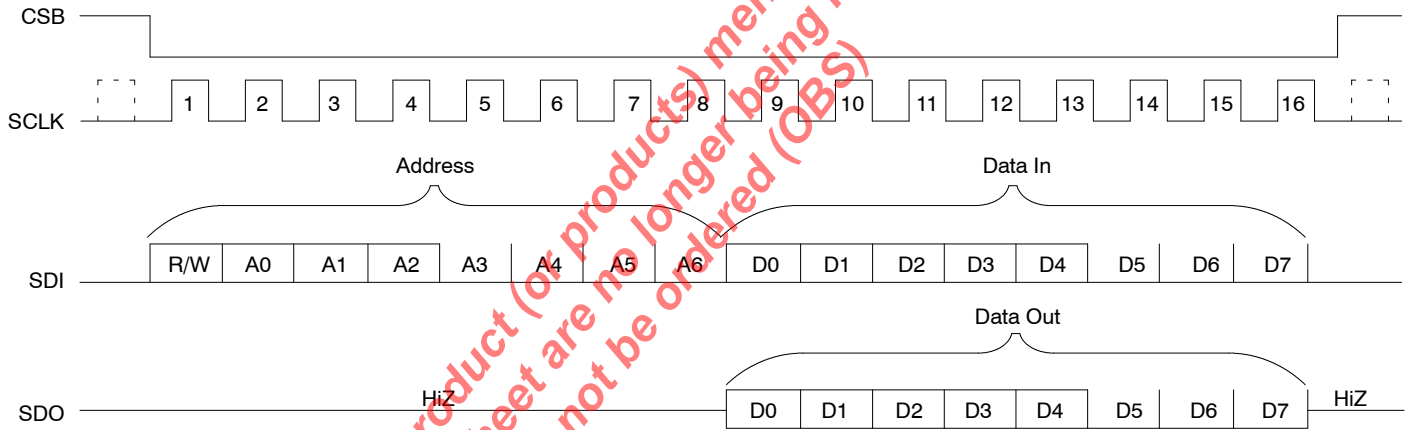


Figure 4. Serial Processor Interface Data Structure

Note:

- A3, A4 and A5 always Low.
- A6 Do not care.
- R/W bit = 1 for a read operation
- 2 for a write operation
- D5, D6 and D7 always Low

SERIAL INTERFACE

The serial interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

- CSB Chip Select (Active Low)
- SCLK Serial Clock Input
- SDI Serial Data Input
- SDO Serial Data Output

Using the Serial Interface

The following instructions, for using the serial interface, are best understood by referring to the diagram in *Figure 4*.

In order to use the serial interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a “Read” or “Write” operation by asserting the active low Chip Select Input pin (CSB). It is important to note that the user assert CSB low coincident with the falling edge of SCLK.

Once the CSB input has been asserted the type of operation and the target register address must be provided by the user. The user will provide this information to the serial interface by writing four serial bits of data to the SDI input. Note: Each of these bits will be “clocked” into the SDI input, on the rising edge of SCLK. These four bits are identified and described below.

Bit 1: The R/W (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a read or a write operation. A “1” in this bit will cause a “Read” operation; whereas a “0” in this bit will cause a “Write” operation.

Bits 2 through 4: The three (3) bit address value (A0, A1, A2)

These next three rising edges of the SCLK signal will clock in the 3-bit address value for this particular read (or write) operation. This address selects the command register within XRT8000 device that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin, in ascending order with the LSB first. (A3 to A5 must be low A6 is a “don’t care”).

Once the “Read/Write” and Address bits have been written, the subsequent action depends upon whether the current operation is a “Read” or “Write” operation.

Read Operation

Once the last address bit (A2) has been clocked into the SDI input, the read operation will proceed through an idle period, lasting four SCLK periods. On the falling edge of SCLK Cycle “8” (See *Figure 4*) the serial output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed command register (at Address A2, A1, A0) via the SDO pin. The SDO pin will output this five bit data word (D0 through D4) in ascending order, with the LSB first, on the rising edges of the SCLK pin.

Write Operation

Once the last address bit (A2) has been clocked into the SDI input, the write operation will proceed through an idle period, lasting four SCLK periods. Prior to the rising edge of SCLK Cycle #9 (See *Figure 4*) the user must begin to apply the eight-bit data word, that he/she wishes to write to the serial input interface onto the SDI input pin. The microprocessor serial interface will catch the value on the SDI pin on the rising edge of the SCLK. The user must apply this word (D0 through D7), serially, in ascending order with the LSB first.

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the serial interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this “combined” signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

Notes:

1. Prior to reading data from (or writing data to) the Serial Interface, the user is not required to provide a clock signal at the SCLK. However, shortly before performing any read or write operations with the Serial Interface, the user must supply the clock signal to the SCLK input pin.
2. Each Read or Write operation, with the Serial Interface, will require 16 SCLK periods, as depicted in *Figure 4*.
3. Upon completion of a Read or Write cycle, the user must negate CSB for at least 250ns (see timing parameter T29 in the AC Characteristics), before asserting it again for the next Read or Write operation.

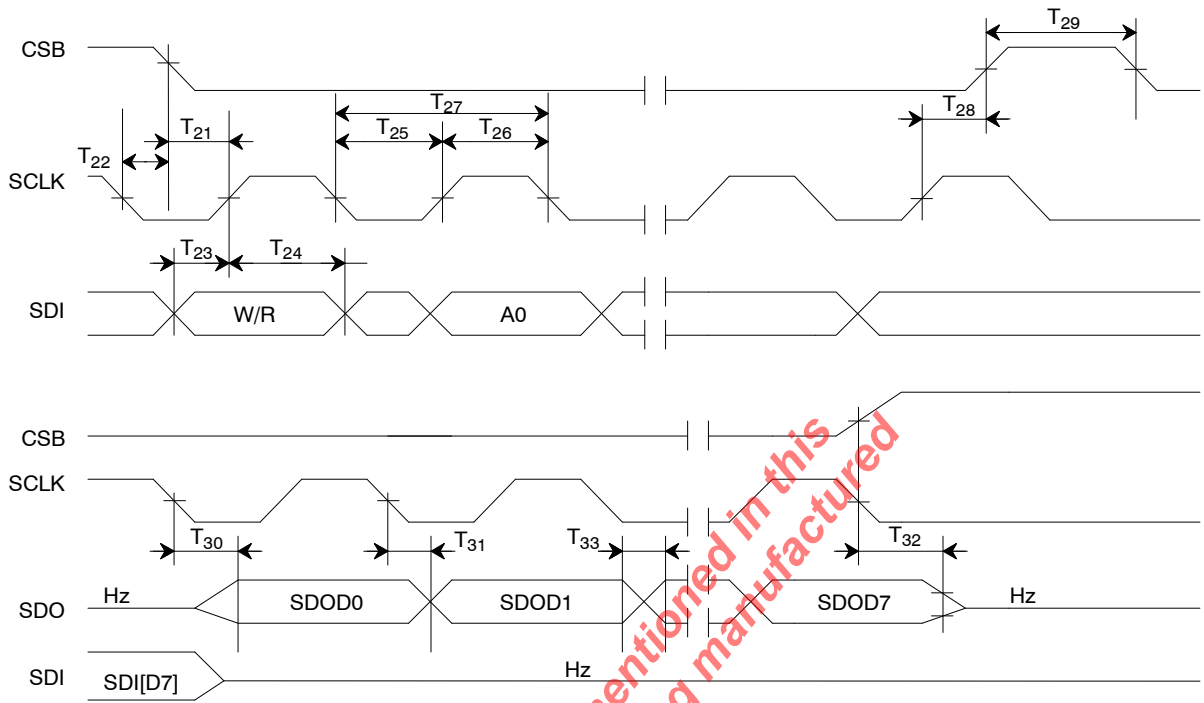


Figure 5. Serial Interface Timing

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CONFIGURATION DIAGRAMS

The following six figures depict all of the configuration possibilities for the XRT8000. The table in the left (F_{IN}) lists different possibilities for reference clock input, while

the table in the right lists all the possibilities for two output clocks.

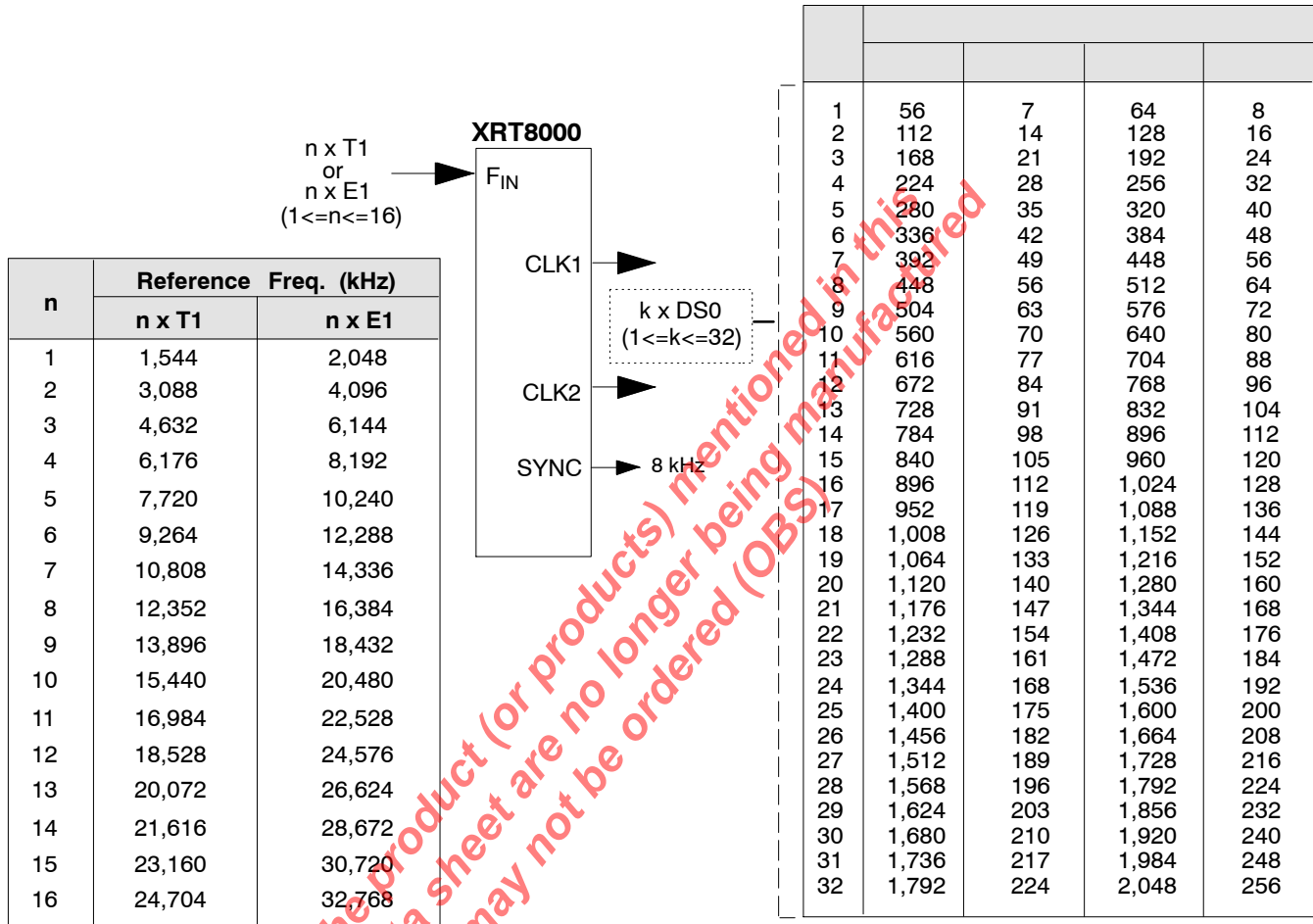


Figure 6. Master Forward Mode

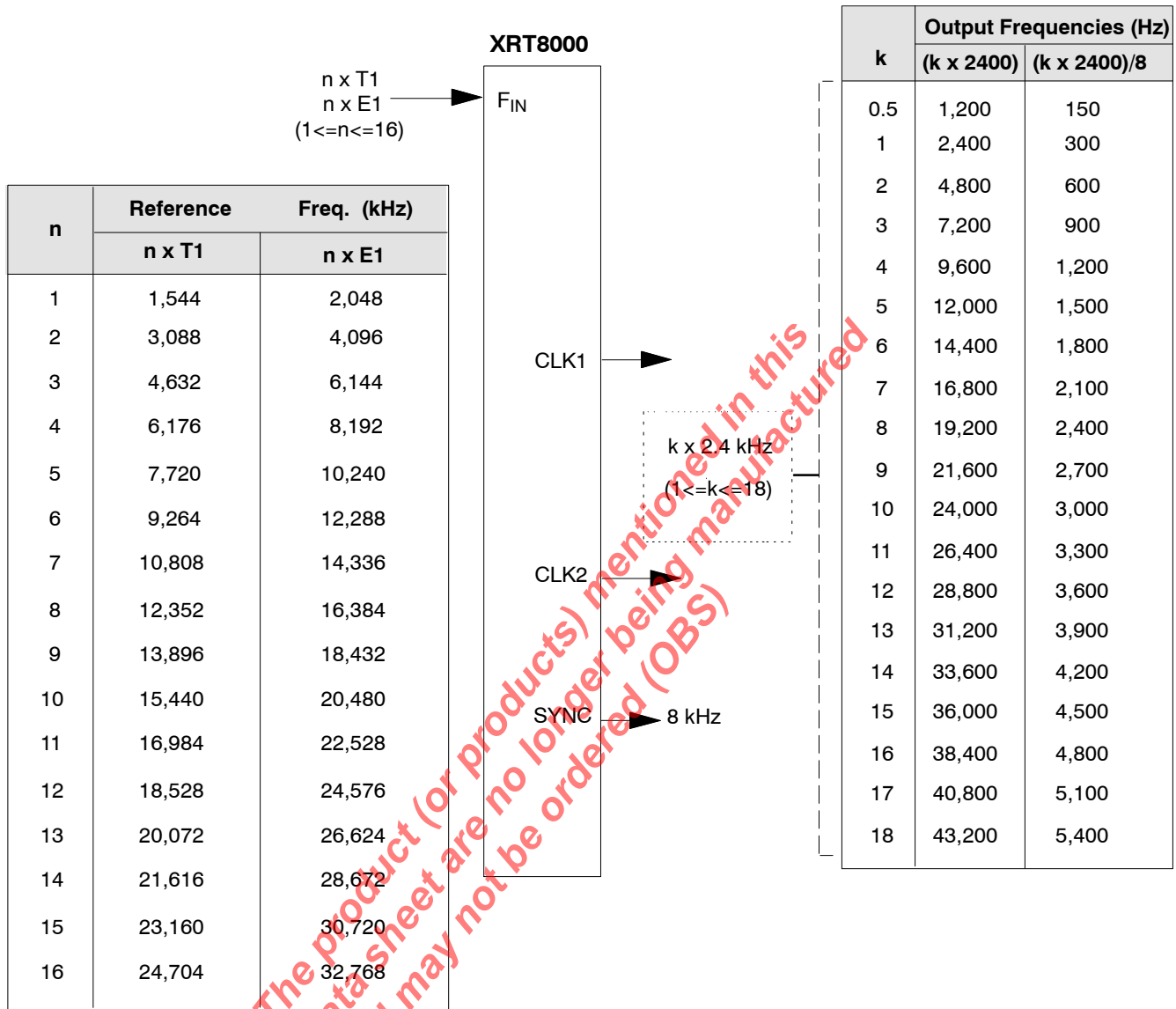


Figure 7. Master Forward Mode (Cont'd)

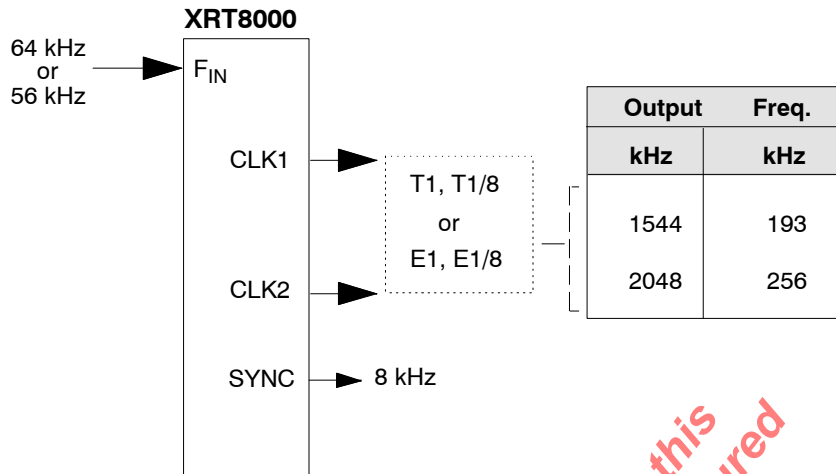


Figure 8. Master Reverse Mode

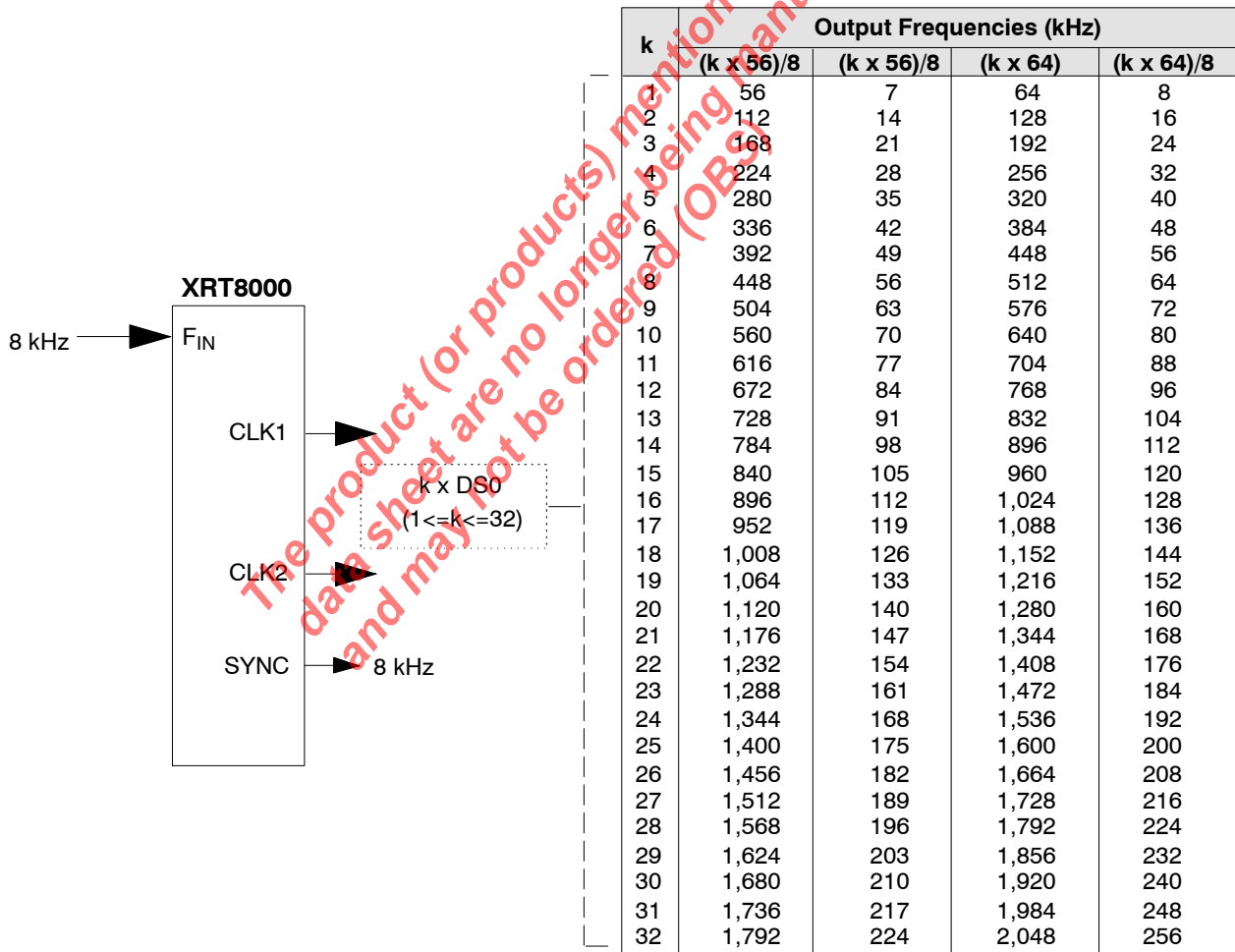


Figure 9. Slave Forward Mode

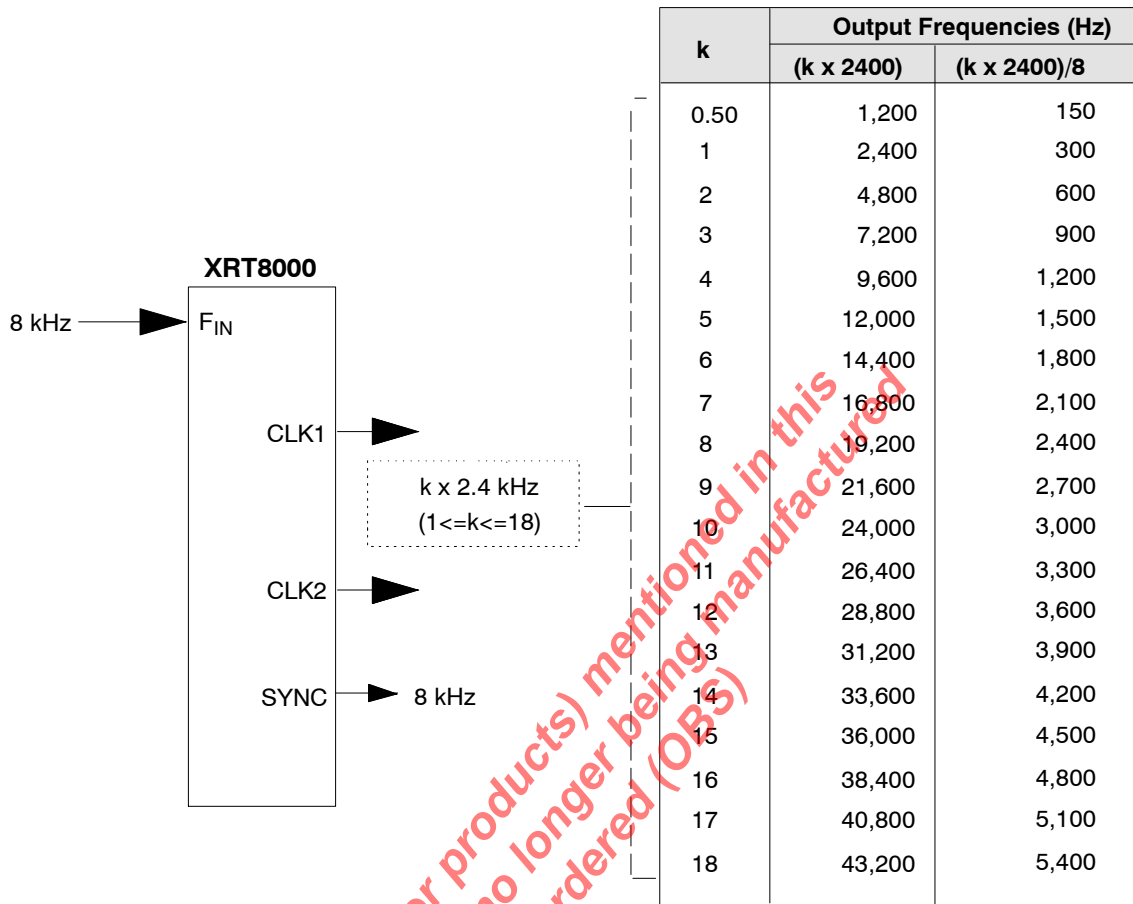


Figure 10. Slave Forward Mode (Cont'd)

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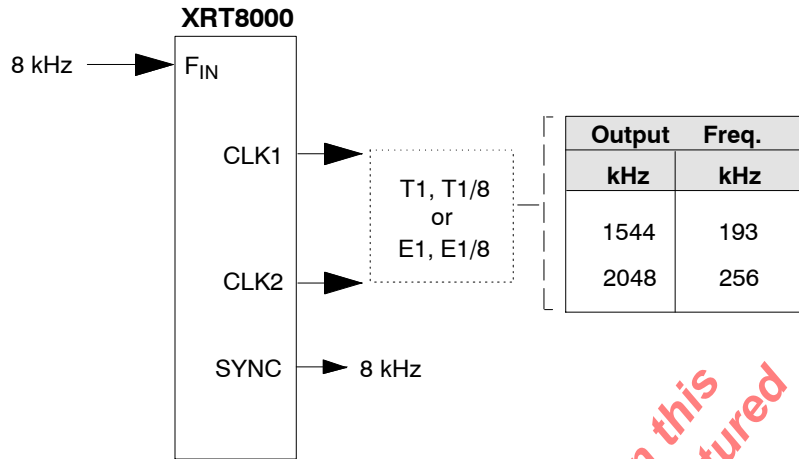


Figure 11. Slave Reverse Mode (Cont'd)

Board Layout Considerations

The CLK1 and CLK2 outputs are surrounded with supply pins (GND(514),Vcc(712). It is recommended to decouple these supplies with a 0.1uF very close to the pins. The positive supply (7,12,15) and ground pins (4,5,14) can all be connected to the Digital Supply and Ground.

The internal VCO has its proper supply's pins (GND 9, Vcc 10) these supply pins have to be decoupled by a 0.1uF capacitor and should be connected to an Analog

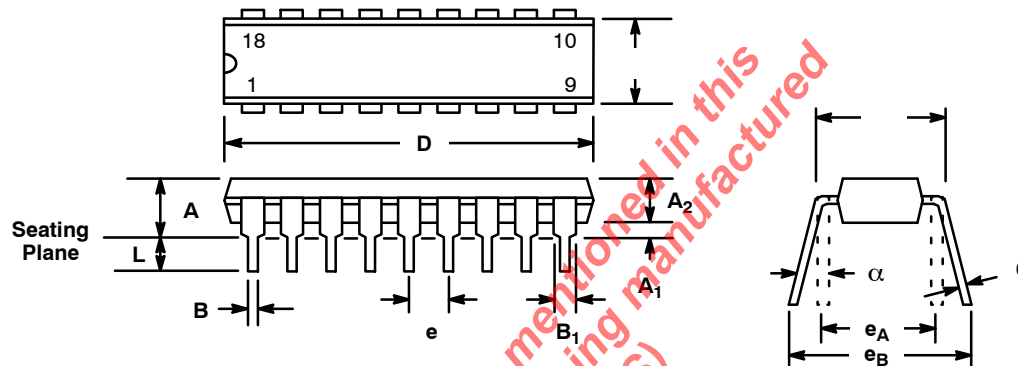
Supply if possible. If there is no Analog Supply, then connect these pins as close as possible to the supply source.

If the layout is done with separate layers for the supplies, cut an island under the XTT8000 such that no current flows under the circuit. It has been observed that coupling can occur because heavy digital currents are flowing under the locations of the XRT8000.

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18 LEAD PLASTIC DUALINLINE (300 MIL PDIP)

Rev. 1.00

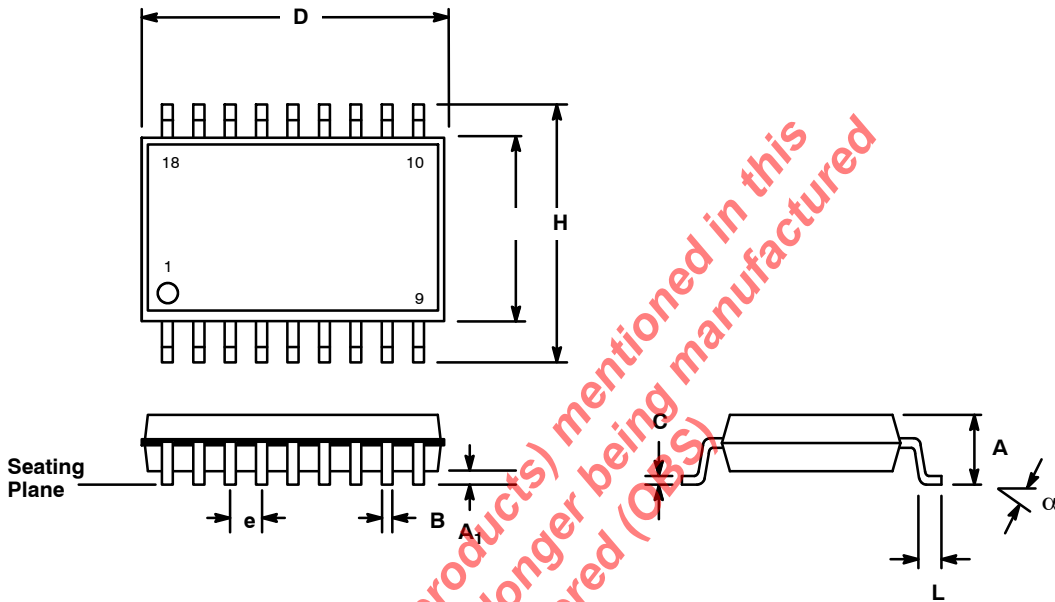


| SYMBOL | INCHES | | MILLIMETERS | |
|----------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.145 | 0.210 | 3.68 | 5.33 |
| A ₁ | 0.015 | 0.070 | 0.38 | 1.78 |
| A ₂ | 0.115 | 0.195 | 2.92 | 4.95 |
| B | 0.014 | 0.024 | 0.36 | 0.56 |
| B ₁ | 0.030 | 0.070 | 0.76 | 1.78 |
| C | 0.008 | 0.014 | 0.20 | 0.38 |
| D | 0.845 | 0.925 | 21.46 | 23.50 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E ₁ | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| e _A | 0.300 BSC | | 7.62 BSC | |
| e _B | 0.310 | 0.430 | 7.87 | 10.92 |
| L | 0.115 | 0.160 | 2.92 | 4.06 |
| α | 0° | 15° | 0° | 15° |

Note: The control dimension is the inch column

18 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)

Rev. 1.00



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

| SYMBOL | INCHES | | MILLIMETERS | |
|----------------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A ₁ | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.447 | 0.463 | 11.35 | 11.75 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

Note: The control dimension is the millimeter column

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