THE DATASHEET OF

XR16V2652IL-F

GENERAL DESCRIPTION

The XR16V2652[1] (V2652) is a high performance dual universal asynchronous receiver and transmitter (UART) with 32 byte TX and RX FIFOs. The device operates from 2.25 to 3.6 volts with 5 Volt tolerant inputs and is pin-to-pin compatible to Exar's ST16C2552, XR16L2552, XR16V2552 and XR16L2752. The V2652 register set is compatible to the ST16C2552 and the XR16V2552. It supports the Exar's enhanced features of selectable FIFO trigger level, automatic hardware (RTS/CTS) and software flow control and a complete modem interface. Onboard registers provide the user with operational status and data error flags. An internal loopback capability allows system diagnostics. Independent programmable baud rate generators are provided in each channel to select data rates up to 16 Mbps at 3.3 Volt with 4X sampling clock. The V2652 is available in 44-pin PLCC and 32-pin QFN packages.

NOTE: *1 Covered by U.S. Patent #5,649,122*

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

- 2.25 to 3.6 Volt Operation
- 5 Volt Tolerant Inputs
- Pin-to-pin compatible to Exar's XR16V2752 in the 44-PLCC package
- Two independent UART channels
  - Register set compatible to ST16C2552
  - Data rate of up to **16 Mbps at 3.3 V** and **12.5 Mbps at 2.5 V** with 4X sampling rate
  - Fractional Baud Rate Generator
  - Transmit and Receive FIFOs of 32 bytes
  - Selectable TX and RX FIFO Trigger Levels
  - Automatic Hardware (RTS/CTS) Flow Control
  - Automatic Software (Xon/Xoff) Flow Control
  - Wireless Infrared (IrDA 1.0) Encoder/Decoder
  - Automatic sleep mode
  - Full modem interface
- Alternate Function Register
- Device Identification and Revision
- Crystal oscillator or external clock input
- Crystal oscillator (up to 32 MHz) or external clock (up to 64 MHz) input
- 44-PLCC and 32-QFN packages

FIGURE 1. XR16V2652 BLOCK DIAGRAM

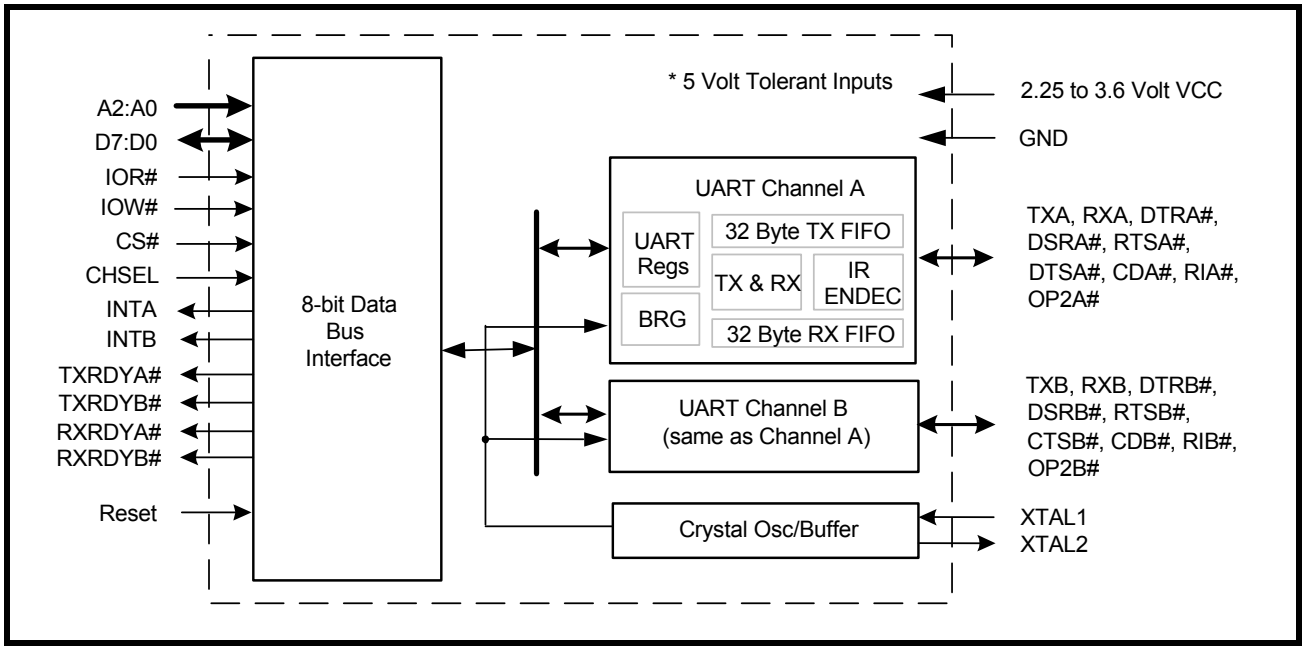
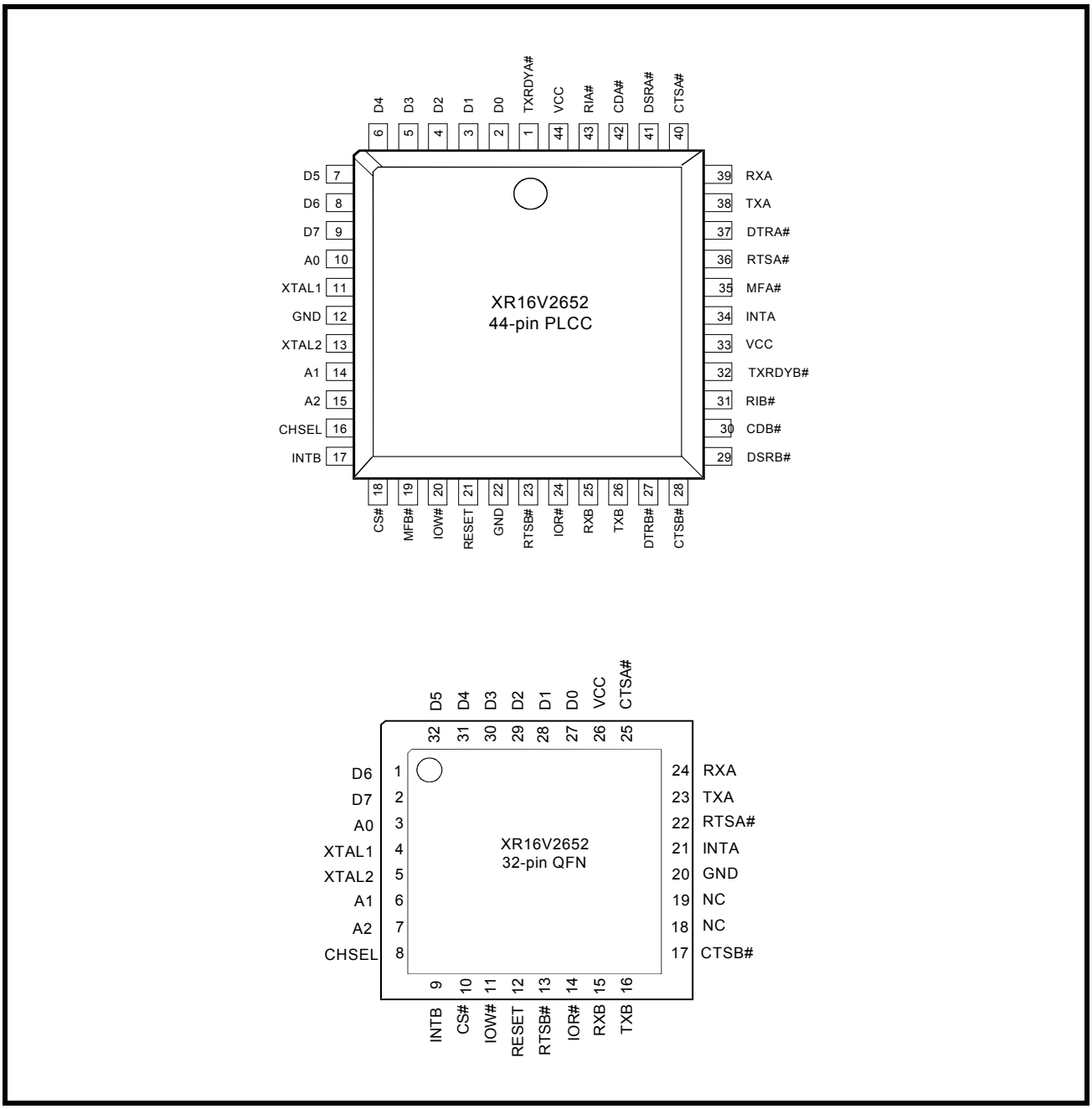


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16V2652IL32	32-QFN	-40°C to +85°C	Active
XR16V2652IJ	44-Lead PLCC	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	32-QFN PIN #	44-PLCC PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE				
A2 A1 A0	7 6 3	15 14 10	I	Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction.
D7 D6 D5 D4 D3 D2 D1 D0	2 1 32 31 30 29 28 27	9 8 7 6 5 4 3 2	I/O	Data bus lines [7:0] (bidirectional).
IOR#	14	24	I	Input/Output Read Strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed to by the address lines [A2:A0]. The data byte is placed on the data bus to allow the host processor to read it on the rising edge.
IOW#	11	20	I	Input/Output Write Strobe (active low). The falling edge instigates an internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed by the address lines.
CS#	10	18	I	UART chip select (active low). This function selects channel A or B in accordance with the logical state of the CHSEL pin. This allows data to be transferred between the user CPU and the V2652.
CHSEL	8	16	I	Channel Select - UART channel A or B is selected by the logical state of this pin when the CS# pin is a logic 0. A logic 0 on the CHSEL selects the UART channel B while a logic 1 selects UART channel A. Normally, CHSEL could just be an address line from the user CPU such as A4. Bit-0 of the Alternate Function Register (AFR) can temporarily override CHSEL function, allowing the user to write to both channel register simultaneously with one write cycle when CS# is low. It is especially useful during the initialization routine.
INTA	21	34	O	UART channel A Interrupt output (active high). A HIGH indicates channel A is requesting for service. For more details, see **Figures 17- 22**.
INTB	9	17	O	UART channel B Interrupt output (active high). A HIGH indicates channel B is requesting for service. For more details, see **Figures 17- 22**.
TXRDYA#	-	1	O	UART channel A Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel A. See Table 2.
TXRDYB#	-	32	O	UART channel B Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel B. See Table 2.
MODEM OR SERIAL I/O INTERFACE				
TXA	23	38	O	UART channel A Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is LOW. If it is not used, leave it unconnected.

Pin Description

NAME	32-QFN PIN #	44-PLCC PIN #	TYPE	DESCRIPTION
RXA	24	39	I	UART channel A Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles LOW but can be inverted by software control prior going in to the decoder, see MCR[6]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSA#	22	36	O	UART channel A Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].
CTSA#	25	40	I	UART channel A Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used.
DTRA#	-	37	O	UART channel A Data-Terminal-Ready (active low) or general purpose output. If this pin is not used, leave it unconnected.
DSRA#	-	41	I	UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDA#	-	42	I	UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIA#	-	43	I	UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
MFA#	-	35	O	Multi-Function Output Channel A. This output pin can function as the OP2A#, BAUDOUTA#, or RXRDYA# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2A# - When OP2A# (active low) is selected, the MF# pin is LOW when MCR bit-3 is set to a logic 1 (see MCR bit-3). MCR bit-3 defaults to a logic 0 condition after a reset or power-up. 2) BAUDOUTA# - When BAUDOUTA# function is selected, the Baud rate clock output is available at this pin. 3) RXRDYA# - RXRDYA# (active low) is intended for monitoring block data transfers. See Table 2 for more details.
TXB	16	26	O	UART channel B Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be HIGH during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/ decoder interface is LOW. If it is not used, leave it unconnected.
RXB	15	25	I	UART channel B Receive Data or infrared receive data. Normal receive data input must idle HIGH. The infrared receiver pulses typically idles LOW but can be inverted by software control prior going in to the decoder, see MCR[6]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor.
RTSB#	13	23	O	UART channel B Request-to-Send (active low) or general purpose output. This port must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1] and IER[6].

Pin Description

NAME	32-QFN PIN #	44-PLCC PIN #	TYPE	DESCRIPTION
CTSB#	17	28	I	UART channel B Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used.
DTRB#	-	27	O	UART channel B Data-Terminal-Ready (active low) or general purpose output. If this pin is not used, leave it unconnected.
DSRB#	-	29	I	UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
CDB#	-	30	I	UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
RIB#	-	31	I	UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART.
MFB#	-	19	O	Multi-Function Output Channel B. This output pin can function as the OP2B#, BAUDOUTB#, or RXRDYB# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2B# - When OP2B# (active low) is selected, the MF# pin is LOW when MCR bit-3 is set HIGH (see MCR bit-3). MCR bit-3 defaults to a logic 0 condition after a reset or power-up. 2) BAUDOUTB# - When BAUDOUTB# function is selected, the Baud rate clock output is available at this pin. 3) RXRDYB# - RXRDYB# (active low) is intended for monitoring block data transfers. See Table 2 for more details.
ANCILLARY SIGNALS				
XTAL1	4	11	I	Crystal or external clock input.
XTAL2	5	13	O	Crystal or buffered clock output.
RESET	12	21	I	Reset (active high) - A longer than 40 ns HIGH pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held HIGH, the receiver input will be ignored and outputs are reset during reset period (see Table 15).
VCC	26	44, 33	Pwr	2.25 to 3.6V power supply. All input pins are 5V tolerant.
GND	20	22, 12	Pwr	Power supply common, ground.
GND	Center Pad	N/A	Pwr	The center pad on the backside of the 32-QFN package is metallic and should be connected to GND on the PCB. The thermal pad size on the PCB should be the approximate size of this center pad and should be solder mask defined. The solder mask opening should be at least 0.0025" inwards from the edge of the PCB thermal pad.
NC	18, 19	-	-	No Connect.

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16V2652 (V2652) integrates the functions of 2 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 32-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control, automatic Xon/Xoff and special character software flow control, selectable transmit and receive FIFO trigger levels, infrared encoder and decoder (IrDA ver 1.0), programmable fractional baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 16 Mbps with 4X sampling clock rate. The XR16V2652 is a 2.25 to 3.6V device with 5 volt tolerant inputs. The V2652 is fabricated with an advanced CMOS process.

Enhanced Features

The V2652 DUART provides a solution that supports 32 bytes of transmit and receive FIFO memory, instead of 16 bytes in the ST16C2550 or one byte in the ST16C2450. The V2652 is designed to work with low supply voltage and high performance data communication systems, that require fast data processing time. Increased performance is realized in the V2652 by the larger transmit and receive FIFOs, FIFO trigger level control and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2 Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 32 byte FIFO in the V2652, the data buffer will not require unloading/loading for 3.06 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the selectable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

Data Rate

The V2652 is capable of operation up to 16 Mbps at 3.3V and 12.5 Mbps at 2.5V with 4X sampling clock rate. The device can operate with an external 32 MHz crystal at 2.5V on pins XTAL1 and XTAL2, or external clock source of up to 64 MHz on XTAL1 pin. With a typical crystal of 14.7456 MHz and through a software option, the user can set the prescaler bit for data rates of up to 3.68 Mbps.

The rich feature set of the V2652 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, programmable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features.

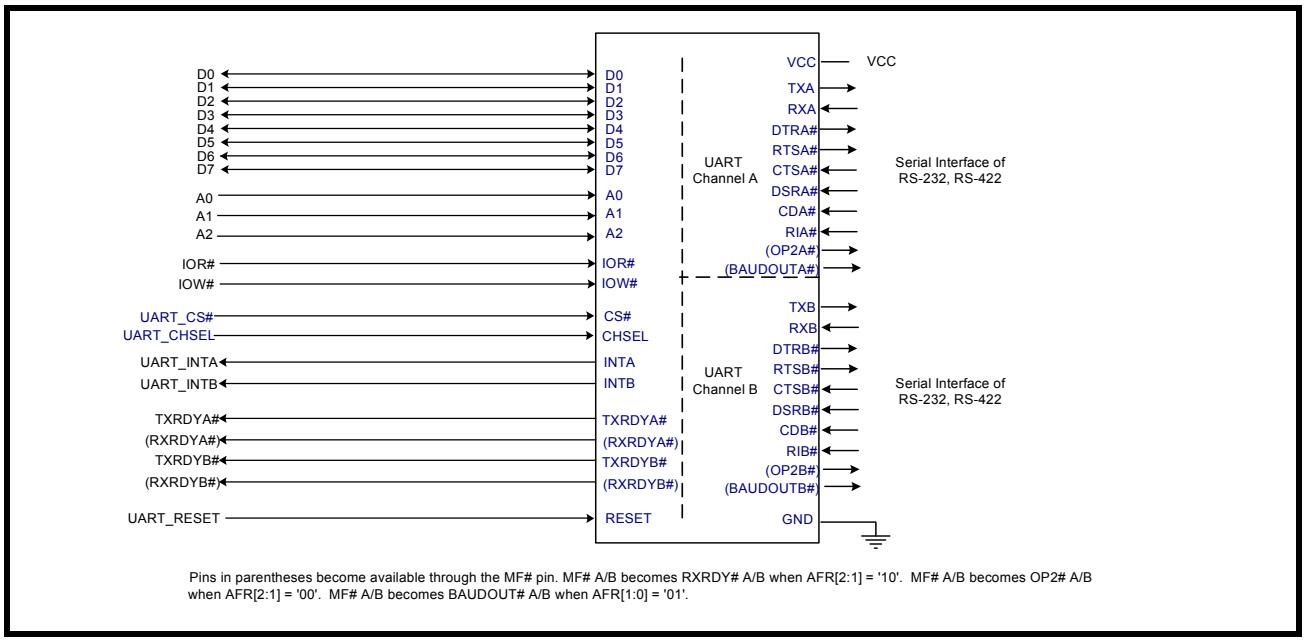
Following a power on reset or an external reset, the V2652 is software compatible with previous generation of UARTs, 16C450, 16C550 and 16C650A.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU Interface

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The V2652 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock (oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 3

FIGURE 3. XR16V2652 DATA BUS INTERCONNECTIONS



2.2 5-Volt Tolerant Inputs

The V2652 can accept up to 5V inputs even when operating at 3.3V or 2.5V. But note that if the V2652 is operating at 2.5V, its V_{OH} may not be high enough to meet the requirements of the V_{IH} of a CPU or a serial transceiver that is operating at 5V.

2.3 Device Reset

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 15). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 Device Identification and Revision

The XR16V2652 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00 (DLD = 0xXX). Now reading the content of the DLM will provide 0x06 for the XR16V2652 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 Channel A and B Selection

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on chip select pin (CS#) allows the user to select the UART and then using the channel select (CHSEL) pin, the user can select channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT

CS#	CHSEL	FUNCTION
1	X	UART de-selected
0	1	Channel A selected
0	0	Channel B selected

2.6 Channel A and B Internal Registers

Each UART channel in the V2652 has a set of enhanced registers for controlling, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM/DLD), and a user accessible Scratchpad Register (SPR).

Beyond the general 16C2550 features and capabilities, the V2652 offers enhanced feature registers (EFR, Xon/Xoff 1, Xon/Xoff 2) that provide automatic RTS and CTS hardware flow control and Xon/Xoff software flow control. All the register functions are discussed in full detail later in **"Section 3.0, UART INTERNAL REGISTERS" on page 21**.

2.7 DMA Mode

The device does not support direct memory access. The DMA Mode (a legacy term) in this document does not mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the V2652 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the selected trigger level. In this mode, the V2652 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see **Figures 17** through **22**.

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

PINS	FCR BIT-0=0 (FIFO DISABLED)	FCR BIT-0=1 (FIFO ENABLED)	
		FCR Bit-3 = 0 (DMA Mode Disabled)	FCR Bit-3 = 1 (DMA Mode Enabled)
RXRDY# A/B	LOW = 1 byte. HIGH = no data.	LOW = at least 1 byte in FIFO. HIGH = FIFO empty.	HIGH to LOW transition when FIFO reaches the trigger level, or time-out occurs. LOW to HIGH transition when FIFO empties.
TXRDY# A/B	LOW = THR empty. HIGH = byte in THR.	LOW = FIFO empty. HIGH = at least 1 byte in FIFO.	LOW = FIFO has at least 1 empty location. HIGH = FIFO is full.

2.8 INTA and INTB Outputs

The INTA and INTB interrupt output changes according to the operating mode and enhanced features setup. Table 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figures 17 through 22.

TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	LOW = a byte in THR HIGH = THR empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or FIFO empty
INTA/B Pin	LOW = a byte in THR HIGH = transmitter empty	LOW = FIFO above trigger level HIGH = FIFO below trigger level or transmitter empty

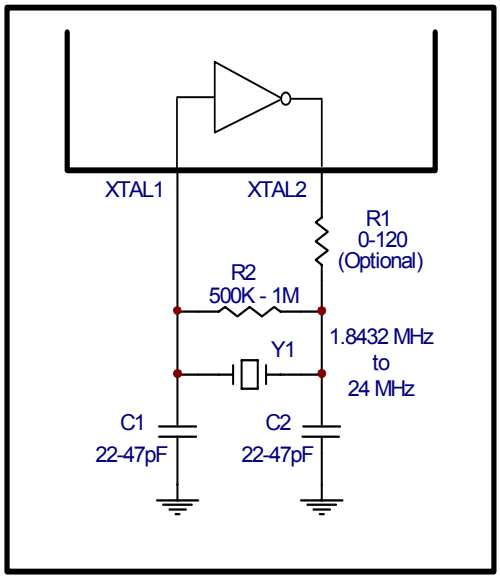
TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER

	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
INTA/B Pin	LOW = no data HIGH = 1 byte	LOW = FIFO below trigger level HIGH = FIFO above trigger level

2.9 Crystal Oscillator or External Clock Input

The V2652 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see "Section 2.10, Programmable Baud Rate Generator with Fractional Divisor" on page 10.

FIGURE 4. TYPICAL CRYSTAL CONNECTIONS



The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100 ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 4**). The programmable Baud Rate Generator is capable of operating with a crystal oscillator frequency of up to 32 MHz at 2.5V. However, with an external clock input on XTAL1 pin, it can extend its operation up to 64 MHz (16 Mbps serial data rate) at 3.3V with an 4X sampling rate. For further reading on the oscillator circuit please see the Application Note DAN108 on the EXAR web site at **http://www.exar.com.**

2.10 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (216 - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 5** shows the standard data rates available with a 24 MHz crystal or external clock at 16X clock rate. If the prescaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 5**. At 8X sampling rate, these data rates would double. And at 4X sampling rate, they would quadruple. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal) =(XTAL1 clock frequency / prescaler) / (serial data rate x 16), with 16X mode **DLD[5:4]='00'**
Required Divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), with 8X mode **DLD[5:4]='01'**
Required Divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 4), with 4X mode **DLD[5:4]='10'**

The closest divisor that is obtainable in the V2652 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 5. BAUD RATE GENERATOR

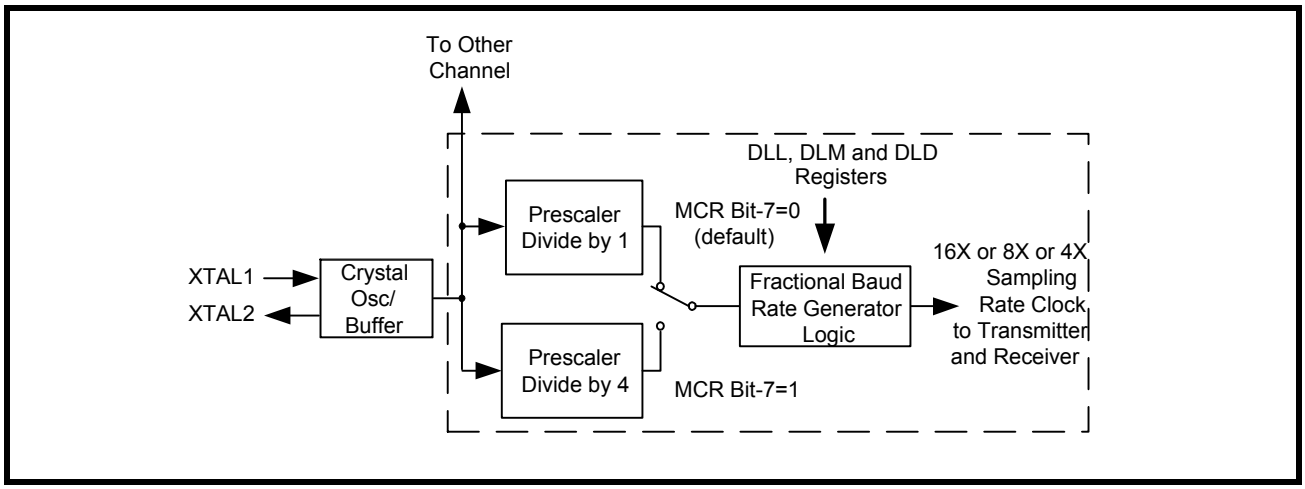


TABLE 5: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN V2652	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX)	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

2.11 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 32 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X/8X/4X internal clock. A bit time is 16/8/4 clock periods (see DLD). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

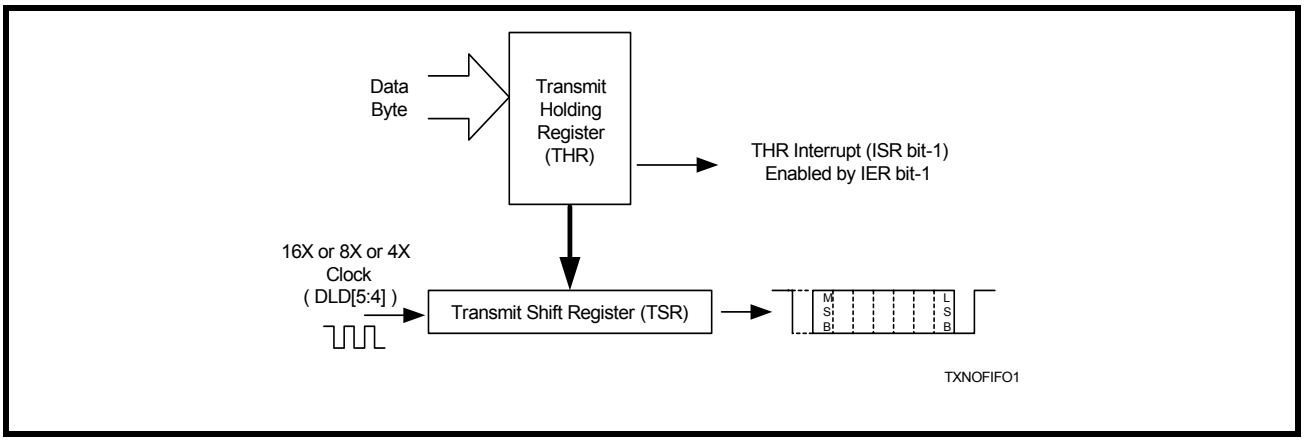
2.11.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 32 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.11.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

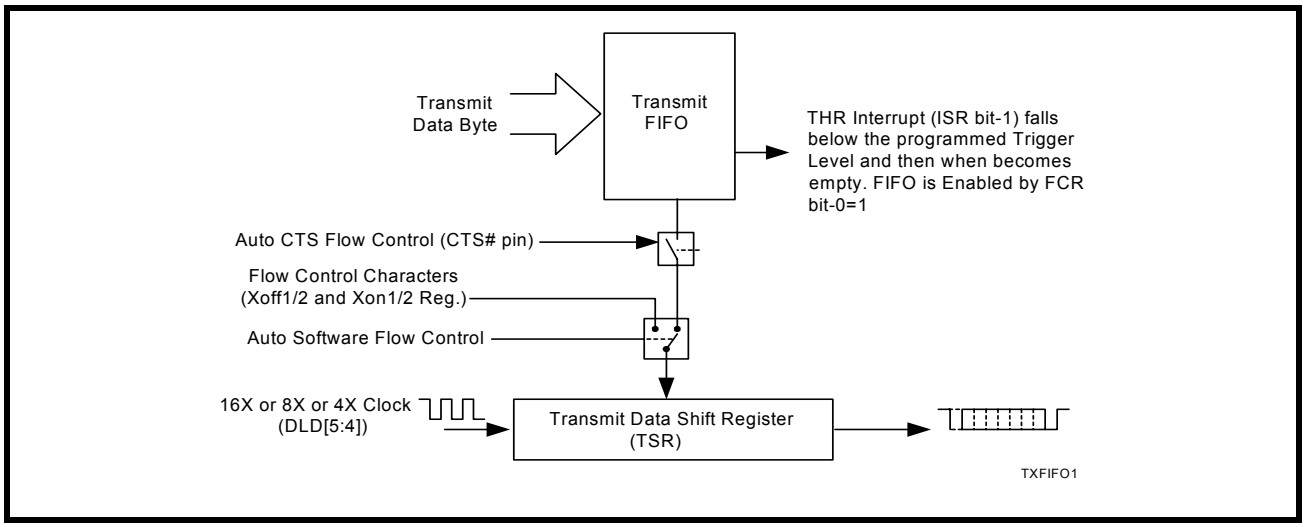
FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE



2.11.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 32 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.12 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 32 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X/8X/4X clock (DLD[5:4]) for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X/8X/4X clock rate. After 8 clocks (or 4 if 8X or 2 if 4X) the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.12.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 32 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE

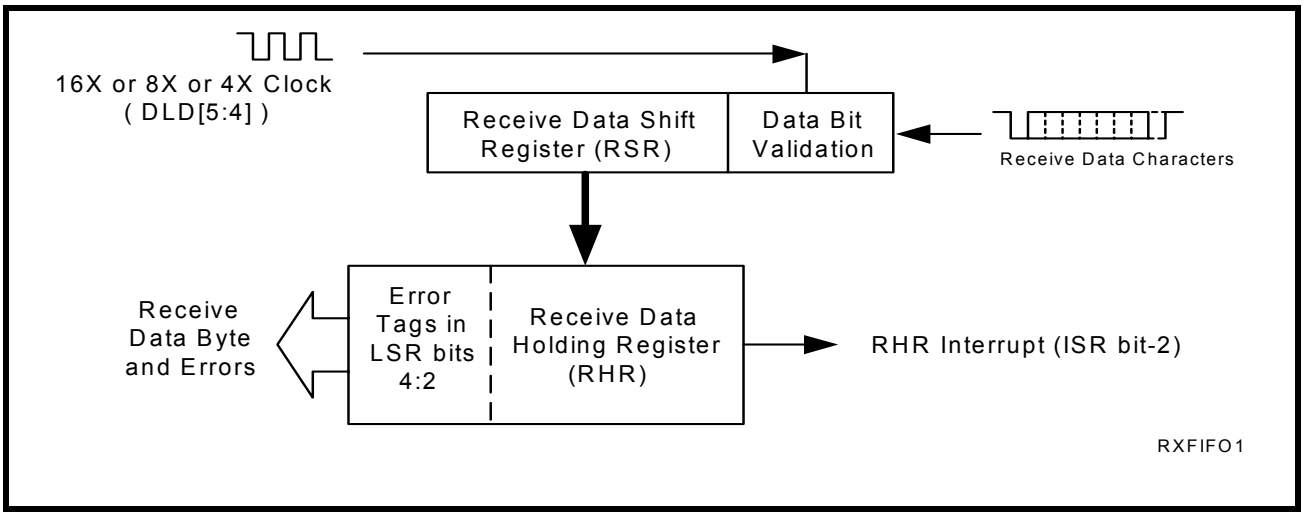
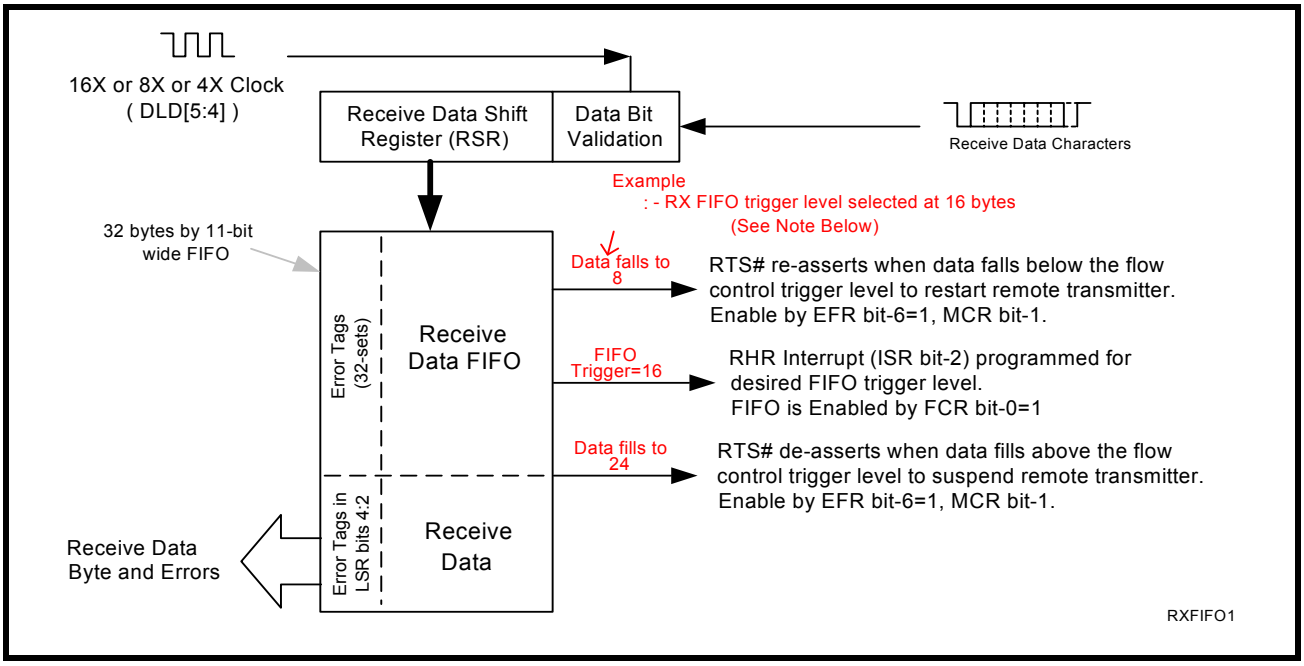


FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



2.13 Auto RTS (Hardware) Flow Control

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 10):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).

If using the Auto RTS interrupt:

- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.14 Auto RTS Hysteresis

The V2652 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the selected RX trigger level. The RTS# pin will not be forced HIGH (RTS off) until the receive FIFO reaches one trigger level above the selected trigger level in the trigger table (Table 11). The RTS# pin will return LOW after the RX FIFO is unloaded to one level below the selected trigger level. Under the above described conditions, the V2652 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted LOW (RTS On).

TABLE 6: AUTO RTS (HARDWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	RTS# DEASSERTED (HIGH) (CHARACTERS IN RX FIFO)	RTS# ASSERTED (LOW) (CHARACTERS IN RX FIFO)
8	8	16	0
16	16	24	8
24	24	28	16
28	28	28	24

2.15 Auto CTS Flow Control

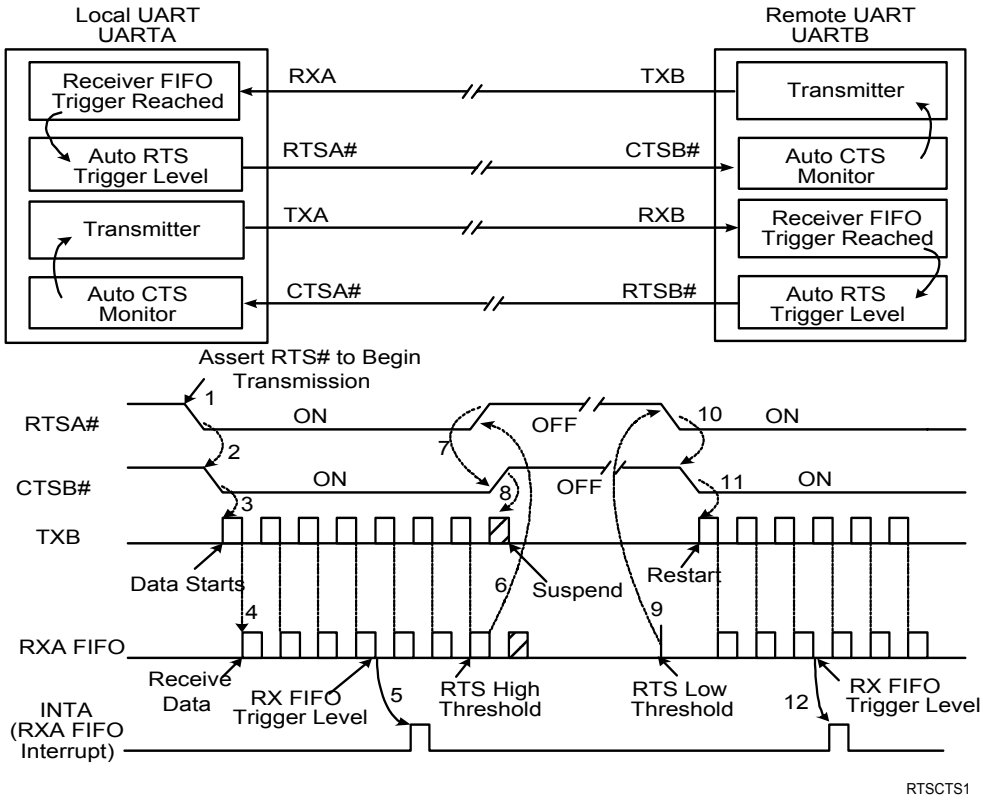
Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 10):

- Enable auto CTS flow control using EFR bit-7.

If using the Auto CTS interrupt:

- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (HIGH): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (LOW), indicating more data may be sent.

FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.16 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (See Table 14), the V2652 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the V2652 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the V2652 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the V2652 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to 0x00. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 14) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the V2652 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the V2652 automatically sends an Xoff message via the serial TX output to the remote modem. The V2652 sends the Xoff-1,2 characters two-character times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the selected trigger level. To clear this condition, the V2652 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the selected trigger level. Table 7 below explains this.

TABLE 7: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

* *After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2* characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

2.17 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The V2652 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

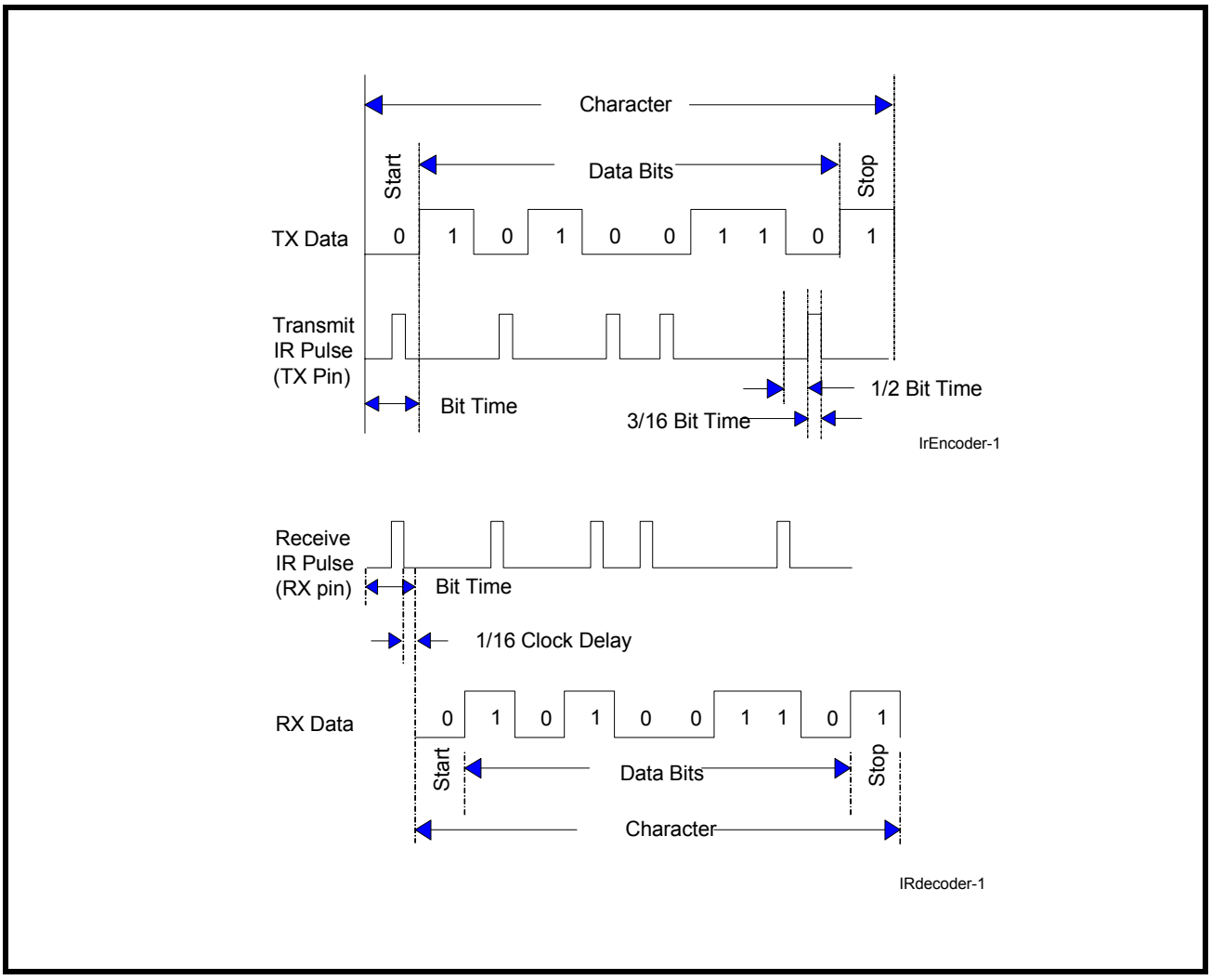
2.18 Infrared Mode

The V2652 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 11** below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see **Figure 11**.

Typically, the wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the V2652 has a provision to invert the input polarity to accommodate this. In this case user can enable MCR bit-2 to invert the input signal.

FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.19 Sleep Mode with Auto Wake-Up

The V2652 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the V2652 to enter sleep mode:

- no interrupts pending for both channels of the V2652 (ISR bit-0 = 1)
- sleep mode of both channels are enabled (IER bit-4 = 1)
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pins are idling HIGH

The V2652 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The V2652 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the V2652 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the V2652 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from channel A or B. The V2652 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

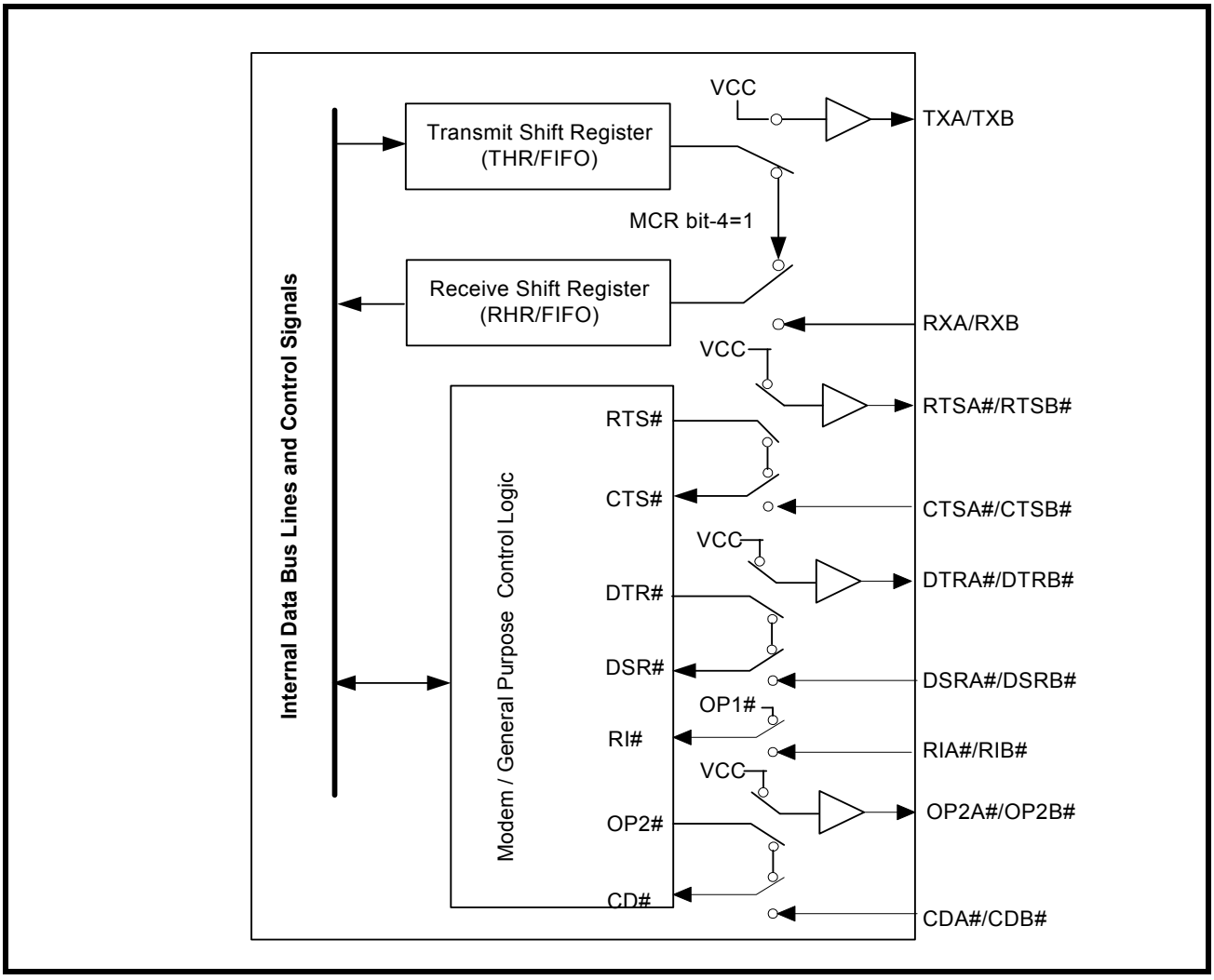
If the address lines, data bus lines, IOW#, IOR#, CS#, CHSEL, and modem input lines remain steady when the V2652 is in sleep mode, the maximum current will be in the microamp range as specified in the DC Electrical Characteristics on page 37. If the input lines are floating or are toggling while the V2652 is in sleep mode, the current can be up to 100 times more. If any of those signals are toggling or floating, then an external buffer would be required to keep the address, data and control lines steady to achieve the low current. As an alternative, please refer to the XR16V2651 which is pin-to-pin and software compatible with the V2652 but with some additional pins and the PowerSave feature that eliminates any unnecessary external buffer.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate. Also, it is important to keep RX A/B inputs idling HIGH or “marking” condition during sleep mode to avoid receiving a “break” condition upon the restart. This may occur when the external interface transceivers (RS-232, RS-422 or another type) are also put to sleep mode and cannot maintain the “marking” condition. To avoid this, the designer can use a 47k-100k ohm pull-up resistor on the RXA and RXB pins.

2.20 Internal Loopback

The V2652 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 12 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held while the CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input pin must be held HIGH during loopback test else upon exiting the loopback test the UART may detect and report a false “break” signal. Also, Auto RTS/CTS flow control is not supported during internal loopback.

FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



3.0 UART INTERNAL REGISTERS

Each of the UART channel in the V2652 has its own set of configuration registers selected by address lines A0, A1 and A2 with CS# or CHSEL selecting the channel. The complete register set is shown on Table 8 and Table 9.

TABLE 8: UART CHANNEL A AND B UART INTERNAL REGISTERS

ADDRESSES A2 A1 A0	REGISTER	READ/WRITE	COMMENTS
16C550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Register THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DLM - Divisor MSB	Read/Write	
0 1 0	AFR - Alternate Function Register	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 0
0 1 0	DLD - Divisor Fractional	Read/Write	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF
0 0 1	DVID - Device Identification Code	Read-only	
0 0 1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Register FCR - FIFO Control Register	Read-only Write-only	
0 1 1	LCR - Line Control Register	Read/Write	
1 0 0	MCR - Modem Control Register	Read/Write	LCR ≠ 0xBF
1 0 1	LSR - Line Status Register	Read-only	
1 1 0	MSR - Modem Status Register	Read-only	
1 1 1	SPR - Scratch Pad Register	Read/Write	
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Register	Read/Write	LCR = 0xBF
1 0 0	Xon-1 - Xon Character 1	Read/Write	
1 0 1	Xon-2 - Xon Character 2	Read/Write	
1 1 0	Xoff-1 - Xoff Character 1	Read/Write	
1 1 1	Xoff-2 - Xoff Character 2	Read/Write	

TABLE 9: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	0/ Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	
0 1 0	ISR	RD	FIFOs Enabled	FIFOs Enabled	0/ INT Source Bit-5	0/ INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 1 0	FCR	WR	RXFIFO Trigger	RXFIFO Trigger	0/ TXFIFO Trigger	0/ TXFIFO Trigger	DMA Mode Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Mode ENable	0/ XonAny	Internal Lopback Enable	OP2# Output Control	OP1# IR Invert	RTS# Output Control	DTR# Output Control	LCR ≠ 0xBF
1 0 1	LSR	RD	RX FIFO Global Error	THR & TSR Empty	THR Empty	RX Break	RX Framing Error	RX Parity Error	RX Over-run Error	RX Data Ready	
1 1 0	MSR	RD	CD# Input	RI# Input	DSR# Input	CTS# Input	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR ≠ 0xBF
Baud Rate Generator Divisor											
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
0 1 0	AFR	RD/WR	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	RXRDY# Select	Baudout# Select	Concur-rent Write	LCR[7]=1 LCR ≠ 0xBF EFR[4] = 0
0 1 0	DLD	RD/WR	0	0	4X Mode	8X Mode	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR ≠ 0xBF EFR[4] = 1

TABLE 9: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1 LCR≠0xBF DLL=0x00 DLM=0x00
0 0 1	DVID	RD	0	0	0	0	0	1	1	0	
Enhanced Registers											
0 1 0	EFR	RD/WR	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5], DLD	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
1 0 0	XON1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1	XON2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0	XOFF1	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1	XOFF2	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read- Only

SEE"RECEIVER" ON PAGE 13.

4.2 Transmit Holding Register (THR) - Write-Only

SEE"TRANSMITTER" ON PAGE 12.

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16V2652 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bit-1 generates an interrupt immediately when the character has been received. LSR bits 2-4 generate an interrupt when the character with errors is read out of the FIFO (default).

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).

- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

4.4 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, **Table 10**, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty.
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.
- CTS# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS flow control.
- RTS# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS flow control.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff interrupt is cleared by a read to ISR or when Xon character(s) is received.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 10: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
3	0	0	0	1	0	0	RXRDY (Received Data Ready)
4	0	0	0	0	1	0	TXRDY (Transmit Ready)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#, RTS# change of state
-	0	0	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source Table 10).

ISR[4]: Xoff/Xon or Special Character Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). If this is an Xoff/Xon interrupt, it can be cleared by a read to the ISR. If it is a special character interrupt, it can be cleared by reading ISR or it will automatically clear after the next character is received.

ISR[5]: RTS#/CTS# Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-5 indicates that the CTS# or RTS# has been de-asserted.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.5 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select (requires EFR bit-4=1)

(logic 0 = default, TX trigger level = 1)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 11 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 11 shows the complete selections.

TABLE 11: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
		0	0		16	16C650A
		0	1		8	
		1	0		24	
		1	1		30	
0	0			8		
0	1			16		
1	0			24		
1	1			28		

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See **Table 12** for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR bit-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced HIGH for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced LOW for the transmit and receive data.

TABLE 12: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, HIGH
1	1	1	Force parity to space, LOW

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space", LOW state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a “space”, LOW, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL, DLM and DLD) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.7 Modem Control Register (MCR) or General Purpose Outputs Control - Read/Write

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# HIGH (default).
- Logic 1 = Force RTS# LOW.

MCR[2]: IrDA RX Inversion or OP1# (legacy term)

When Infrared mode is enabled (MCR[6]=1 and EFR[4]=1), this bit selects the idle state of the encoded IrDA data. In internal loopback mode, this bit functions like the OP1# in the 16C550.

- Logic 0 = Select RX input as active-low encoded IrDA data (Idle state will be low) (default).
- Logic 1 = Select RX input as active-high encoded IrDA data (Idle state will be high).

In the Internal Loopback Mode, this bit controls the state of the modem input RI# bit in the MSR register as shown in Figure 12.

MCR[3]: OP2# Output

If OP2# is selected as the MF# output, then this bit controls the state of this general purpose output.

- Logic 0 = OP2# output set HIGH(default).
- Logic 1 = OP2# output set LOW.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 12**.

MCR[5]: Xon-Any Enable (requires EFR bit-4=1)

- Logic 0 = Disable Xon-Any function (default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO, unless the RX character is an Xon or Xoff character and the V2652 is programmed to use the Xon/Xoff flow control.

MCR[6]: Infrared Encoder/Decoder Enable (requires EFR bit-4=1)

- Logic 0 = Enable the standard modem receive and transmit input/output interface (default).
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. While in this mode, the infrared TX output will be idling LOW. **SEE"INFRARED MODE" ON PAGE 18.**

MCR[7]: Clock Prescaler Select (requires EFR bit-4=1)

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Error Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Error Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was LOW for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used for general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a LOW to HIGH, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 bit is the complement of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

Normally this bit is the complement of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.10 Scratch Pad Register (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.11 Baud Rate Generator Registers (DLL, DLM and DLD) - Read/Write

These registers make-up the value of the baud rate divisor. The concatenation of the contents of DLM and DLL is a 16-bit value is then added to DLD[3:0]/16 to achieve the fractional baud rate divisor. DLD must be enabled via EFR bit-4 before it can be accessed. **SEE"PROGRAMMABLE BAUD RATE GENERATOR WITH FRACTIONAL DIVISOR" ON PAGE 10.**

DLD[5:4]: Sampling Rate Select

These bits select the data sampling rate. By default, the data sampling rate is 16X. The maximum data rate will double if the 8X mode is selected and will quadruple if the 4X mode is selected. See Table below.

TABLE 13: SAMPLING RATE SELECT

DLD[5]	DLD[4]	SAMPLING RATE
0	0	16X
0	1	8X
1	X	4X

DLD[7:6]: Reserved

4.12 Alternate Function Register (AFR) - Read/Write

This register is used to select specific modes of MF# operation and to allow both UART register sets to be written concurrently.

AFR[0]: Concurrent Write Mode

When this bit is set, the CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by the CPU when both channels are initialized to the same state. The external CPU can set or clear this bit by accessing either register set. When this bit is set, the channel select pin still selects the channel to be accessed during read operations. The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0, 1, or 2.

- Logic 0 = No concurrent write (default).
- Logic 1 = Register set A and B are written concurrently with a single external CPU I/O write operation.

AFR[2:1]: MF# Output Select

These bits select a signal function for output on the MF# A/B pins. These signal function are described as: OP2#, BAUDOUT#, or RXRDY#. Only one signal function can be selected at a time.

BIT-2	BIT-1	MF# FUNCTION
0	0	OP2# (default)
0	1	BAUDOUT#
1	0	RXRDY#
1	1	Reserved

AFR[7:3]: Reserved

All are initialized to logic 0.

4.13 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x06 for XR16V2652). Prior to reading this register, DLL and DLM should be set to 0x00 (DLD = 0xXX).

4.14 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00 (DLD = 0xXX).

4.15 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see **Table 14**). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

TABLE 14: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, and DLD are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit of the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]= '10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]= '01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt, if enabled via IER bit-5.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts HIGH at the next upper trigger level or hysteresis level. RTS# will return LOW when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (LOW) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts HIGH. Data transmission resumes when CTS# returns LOW.

4.15.1 Software Flow Control Registers (XOFF1, XOFF2, XON1, XON2) - Read/Write

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 7.

TABLE 15: UART RESET CONDITIONS FOR CHANNEL A AND B

REGISTERS	RESET STATE
DLM, DLL	DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted.
DLD	Bits 7-0 = 0x00
AFR	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted
SPR	Bits 7-0 = 0xFF
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX	HIGH
OP2#	HIGH
RTS#	HIGH
DTR#	HIGH
RXRDY#	HIGH
TXRDY#	LOW
INT	LOW

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	GND-0.3V to 7V
Operating Temperature	-40° to +85°C
Storage Temperature	-65° to +150°C
Package Dissipation	500 mW

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

Thermal Resistance (44-PLCC)	theta-ja = 50°C/W, theta-jc = 21°C/W
Thermal Resistance (32-QFN)	theta-ja = 33°C/W, theta-jc = 22°C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.25V TO 3.6V

SYMBOL	PARAMETER	LIMITS 2.5V MIN	LIMITS 2.5V MAX	LIMITS 3.3V MIN	LIMITS 3.3V MAX	UNITS	CONDITIONS
V_{ILCK}	Clock Input Low Level	-0.3	0.4	-0.3	0.6	V	
V_{IHCK}	Clock Input High Level	2.0	VCC	2.4	VCC	V	
V_{IL}	Input Low Voltage	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.8	5.5	2.0	5.5	V	
V_{OL}	Output Low Voltage		0.4		0.4	V V	I_{OL} = 6 mA I_{OL} = 4 mA
V_{OH}	Output High Voltage	1.8		2.0		V V	I_{OH} = -4 mA I_{OH} = -2 mA
I_{IL}	Input Low Leakage Current		±10		±10	uA	
I_{IH}	Input High Leakage Current		±10		±10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		1.5		2.5	mA	Ext Clk = 2 MHz
I_{SLEEP}	Sleep Current		15		30	uA	See Test 1

Test 1: The following inputs must remain steady at VCC or GND state to minimize Sleep current: A0-A2, D0-D7, IOR#, IOW#, CSA#, CSB# and all modem inputs. Also, RXA and RXB inputs must idle HIGH while asleep. Floating inputs will result in sleep currents in the mA range. For PowerSave feature that isolates address, data and control signals, please see the XR16V2651 datasheet.

AC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC=2.25 - 3.63V, 70 PF LOAD WHERE APPLICABLE

SYMBOL	PARAMETER	LIMITS 2.5V ± 10%		LIMITS 3.3V ± 10%		UNIT
		MIN	MAX	MIN	MAX	
XTAL1	UART Crystal Oscillator		32		24	MHz
ECLK	External Clock		50		64	MHz
T_{ECLK}	External Clock Time Period	10		7		ns
T_{AS}	Address Setup Time	0		0		ns
T_{AH}	Address Hold Time	0		0		ns
T_{CS}	Chip Select Width	40		35		ns
T_{RD}	IOR# Strobe Width	40		35		ns
T_{DY}	Read Cycle Delay	40		35		ns
T_{RDV}	Data Access Time		35		30	ns
T_{DD}	Data Disable Time		25		25	ns
T_{WR}	IOW# Strobe Width	40		35		ns
T_{DY}	Write Cycle Delay	40		35		ns
T_{DS}	Data Setup Time	10		10		ns
T_{DH}	Data Hold Time	3		3		ns
T_{WDO}	Delay From IOW# To Output		50		50	ns
T_{MOD}	Delay To Set Interrupt From MODEM Input		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		45	ns
T_{SI}	Delay From Stop To Interrupt		45		45	ns
T_{INT}	Delay From Initial INT Reset To Transmit Start	8	24	8	24	Bclk
T_{WRI}	Delay From IOW# To Reset Interrupt		45		45	ns
T_{SSR}	Delay From Stop To Set RXRDY#		1		1	Bclk
T_{RR}	Delay From IOR# To Reset RXRDY#		45		45	ns
T_{WT}	Delay From IOW# To Set TXRDY#		45		45	ns
T_{SRT}	Delay From Center of Start To Reset TXRDY#		8		8	Bclk
T_{RST}	Reset Pulse Width	40		40		ns
Bclk	Baud Clock	16X or 8X or 4X of data rate				Hz

FIGURE 13. CLOCK TIMING

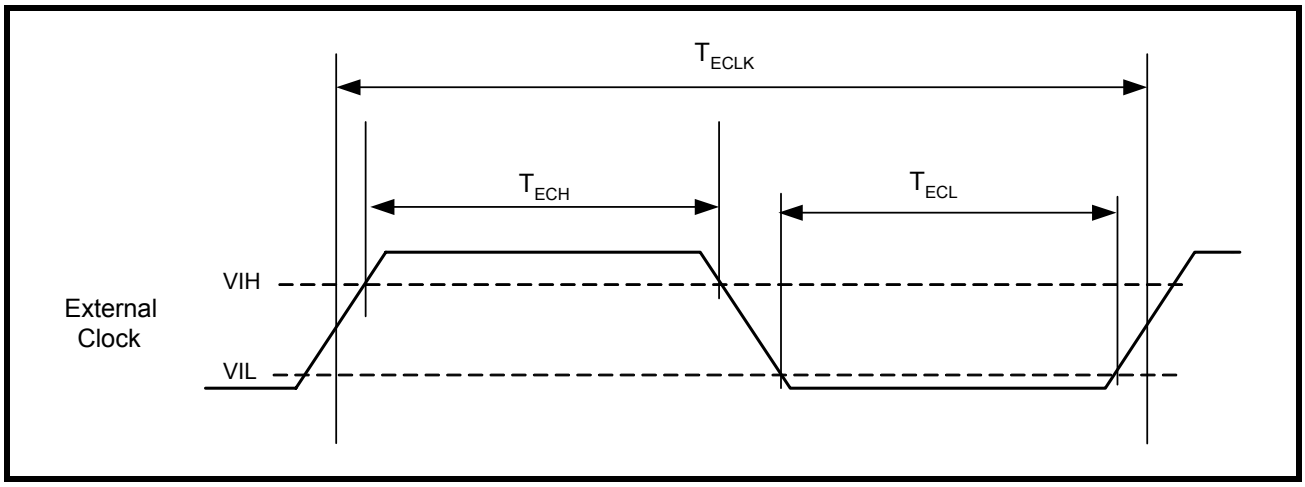


FIGURE 14. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B

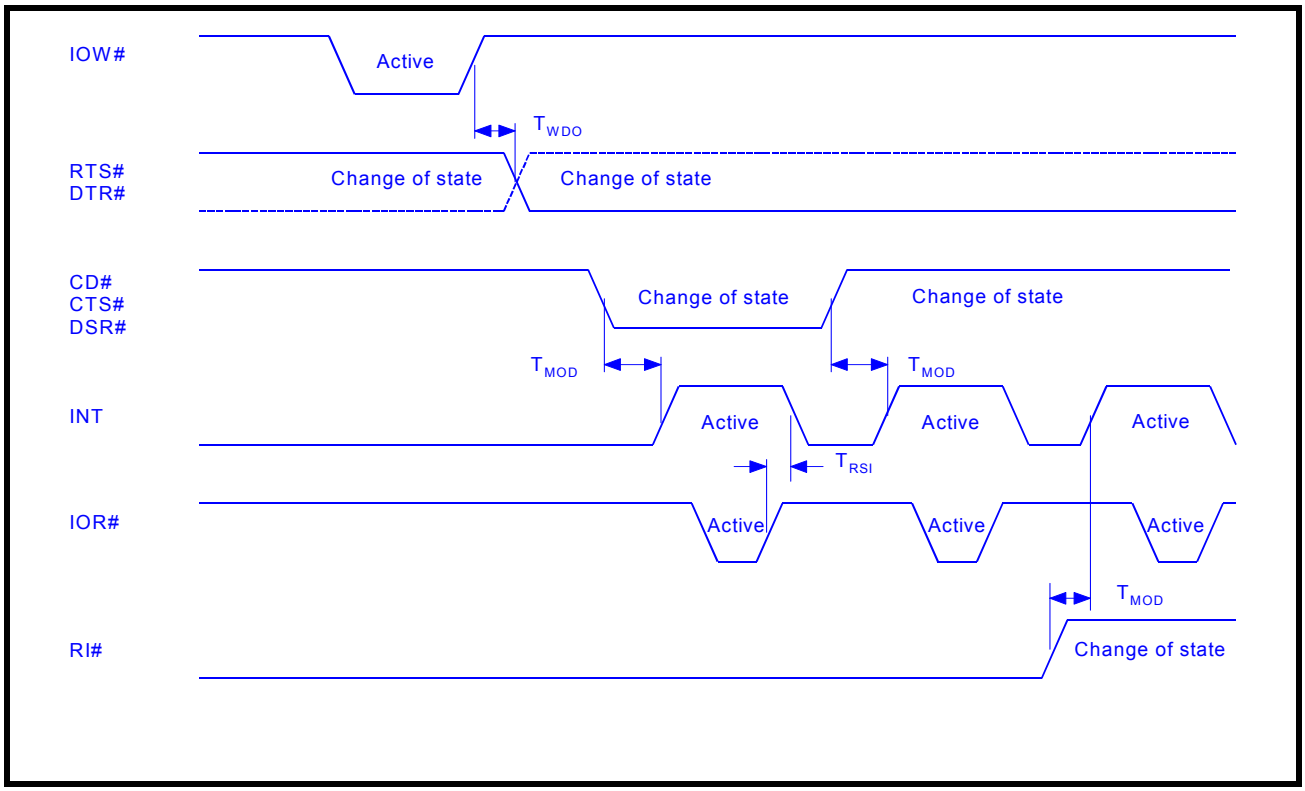


FIGURE 15. DATA BUS READ TIMING

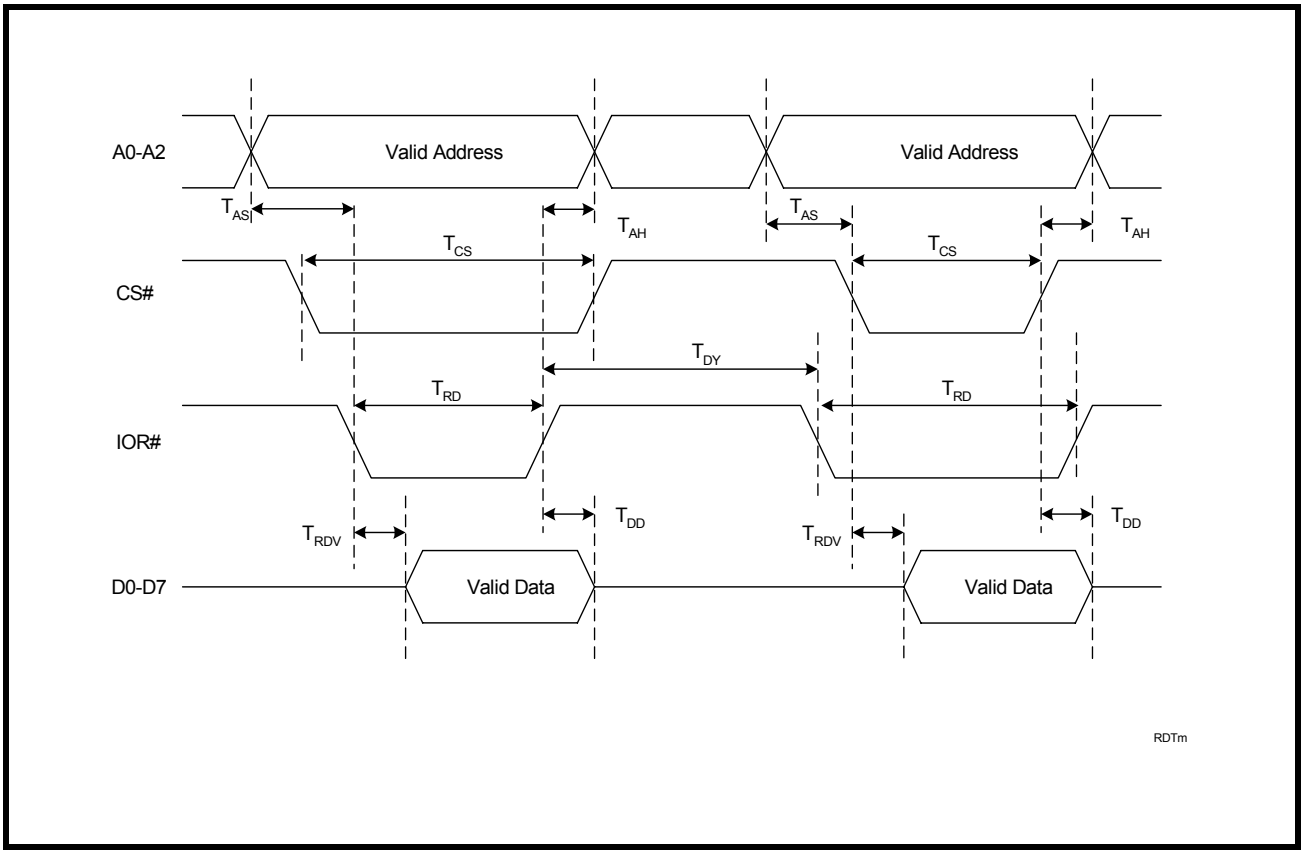


FIGURE 16. DATA BUS WRITE TIMING

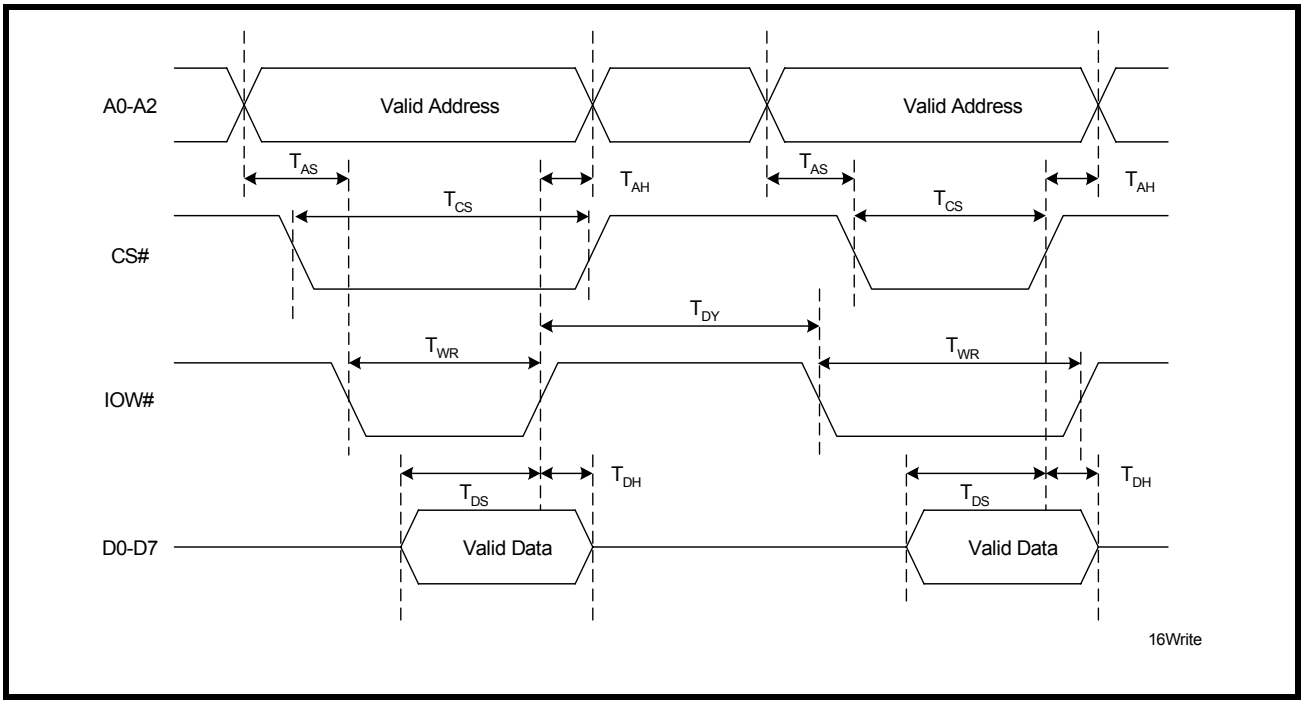


FIGURE 17. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

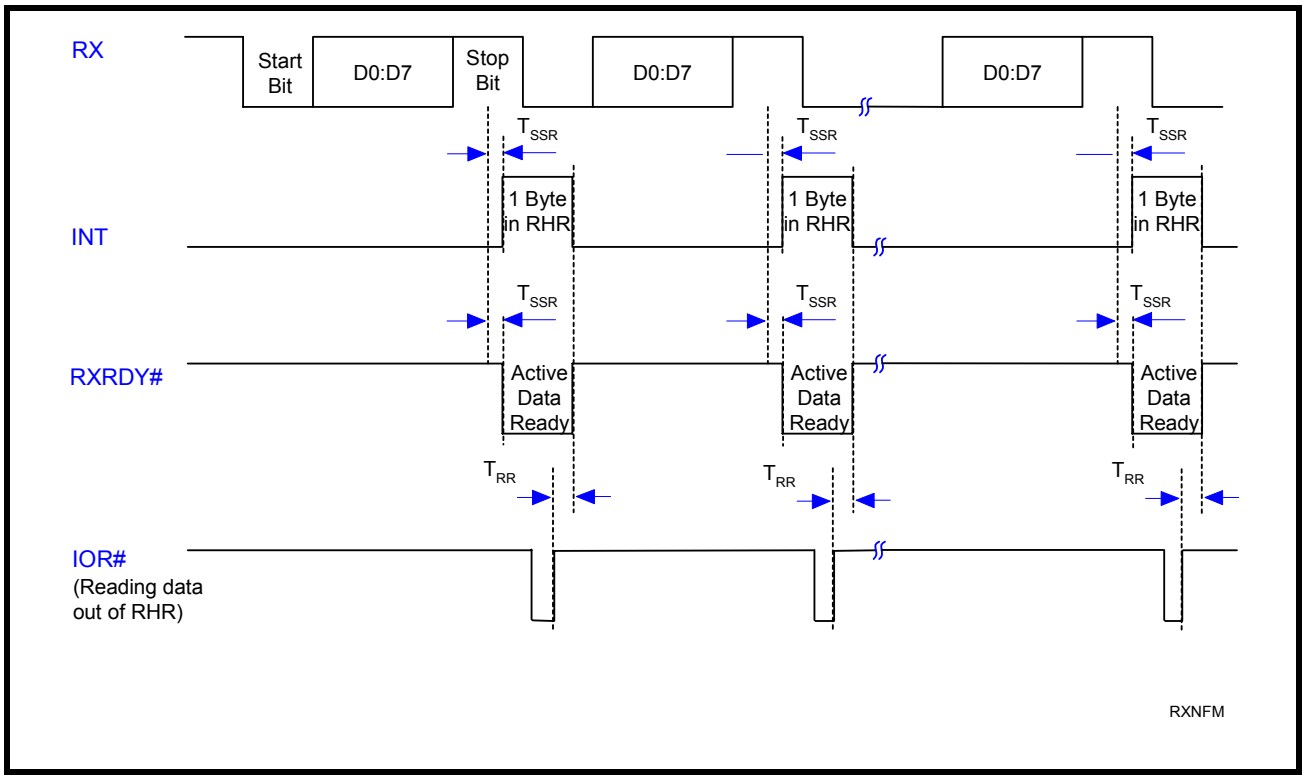


FIGURE 18. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

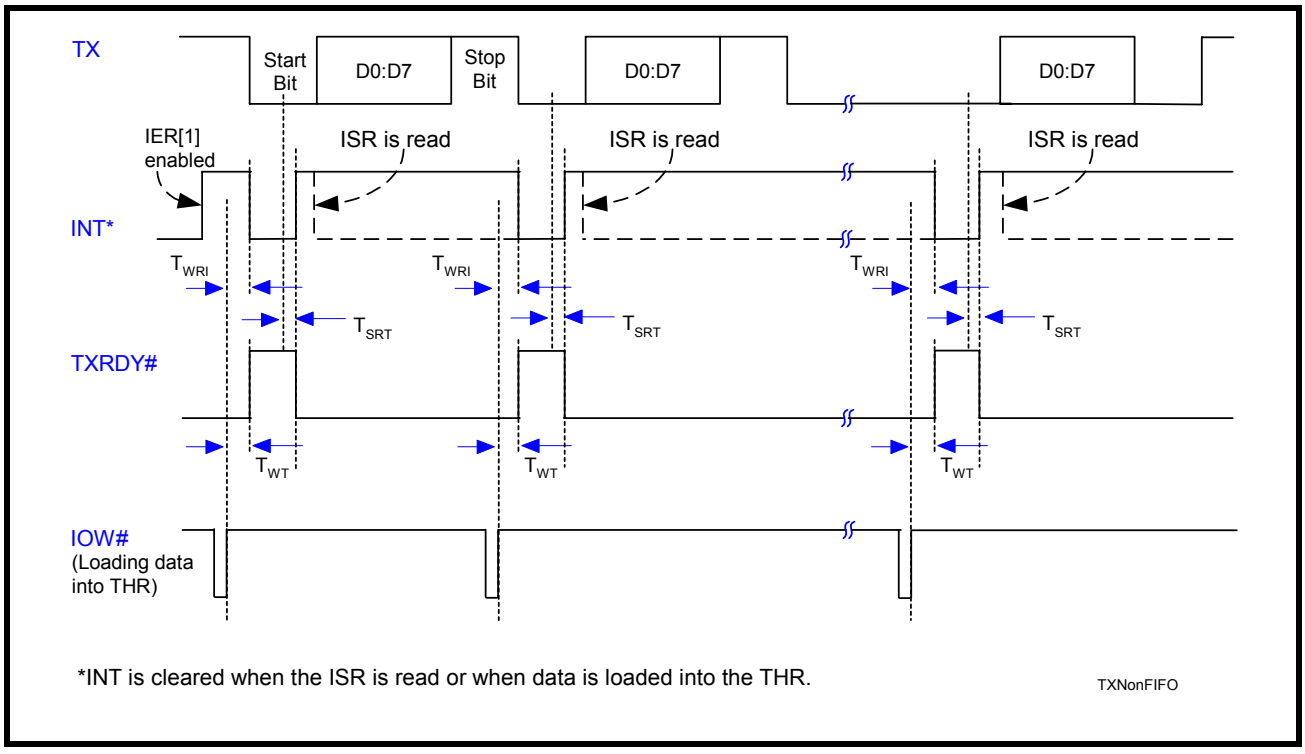


FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A & B

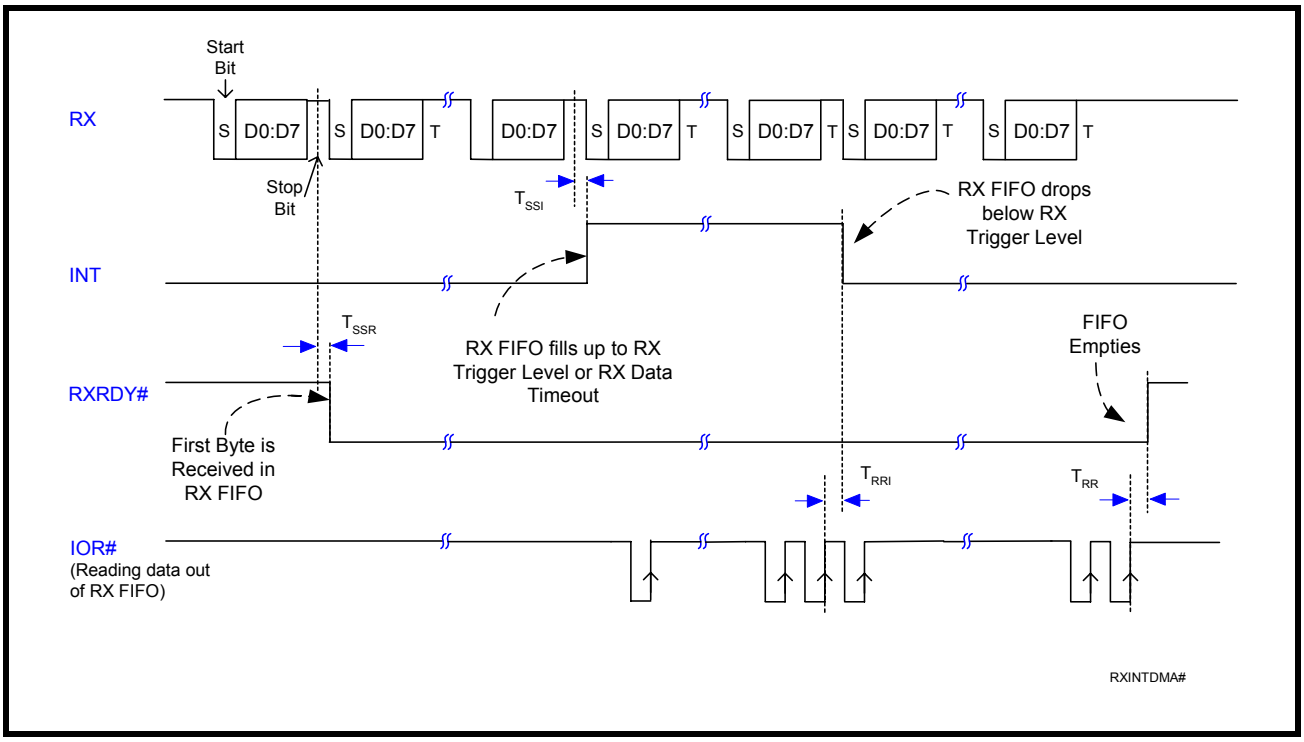


FIGURE 20. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A & B

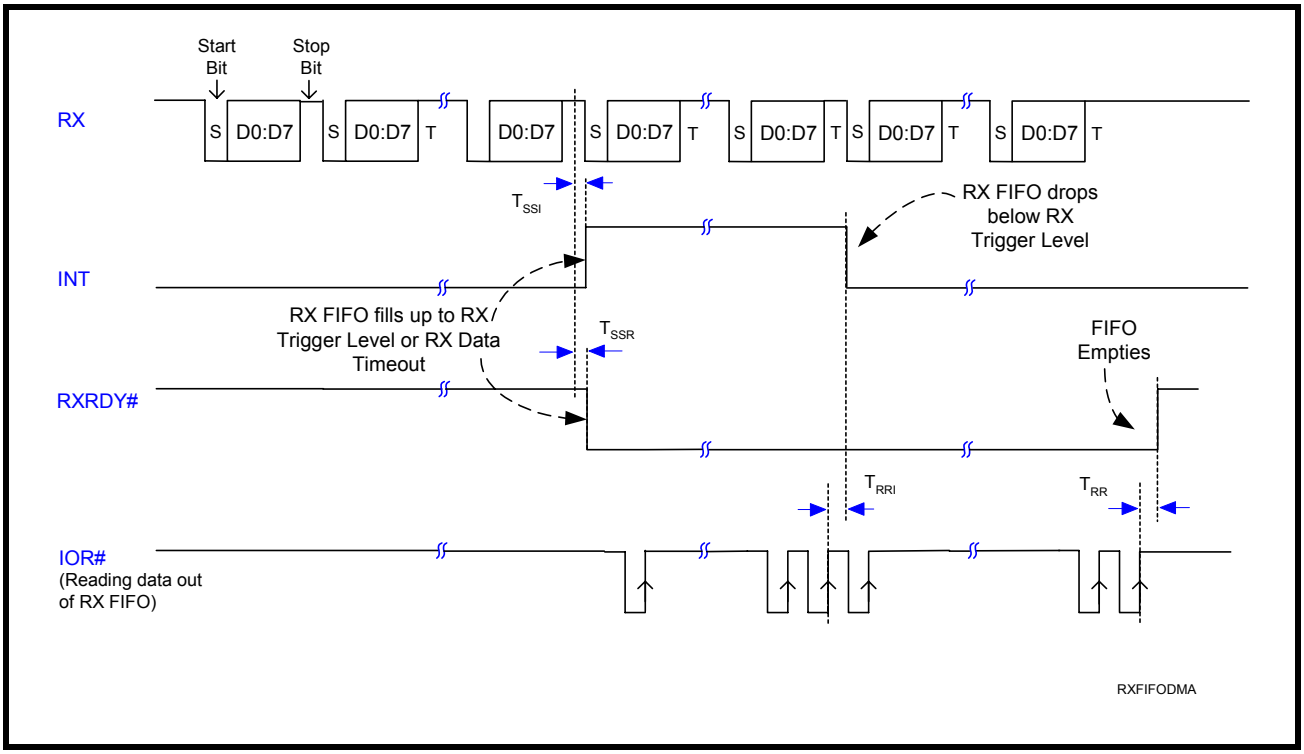


FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A & B

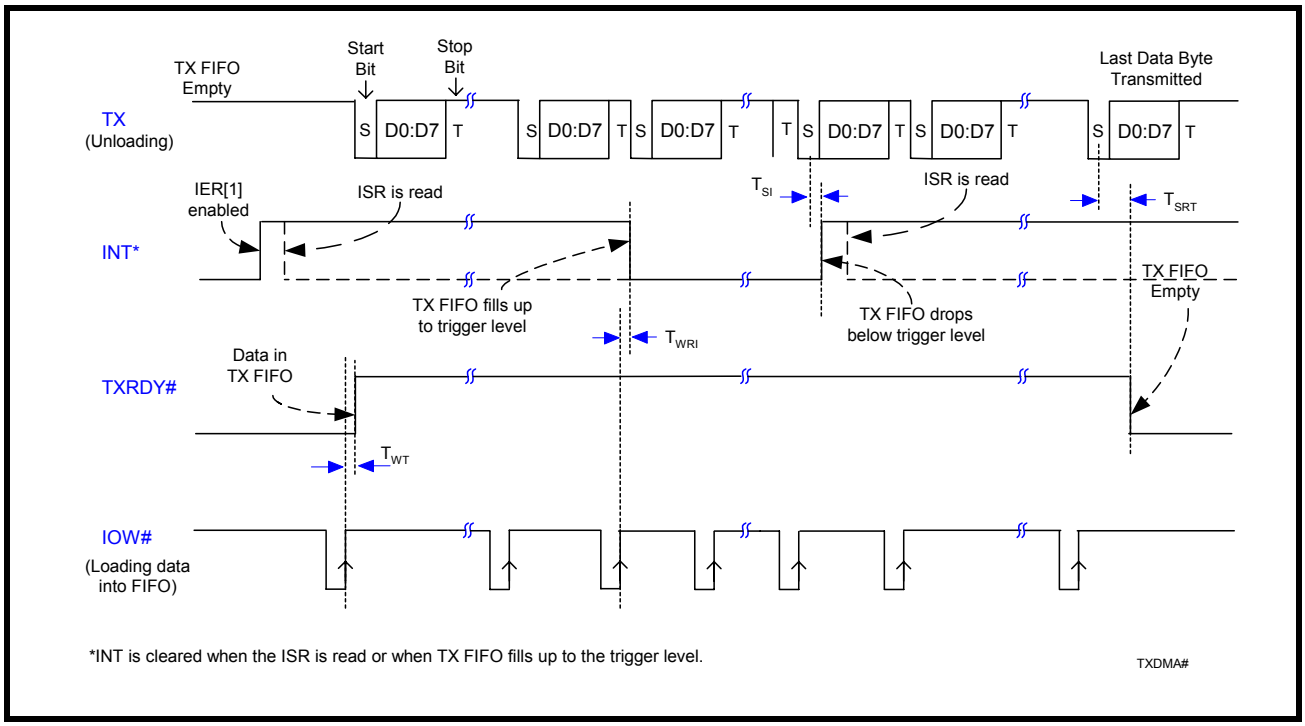
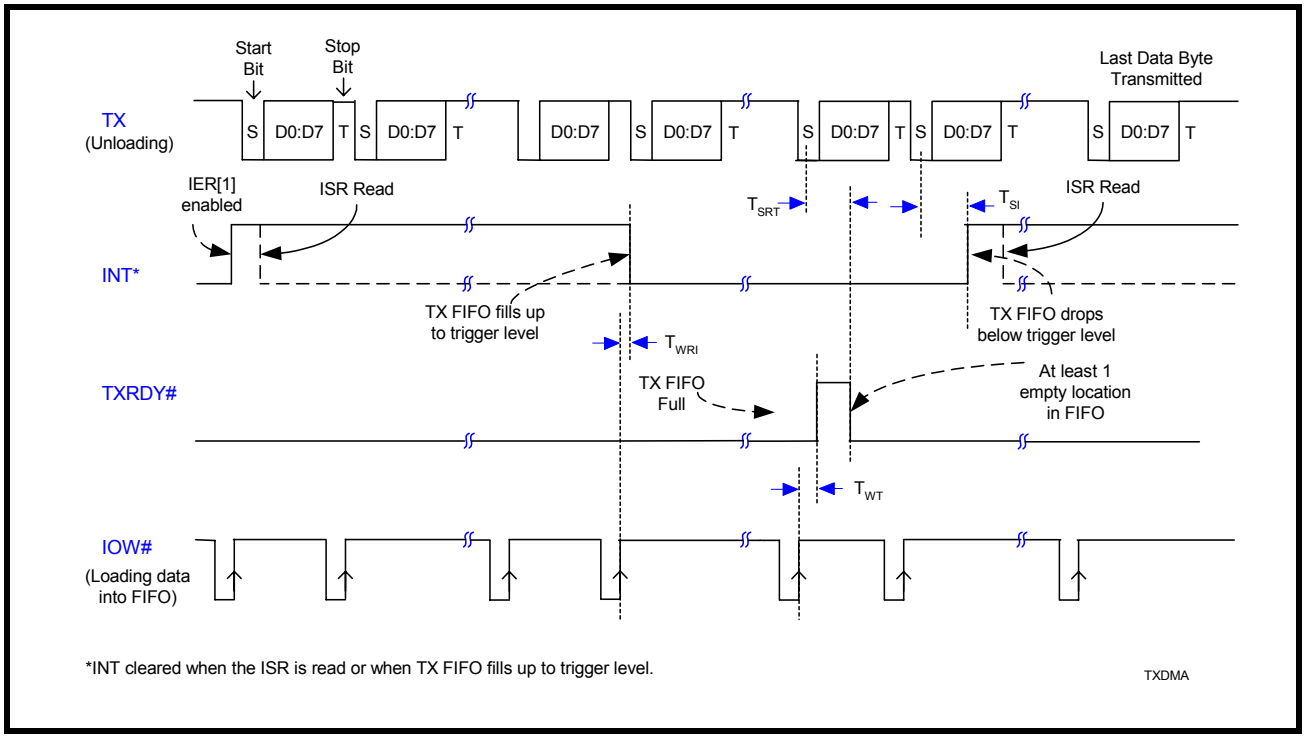
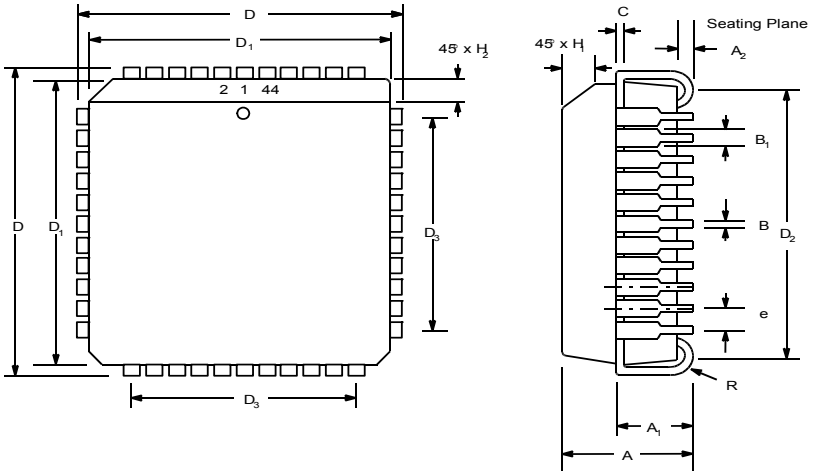


FIGURE 22. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A & B



PACKAGE DIMENSIONS (44 PIN PLCC)

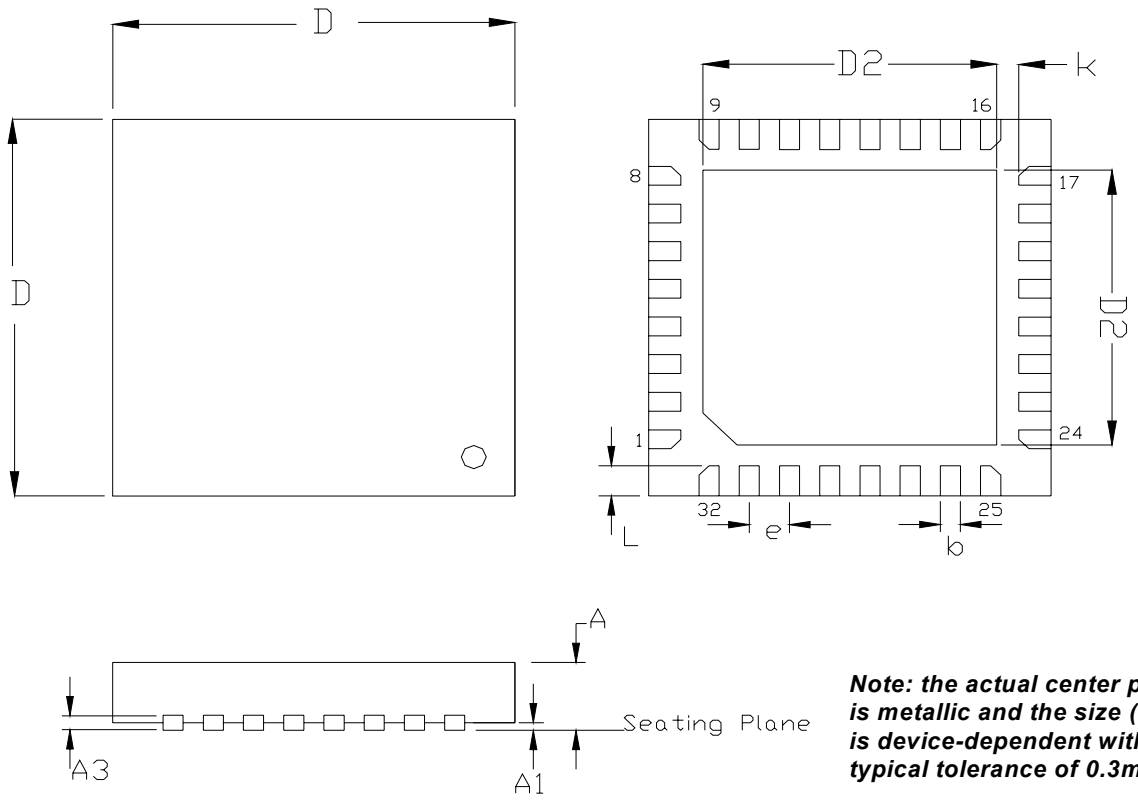
44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)
Rev. 1.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

PACKAGE DIMENSIONS (32 PIN QFN - 5 X 5 X 0.9 mm)



Note: the actual center pad is metallic and the size (D2) is device-dependent with a typical tolerance of 0.3mm

Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A3	0.006	0.010	0.15	0.25
D	0.193	0.201	4.90	5.10
D2	0.138	0.150	3.50	3.80
b	0.007	0.012	0.18	0.30
e	0.0197 BSC		0.50 BSC	
L	0.012	0.020	0.35	0.45
k	0.008	-	0.20	-

REVISION HISTORY

DATE	REVISION	DESCRIPTION
June 2006	P1.0.0	Preliminary Datasheet.
March 2007	1.0.0	Final Datasheet. Updated AC Electrical Characteristics.
May 2007	1.0.1	Added "GND Center Pad" to pin description. Updated 32 pin QFN package dimensions drawing to show minimum "k" parameter.
May 2007	1.0.2	Updated "AC electrical characteristics" table and pin description table.

Datasheet May 2007.

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TABLE OF CONTENTS

GENERAL DESCRIPTION 1
APPLICATIONS 1
FEATURES 1
FIGURE 1. XR16V2652 BLOCK DIAGRAM 1
FIGURE 2. PIN OUT ASSIGNMENT 2
ORDERING INFORMATION 2
PIN DESCRIPTIONS 3
1.0 PRODUCT DESCRIPTION 6
2.0 FUNCTIONAL DESCRIPTIONS 7
2.1 CPU INTERFACE 7
FIGURE 3. XR16V2652 DATA BUS INTERCONNECTIONS 7
2.2 5-VOLT TOLERANT INPUTS 7
2.3 DEVICE RESET 7
2.4 DEVICE IDENTIFICATION AND REVISION 7
2.5 CHANNEL A AND B SELECTION 7
TABLE 1: CHANNEL A AND B SELECT 8
2.6 CHANNEL A AND B INTERNAL REGISTERS 8
2.7 DMA MODE 8
TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE 8
2.8 INTA AND INTB OUTPUTS 9
TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER 9
TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER 9
2.9 CRYSTAL OSCILLATOR OR EXTERNAL CLOCK INPUT 9
FIGURE 4. TYPICAL CRYSTAL CONNECTIONS 9
2.10 PROGRAMMABLE BAUD RATE GENERATOR WITH FRACTIONAL DIVISOR 10
FIGURE 5. BAUD RATE GENERATOR 11
TABLE 5: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING 11
2.11 TRANSMITTER 12
2.11.1 TRANSMIT HOLDING REGISTER (THR) - WRITE ONLY 12
2.11.2 TRANSMITTER OPERATION IN NON-FIFO MODE 12
FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE 12
2.11.3 TRANSMITTER OPERATION IN FIFO MODE 12
FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE 13
2.12 RECEIVER 13
2.12.1 RECEIVE HOLDING REGISTER (RHR) - READ-ONLY 13
FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE 14
FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE 14
2.13 AUTO RTS (HARDWARE) FLOW CONTROL 15
2.14 AUTO RTS HYSTERESIS 15
TABLE 6: AUTO RTS (HARDWARE) FLOW CONTROL 15
2.15 AUTO CTS FLOW CONTROL 15
FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION 16
2.16 AUTO XON/XOFF (SOFTWARE) FLOW CONTROL 17
TABLE 7: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL 17
2.17 SPECIAL CHARACTER DETECT 17
2.18 INFRARED MODE 18
FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING 18
2.19 SLEEP MODE WITH AUTO WAKE-UP 19
2.20 INTERNAL LOOPBACK 20
FIGURE 12. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING 20
3.0 UART INTERNAL REGISTERS 21
TABLE 8: UART CHANNEL A AND B UART INTERNAL REGISTERS 21
TABLE 9: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1 22
4.0 INTERNAL REGISTER DESCRIPTIONS 23
4.1 RECEIVE HOLDING REGISTER (RHR) - READ- ONLY 23
4.2 TRANSMIT HOLDING REGISTER (THR) - WRITE-ONLY 23
4.3 INTERRUPT ENABLE REGISTER (IER) - READ/WRITE 23
4.3.1 IER VERSUS RECEIVE FIFO INTERRUPT MODE OPERATION 23
4.3.2 IER VERSUS RECEIVE/TRANSMIT FIFO POLLED MODE OPERATION 24

4.4 INTERRUPT STATUS REGISTER (ISR) - READ-ONLY 25
4.4.1 INTERRUPT GENERATION: 25
4.4.2 INTERRUPT CLEARING: 25
TABLE 10: INTERRUPT SOURCE AND PRIORITY LEVEL 26
4.5 FIFO CONTROL REGISTER (FCR) - WRITE-ONLY 26
TABLE 11: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION 27
4.6 LINE CONTROL REGISTER (LCR) - READ/WRITE 27
TABLE 12: PARITY SELECTION 29
4.7 MODEM CONTROL REGISTER (MCR) OR GENERAL PURPOSE OUTPUTS CONTROL - READ/WRITE .. 29
4.8 LINE STATUS REGISTER (LSR) - READ ONLY 30
4.9 MODEM STATUS REGISTER (MSR) - READ ONLY 31
4.10 SCRATCH PAD REGISTER (SPR) - READ/WRITE 32
4.11 BAUD RATE GENERATOR REGISTERS (DLL, DLM AND DLD) - READ/WRITE 32
TABLE 13: SAMPLING RATE SELECT 32
4.12 ALTERNATE FUNCTION REGISTER (AFR) - READ/WRITE 32
4.13 DEVICE IDENTIFICATION REGISTER (DVID) - READ ONLY 33
4.14 DEVICE REVISION REGISTER (DREV) - READ ONLY 33
4.15 ENHANCED FEATURE REGISTER (EFR) 33
TABLE 14: SOFTWARE FLOW CONTROL FUNCTIONS 34
4.15.1 SOFTWARE FLOW CONTROL REGISTERS (XOFF1, XOFF2, XON1, XON2) - READ/WRITE 35
TABLE 15: UART RESET CONDITIONS FOR CHANNEL A AND B 36
ABSOLUTE MAXIMUM RATINGS 37
TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%) 37
ELECTRICAL CHARACTERISTICS 37
DC ELECTRICAL CHARACTERISTICS 37
TA=0o to 70oC (-40o to +85oC for industrial grade package), Vcc is 2.25V to 3.6V 37
AC ELECTRICAL CHARACTERISTICS 38
Unless otherwise noted: TA = -40o to +85oC, Vcc=2.25 - 3.63V, 70 pF load where applicable 38
FIGURE 13. CLOCK TIMING 39
FIGURE 14. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B 39
FIGURE 16. DATA BUS WRITE TIMING 40
FIGURE 15. DATA BUS READ TIMING 40
FIGURE 17. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B 41
FIGURE 18. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B 41
FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A & B 42
FIGURE 20. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A & B 42
FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A & B 43
FIGURE 22. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A & B 43
PACKAGE DIMENSIONS (44 PIN PLCC) 44
PACKAGE DIMENSIONS (32 PIN QFN - 5 X 5 X 0.9 mm) 45
REVISION HISTORY 46
TABLE OF CONTENTS ..... *I*

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