



**THE DATASHEET OF
VNQ7040AYTR-E**



Quad channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



PowerSSO-36

- Self limiting of fast thermal transients
- Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
- Loss of ground and loss of V_{CC}
- Reverse battery through self turn-on
- Electrostatic discharge protection

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per ch)	R_{ON}	40 m Ω
Current limitation (typ)	I_{LIMH}	34 A
Standby current (max)	I_{STBY}	0.5 μ A

- General
 - Quad channel smart high-side driver with MultiSense analog feedback
 - LED Mode for channel 0 and 1
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
 - Multiplexed analog feedback of: Load current with high precision proportional current mirror; V_{CC} supply voltage; T_{CHIP} device temperature
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 and R5W paralleled or LED Rear Combinations)

Description

The VNQ7040AY-E is a quad channel high-side driver manufactured using the latest ST proprietary VIPower[®] technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions such as high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

The device features a dedicated LED Mode.

Contents

1	Block diagram and pin description	7
2	Electrical specification	9
2.1	Absolute maximum ratings	9
2.2	Thermal data	10
2.3	Electrical characteristics	11
2.3.1	General electrical specification	11
2.3.2	Bulb mode (default)	17
2.4	Electrical characteristics curves - Bulb Mode	21
2.4.1	LED Mode (Channel 0 and 1)	24
2.5	Electrical characteristics curves - LED mode	28
2.5.1	Truth tables	32
2.5.2	Immunity to electrical transient disturbances on VCC (ISO 7637-2)	34
3	Protections	35
3.1	Power limitation	35
3.2	Thermal shutdown	35
3.3	Current limitation	35
3.4	Negative voltage clamp	35
4	Application information	36
4.1	Protection against reverse battery	36
4.2	Immunity against transient electrical disturbances	37
4.3	MCU I/Os protection	37
4.4	Multisense - analog current sense	38
4.4.1	Principle of Multisense signal generation	40
4.4.2	T _{CASE} and V _{CC} monitor	42
4.4.3	Short to VCC and OFF-state open-load detection	43
4.5	Maximum demagnetization energy (V _{CC} = 16 V)	44
5	Package and PCB thermal data	45
5.1	PowerSSO-36 thermal data	45

6	Package information	49
6.1	ECOPACK®	49
6.2	PowerSSO-36 mechanical data	49
6.3	Packing information	51
7	Order codes	52
8	Revision history	53

List of tables

Table 1.	Pin functions	7
Table 2.	Suggested connections for unused and not connected pins	8
Table 3.	Absolute maximum ratings	9
Table 4.	Thermal data	10
Table 5.	Power section	11
Table 6.	Logic Inputs ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)	12
Table 7.	Protections ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)	13
Table 8.	MultiSense ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)	14
Table 9.	Power section in Bulb Mode ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)	17
Table 10.	Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)	17
Table 11.	MultiSense in Bulb Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)	18
Table 12.	Switching in LED Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)	24
Table 13.	Power section in LED Mode ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)	25
Table 14.	MultiSense in LED Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)	25
Table 15.	Truth table	32
Table 16.	MultiSense multiplexer addressing	32
Table 17.	Bulb/LED Mode Configuration	33
Table 18.	Electrical transient requirements (part 1/3)	34
Table 19.	Electrical transient requirements (part 2/3)	34
Table 20.	Electrical transient requirements (part 3/3)	34
Table 21.	ISO 7637-2 - electrical transient conduction along supply line	37
Table 22.	MultiSense pin levels in off-state	42
Table 23.	PCB properties	46
Table 24.	Thermal parameters	48
Table 25.	PowerSSO-36 mechanical data	50
Table 26.	Device summary	52
Table 27.	Document revision history	53

List of figures

Figure 1.	Block diagram	7
Figure 2.	Configuration diagram (top view)	8
Figure 3.	Current and voltage conventions	9
Figure 4.	Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}	20
Figure 5.	Bulb Mode - current sense precision vs. I_{OUT}	20
Figure 6.	OFF-state output current	21
Figure 7.	Standby current	21
Figure 8.	$I_{GND(ON)}$ vs. I_{out}	21
Figure 9.	Logic Input high level voltage	21
Figure 10.	Logic Input low level voltage	21
Figure 11.	High level logic input current	21
Figure 12.	Low level logic input current	22
Figure 13.	Logic Input hysteresis voltage	22
Figure 14.	FaultRST Input clamp voltage	22
Figure 15.	Undervoltage shutdown	22
Figure 16.	On-state resistance vs. T_{case}	22
Figure 17.	On-state resistance vs. V_{CC}	22
Figure 18.	Turn-on voltage slope	23
Figure 19.	Turn-off voltage slope	23
Figure 20.	W_{on} vs. T_{case}	23
Figure 21.	W_{off} vs. T_{case}	23
Figure 22.	I_{LIMH} vs. T_{case}	23
Figure 23.	OFF-state open-load voltage detection threshold	23
Figure 24.	V_{sense} clamp vs. T_{case}	24
Figure 25.	V_{senseh} vs. T_{case}	24
Figure 26.	LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}	26
Figure 27.	LED Mode - current sense precision vs. I_{OUT}	27
Figure 28.	On-state resistance vs. T_{case}	28
Figure 29.	On-state resistance vs. V_{CC}	28
Figure 30.	Turn-on voltage slope	28
Figure 31.	Turn-off voltage slope	28
Figure 32.	W_{on} vs. T_{case}	29
Figure 33.	W_{off} vs. T_{case}	29
Figure 34.	I_{LIMH} vs. T_{case}	29
Figure 35.	Switching times and Pulse skew	30
Figure 36.	MultiSense timings (current sense mode)	30
Figure 37.	Multisense timings (chip temperature and VCC sense mode)	31
Figure 38.	T_{DSKON}	31
Figure 39.	Application diagram	36
Figure 40.	Simplified internal structure	36
Figure 41.	Multisense and diagnostic – block diagram	39
Figure 42.	Multisense block diagram	40
Figure 43.	Analogue HSD – open-load detection in off-state	41
Figure 44.	Open-load / short to VCC condition	42
Figure 45.	GND voltage shift	43
Figure 46.	Maximum turn off current versus inductance	44
Figure 47.	PowerSSO-36 PC board	45
Figure 48.	Rthj-amb vs PCB copper area in open box free air condition	46

Figure 49.	PowerSSO-36 thermal impedance junction ambient	47
Figure 50.	Thermal fitting model of a HSD in PowerSSO-36	47
Figure 51.	PowerSSO-36 package dimensions	49
Figure 52.	PowerSSO-36 tube shipment (no suffix)	51
Figure 53.	PowerSSO-36 tape and reel shipment (suffix "TR")	51

1 Block diagram and pin description

Figure 1. Block diagram

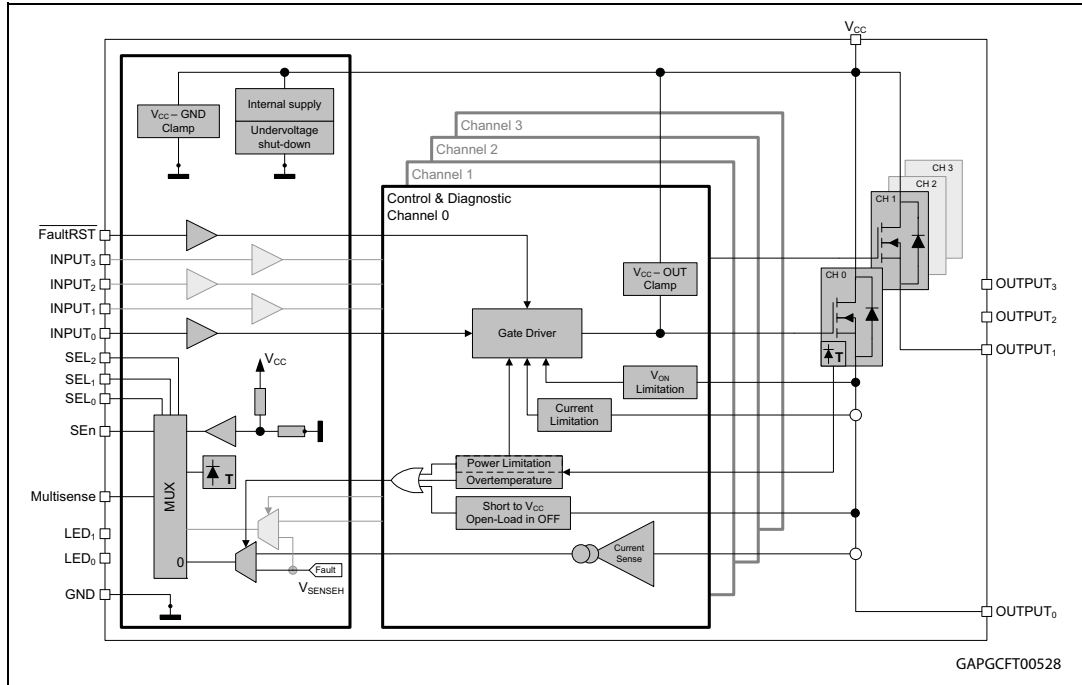


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT _{0,1,2,3}	Power output.
GND	Ground connection.
INPUT _{0,1,2,3}	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin
LED _{0,1}	Active high compatible with 3 V and 5 V CMOS outputs pin; they enable the LED mode on logic high level (see Table 15: Truth table).
SEL _{0,1,2}	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer (see Table 15: Truth table).
$\overline{\text{FaultRST}}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

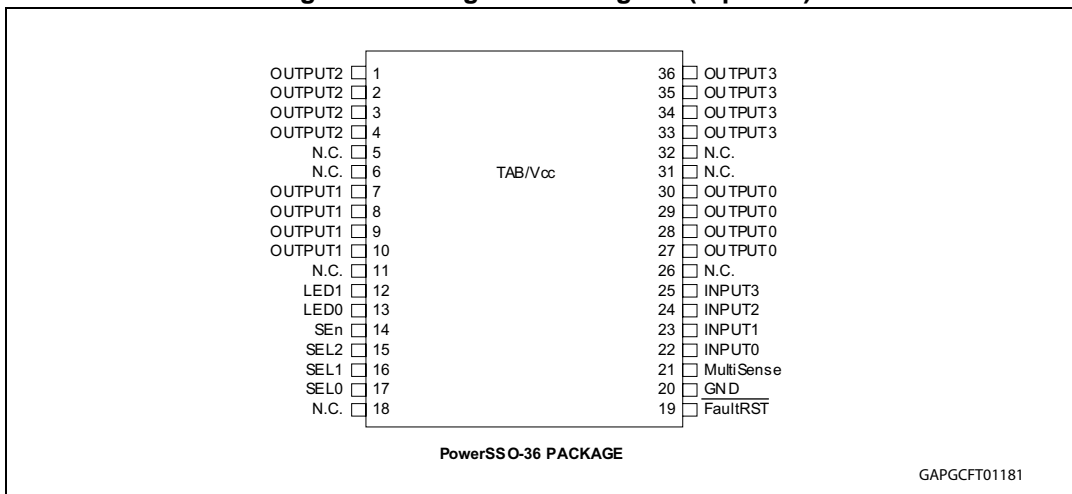


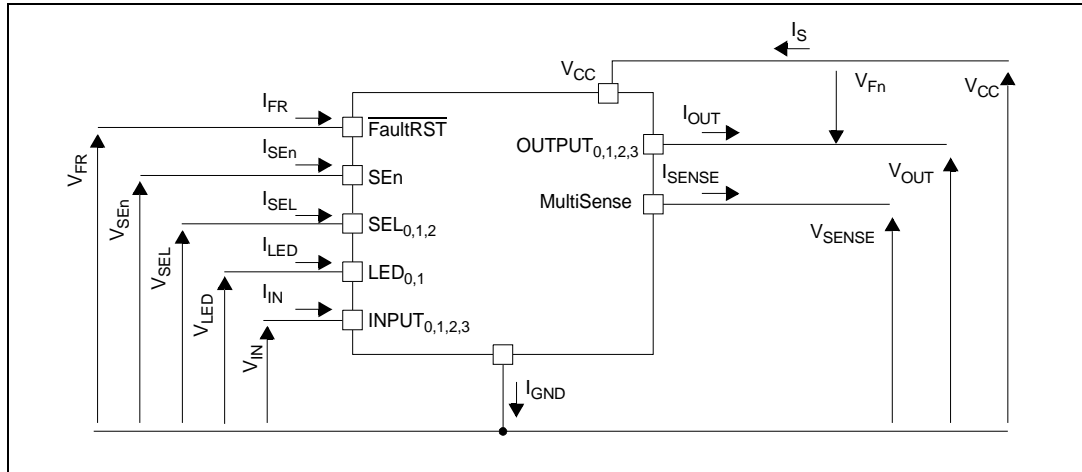
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, LEDx, FaultRST
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{OUTn} - V_{CC}$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; $R_L = 4 \Omega$)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT _{0,1,2,3} DC output current	Internally limited	A
$-I_{OUT_0,1}$	OUTPUT _{0,1} Reverse DC output current	10	
$-I_{OUT_2,3}$	OUTPUT _{2,3} Reverse DC output current	10	
I_{IN}	INPUT _{0,1,2,3} DC input current	-1 to 10	mA
I_{LED}	LED _{0,1} DC input current		
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1,2} DC input current		
I_{FR}	FaultRST DC input current		

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	-10	mA
	MultiSense pin DC output current in reverse ($V_{CC} < 0$ V)	20	mA
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150$ °C)	36	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	– $INPUT_{0,1,2,3}$	4000	V
	– MultiSense	2000	V
	– $LED_{0,1}$, SEn , $SEL_{0,1,2}$, $\overline{FaultRST}$	4000	V
	– $OUTPUT_{0,1,2,3}$	4000	V
	– V_{CC}	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾	4.9	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾	52.5	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	18	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB
3. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace

2.3 Electrical characteristics

$7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

All typical values refer to $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$, unless otherwise specified.

2.3.1 General electrical specification

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$; $25\text{ °C} < T_j < 150\text{ °C}$	41	46	52	V
		$I_S = 20\text{ mA}$; $T_j = -40\text{ °C}$	38			V
I_{STBY}	Supply current in standby at $V_{CC} = 13\text{ V}^{(1)}$	$V_{CC} = 13\text{ V}$; $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0\text{ V}$; $V_{SELO,1,2} = 0\text{ V}$; $V_{LED0,1} = 0\text{ V}$; $T_j = 25\text{ °C}$			0.5	μA
		$V_{CC} = 13\text{ V}$; $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0\text{ V}$; $V_{SELO,1,2} = 0\text{ V}$; $V_{LED0,1} = 0\text{ V}$; $T_j = 85\text{ °C}^{(2)}$			0.5	μA
		$V_{CC} = 13\text{ V}$; $V_{INx} = V_{OUTx} = V_{FR} = V_{SEn} = 0\text{ V}$; $V_{SELO,1,2} = 0\text{ V}$; $V_{LED0,1} = 0\text{ V}$; $T_j = 125\text{ °C}$;			3	μA
t_{D_STBY}	Standby mode blanking time	$V_{CC} = 13\text{ V}$; $V_{INx} = V_{OUTx} = V_{FR} = 0\text{ V}$; $V_{SELO,1,2} = 0\text{ V}$; $V_{LED0,1} = 0\text{ V}$; $V_{SEn} = 5\text{ V to } 0\text{ V}$	60	300	550	μs
$I_{S(ON)}$	Supply current	$V_{CC} = 13\text{ V}$; $V_{SEn} = V_{FR} = V_{SELO,1} = 0\text{ V}$; $V_{INx} = 5\text{ V}$; $I_{OUT0,1,2,3} = 0\text{ A}$;		10	16	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	$V_{CC} = 13\text{ V}$; $V_{SEn} = 5\text{ V}$; $V_{FR} = V_{SELO,1} = 0\text{ V}$; $V_{INx} = 5\text{ V}$; $I_{OUT0,1,2,3} = 2.5\text{ A}$			18.5	mA
$I_{L(off)}$	Off-state output current at $V_{CC} = 13\text{ V}^{(1)}$	$V_{INx} = V_{OUTx} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	0.5	μA
		$V_{INx} = V_{OUTx} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		3	
V_F	Output - V_{CC} diode voltage ⁽³⁾	$I_{OUT} = -2.5\text{ A}$; $T_j = 150\text{ °C}$			0.7	V

1. PowerMOS leakage included.

- 2. Parameter specified by design; not subject to production test.
- 3. For each channel.

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT_{0,1,2,3} characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics						
V _{FRL}	Input low level voltage				0.9	V
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		
SEL_{0,1,2} characteristics (7 V < V_{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
LED_{0,1} characteristics (7 V < V_{CC} < 18 V)						
V _{LEDL}	Input low level voltage				0.9	V
I _{LEDL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{LEDH}	Input high level voltage		2.1			V
I _{LEDH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{LED(hyst)}	Input hysteresis voltage		0.2			V

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{LEDCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 7. Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 5		
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R) ⁽¹⁾			5		
ΔT _{J_SD}	Dynamic temperature			60		
t _{LATCH_RST}	Fault reset time for output unlatch ⁽¹⁾	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V; V _{INx} = 5 V; V _{SEL0,1,2} = 0 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40 °C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25 °C to 150 °C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V
V _{ON}	Output voltage drop limitation	I _{OUT} = 0.25 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	MultiSense clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		-0.7		V
Current Sense characteristics						
I _{SENSE0}	MultiSense leakage current	MultiSense disabled: V _{SEn} = 0 V;	0		0.5	μA
		MultiSense disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾	-0.5		0.5	
		MultiSense enabled: V _{SEn} = 5 V All channels ON; I _{OUTX} = 0 A; Ch _X diagnostic selected; – E.G. Ch ₀ : V _{IN0} = 5 V; V _{IN1,2,3} = 5 V; V _{SELO,1,2} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 2.5 A	0		2	
		MultiSense enabled: V _{SEn} = 5 V Ch _X OFF; Ch _X diagnostic selected: – E.G. Ch ₀ : V _{IN0} = 0 V; V _{IN1,2,3} = 5 V; V _{SELO,1,2} = 0 V; I _{OUT0} = 0 A; I _{OUT1,2,3} = 2.5 A	0		2	
V _{OUT_MSD} ⁽¹⁾	Output Voltage for MultiSense shutdown	V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ – E.g. Ch ₀ : V _{IN0} = 5 V; V _{SELO,1,2} = 0 V; I _{OUT0} = 2.5 A		5		V
V _{SENSE_SAT}	Multisense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 2.7 K; V _{SEn} = 5 V; V _{IN0} = 5 V; V _{SELO,1,2} = 0 V; I _{OUT0} = 4.5 A; T _j = 150°C	5			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C	4			mA
I _{OUT_SAT_BULB} ⁽¹⁾	Output saturation current in BULB mode	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C	8			A
I _{OUT_SAT_LED} ⁽¹⁾	Output saturation current in LED mode	V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SELO,1,2} = 0 V; T _j = 150°C	2.3			A
OFF-state diagnostic						
V _{OL}	OFF state open load voltage detection threshold	V _{SEn} = 5V; Ch _X OFF; Ch _X diagnostic selected – E.G. Ch ₀ V _{IN0} = 0 V; V _{SELO,1,2} = 0 V	2	3	4	V
I _{L(off2)}	OFF state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _j = -40°C to 125°C	-100		-15	μA

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSTKON}	OFF state diagnostic delay time from falling edge of INPUT (see Figure 35)	V _{SEn} = 5 V; Ch _X ON to OFF transition; Ch _X diagnostic selected – E.G: Ch ₀ V _{IN0} = 5 V to 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} > 4 V	100	350	700	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SE _n	V _{INx} = 0 V; V _{FR} = 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF state diagnostic delay time from rising edge of V _{OUT}	V _{SEn} = 5V; Ch _X OFF; Ch _X diagnostic selected – E.G: Ch ₀ V _{IN0} = 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} = 0 V to 4 V		5	30	μs
Chip temperature analog feedback						
V _{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = -40°C	2.325	2.41	2.495	V
		V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 25°C	1.985	2.07	2.155	V
		V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 125°C	1.435	1.52	1.605	V
dV _{SENSE_TC} /dT ⁽²⁾	Temperature coefficient	T _j = -40°C to 150°C		-5.5		mV/K
Transfer function		V _{SENSE_TC} (T) = V _{SENSE_TC} (T ₀) + dV _{SENSE_TC} /dT * (T-T ₀)				
V_{CC} supply voltage analog feedback						
V _{SENSE_VCC}	MultiSense output voltage proportional to V _{CC} supply voltage	V _{CC} = 13 V; V _{SEn} = 5 V; V _{SEL0,1,2} = 5 V; V _{INx} = 0 V; R _{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function ⁽²⁾		V _{SENSE_VCC} = V _{CC} / 4				
Fault diagnostic feedback (see Table 15)						
V _{SENSEH}	MultiSense output voltage in fault condition ⁽¹⁾	V _{CC} = 13 V; R _{SENSE} = 1 kΩ	5		6.6	V
I _{SENSEH}	MultiSense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
MultiSense timings (Chip Temperature Sense mode - see Figure 37)						
t _{DSSENSE3H}	V _{SENSE_TC} settling time from rising edge of SE _n	V _{SEn} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			60	μs

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE3L}	V _{SENSE_TC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (V_{CC} Voltage Sense mode - see Figure 37)						
t _{DSENSE4H}	V _{SENSE_VCC} settling time from rising edge of SEn	V _{SEn} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSENSE4L}	V _{SENSE_VCC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense Timings (Multiplexer transition times)⁽³⁾						
t _{D_XtoY}	MultiSense transition delay from Ch _X to Ch _Y	V _{IN2} = 5 V; V _{IN3} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V; I _{OUT2} = 0 A; I _{OUT3} = 2.5 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CS to TC}	MultiSense transition delay from current sense to T _C sense	V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 0 V to 5 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_TC to CS}	MultiSense transition delay from T _C sense to current sense	V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 5 V to 0 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CS to VCC}	MultiSense transition delay from current sense to V _{CC} sense	V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V to 5 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_VCC to CS}	MultiSense transition delay from V _{CC} sense to current sense	V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL1} = 5 V; V _{SEL0} = V _{SEL2} = 5 V to 0 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_TC to VCC}	MultiSense transition delay from T _C sense to V _{CC} sense	V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 0 V to 5 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_VCC to TC}	MultiSense transition delay from V _{CC} sense to T _C sense	V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 5 V to 0 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_CS to VSENSEH}	MultiSense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y	V _{IN0} = 5 V; V _{IN1} = 0 V; V _{OUT1} > 4 V; V _{SEn} = 5 V; V _{SEL2} = 0 V; V _{SEL1} = 0 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 2.5 A; R _{SENSE} = 1 kΩ			60	μs

1. Parameter guaranteed by design and characterization; not subject to production test.
2. V_{CC} sensing and T_C sensing are referred to GND potential.
3. Transition delay are measured up to +/- 10% of final conditions.

2.3.2 Bulb mode (default)

Table 9. Power section in Bulb Mode ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON_0,1,2,3_BULB}$	On-state resistance in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$I_{OUT} = 2.5\text{ A}$; $T_j = 25\text{ °C}$		40		mΩ
		$I_{OUT} = 2.5\text{ A}$; $T_j = 150\text{ °C}$			80	
		$I_{OUT} = 2.5\text{ A}$; $V_{CC} = 4\text{ V}$; $T_j = 25\text{ °C}$			60	
$R_{ON_REV_0,1,2,3}$	On-state resistance in Reverse Battery Ch0, Ch1, Ch2 and Ch3	$V_{CC} = -13\text{ V}$; $I_{OUT} = -2.5\text{ A}$; $T_j = 25\text{ °C}$		40		mΩ
$I_{LIMH_0,1,2,3_BULB}^{(1)}$	DC short circuit current in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$V_{CC} = 13\text{ V}$	24	34	48	A
		$4\text{ V} < V_{CC} < 18\text{ V}^{(2)}$			48	
$I_{LIML_0,1,2,3_BULB}$	Short circuit current during thermal cycling in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$V_{CC} = 13\text{ V}$; $T_R < T_j < T_{TSD}$		9		
$V_{ON_0,1,2,3_BULB}$	Output voltage drop limitation in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$I_{OUT} = 0.25\text{ A}$		20		mV

1. Parameter guaranteed by an indirect test sequence.

2. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Channel 0, 1, 2 and 3						
$t_{d(on)_0,1,2,3}^{(1)}$	Turn-on delay time at $T_j = 25\text{ °C}$	$R_L = 5.2\text{ Ω}$	10	60	120	μs
$t_{d(off)_0,1,2,3}^{(1)}$	Turn-off delay time at $T_j = 25\text{ °C}$	$R_L = 5.2\text{ Ω}$	10	50	100	
$(dV_{OUT}/dt)_{on_0,1,2,3}^{(1)}$	Turn-on voltage slope at $T_j = 25\text{ °C}$	$R_L = 5.2\text{ Ω}$	0.1	0.5	0.7	V/μs
$(dV_{OUT}/dt)_{off_0,1,2,3}^{(1)}$	Turn-off voltage slope at $T_j = 25\text{ °C}$	$R_L = 5.2\text{ Ω}$	0.1	0.5	0.7	
$W_{ON_0,1,2,3}$	Switching energy losses at turn-on (t_{won})	$R_L = 5.2\text{ Ω}$	—	0.2	$0.52^{(2)}$	mJ

Table 10. Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$W_{\text{OFF}_0,1,2,3}$	Switching energy losses at turn-off (t_{woff})	$R_L = 5.2\ \Omega$	—	0.2	$0.5^{(2)}$	mJ
$t_{\text{SKEW}_0,1,2,3}^{(1)}$	Differential pulse skew ($t_{\text{PHL}} - t_{\text{PLH}}$)	$R_L = 5.2\ \Omega$	-65	-15	35	μs

1. See [Figure 35: Switching times and Pulse skew](#).
2. Parameter guaranteed by design and characterization, not subject to production test.

Table 11. MultiSense in Bulb Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current sense characteristics						
Channel 0, 1, 2 and 3						
$K_{\text{OL_CH0,1_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 10\text{ mA}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	430			
$K_{\text{OL_CH2,3_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 10\text{ mA}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	430			
$dK_{\text{cal}}/K_{\text{cal}}^{(1)(2)}$	Current sense ratio drift at calibration point	$I_{\text{CAL}} = 30\text{ mA}$; $I_{\text{OUT}} = 10\text{ mA to } 50\text{ mA}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	-35		35	%
$K_{\text{LED_CH0,1_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.05\text{ A}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	720	1440	2160	
$K_{\text{LED_CH2,3_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.05\text{ A}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	720	1440	2160	
$K_0_{\text{CH0,1_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.25\text{ A}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	930	1550	2170	
$K_0_{\text{CH2,3_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.25\text{ A}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	930	1550	2170	
$dK_0/K_0^{(1)(2)}$	Current sense ratio drift	$I_{\text{OUT}} = 0.25\text{ A}$; $V_{\text{SENSE}} = 0.5\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	-20		20	%
$K_1_{\text{CH0,1_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.5\text{ A}$; $V_{\text{SENSE}} = 4\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	1110	1590	2070	
$K_1_{\text{CH2,3_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 0.5\text{ A}$; $V_{\text{SENSE}} = 4\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	1085	1550	2015	
$dK_1/K_1^{(1)(2)}$	Current sense ratio drift	$I_{\text{OUT}} = 0.5\text{ A}$; $V_{\text{SENSE}} = 4\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	-15		15	%
$K_2_{\text{CH0,1_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 2\text{ A}$; $V_{\text{SENSE}} = 4\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	1160	1450	1740	
$K_2_{\text{CH2,3_B}}$	$I_{\text{OUT}}/I_{\text{SENSE}}$	$I_{\text{OUT}} = 2\text{ A}$; $V_{\text{SENSE}} = 4\text{ V}$; $V_{\text{SEN}} = 5\text{ V}$	1130	1410	1690	

Table 11. MultiSense in Bulb Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dK_2/K_2^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 2\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	-10		10	%
$K_3_{CH0,1_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 6\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	1295	1440	1585	
$K_3_{CH2,3_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 6\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	1260	1400	1540	
$dK_3/K_3^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 6\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	-5		5	%
MultiSense timings (Current Sense mode see Figure 36)						
Channel 0, 1, 2 and 3						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEN	$V_{IN} = 5\text{ V}$; $V_{SEn} = 0\text{ V}$ to 5 V ; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 5.2\text{ }\Omega$			60	μs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEN	$V_{SEn} = 5\text{ V}$ to 0 V ; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 5.2\text{ }\Omega$		5	20	μs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	$V_{IN} = 0\text{ V}$ to 5 V ; $V_{SEn} = 5\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 5.2\text{ }\Omega$		100	250	μs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$V_{IN} = 5\text{ V}$; $V_{SEn} = 5\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 5.2\text{ }\Omega$			100	μs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	$V_{IN} = 5\text{ V}$ to 0 V ; $V_{SEn} = 5\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 5.2\text{ }\Omega$		50	250	μs

- Parameter specified by design; not subject to production test.
- All values refer to $V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Figure 4. Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}

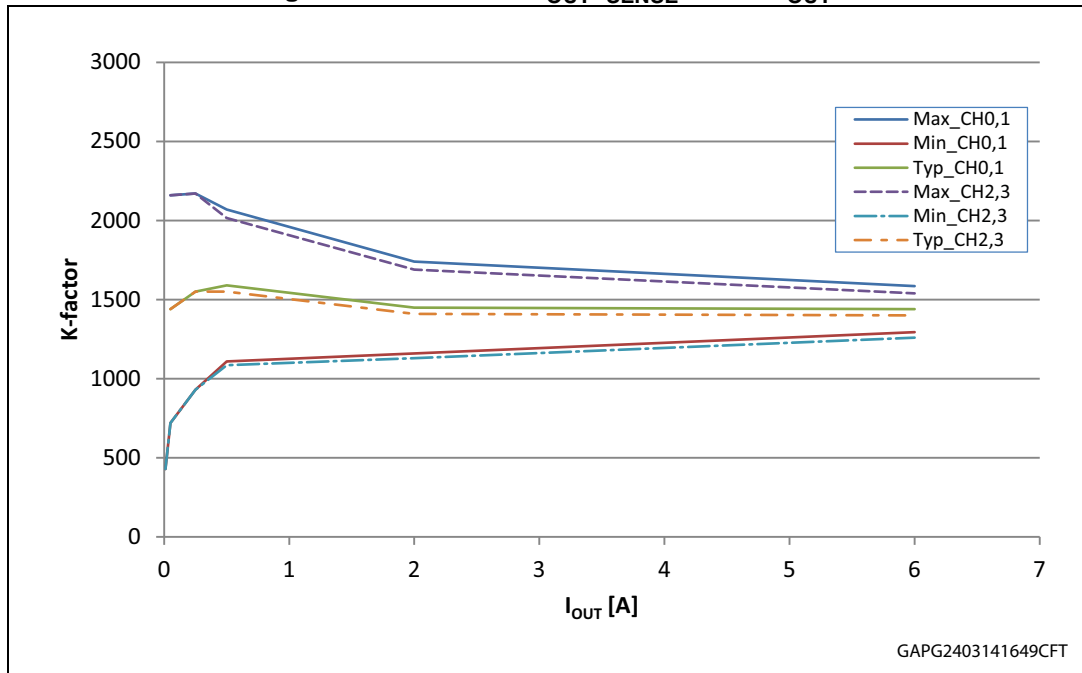
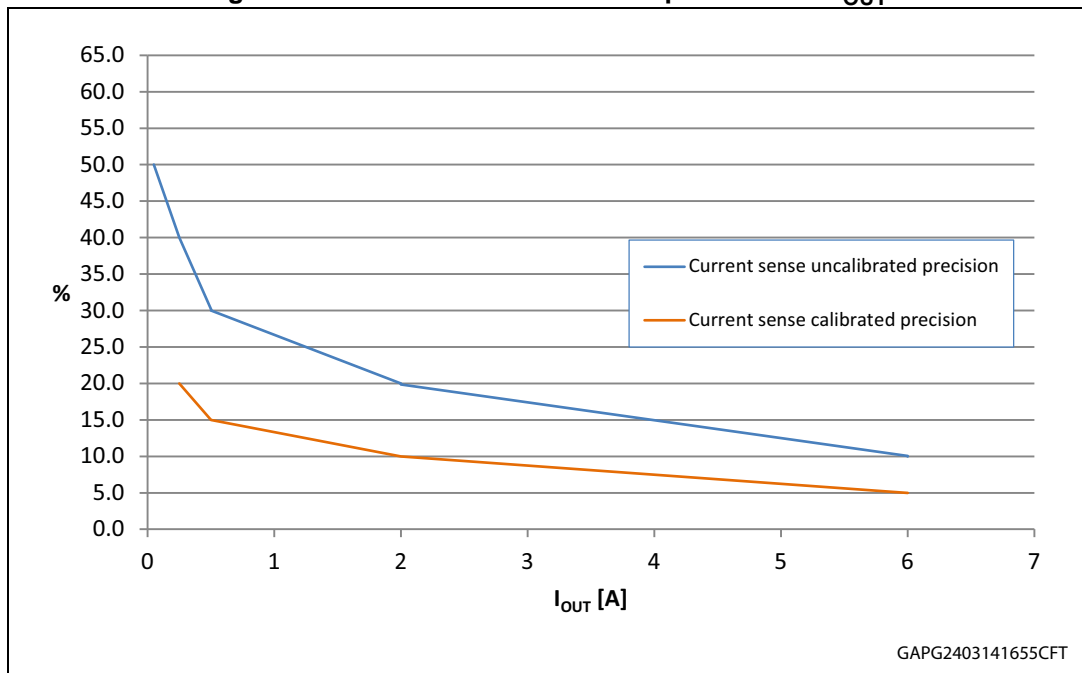


Figure 5. Bulb Mode - current sense precision vs. I_{OUT}



2.4 Electrical characteristics curves - Bulb Mode

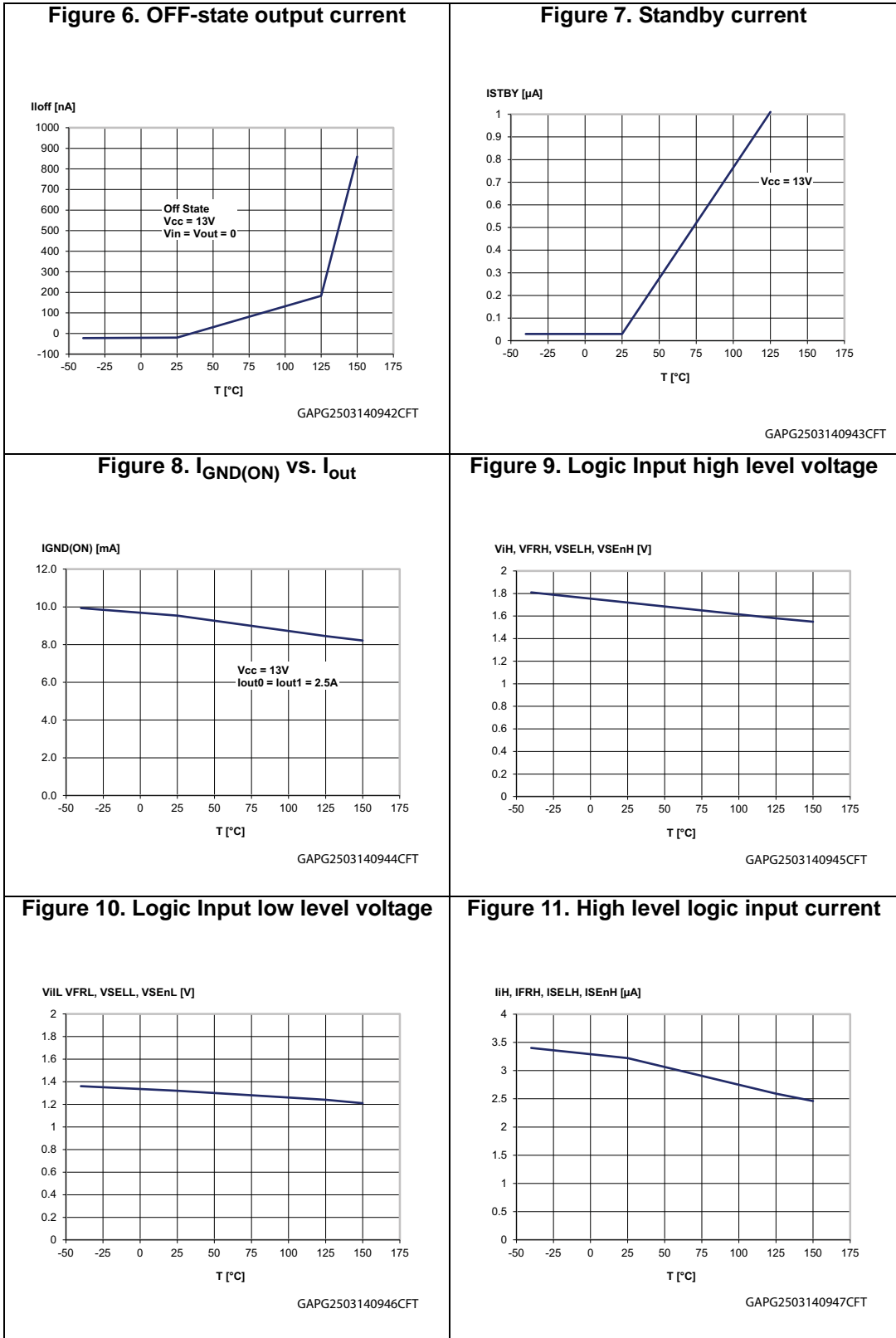
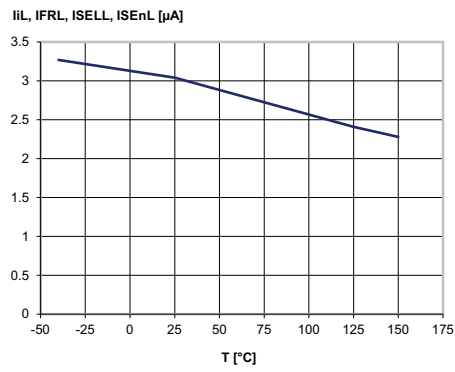
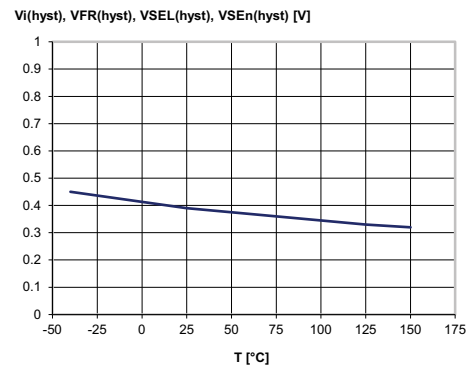


Figure 12. Low level logic input current



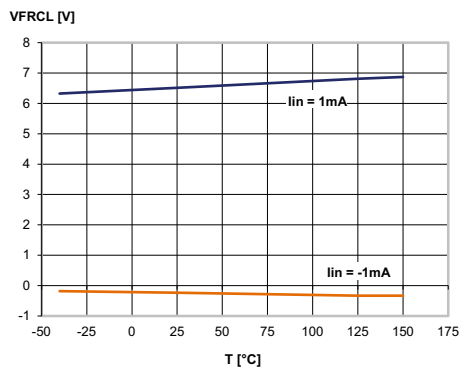
GAPG2503140948CFT

Figure 13. Logic Input hysteresis voltage



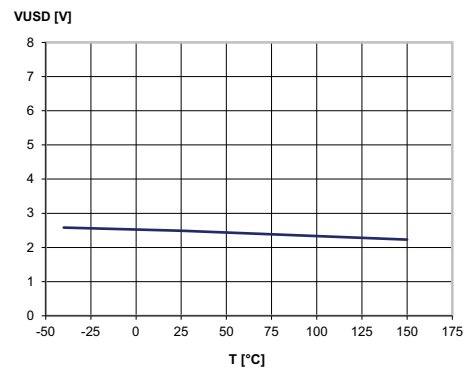
GAPG2503140949CFT

Figure 14. FaultRST Input clamp voltage



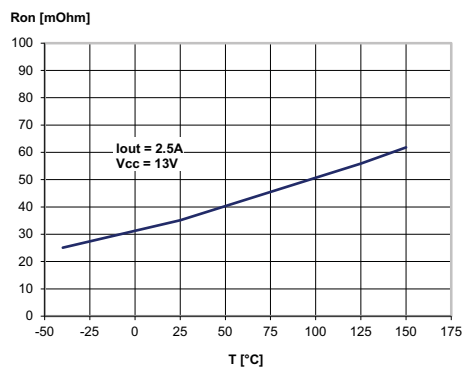
GAPG2503140950CFT

Figure 15. Undervoltage shutdown



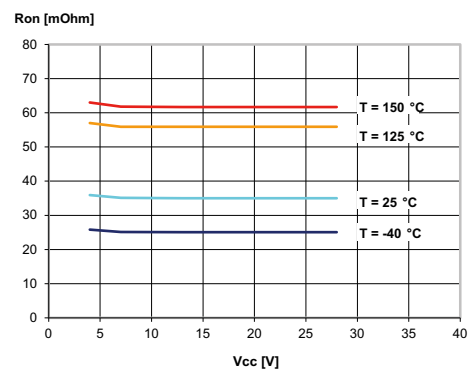
GAPG2503140951CFT

Figure 16. On-state resistance vs. T_{case}



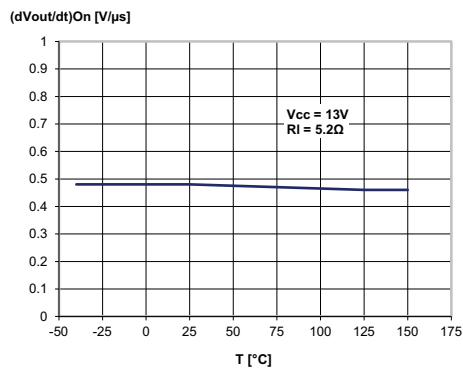
GAPG2503140952CFT

Figure 17. On-state resistance vs. V_{CC}



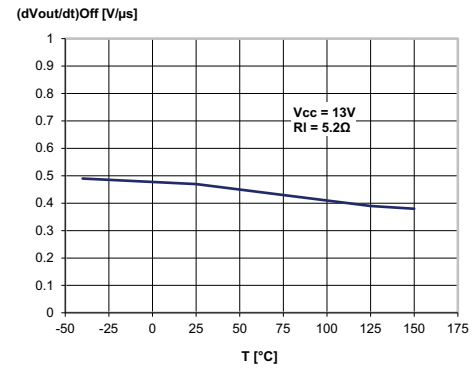
GAPG2503140953CFT

Figure 18. Turn-on voltage slope



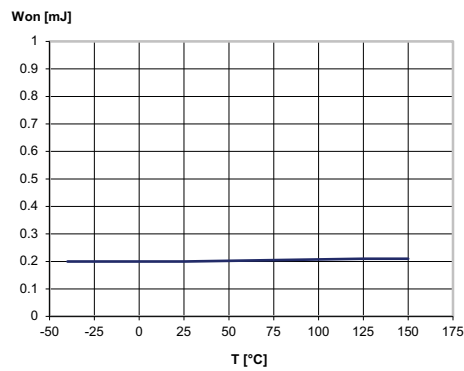
GAPG2503140954CFT

Figure 19. Turn-off voltage slope



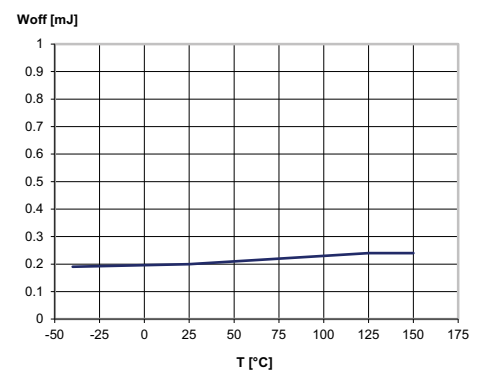
GAPG2503140955CFT

Figure 20. Won vs. T_{case}



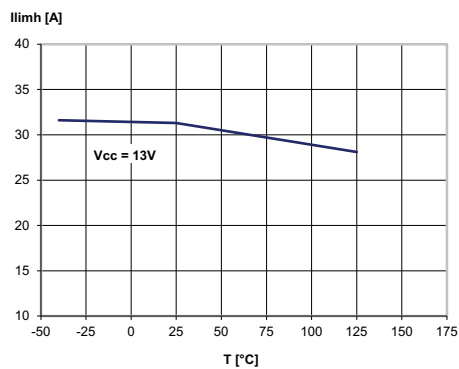
GAPG2503141122CFT

Figure 21. Woff vs. T_{case}



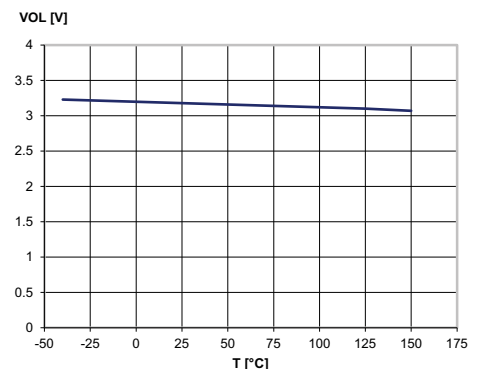
GAPG2503141123CFT

Figure 22. I_{LIMH} vs. T_{case}

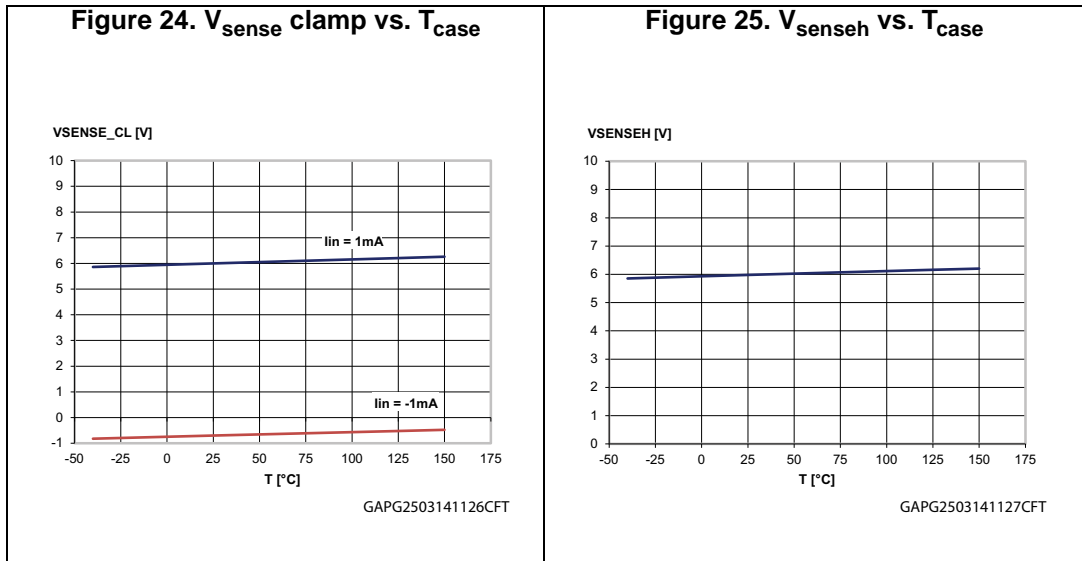


GAPG2503141124CFT

Figure 23. OFF-state open-load voltage detection threshold



GAPG2503141125CFT



2.4.1 LED Mode (Channel 0 and 1)

Table 12. Switching in LED Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)_{0,1_LED}}^{(1)}$	Turn-on delay time at $T_j = 25\text{ }^\circ\text{C}$	$R_L = 22.8\ \Omega$	10	65	120	μs
$t_{d(off)_{0,1_LED}}^{(1)}$	Turn-off delay time at $T_j = 25\text{ }^\circ\text{C}$	$R_L = 22.8\ \Omega$	10	40	100	
$(dV_{OUT}/dt)_{on_{0,1_LED}}^{(1)}$	Turn-on voltage slope at $T_j = 25\text{ }^\circ\text{C}$	$R_L = 22.8\ \Omega$	0.2	0.5	0.8	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off_{0,1_LED}}^{(1)}$	Turn-off voltage slope at $T_j = 25\text{ }^\circ\text{C}$	$R_L = 22.8\ \Omega$	0.1	0.5	0.7	
$W_{ON_{0,1_LED}}$	Switching energy losses at turn-on (t_{won})	$R_L = 22.8\ \Omega$	—	0.04	0.1 ⁽²⁾	mJ
$W_{OFF_{0,1_LED}}$	Switching energy losses at turn-off (t_{woff})	$R_L = 22.8\ \Omega$	—	0.045	0.11 ⁽²⁾	mJ
$t_{SKEW_{0,1_LED}}^{(1)}$	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 22.8\ \Omega$	-75	-25	25	μs

1. See [Figure 35: Switching times and Pulse skew](#).
2. Parameter guaranteed by design and characterization, not subject to production test.

Table 13. Power section in LED Mode ($7\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON_0,1_LED}$	On-state resistance in LED Mode Ch0 and Ch1	$I_{OUT} = 0.57\text{ A}$; $T_j = 25\text{ °C}$		140		mΩ
		$I_{OUT} = 0.57\text{ A}$; $T_j = 150\text{ °C}$			280	
		$I_{OUT} = 0.57\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ °C}$			210	
$I_{LIMH_0,1_LED}^{(1)}$	DC short circuit current in Bulb Mode Ch0 and Ch1	$V_{CC} = 13\text{ V}$	5.5	8	11	A
		$4\text{ V} < V_{CC} < 18\text{ V}^{(2)}$				
$I_{LIML_0,1_LED}$	Short circuit current during thermal cycling in Bulb Mode Ch0 and Ch1	$V_{CC} = 13\text{ V}$; $T_R < T_j < T_{TSD}$		2		
$V_{ON_0,1_LED}$	Output voltage drop limitation in LED Mode Ch0 and Ch1	$I_{OUT} = 0.07\text{ A}$		20		

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 14. MultiSense in LED Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.01\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $V_{SEn} = 5\text{ V}$	120			
$dK_{cal}/K_{cal}^{(1)(2)}$	Current sense ratio drift at calibration point	$I_{cal} = 17.5\text{ mA}$; $I_{OUT} = 10\text{ mA to }25\text{ mA}$; $V_{SENSE} = 0.5\text{ V}$; $V_{SEn} = 5\text{ V}$	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.025\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $V_{SEn} = 5\text{ V}$	150	380	610	
$dK_{LED}/K_{LED}^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 0.025\text{ A}$; $V_{SENSE} = 0.5\text{ V}$; $V_{SEn} = 5\text{ V}$	-25		25	%
$K_{0_CH0,1_L}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.15\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	240	405	570	
$dK_0/K_0^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 0.15\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	-15		15	%
$K_{1_CH0,1_L}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.7\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	300	380	460	
$dK_1/K_1^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 0.7\text{ A}$; $V_{SENSE} = 4\text{ V}$; $V_{SEn} = 5\text{ V}$	-8		8	%
MultiSense timings (Current Sense mode - see Figure 36)						
$t_{DSSENSE1H}$	Current sense settling time from rising edge of SEn	$V_{IN} = 5\text{ V}$; $V_{SEn} = 0\text{ V to }5\text{ V}$; $R_{SENSE} = 1\text{ k}\Omega$; $R_L = 22.8\text{ }\Omega$			60	μs

Table 14. MultiSense in LED Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSENSE1L}	Current sense disable delay time from falling edge of SEn	$V_{\text{SEn}} = 5\text{ V to } 0\text{ V}$; $R_{\text{SENSE}} = 1\text{ k}\Omega$; $R_L = 22.8\ \Omega$		5	20	μs
t_{DSENSE2H}	Current sense settling time from rising edge of INPUT	$V_{\text{IN}} = 0\text{ V to } 5\text{ V}$; $V_{\text{SEn}} = 5\text{ V}$; $R_{\text{SENSE}} = 1\text{ k}\Omega$; $R_L = 22.8\ \Omega$			250	μs
$\Delta t_{\text{DSENSE2H}}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$V_{\text{IN}} = 5\text{ V}$; $V_{\text{SEn}} = 5\text{ V}$; $R_{\text{SENSE}} = 1\text{ k}\Omega$; $R_L = 22.8\ \Omega$			100	μs
t_{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	$V_{\text{IN}} = 5\text{ V to } 0\text{ V}$; $V_{\text{SEn}} = 5\text{ V}$; $R_{\text{SENSE}} = 1\text{ k}\Omega$; $R_L = 22.8\ \Omega$		50	250	μs

1. Parameter specified by design; not subject to production test.
2. All values refer to $V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Figure 26. LED Mode - $I_{\text{OUT}}/I_{\text{SENSE}}$ versus I_{OUT}

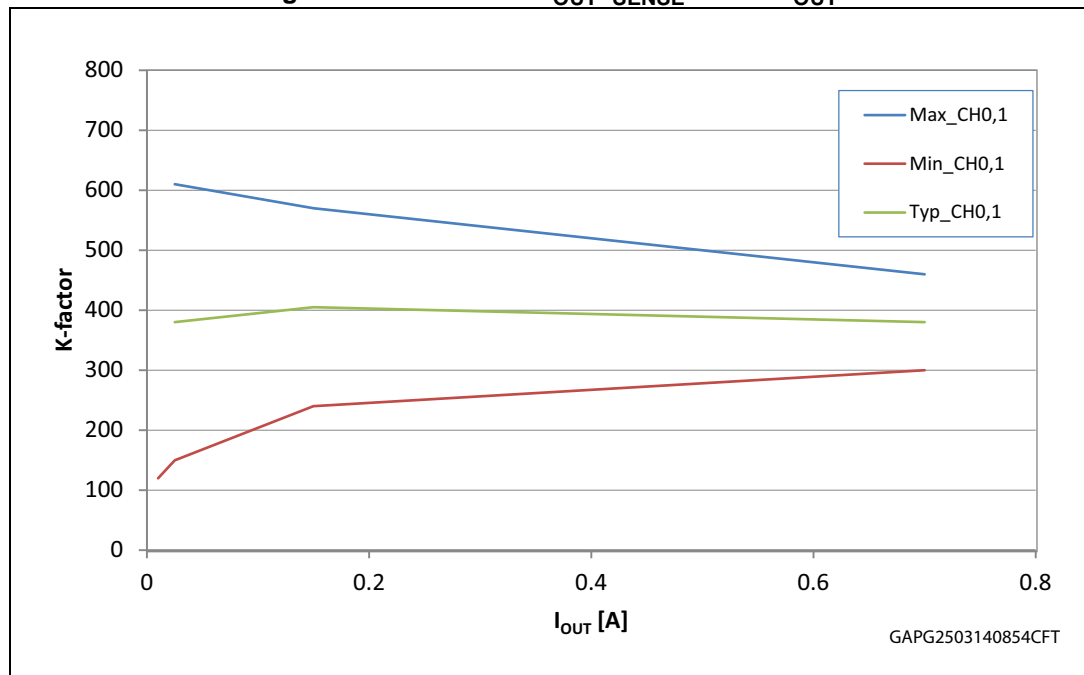
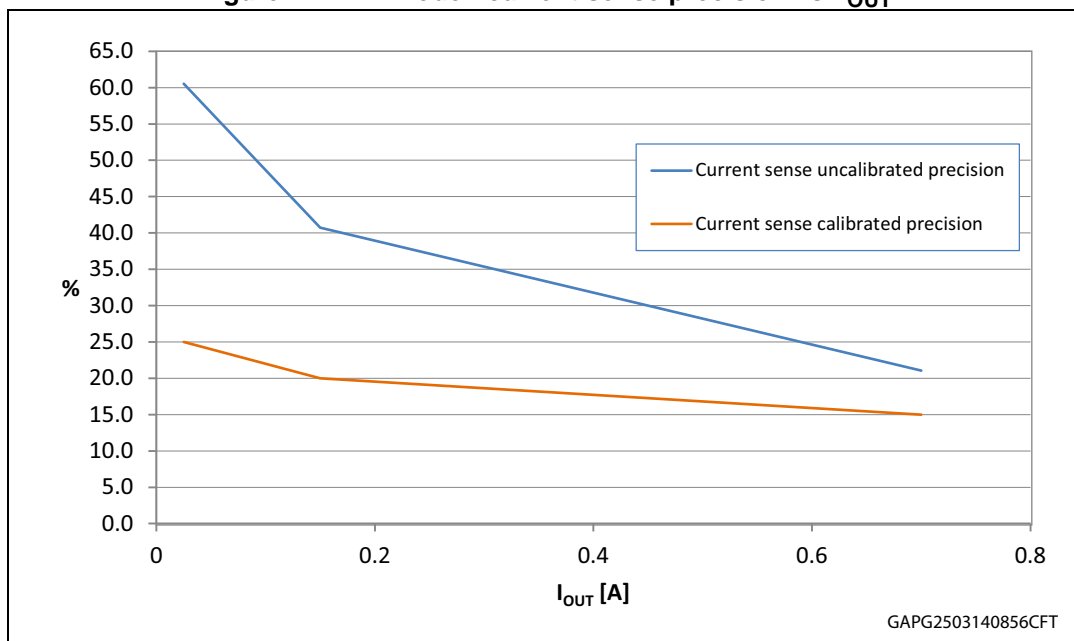
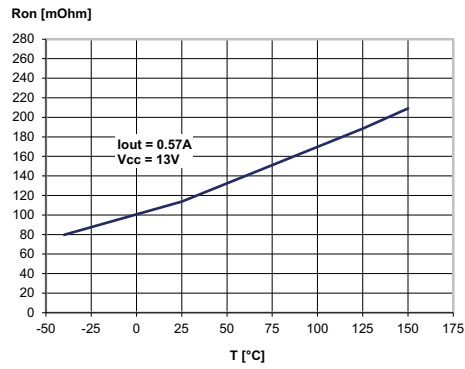


Figure 27. LED Mode - current sense precision vs. I_{OUT}



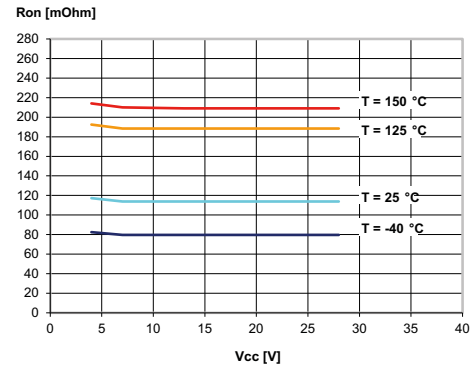
2.5 Electrical characteristics curves - LED mode

Figure 28. On-state resistance vs. T_{case}



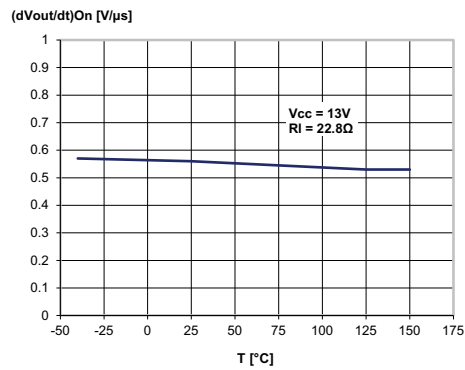
GAPG2503141130CFT

Figure 29. On-state resistance vs. V_{CC}



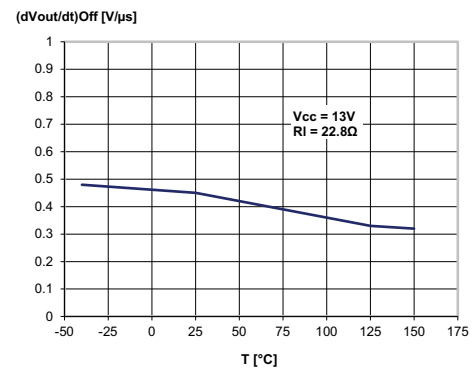
GAPG2503141131CFT

Figure 30. Turn-on voltage slope



GAPG2503141132CFT

Figure 31. Turn-off voltage slope



GAPG2503141133CFT

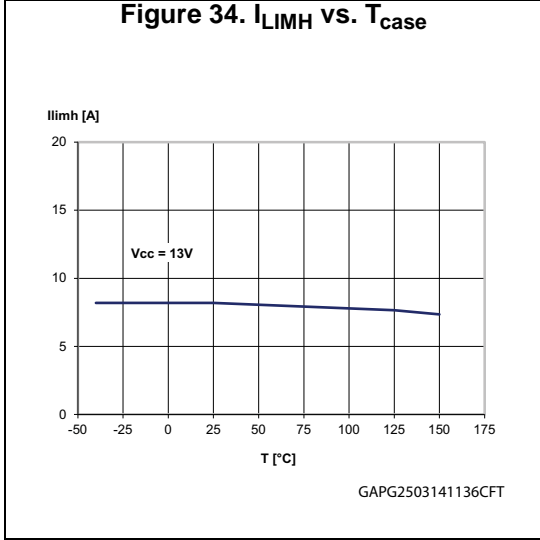
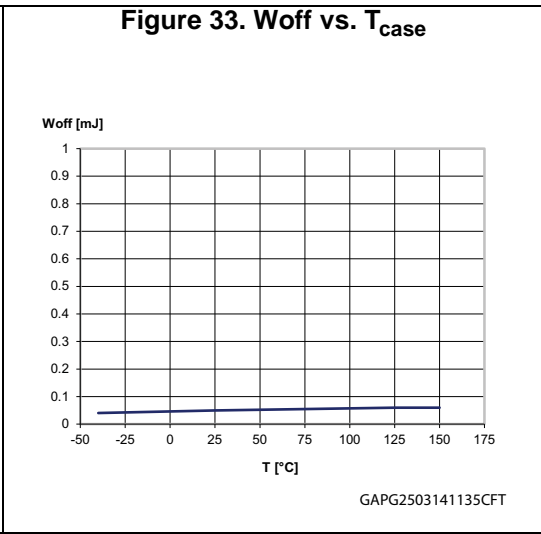
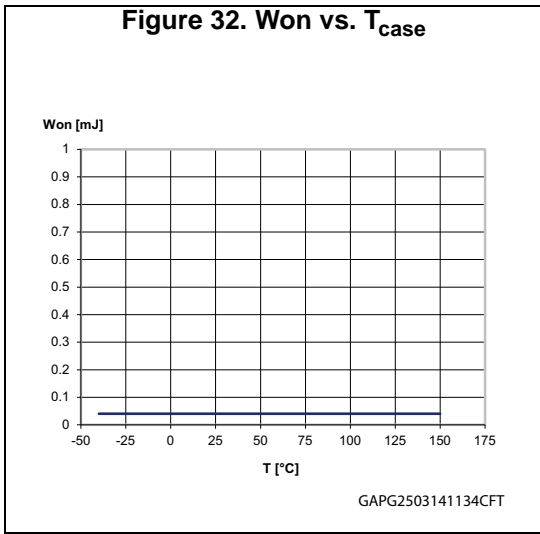


Figure 35. Switching times and Pulse skew

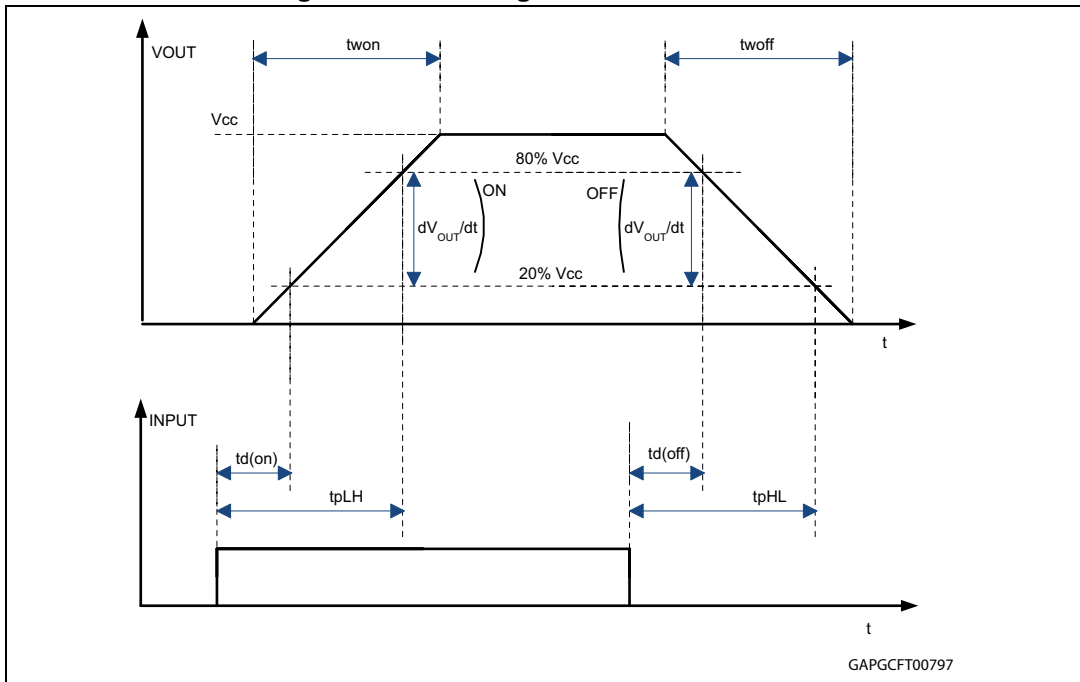


Figure 36. MultiSense timings (current sense mode)

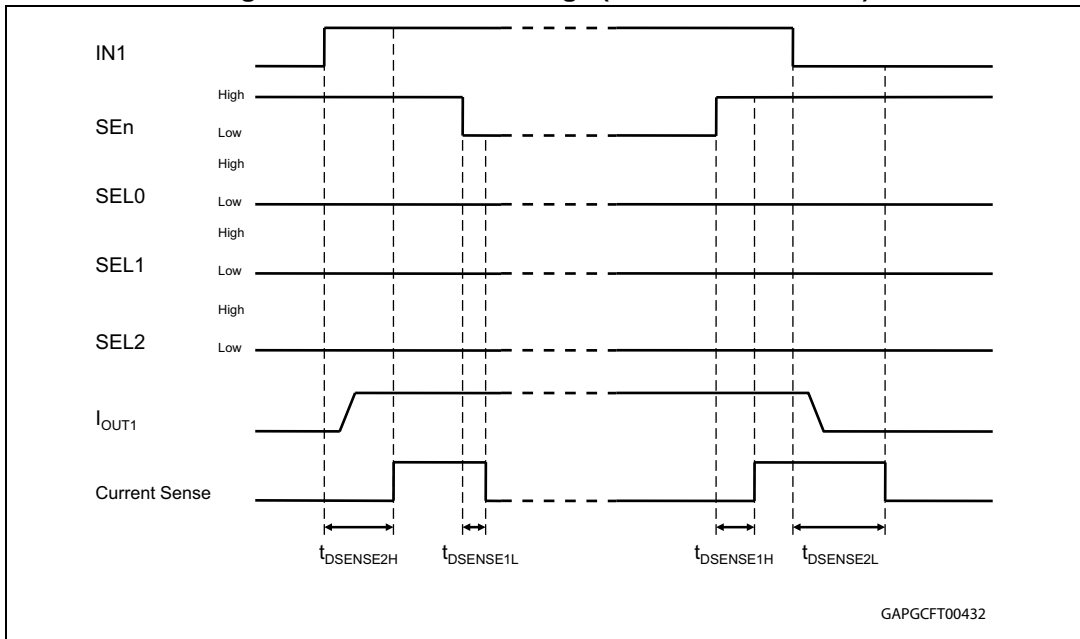


Figure 37. Multisense timings (chip temperature and V_{CC} sense mode)

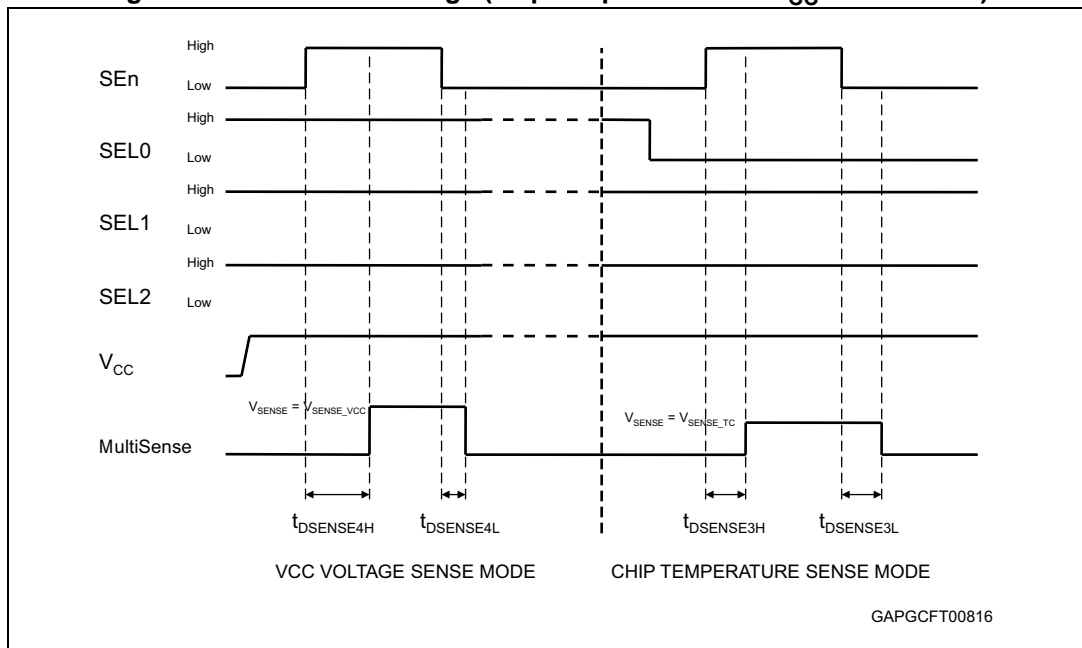
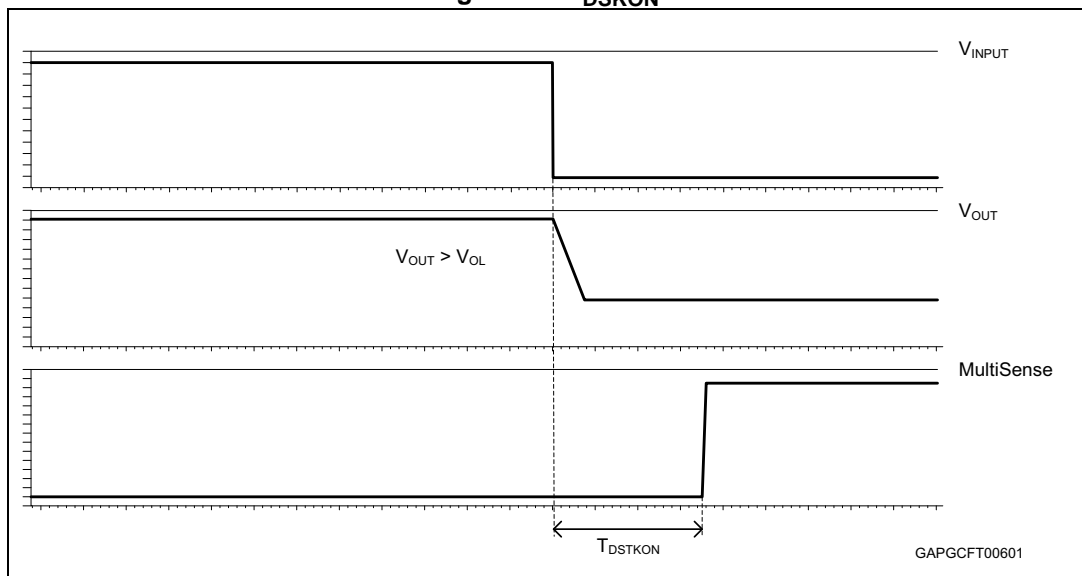


Figure 38. T_{DSTKON}



2.5.1 Truth tables

Table 15. Truth table

Mode	Conditions	IN _x	FR	SEn	SEL _x	OUT _x	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T _j < 150°C	L	X	Refer to Table 16		L	Refer to Table 16	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off
Overload	Overload or short to GND causing: T _j > T _{TSD} or ΔT _j > ΔT _{j_SD}	L	X	Refer to Table 16		L	Refer to Table 16	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off
Under-voltage	V _{CC} < V _{USD} (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising)
OFF-state diagnostics	Short to V _{CC}	L	X	Refer to Table 16		H	Refer to Table 16	
	Open load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn off	L	X	Refer to Table 16		< 0V	Refer to Table 16	

Table 16. MultiSense multiplexer addressing

SEn	SEL ₂	SEL ₁	SEL ₀	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag. ⁽¹⁾	Negative output
L	X	X	X		Hi-Z			
H	L	L	L	Channel 0 diagnostic	I _{SENSE} = 1/K * I _{OUT0}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	L	L	H	Channel 1 diagnostic	I _{SENSE} = 1/K * I _{OUT1}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	L	H	L	Channel 2 diagnostic	I _{SENSE} = 1/K * I _{OUT2}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	L	H	H	Channel 3 diagnostic	I _{SENSE} = 1/K * I _{OUT3}	V _{SENSE} = V _{SENSEH}	V _{SENSE} = V _{SENSEH}	Hi-Z
H	H	L	L	T _{CHIP} Sense	V _{SENSE} = V _{SENSE_TC}			
H	H	L	H	V _{CC} Sense	V _{SENSE} = V _{SENSE_VCC}			



Table 16. MultiSense multiplexer addressing (continued)

SEn	SEL ₂	SEL ₁	SEL ₀	MUX channel	MultiSense output			
					Normal mode	Overload	OFF-state diag. ⁽¹⁾	Negative output
H	H	H	L	T _{CHIP} Sense	V _{SENSE} = V _{SENSE_TC}			
H	H	H	H	V _{CC} Sense	V _{SENSE} = V _{SENSE_VCC}			

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
 Example 1: FR = 1; IN₀ = 0; OUT₀ = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0
 Example 2: FR = 1; IN₀ = 0; OUT₀ = latched, V_{OUT0} > V_{OL}; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

Table 17. Bulb/LED Mode Configuration

LED ₁	LED ₀	Configuration	
		Channel 1	Channel 0
L	L	Bulb	Bulb
L	H	Bulb	LED
H	L	LED	Bulb
H	H	LED	LED

2.5.2 Immunity to electrical transient disturbances on V_{CC} (ISO 7637-2)

Table 18. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 19. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽¹⁾	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 20. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD} . According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (see [Table 7](#), FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see [Table 7](#)), allowing the inductor energy to be dissipated without damaging the device.

The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 21](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 21. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10 Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50 μ s, 2 Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽²⁾	IV	-7V	1 pulse			100ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		40V	5 pulse	1 min		400ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -150 \text{ V}$; $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega.$$

Recommended values: $R_{prot} = 15 \text{ k}\Omega$

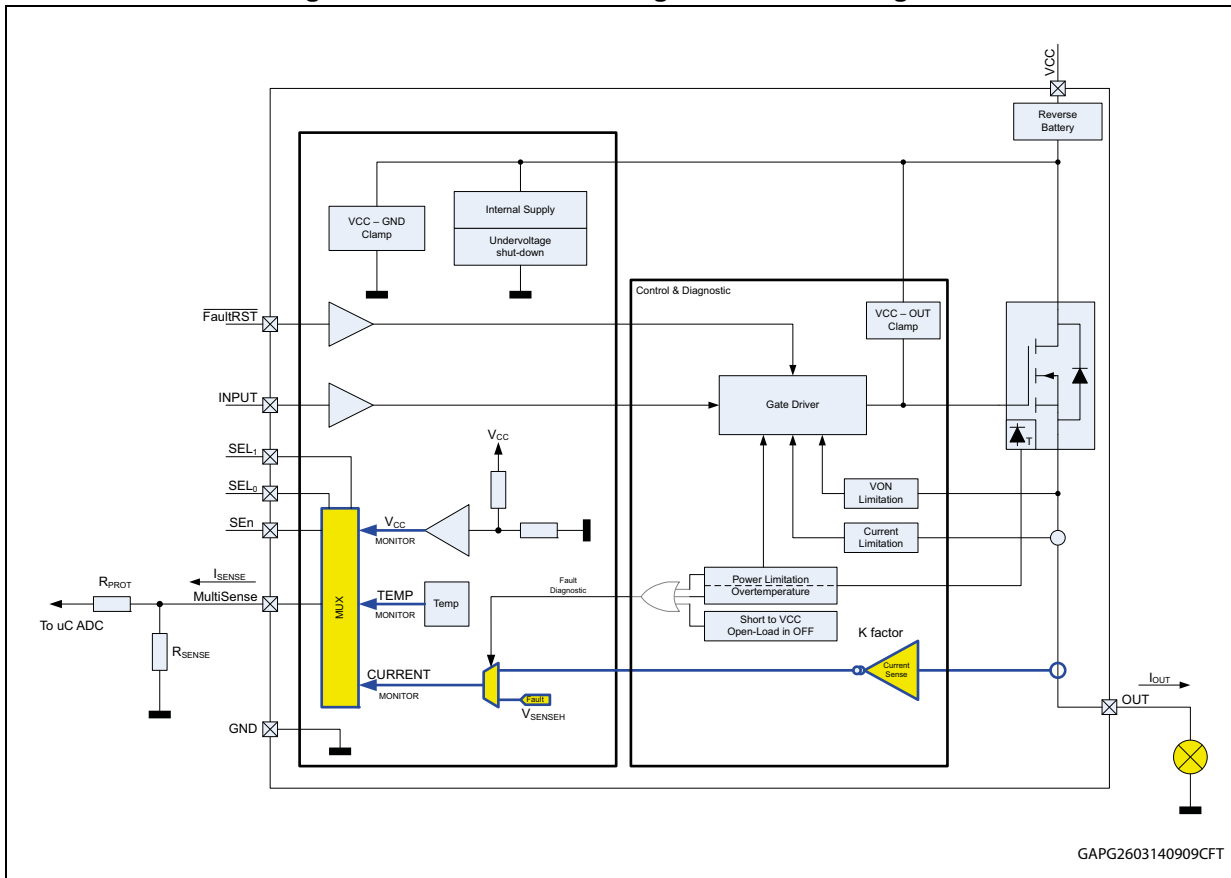
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (Multisense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage proportional to V_{CC}
- T_{CASE} : voltage proportional to chip temperature

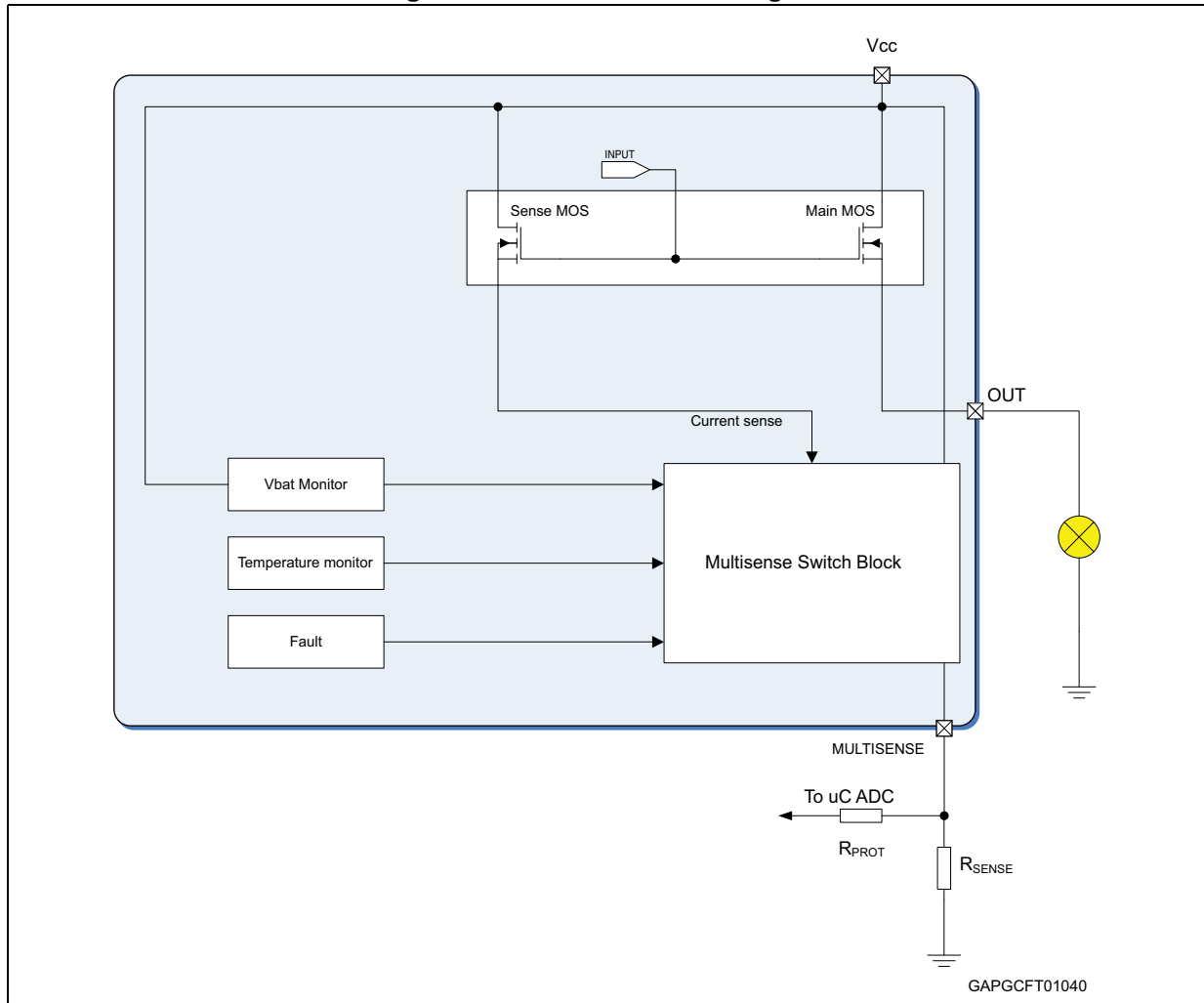
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEN pins, according to the address map in [Table 16](#).

Figure 41. Multisense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 42. Multisense block diagram



Current monitor

When current mode is selected in the Multisense, this output is capable to provide:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by Multisense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from Multisense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represent the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the Multisense pin which is switched to a “current limited” voltage source, V_{SENSEH} (see [Table 8](#)).

In any case, the current sourced by the Multisense in this condition is limited to I_{SENSEH} (see [Table 8](#)).

Figure 43. Analogue HSD – open-load detection in off-state

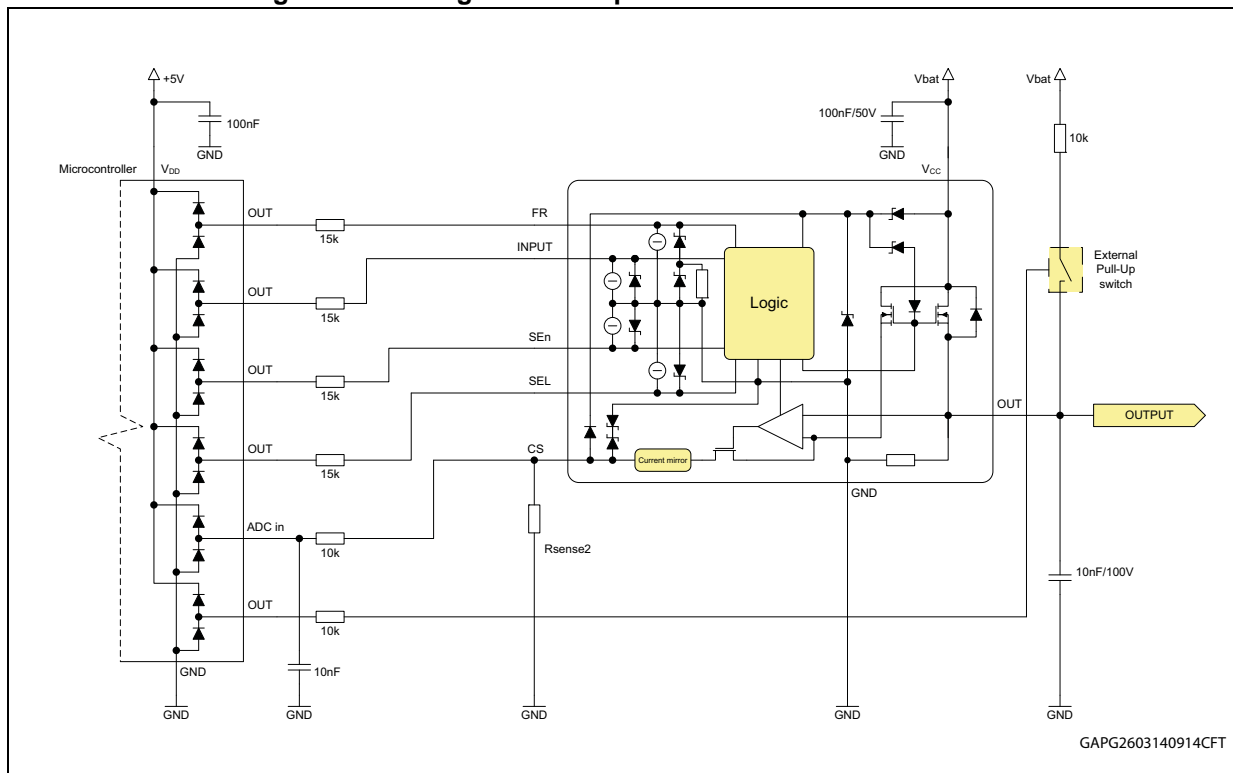


Figure 44. Open-load / short to V_{CC} condition

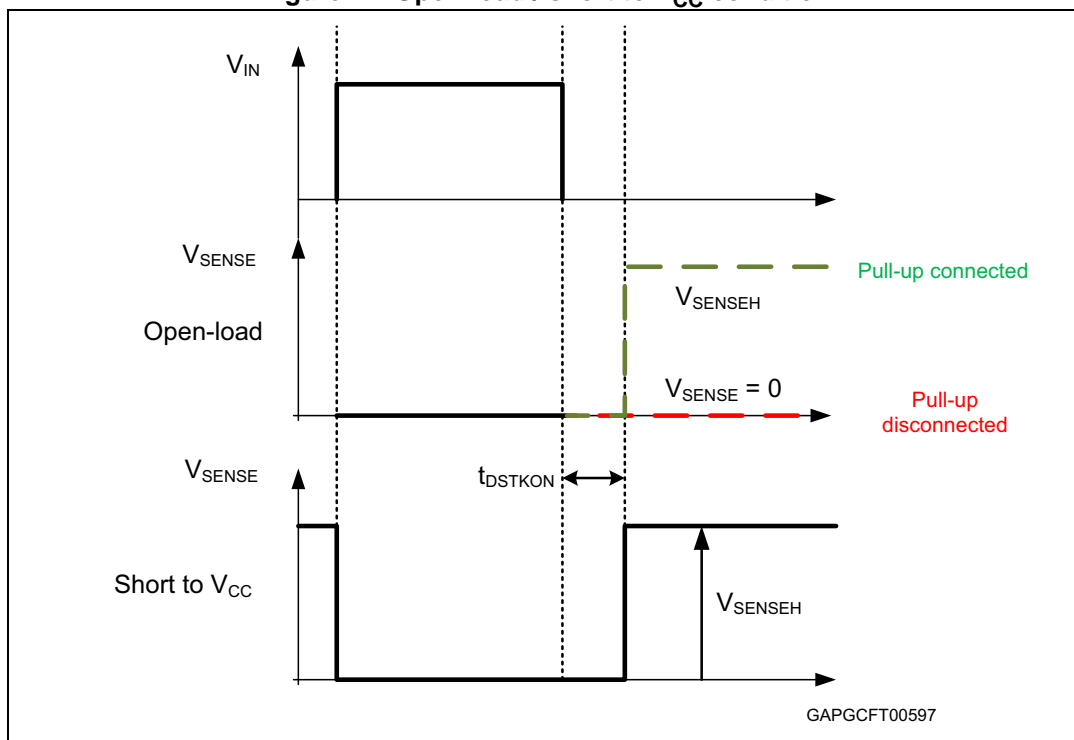


Table 22. MultiSense pin levels in off-state

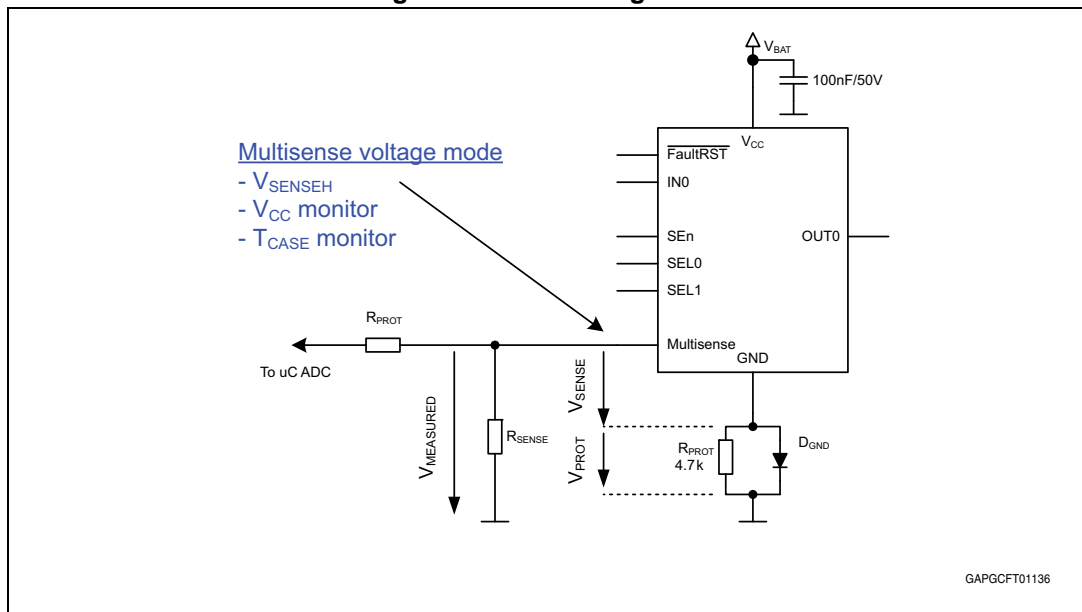
Condition	Output	MultiSense	SEn
Open-load	V _{OUT} > V _{OL}	Hi-Z	L
		V _{SENSEH}	H
Open-load	V _{OUT} < V _{OL}	Hi-Z	L
		0	H
Short to V _{CC}	V _{OUT} > V _{OL}	Hi-Z	L
		V _{SENSEH}	H
Nominal	V _{OUT} < V _{OL}	Hi-Z	L
		0	H

4.4.2 T_{CASE} and V_{CC} monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because of a voltage shift is generated between device GND and the microcontroller input GND reference.

Figure 45 shows link between V_{MEASURED} and real V_{SENSE} signal.

Figure 45. GND voltage shift



V_{CC} monitor

Battery monitoring channel provides $V_{SENSE} = V_{CC} / 4$.

Case temperature monitor

Case temperature monitor is capable to provide information about actual device temperature. Since diode is used for temperature sensing, following equation describe link between temperature and output V_{SENSE} level:

$$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$$

where $dV_{SENSE_TC} / dT \sim$ typically -5.5 mV/K (for temperature range $(-40^\circ\text{C}$ to $+150^\circ\text{C})$).

4.4.3 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

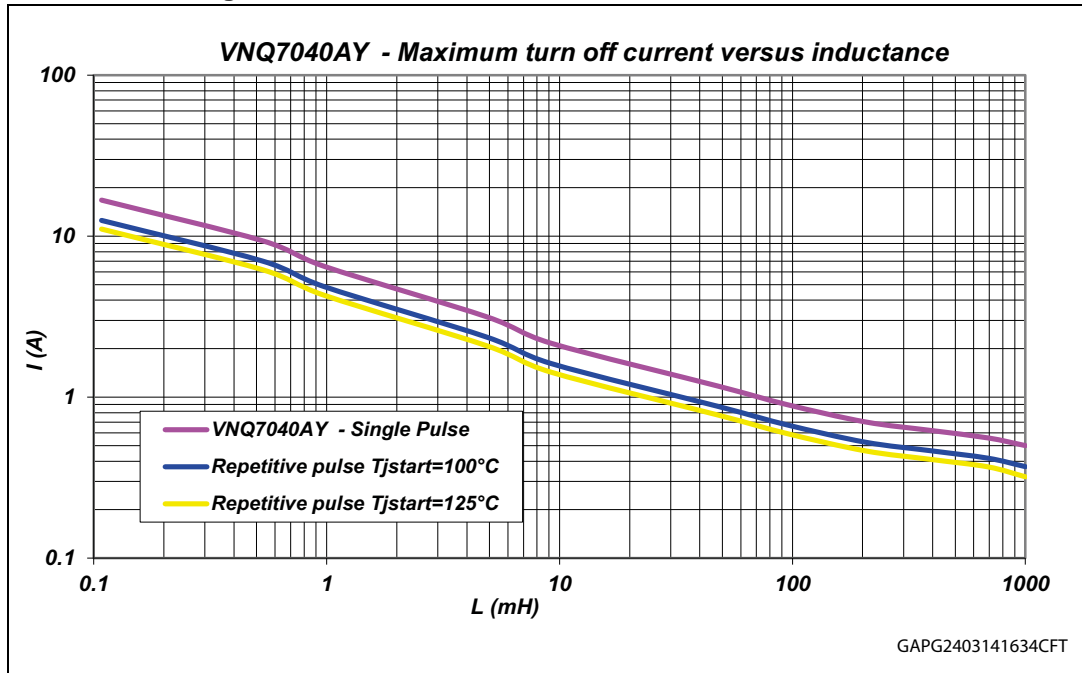
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with to following equation:

Equation 2

$$R_{PU} < \frac{V_{PU}^{-4}}{I_{L(off2)min @ 4V}}$$

4.5 Maximum demagnetization energy ($V_{CC} = 16 V$)

Figure 46. Maximum turn off current versus inductance



5 Package and PCB thermal data

5.1 PowerSSO-36 thermal data

Figure 47. PowerSSO-36 PC board

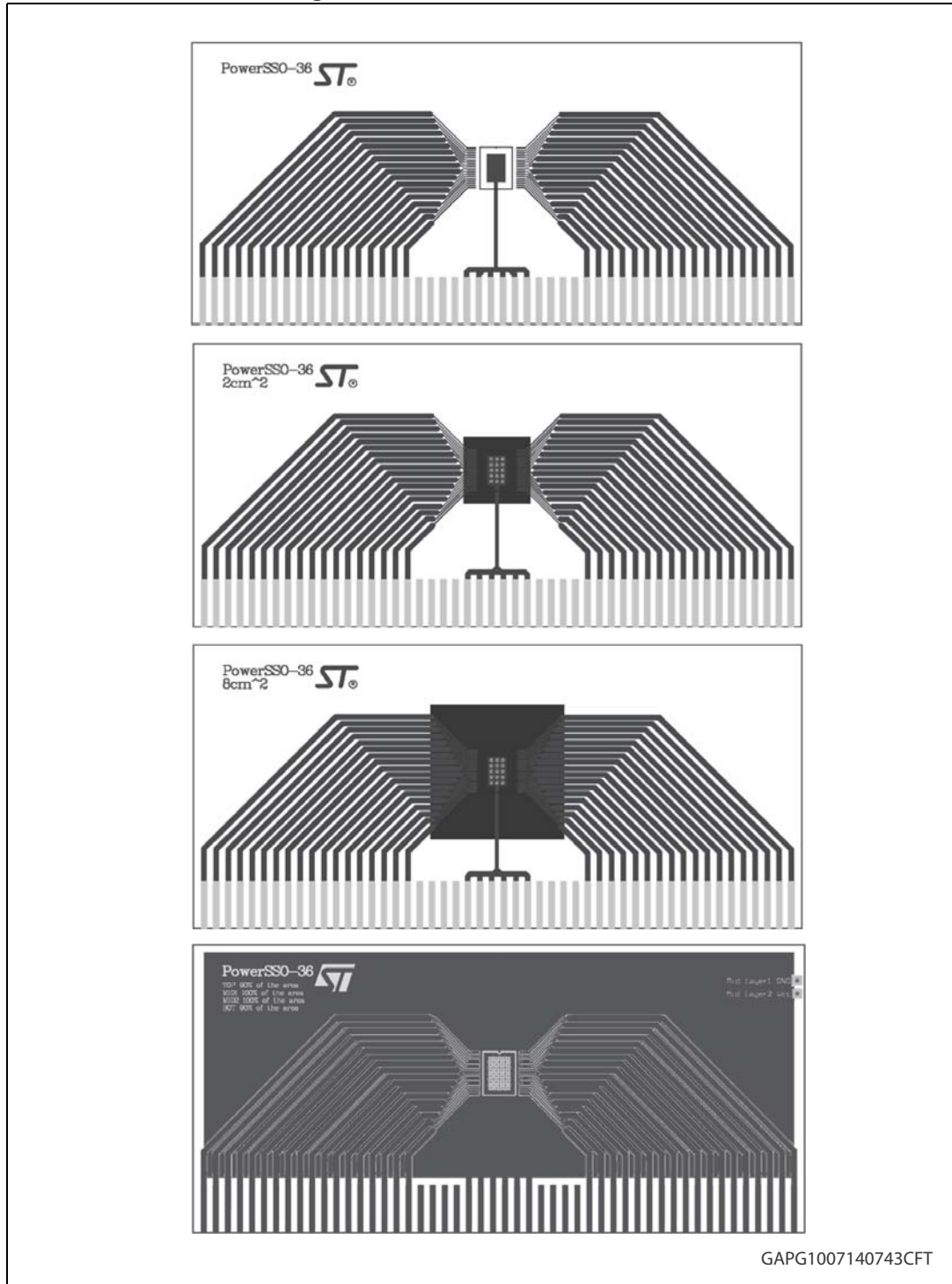


Table 23. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Cu thickness (outer layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension	4.1 mm x 6.5 mm

Figure 48. Rthj-amb vs PCB copper area in open box free air condition

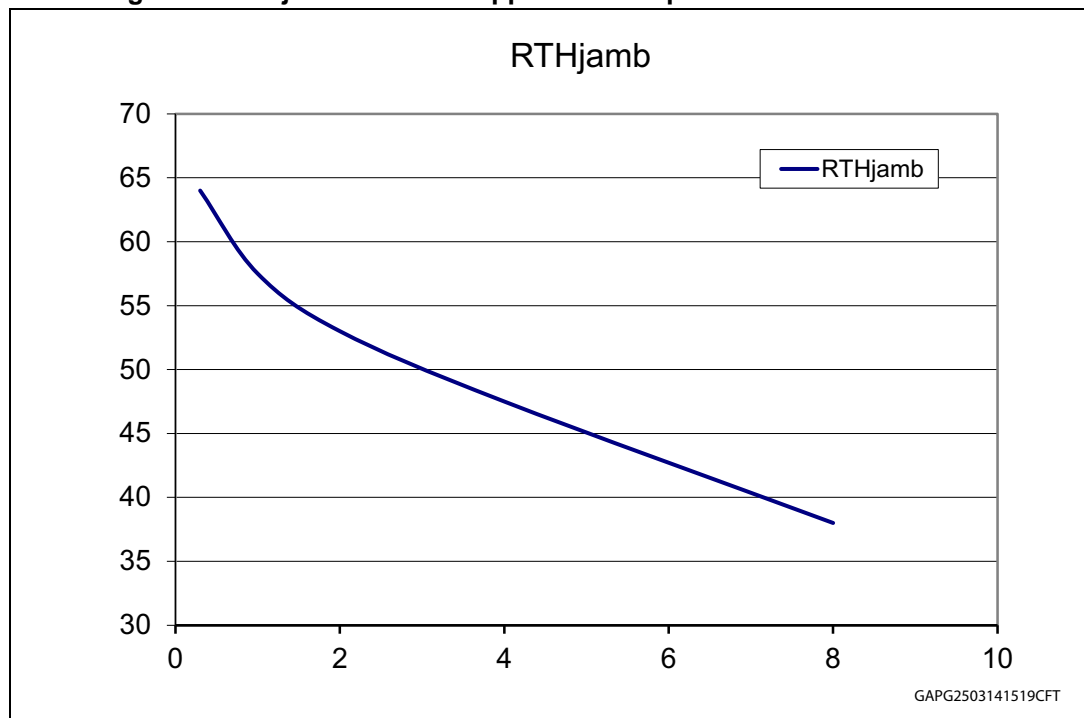


Figure 49. PowerSSO-36 thermal impedance junction ambient

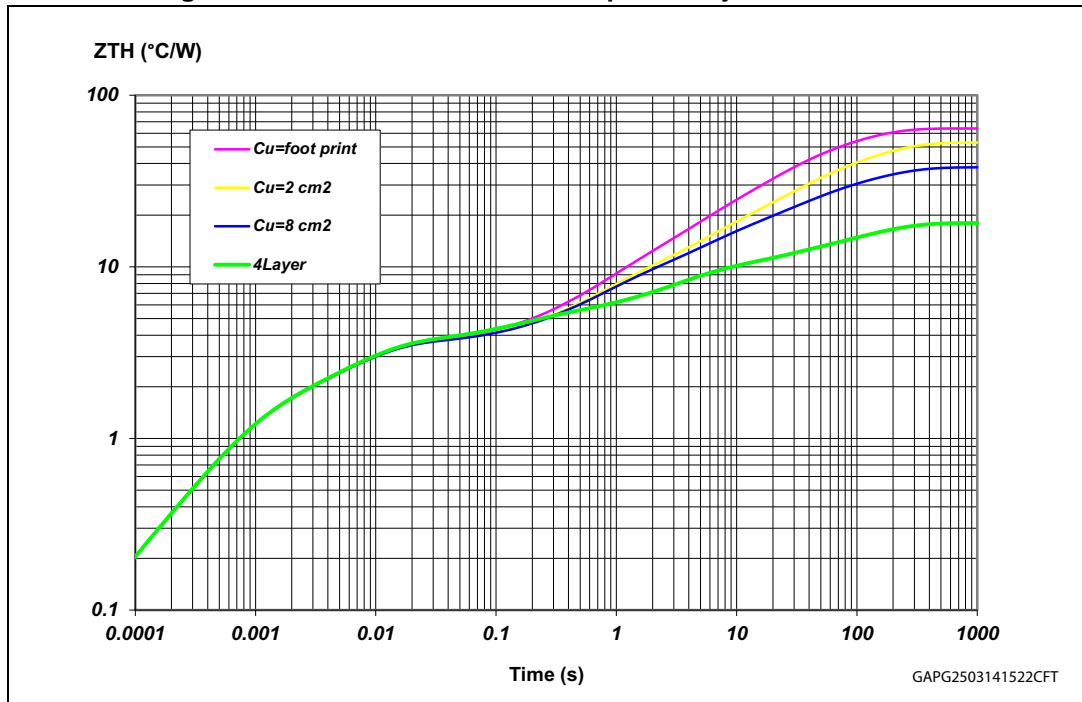


Figure 50. Thermal fitting model of a HSD in PowerSSO-36

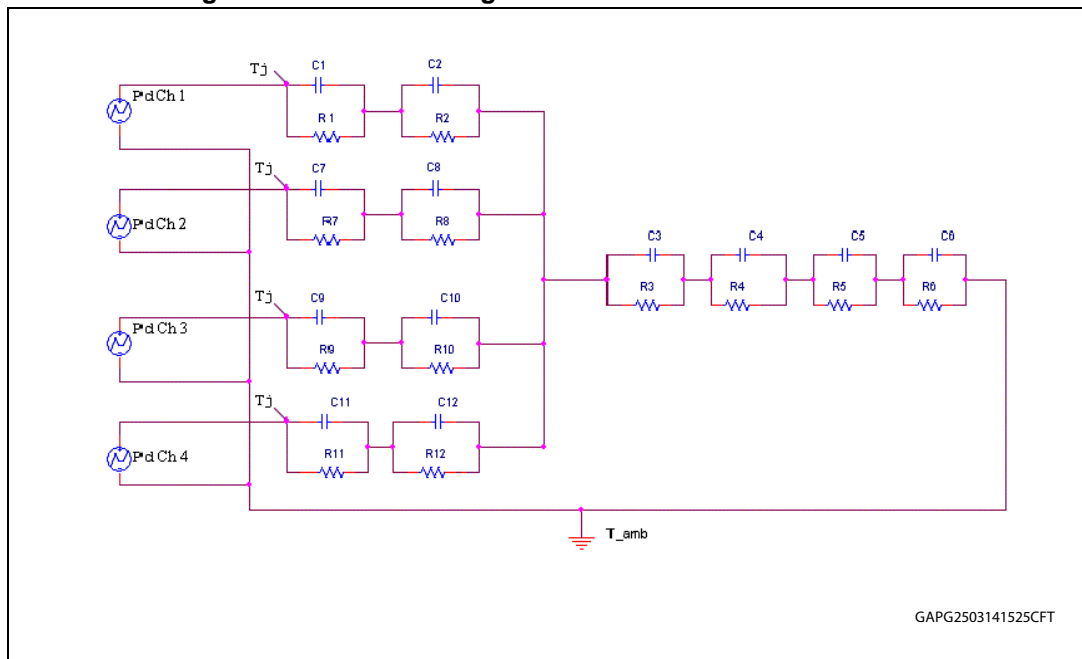


Table 24. Thermal parameters

Area/island (cm ²)	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	1.2			
R2 = R8 = R10 = R12 (°C/W)	2.3			
R3 (°C/W)	3.5	3.5	3.5	3.5
R4 (°C/W)	7	6	6	4
R5 (°C/W)	20	14	10	2
R6 (°C/W)	30	26	15	7
C1 = C7 = C9 = C11 (W·s/°C)	0.0006			
C2 = C8 = C10 = C12 (W·s/°C)	0.003			
C3 (W·s/°C)	0.02	0.02	0.02	0.01
C4 (W·s/°C)	0.5	0.8	0.8	0.8
C5 (W·s/°C)	1	2	3	10
C6 (W·s/°C)	3	5	9	18

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-36 mechanical data

Figure 51. PowerSSO-36 package dimensions

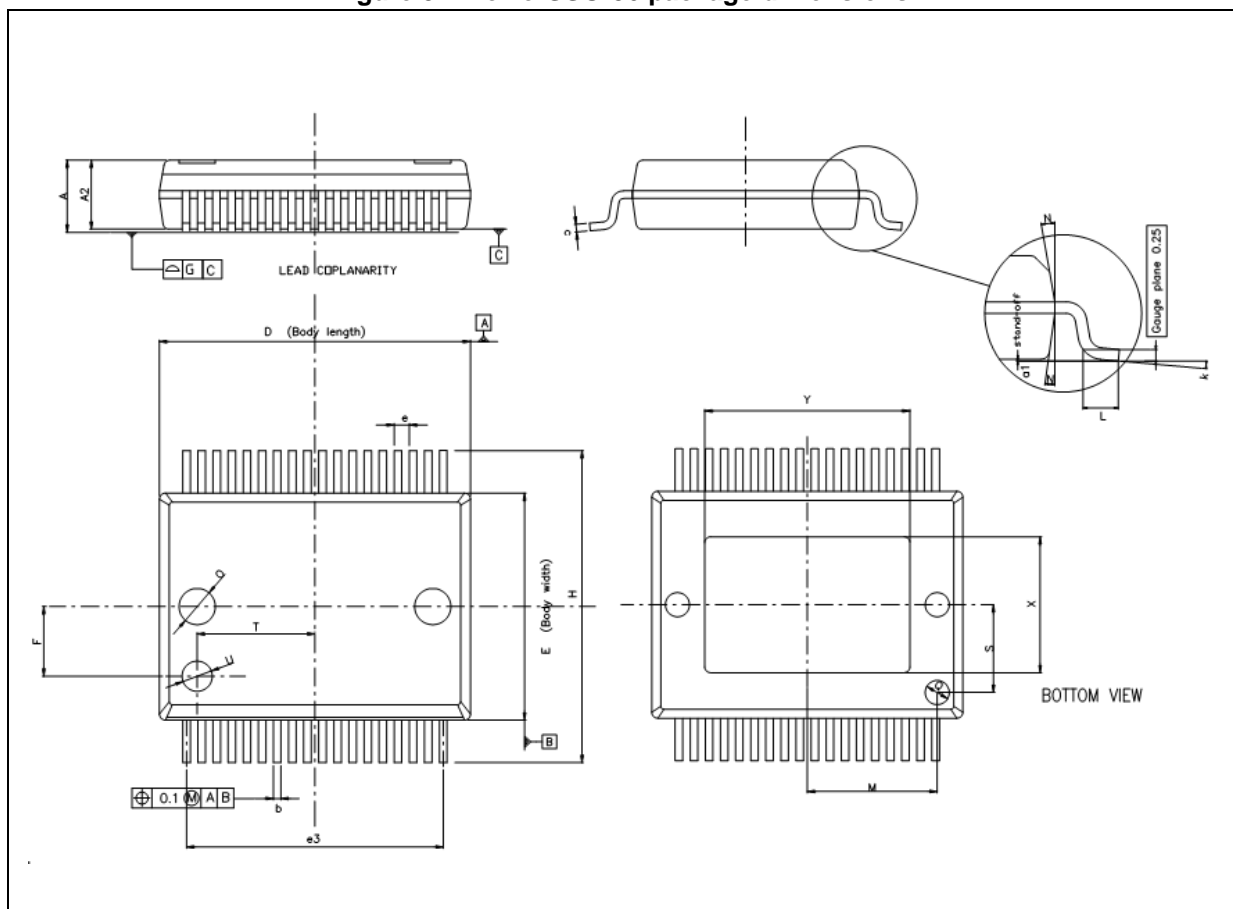


Table 25. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1.0	-
X ⁽¹⁾	4.3	-	5.2
Y ⁽¹⁾	6.9	-	7.5

1. Corresponding to internal variation C.

6.3 Packing information

Figure 52. PowerSSO-36 tube shipment (no suffix)

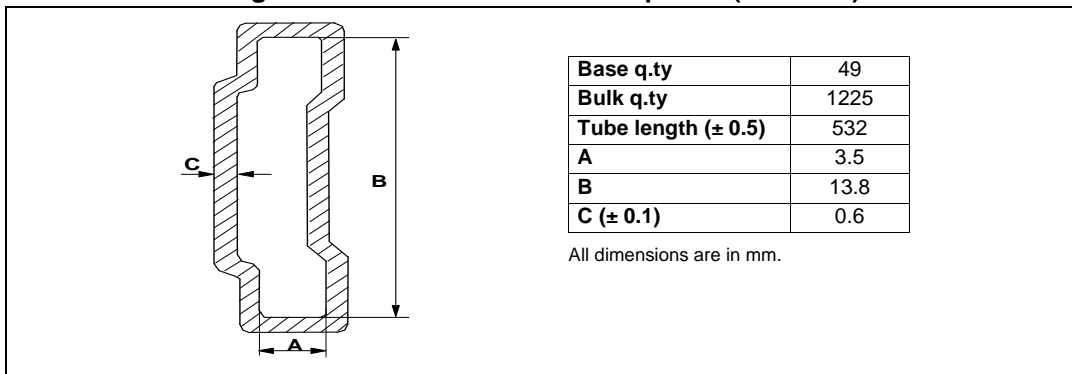
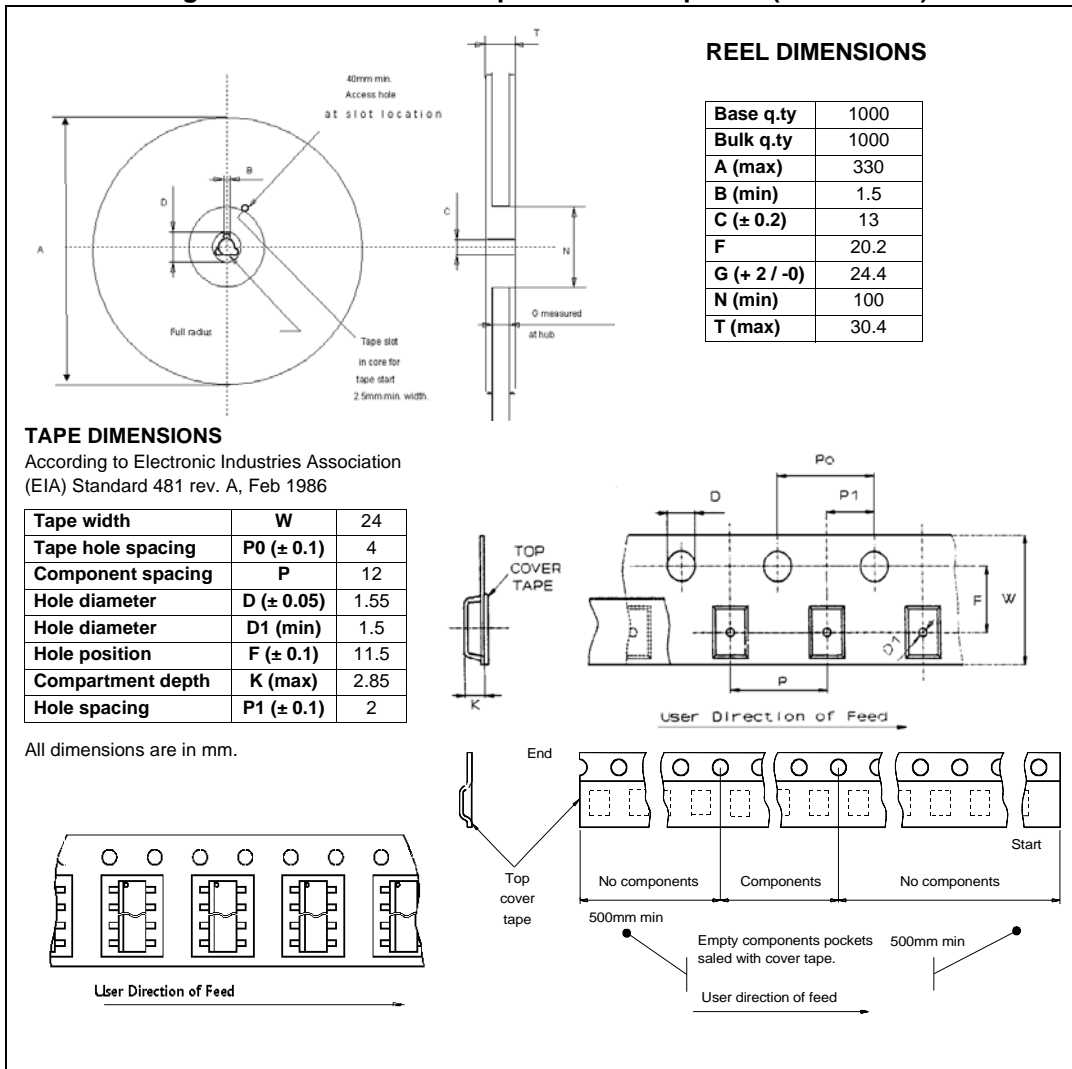


Figure 53. PowerSSO-36 tape and reel shipment (suffix "TR")



7 Order codes

Table 26. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VNQ7040AY-E	VNQ7040AYTR-E

8 Revision history

Table 27. Document revision history

Date	Revision	Changes
14-Nov-2011	1	Initial release.
14-Feb-2013	2	Updated Figure 2: Configuration diagram (top view) Table 1: Pin functions : – GND: updated function description
20-Mar-2013	3	Updated Features list Updated Table 1: Pin functions and Table 3: Absolute maximum ratings : – V_{CC} , $-V_{CC}$, V_{FR} , $-I_{OUT_0,1}$, $-I_{OUT_2,3}$: updated value – V_{CCPK} , I_{SENSE} , V_{ESD} : updated parameter and value – V_{CCJS} : added row – $-V_{SENSE}$: removed row Updated Table 4: Thermal data Table 5: Power section : – $V_{USDRreset}$, $I_{GND(ON)}$: added row – t_{D_STBY} : updated test conditions and value – V_{clamp} , I_{STBY} , $I_{S(ON)}$, $I_{L(off)}$: updated test conditions row Table 7: Protections ($7 V < V_{CC} < 18 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) : – V_{DEMAG} , T_{HYST} : updated value – t_{LATCH_RST} : updated test conditions and values Table 8: MultiSense ($7 V < V_{CC} < 18 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) : – V_{SENSE_CL} , V_{OL} , t_{STKON} , t_{D_VOL} , $t_{DSSENSE3H}$, $t_{DSSENSE3L}$, $t_{DSSENSE4H}$, $t_{DSSENSE4L}$, t_{D_XtoY} , t_{D_CStoTC} , t_{D_TCtoCS} , $t_{D_CStoVCC}$, $t_{D_VCCtoCS}$, $t_{D_TCtoVCC}$, $t_{D_VCCtoTC}$, $t_{D_CStoVSENSEH}$: updated test conditions – I_{SENSE0} , $I_{L(off2)}$, V_{SENSE_TC} , V_{SENSE_VCC} , V_{SENSEH} : updated test conditions and values – V_{OUT_MSD} , V_{SENSE_SAT} , I_{SENSE_SAT} , $I_{OUT_SAT_BULB}$, $I_{OUT_SAT_LED}$, $t_{D_OL_V}$: added rows – I_{SENSEH} : updated value Table 9: Power section in Bulb Mode ($7 V < V_{CC} < 28 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified) : – $R_{ON_0,1,2,3_BULB}$: updated test conditions and values – $R_{ON_REV_0,1,2,3}$: updated value Updated Table 10: Switching in Bulb Mode ($V_{CC} = 13 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified) , Table 11: MultiSense in Bulb Mode ($7 V < V_{CC} < 18 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) , Table 12: Switching in LED Mode ($V_{CC} = 13 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified) and Table 14: MultiSense in LED Mode ($7 V < V_{CC} < 18 V$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$) Removed Figure: Switching times and Figure: Pulse skew Added Figure 35: Switching times and Pulse skew Updated Figure 36: MultiSense timings (current sense mode) and Figure 37: Multisense timings (chip temperature and VCC sense mode)

Table 27. Document revision history (continued)

Date	Revision	Changes
20-Mar-2013	3 (cont'd)	Added <i>Figure 38: T_{DSKON}</i> <i>Table 15: Truth table:</i> – Overload: updated conditions Updated <i>Table 16: MultiSense multiplexer addressing</i> Removed <i>Section: Waveforms</i>
22-Jul-2013	4	<i>Table 10: Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified):</i> – $t_{SKEW_0,1,2,3}$: updated values Updated <i>Table 11: MultiSense in Bulb Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)</i> <i>Table 12: Switching in LED Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified):</i> – $t_{SKEW_0,1_LED}$: updated values Updated <i>Table 14: MultiSense in LED Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$)</i>
18-Sep-2013	5	Updated disclaimer.
11-Feb-2014	6	Updated <i>Table 10: Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)</i> and <i>Table 12: Switching in LED Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)</i>
19-Jun-2014	7	<i>Table 3: Absolute maximum ratings:</i> – E_{MAX} : updated value <i>Table 4: Thermal data</i> Added <i>Figure 4: Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}</i> and <i>Figure 5: Bulb Mode - current sense precision vs. I_{OUT}</i> Added <i>Section 2.4: Electrical characteristics curves - Bulb Mode</i> Added <i>Figure 26: LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}</i> and <i>Figure 27: LED Mode - current sense precision vs. I_{OUT}</i> Added <i>Section 2.5: Electrical characteristics curves - LED mode</i> Removed <i>Section: Immunity to electrical transient disturbances on VCC (ISO 7637-2)</i> Added <i>Chapter 3: Protections</i> , <i>Chapter 4: Application information</i> and <i>Chapter 5: Package and PCB thermal data</i>
30-Sep-2014	8	Updated <i>Chapter 5: Package and PCB thermal data</i>

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