



**THE DATASHEET OF
TLV2623IDGSR**

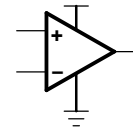


FAMILY OF LOW-POWER WIDE BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS WITH SHUTDOWN

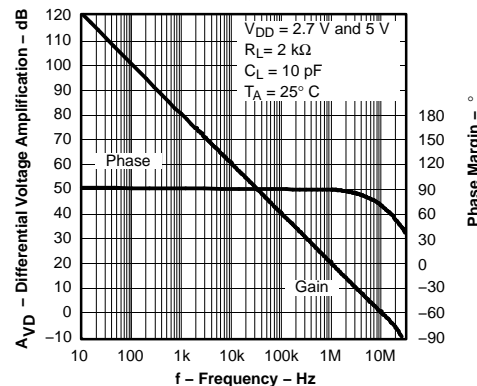
FEATURES

- CMOS Rail-To-Rail Output
- V_{ICR} Includes Positive Rail
- Wide Bandwidth . . . 11 MHz
- Slew Rate . . . 10 V/ μ s
- Supply Current . . . 800 μ A/Channel
- Input Noise Voltage . . . 27 nV/ $\sqrt{\text{Hz}}$
- Ultralow Power-Down Mode:
 $I_{DD(\text{SHDN})} = 4 \mu\text{A/Channel}$
- Supply Voltage Range . . . 2.7 V to 5.5 V
- Specified Temperature Range:
-40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging:
5 or 6 Pin SOT-23 (TLV2620/1)
8 or 10 Pin MSOP (TLV2622/3)
- Universal Opamp EVM (See SLOU060 for More Information)

Operational Amplifier



DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
vs
FREQUENCY



DESCRIPTION

The TLV262x single supply operational amplifiers provide rail-to-rail output with an input range that includes the positive rail. The TLV262x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range (-40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV262x also provides 11-MHz bandwidth from only 800 μ A of supply current. The maximum recommended supply voltage is 5.5 V, which, when coupled with a 2.7-V minimum, allows the devices to be operated from lithium ion cells. The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. The positive input range allows it to directly interface to positive rail referred systems. All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power micro-controllers available today including TI's MSP430.

AMPLIFIER SELECTION TABLE

| DEVICE | V_{DD} [V] | $I_{DD/\text{ch}}$ [μ A] | V_{IO} [μ V] | I_{IB} [μ A] | V_{ICR} [V] | GBW [MHz] | SLEW RATE [V/ μ s] | V_n , 1 kHz [nV/ $\sqrt{\text{Hz}}$] | I_o [mA] | SHUT-DOWN |
|---------|--------------|-------------------------------|---------------------|---------------------|------------------------|-----------|------------------------|---|------------|-----------|
| TLV262x | 2.7-5.5 | 750 | 250 | 1 | 1 V to $V_{DD} + 0.2$ | 11 | 10 | 27 | 28 | Y |
| TLV263x | 2.7-5.5 | 750 | 250 | 1 | GND to $V_{DD} - 0.8$ | 10 | 9 | 27 | 28 | Y |
| TLV278x | 1.8-3.6 | 650 | 250 | 2.5 | -0.2 to $V_{DD} + 0.2$ | 8 | 5 | 9 | 10 | Y |
| TLC07x | 4.5 - 16 | 1900 | 60 | 1.5 | 0.5 to $V_{DD} - 0.8$ | 10 | 19 | 7 | 55 | Y |
| TLC08x | 4.5 - 16 | 1900 | 60 | 3 | GND to $V_{DD} - 1$ | 10 | 19 | 8.5 | 55 | Y |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TLV2620 AND TLV2621 AVAILABLE OPTIONS⁽¹⁾

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | | | |
|----------------|-----------------------------|----------------------------------|----------------------------|--------------|------------------------|
| | | SMALL OUTLINE (D) ⁽²⁾ | SOT-23 | | PLASTIC DIP (P) |
| | | | (DBV) ⁽³⁾ | SYMBOL | |
| -40°C to 125°C | 3500 μV | TLV2620ID TLV2621ID | TLV2620IDBV TLV2621IDBV | VBAI VBBI | TLV2620IP TLV2621IP |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2620IDR).
 (3) The SOT23 package devices are only available taped and reeled. The **R** Suffix denotes quantities (3,000 pieces per reel). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g. TLV2620IDBVT).

TLV2622 AND TLV2623 AVAILABLE OPTIONS⁽¹⁾

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | | | | | | |
|----------------|-----------------------------|----------------------------------|----------------------|--------------|----------------------|--------------|-----------------|-----------------|
| | | SMALL OUTLINE ⁽²⁾ (D) | MSOP | | | | PLASTIC DIP (N) | PLASTIC DIP (P) |
| | | | (DGK) ⁽²⁾ | SYMBOL | (DGS) ⁽²⁾ | SYMBOL | | |
| -40°C to 125°C | 3500 μV | TLV2622ID TLV2623ID | TLV2622IDGK — | xxTIAKM — | — TLV2623IDGS | — xxTIALC | — TLV2623IN | TLV2622IP — |

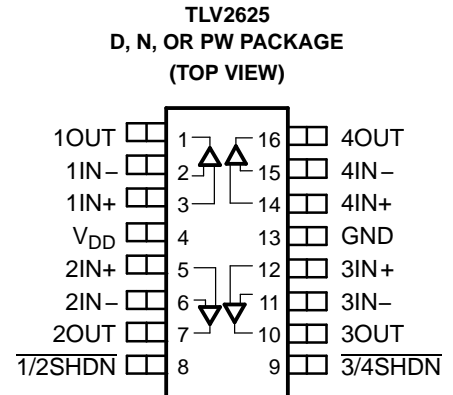
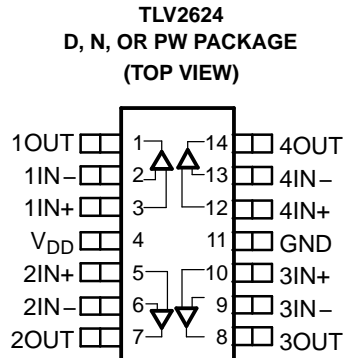
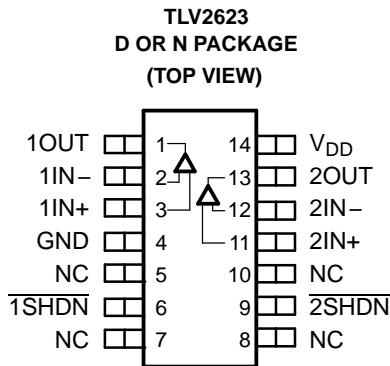
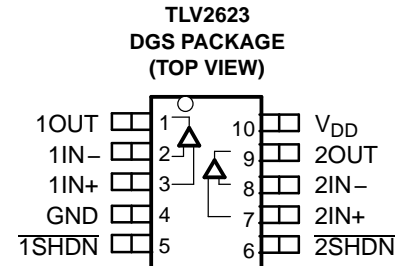
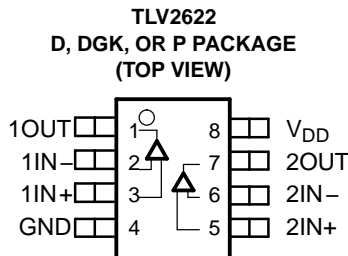
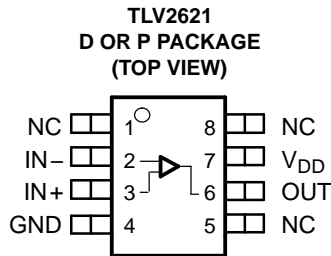
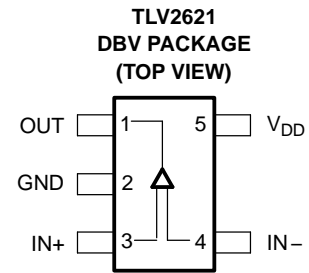
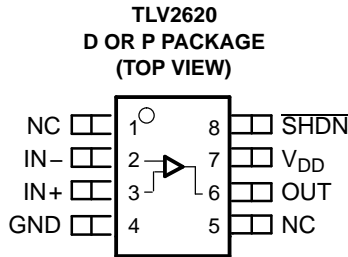
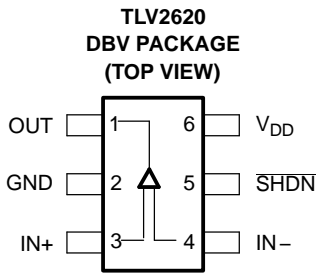
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 (2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2622IDR).

TLV2624 AND TLV2625 AVAILABLE OPTIONS⁽¹⁾

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | | |
|----------------|-----------------------------|----------------------------------|------------------------|--------------------------|
| | | SMALL OUTLINE (D) ⁽²⁾ | PLASTIC DIP (N) | TSSOP (PW) |
| -40°C to 125°C | 3500 μV | TLV2624ID TLV2625ID | TLV2624IN TLV2625IN | TLV2624IPW TLV2625IPW |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2624IDR).

TLV262X PACKAGE PINOUTS⁽¹⁾

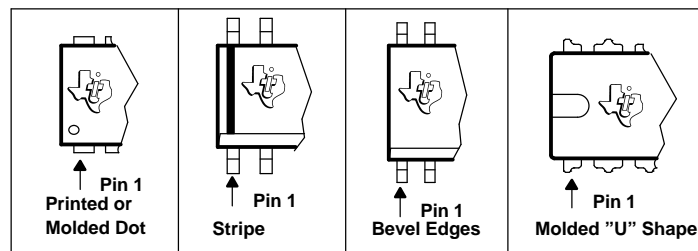


NC – No internal connection

$\overline{1/2SHDN}$ Pin (8) controls amplifiers 1 and 2.
 $\overline{3/4SHDN}$ Pin (9) controls amplifiers 3 and 4.

(1) SOT-23 may or may not be indicated.

TYPICAL PIN 1 INDICATORS



NOTE:

If there is not a Pin 1 indicator, turn device to enable reading the symbol from left to right. Pin 1 is at the lower left corner of the device.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | |
|-----------|--|------------------------------|
| V_{DD} | Supply voltage ⁽²⁾ | 6 V |
| V_{ID} | Differential input voltage | $\pm V_{DD}$ |
| V_I | Input voltage range ⁽²⁾ | +1 to $V_{DD} + 0.2$ V |
| I_I | Input current (any input) | ± 10 mA |
| I_O | Output current | ± 40 mA |
| | Continuous total power dissipation | See Dissipation Rating Table |
| T_A | Operating free-air temperature range: I-suffix | -40°C to 125°C |
| T_J | Maximum junction temperature | 150°C |
| T_{stg} | Storage temperature range | -65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|------------|-------------------------|-------------------------|---|---|
| D (8) | 38.3 | 176 | 710 mW | 142 mW |
| D (14) | 26.9 | 122.3 | 1022 mW | 204.4 mW |
| D (16) | 25.7 | 114.7 | 1090 mW | 218 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 77.1 mW |
| DBV (6) | 55 | 294.3 | 425 mW | 85 mW |
| DGK (8) | 54.2 | 259.9 | 481 mW | 96.1 mW |
| DGS (10) | 54.1 | 259.7 | 485 mW | 97 mW |
| N (14, 16) | 32 | 78 | 1600 mW | 320.5 mW |
| P (8) | 41 | 104 | 1200 mW | 240.4 mW |
| PW (14) | 29.3 | 173.6 | 720 mW | 144 mW |
| PW (16) | 28.7 | 161.4 | 774 mW | 154.9 mW |

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|-----------|--|---------------|------------|----------------|------|
| V_{DD} | Supply voltage | Single supply | 2.7 | 5.5 | V |
| | | Split supply | ± 1.35 | ± 2.75 | |
| V_{ICR} | Common-mode input voltage range | | 1 | $V_{DD} + 0.2$ | V |
| T_A | Operating free-air temperature | I-suffix | -40 | 125 | °C |
| | Shutdown on/off voltage level ⁽¹⁾ | V_{IL} | | 0.4 | V |
| | | V_{IH} | 2 | | |

- (1) Relative to GND.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD} = 2.7\text{ V}, 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT | |
|-------------------------------|---|--|--|-------------|----------|------|-----|------------------------------|--|
| DC PERFORMANCE | | | | | | | | | |
| V_{IO} | Input offset voltage | $V_{IC} = V_{DD}/2, V_O = V_{DD}/2,$ $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 250 | 3500 | | μV | |
| | | | | Full range | 4500 | | | | |
| α_{VIO} | Temperature coefficient of input offset voltage | | $V_{DD} = 2.7\text{ V}$ | 25°C | 3 | | | $\mu\text{V}/^\circ\text{C}$ | |
| | | | | Full range | | | | | |
| $CMRR$ | Common-mode rejection ratio | $V_{IC} = 1\text{ to }V_{DD},$ $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 77 | 98 | | dB | |
| | | | | Full range | 63 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 78 | 99 | | | |
| | | | | Full range | 75 | | | | |
| A_{VD} | Large-signal differential voltage amplification | $V_{DD} = 2.7\text{ V}, R_L = 2\text{ k}\Omega,$ $V_{O(PP)} = 1.7\text{ V}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 90 | 100 | | dB | |
| | | | | Full range | 82 | | | | |
| | | | $V_{DD} = 5\text{ V}, R_L = 2\text{ k}\Omega,$ $V_{O(PP)} = 4\text{ V}$ | 25°C | 95 | 100 | | | |
| | | | | Full range | 90 | | | | |
| INPUT CHARACTERISTICS | | | | | | | | | |
| I_{IO} | Input offset current | $V_{IC} = V_{DD}/2, V_O = V_{DD}/2,$ $R_S = 50\ \Omega$ | | 25°C | 2 | 50 | | pA | |
| | | | | Full Range | 100 | | | | |
| I_{IB} | Input bias current | | $V_{DD} = 2.7\text{ V}$ | 25°C | 2 | 50 | | | |
| | | | | Full Range | 200 | | | | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | 100 | | | G Ω | |
| $C_{i(c)}$ | Common-mode input capacitance | $f = 1\text{ kHz}$ | | 25°C | 8 | | | pF | |
| OUTPUT CHARACTERISTICS | | | | | | | | | |
| V_{OH} | High-level output voltage | $V_{IC} = V_{DD}/2,$ $I_{OH} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.6 | 2.67 | | V | |
| | | | | Full range | 2.55 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 4.95 | 4.98 | | | |
| | | | | Full range | 4.9 | | | | |
| | | $V_{IC} = V_{DD}/2,$ $I_{OH} = -10\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.3 | 2.43 | | | |
| | | | | Full range | 2.2 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 4.7 | 4.8 | | | |
| | | | | Full range | 4.6 | | | | |
| V_{OL} | Low-level output voltage | $V_{IC} = V_{DD}/2,$ $I_{OL} = 1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.03 | 0.1 | | V | |
| | | | | Full range | 0.15 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 0.025 | 0.05 | | | |
| | | | | Full range | 0.1 | | | | |
| | | $V_{IC} = V_{DD}/2,$ $I_{OL} = 10\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.26 | 0.4 | | | |
| | | | | Full range | 0.45 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 0.2 | 0.25 | | | |
| | | | | Full range | 0.35 | | | | |
| I_O | Output current | $V_{DD} = 2.7\text{ V},$ $V_O = 0.5\text{ V from rail}$ | Sourcing | 25°C | 14 | | | mA | |
| | | | Sinking | | 19 | | | | |
| | | | $V_{DD} = 5\text{ V},$ $V_O = 0.5\text{ V from rail}$ | | Sourcing | 28 | | | |
| | | | Sinking | | 28 | | | | |
| I_{OS} | Short-circuit output current | | $V_{DD} = 2.7\text{ V}$ | 25°C | 50 | | | mA | |
| | | | $V_{DD} = 5\text{ V}$ | | 95 | | | | |
| | | | $V_{DD} = 2.7\text{ V}$ | | 50 | | | | |
| | | | $V_{DD} = 5\text{ V}$ | | 95 | | | | |

(1) Full range is -40°C to 125°C for the I-suffix.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--|-----------------------------------|-------------|--------|------|------------------------------|------------------------|
| POWER SUPPLY | | | | | | | | |
| I_{DD} | Supply current (per channel) | $V_O = V_{DD}/2$, | $\overline{\text{SHDN}} = V_{DD}$ | 25°C | 800 | 1000 | | μA |
| | | | | Full range | | 1300 | | |
| PSRR | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD} = 2.7\text{ V}$ to 3.3 V , $V_{IC} = V_{DD}/2$ | No load | 25°C | 80 | 98 | | dB |
| | | | | Full range | 75 | | | |
| | | 25°C | | 75 | 90 | | | |
| | | Full range | | 70 | | | | |
| DYNAMIC PERFORMANCE | | | | | | | | |
| UGBW | Unity gain bandwidth | $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$ | | 25°C | | 11 | | MHz |
| SR+ | Positive slew rate at unity gain | $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$ | | 25°C | 3.5 | 4.5 | | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 2.7 | | | |
| | | | | 25°C | 5.4 | 7 | | |
| | | | | Full range | 3.4 | | | |
| SR- | Negative slew rate at unity gain | $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$ | | 25°C | 2.7 | 5 | | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 2.3 | | | |
| | | | | 25°C | 4.5 | 6 | | |
| | | | | Full range | 3.2 | | | |
| ϕ_m | Phase margin | $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$ | | 25°C | 63° | | | dB |
| | Gain margin | | | | 8 | | | |
| NOISE/DISTORTION PERFORMANCE | | | | | | | | |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)} = V_{DD}/2$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | 0.002% | | | |
| | | | $A_V = 10$ | | 0.019% | | | |
| | | | $A_V = 100$ | | 0.095% | | | |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ $f = 10\text{ kHz}$ | | 25°C | 53 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | | | | 27 | | | |
| I_n | Equivalent input noise current | $f = 1\text{ kHz}$ | | 25°C | 0.9 | | $\text{fA}/\sqrt{\text{Hz}}$ | |
| SHUTDOWN CHARACTERISTICS | | | | | | | | |
| $I_{DD(\text{SHDN})}$ | Supply current, per channel in shutdown mode (TLV2620, TLV2623, TLV2625) | $\overline{\text{SHDN}} = 0.4\text{ V}$ | | 25°C | 4 | 11 | | μA |
| | | | | Full range | | 13 | | |
| $t_{(\text{on})}$ | Amplifier turnon time ⁽²⁾ | $R_L = 2\text{ k}\Omega$ | | 25°C | 4.5 | | μs | |
| | | | | | 1.5 | | | |
| $t_{(\text{off})}$ | Amplifier turnoff time ⁽²⁾ | $R_L = 2\text{ k}\Omega$ | | 25°C | 200 | | ns | |

(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{\text{SHDN}}$ and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

| | | | FIGURE |
|----------------|--|------------------------------|---------------|
| V_{IO} | Input offset voltage | vs Common-mode input voltage | 1, 2 |
| CMRR | Common-mode rejection ratio | vs Frequency | 3 |
| V_{OH} | High-level output voltage | vs High-level output current | 4, 6 |
| V_{OL} | Low-level output voltage | vs Low-level output current | 5, 7 |
| I_{DD} | Supply current | vs Supply voltage | 8 |
| I_{DD} | Supply current | vs Free-air temperature | 9 |
| PSRR | Power supply rejection ratio | vs Frequency | 10 |
| A_{VD} | Differential voltage amplification & phase | vs Frequency | 11 |
| | Gain-bandwidth product | vs Free-air temperature | 12 |
| SR | Slew rate | vs Supply voltage | 13 |
| | | vs Free-air temperature | 14, 15 |
| ϕ_m | Phase margin | vs Load capacitance | 16 |
| V_n | Equivalent input noise voltage | vs Frequency | 17 |
| | Voltage-follower large-signal pulse response | | 18 |
| | Voltage-follower small-signal pulse response | | 19 |
| | Crosstalk | vs Frequency | 20 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Free-air temperature | 21 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Supply voltage | 22 |
| $I_{DD(SHDN)}$ | Shutdown supply current/output voltage | vs Time | 23 |

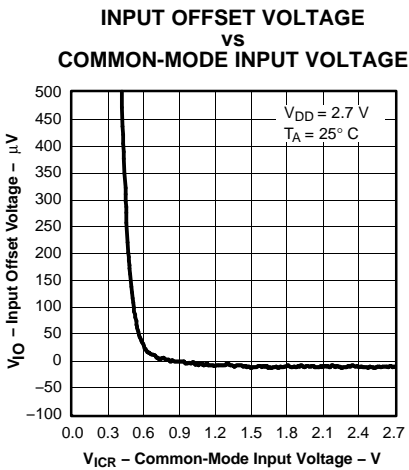


Figure 1.

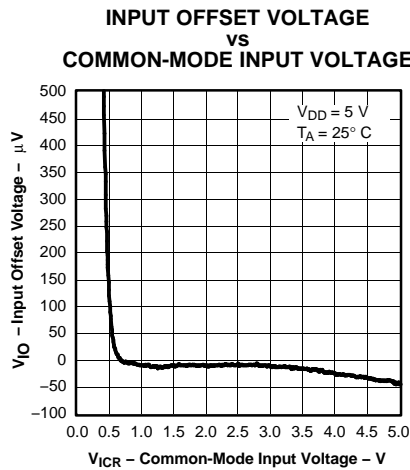


Figure 2.

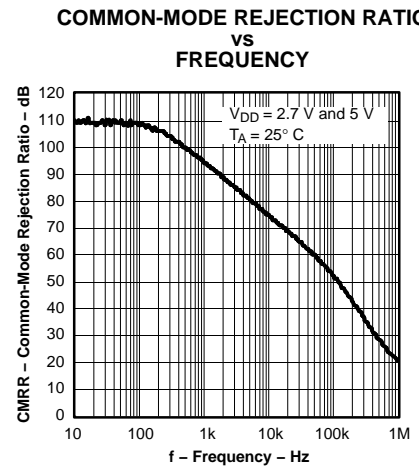


Figure 3.

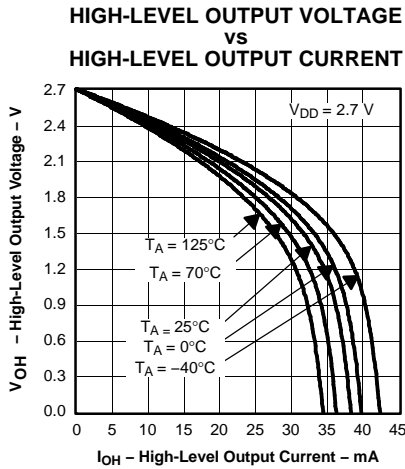


Figure 4.

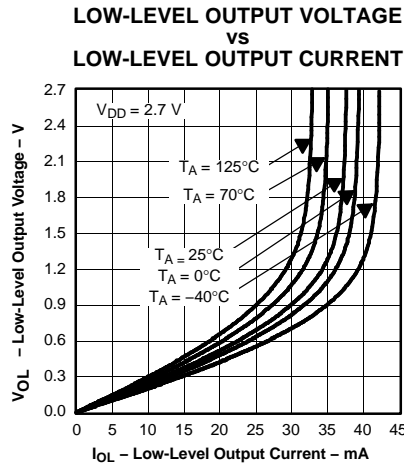


Figure 5.

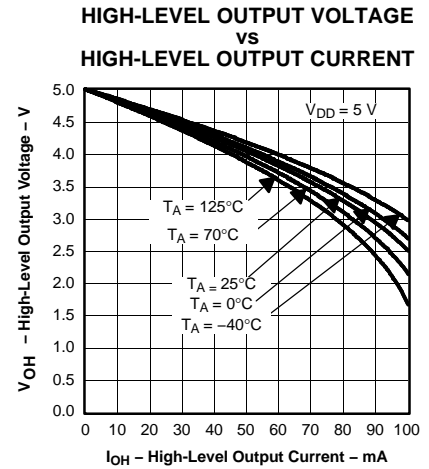


Figure 6.

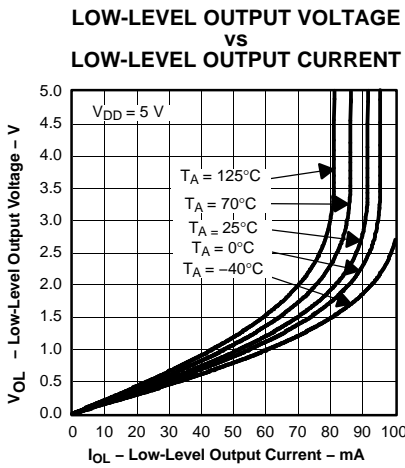


Figure 7.

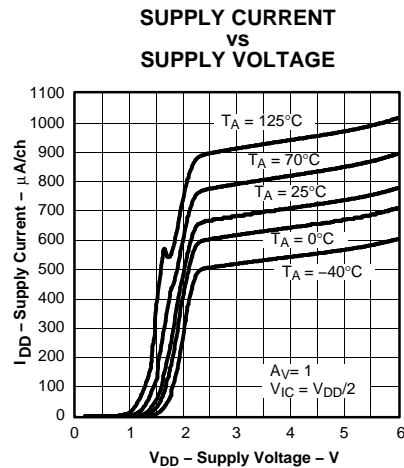


Figure 8.

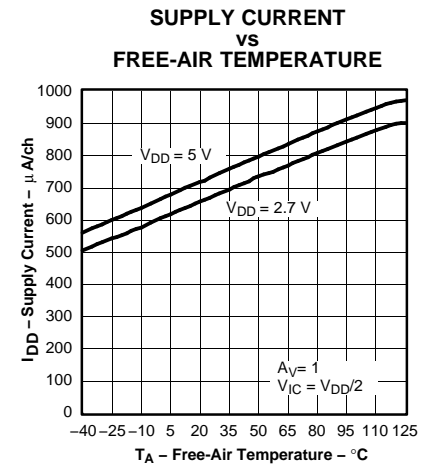


Figure 9.

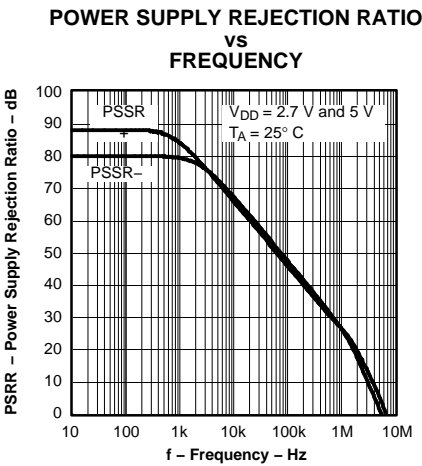


Figure 10.

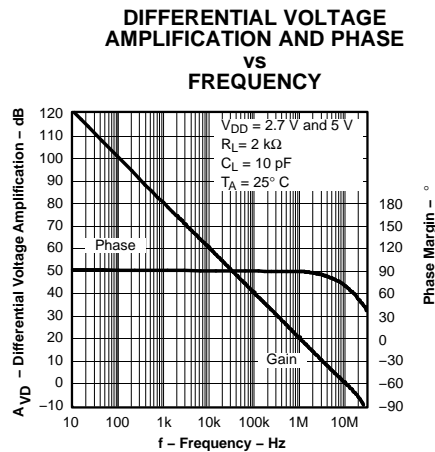


Figure 11.

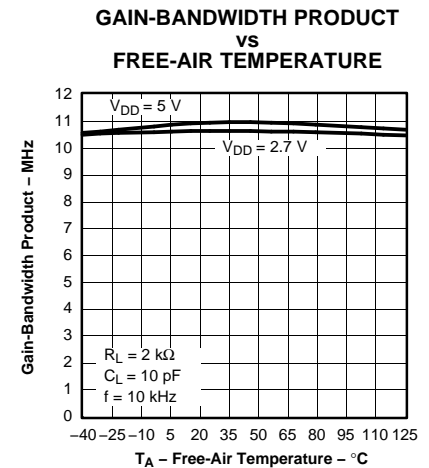


Figure 12.

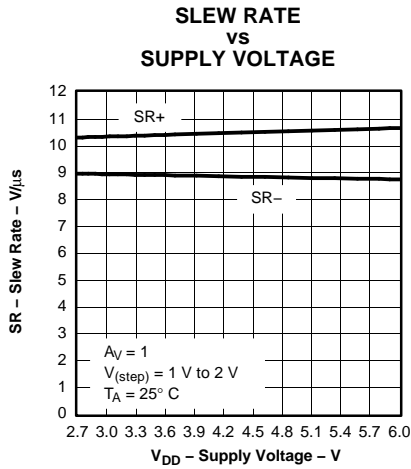


Figure 13.

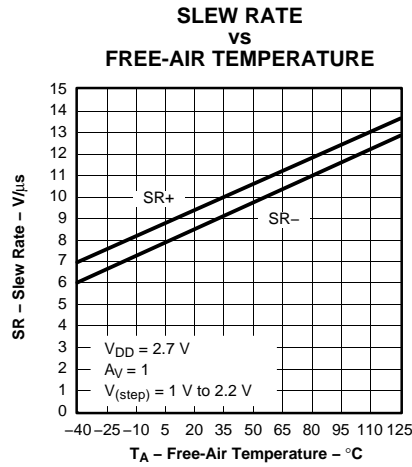


Figure 14.

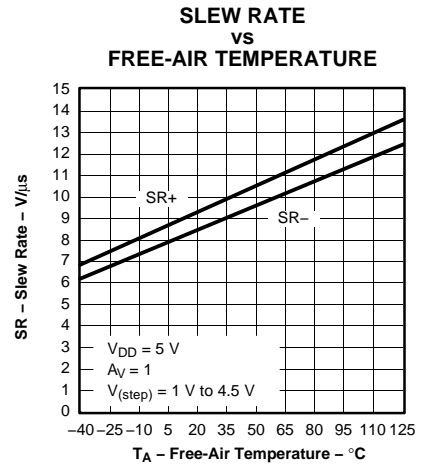


Figure 15.

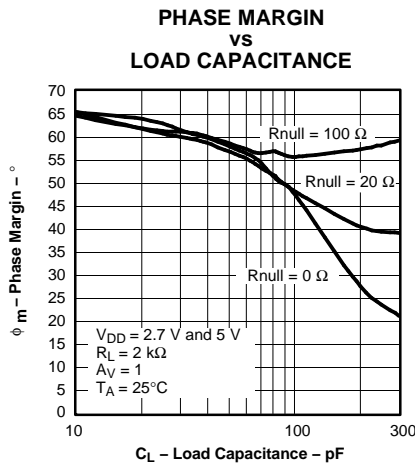


Figure 16.

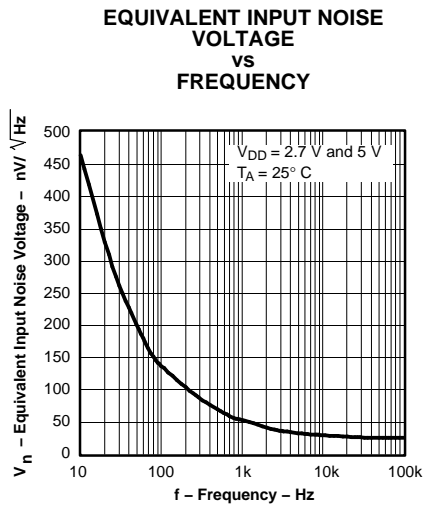


Figure 17.

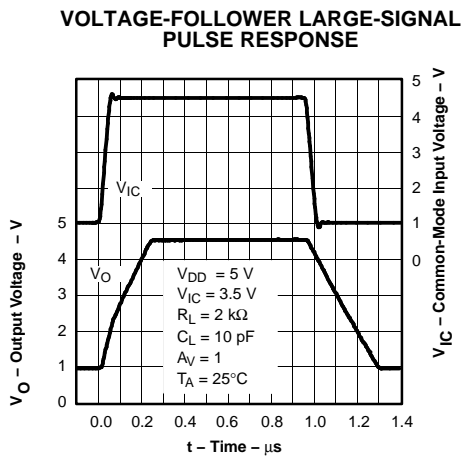


Figure 18.

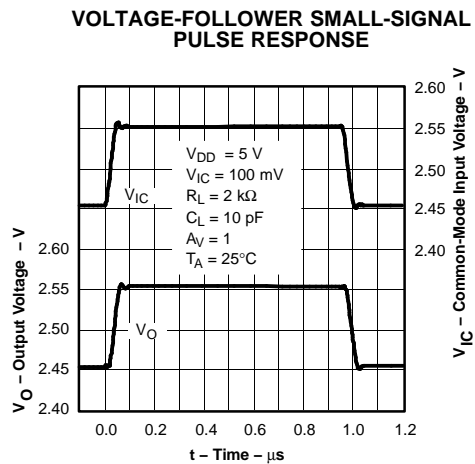


Figure 19.

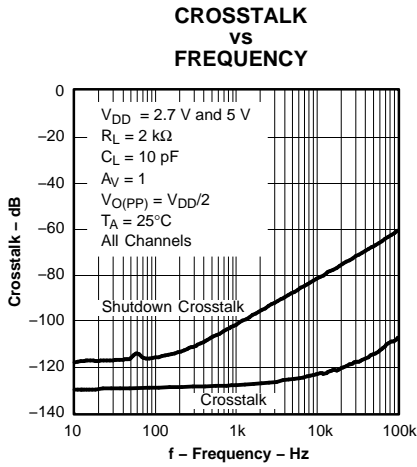


Figure 20.

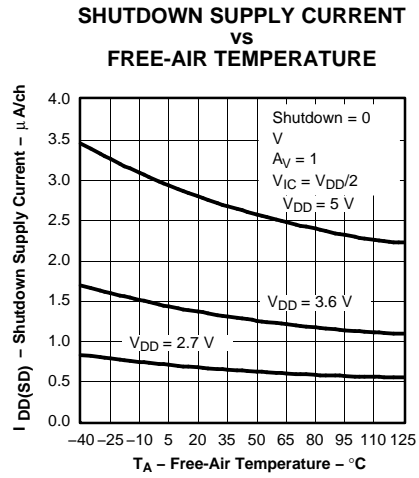


Figure 21.

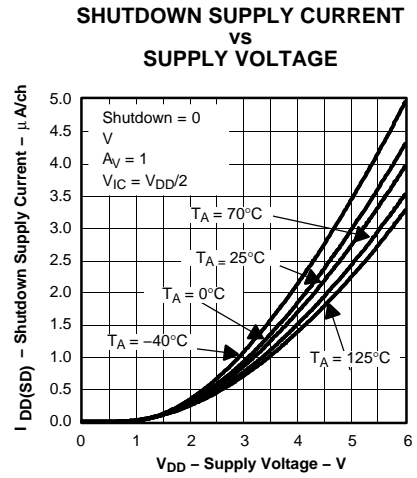


Figure 22.

**SHUTDOWN SUPPLY CURRENT/OUTPUT VOLTAGE
 vs
 TIME**

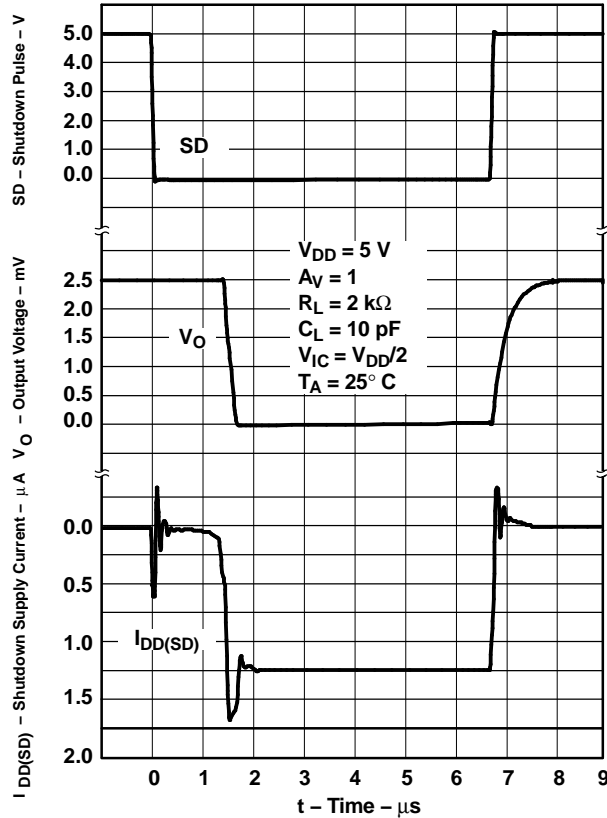


Figure 23.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2620IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBAI | Samples |
| TLV2620IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBAI | Samples |
| TLV2620IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2620I | Samples |
| TLV2621IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBBI | Samples |
| TLV2621IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBBI | Samples |
| TLV2621IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2621I | Samples |
| TLV2622ID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2622I | Samples |
| TLV2622IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AKM | Samples |
| TLV2622IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2622I | Samples |
| TLV2623IDGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ALC | Samples |
| TLV2623IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ALC | Samples |
| TLV2624ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2624I | Samples |
| TLV2624IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2624I | Samples |
| TLV2624IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2624I | Samples |
| TLV2624IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2624I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

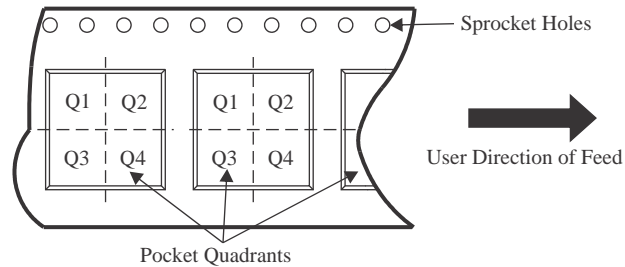
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2620IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2620IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2620IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2621IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2621IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2621IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2622IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2622IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2623IDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2624IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2624IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

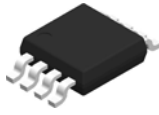
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2620IDBVR | SOT-23 | DBV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2620IDBVT | SOT-23 | DBV | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2620IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2621IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2621IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2621IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2622IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2622IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2623IDGSR | VSSOP | DGS | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2624IDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TLV2624IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TLV2622ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TLV2624ID | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLV2624IPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

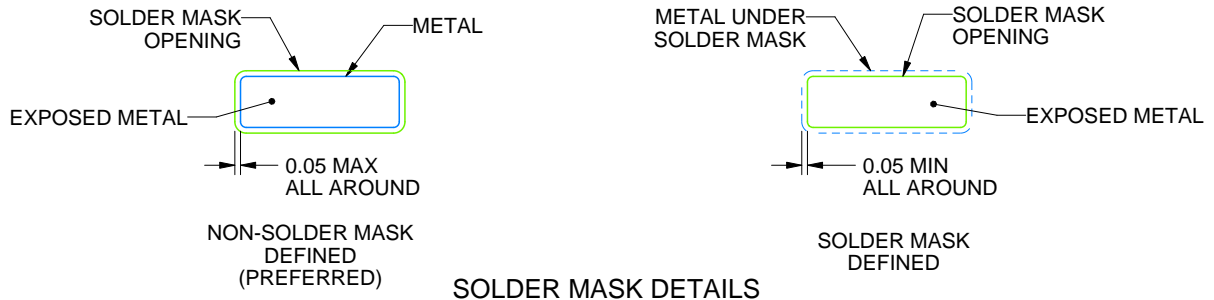
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

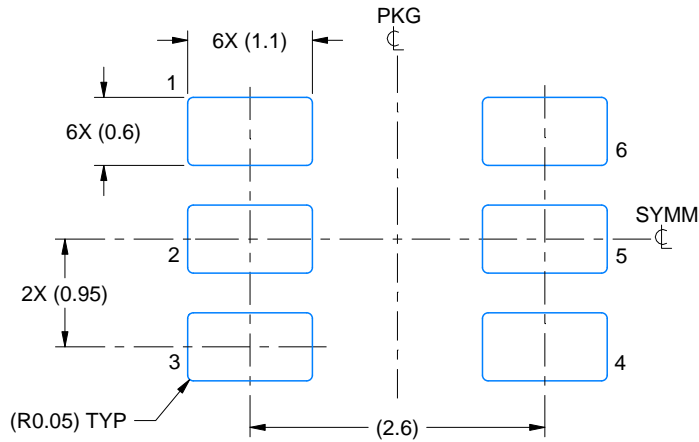
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

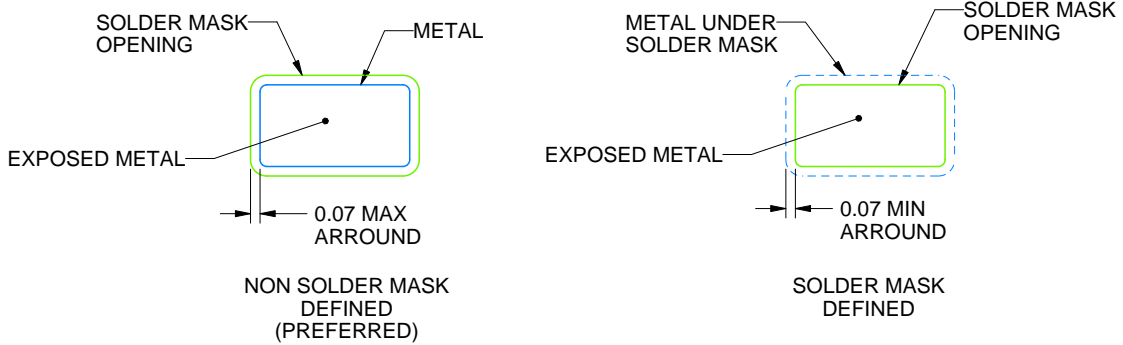
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

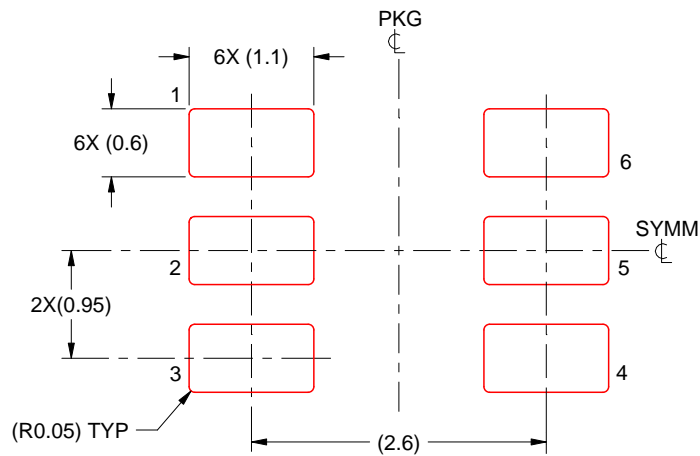
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

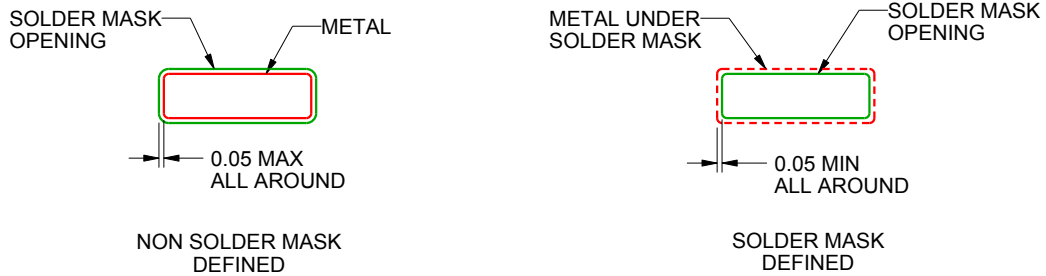
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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